MSPM0Gx51x Mixed-Signal Microcontrollers With CAN-FD Interface

1 Features

- **Core**
  - Arm® 32-bit Cortex® M0+ CPU with memory protection unit, frequency up to 80MHz
- Functional Safety-Compliant targeted
  - Developed for functional safety applications
  - Functional Safety Manual and FMEDA available to aid in functional safety system design
  - Systematic capability up to ASIL B targeted
- **Operating characteristics**
  - Extended temperature: –40°C up to 125°C
  - Wide supply voltage range: 1.62V to 3.6V
- **Memories**
  - Up to 512KB of flash memory with error correction code (ECC)
    - Dual-bank with address swap for OTA updates
  - 16KB data flash bank with ECC protection
  - 128KB total SRAM
    - SRAM (Bank 0): 64kB SRAM with ECC protection or hardware parity, and retention down to STANDBY mode
    - SRAM (Bank 1) : 64kB SRAM with retention down to SLEEP mode
- **High-performance analog peripherals**
  - Two simultaneous sampling 12-bit 4Msps analog-to-digital converters (ADCs) with up to 27 external channels
    - 14-bit effective resolution at 250ksps with hardware averaging
  - One 12-bit 1-MSPS digital-to-analog converter with integrated output buffer (DAC)
  - Three high-speed comparators (COMP) with integrated 8-bit reference DACs
    - 32ns propagation delay in high-speed mode
    - Support low-power mode operation down to <1µA
  - Programmable analog connections between ADC, COMP and DAC
  - Configurable 1.4V or 2.5V internal shared voltage reference (VREF)
  - Integrated temperature sensor
- **Optimized low-power modes**
  - RUN: 121µA/MHz (CoreMark)
  - SLEEP: 614µA at 4MHz
  - STOP: 56µA at 32 kHz
  - STANDBY: 1.7µA with RTC and SRAM retention
  - SHUTDOWN: 93nA with IO wake-up capability
- **Intelligent digital peripherals**
  - 12-channel DMA controller
  - Math accelerator supports DIV, SQRT, MAC and TRIG computations
  - Nine timers support up to 28 PWM channels
    - Three 16-bit general-purpose timers
    - Two 16-bit general-purpose timers support QEI
    - One 16-bit general-purpose timer support low-power operation in STANDBY mode
    - One 32-bit high-resolution general-purpose timer
    - Two 16-bit advanced timers with deadband support and complimentary outputs up to 12 PWM channels
  - Two windowed watchdog timers (WWDT), one independent watchdog timer (IWDT)
  - RTC with alarm and calendar mode
- **Enhanced communication interfaces**
  - Seven UART interfaces
    - Two supporting LIN, IrDA, DALI, Smart Card, Manchester
    - Five basic instances, including one supporting low-power operation in STANDBY mode
  - Three I^2C interfaces supporting up to FM+ (1Mbit/s), SMBus/PMBus, and wakeup from STOP mode
  - Three SPIs supports up to 32Mbits/s
  - Two Controller Area Network (CAN) interfaces support CAN 2.0 A or B and CAN-FD
- **Clock system**
  - Internal 4 to 32MHz oscillator with up to ±1.2% accuracy (SYSOSC)
  - Phase-locked loop (PLL) up to 80MHz
  - Internal 32kHz low-frequency oscillator (LFOSC) with ±3% accuracy
  - External 4 to 48MHz crystal oscillator (HFXT)
  - External 32kHz crystal oscillator(LFXT)
  - External clock input
- **Data integrity and encryption**
  - AES-128/256 accelerator with support for GCM/GMAC, CCM/CBC-MAC, CBC, CTR
  - Secure Key Storage for up to four AES keys
  - Flexible firewalls for protecting code and data
  - True random number generator (TRNG)
  - Cyclic redundancy checker (CRC-16, CRC-32)
  - Extensive security features
- **Flexible I/O features**
  - Up to 94 GPIOs
    - Two 5V-tolerant open-drain IOs

ADVANCE INFORMATION

    - Three high-drive IOs with 20mA drive strength
    - Four high-speed IOs
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options**
  - 100-pin LQFP (0.5mm pitch)
  - 80-pin LQFP (0.5mm pitch)
  - 64-pin LQFP (0.5mm pitch)
  - 48-pin LQFP (0.5mm pitch)
  - 48-pin VQFN (0.5mm pitch)
  - 32-pin VQFN (0.5mm pitch)
- **Family members** (also see *Device Comparison*)
  - MSPM0G3519: 512KB flash, 128KB RAM
  - MSPM0G3518: 256KB flash, 128KB RAM
  - MSPM0G1519: 512KB flash, 128KB RAM
  - MSPM0G1518: 256KB flash, 128KB RAM
- **Development kits and software** (also see *Tools and Software*)
  - LP-MSPM0G3519 LaunchPad™ development kit
  - MSPM0 Software Development Kit (SDK)

2 Applications

- Motor control
- Home appliances
- Uninterruptible power supplies and inverters
- Electronic point of sale systems
- Medical and healthcare
- Test and measurement
- Factory automation and control
- Industrial transport
- Grid infrastructure
- Smart metering
- Communication modules
- Lighting

3 Description

MSPM0Gx51x microcontrollers (MCUs) are part of the MSP highly integrated, ultra-low-power 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ 32-bit core platform, operating at up to 80MHz frequency. These MCUs offer a blend of cost optimization and design flexibility for applications requiring 256KB to 512KB of flash memory in small packages (down to 5mm x 5mm) or high pin count packages (up to 100 pins). These devices include dual CAN-FD controllers, cybersecurity enablers, high performance integrated analog, and provide excellent low power performance across the operating temperature range.

Up to 512KB of embedded flash program memory with built-in error correction code (ECC) and up to 128KB SRAM (with ECC and parity protection for the first 64kB). The flash memory is organized into two main banks to support field firmware updates, with address swap support provided between the two main banks.

Flexible cybersecurity enablers can be used to support secure boot, secure in-field firmware updates, IP protection (execute-only memory), key storage, and more. Hardware acceleration is provided for a variety of AES symmetric cipher modes, as well as a TRNG entropy source. The cybersecurity architecture is pending Arm® PSA Level 1 certification.

A set of high performance analog modules is provided, such as two simultaneously sampling 12-bit 4Msps ADCs supporting up to 27 external channels, on-chip voltage reference (1.4V or 2.5V), one 12-bit 1Msps DAC, and three high speed comparators with built-in 8-bit reference DACs operable in low-power and high-speed modes.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets their project's needs. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

MSPM0Gx51x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad available for purchase. TI also provides a free MSPM0 Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See *MSP430™ System-Level ESD Considerations* for more information. The principles in this application note are applicable to MSPM0 MCUs.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
MSPM0G1518SPZR	PZ (LQFP, 100)	16mm x 16mm
MSPM0G1519SPZR		
MSPM0G3518SPZR		
MSPM0G3519SPZR		
MSPM0G1518SPNR	PN (LQFP, 80)	14mm x 14mm
MSPM0G1519SPNR		
MSPM0G3518SPNR		
MSPM0G3519SPNR		
MSPM0G1518SPMR	PM (LQFP, 64)	12mm x 12mm
MSPM0G1519SPMR		
MSPM0G3518SPMR		
MSPM0G3519SPMR		
MSPM0G1518SPTR	PT (LQFP, 48)	9mm x 9mm
MSPM0G1519SPTR		
MSPM0G3518SPTR		
MSPM0G3519SPTR		
MSPM0G1518SRGZR	RGZ (VQFN, 48)	7mm x 7mm
MSPM0G1519SRGZR		
MSPM0G3518SRGZR		
MSPM0G3519SRGZR		
MSPM0G1518SRHBR	RHB (VQFN, 32)	5mm x 5mm
MSPM0G1519SRHBR		
MSPM0G3518SRHBR		
MSPM0G3519SRHBR		

(1) For more information, see Section 11.
(2) The package size (length x width) is a nominal value and includes pins, where applicable

ADVANCE INFORMATION

ADVANCE INFORMATION

4 Functional Block Diagram

MSPM0Gx51x Functional Block Diagram shows the MSPM0Gx51x functional block diagram.

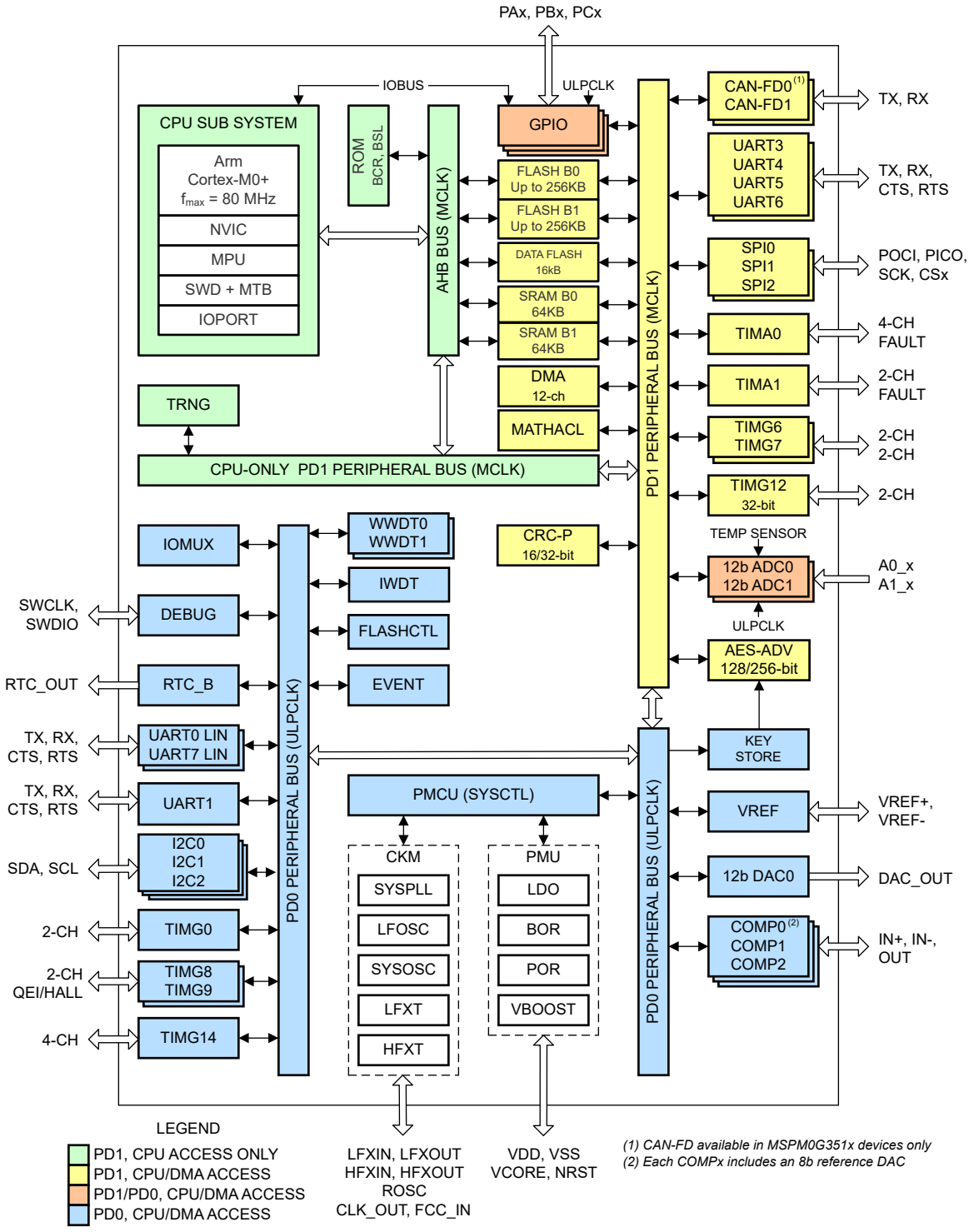


Figure 4-1. MSPM0Gx51x Functional Block Diagram

Table of Contents

ADVANCE INFORMATION

5 Device Comparison

The following table summarizes the features of each device that is described in this data sheet.

Table 5-1. Device Comparison Table

DEVICE NAME	FLASH / SRAM (KB)	QUAL	CAN	ADC CHANNELS	GPIO	PACKAGE
MSPM0G1518SPZR	256 / 128	S	0	27	94	100 LQFP (0.5mm pitch) [16mm x 16mm]
MSPM0G1519SPZR	512 / 128	S	0	27	94	
MSPM0G3518SPZR	256 / 128	S	2	27	94	
MSPM0G3519SPZR	512 / 128	S	2	27	94	
MSPM0G1518SPNR	256 / 128	S	0	27	74	80 LQFP (0.5mm pitch) [14mm x 14mm]
MSPM0G1519SPNR	512 / 128	S	0	27	74	
MSPM0G3518SPNR	256 / 128	S	2	27	74	
MSPM0G3519SPNR	512 / 128	S	2	27	74	
MSPM0G1518SPMR	256 / 128	S	0	27	60	64 LQFP (0.5mm pitch) [12mm x 12mm]
MSPM0G1519SPMR	512 / 128	S	0	27	60	
MSPM0G3518SPMR	256 / 128	S	2	27	60	
MSPM0G3519SPMR	512 / 128	S	2	27	60	
MSPM0G1518SPTR	256 / 128	S	0	21	44	48 LQFP (0.5mm pitch) [9mm x 9mm]
MSPM0G1519SPTR	512 / 128	S	0	21	44	
MSPM0G3518SPTR	256 / 128	S	1	21	44	
MSPM0G3519SPTR	512 / 128	S	1	21	44	
MSPM0G1518SRGZR	256 / 128	S	0	21	44	48 VQFN (0.5mm pitch) [7mm x 7mm]
MSPM0G1519SRGZR	512 / 128	S	0	21	44	
MSPM0G3518SRGZR	256 / 128	S	1	21	44	
MSPM0G3519SRGZR	512 / 128	S	1	21	44	
MSPM0G1518SRHBR	256 / 128	S	0	16	28	32 VQFN (0.5mm pitch) [5mm x 5mm]
MSPM0G1519SRHBR	512 / 128	S	0	16	28	
MSPM0G3518SRHBR	256 / 128	S	1	16	28	
MSPM0G3519SRHBR	512 / 128	S	1	16	28	

5.1 Device Comparison Chart

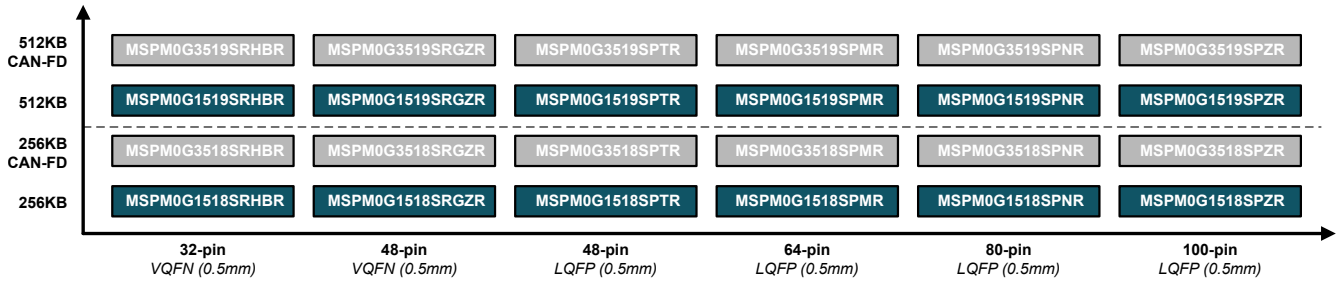


Figure 5-1. Device Comparison Chart

ADVANCE INFORMATION

6 Pin Configuration and Functions

The System Configuration tool provides a graphical interface to enable, configurable, and generate initialization code for pin multiplexing and simplifying pin settings. The pin diagrams shown in the data sheet show the primary peripheral functions, some of the integrated device features, and available clock signals to simplify the device pinout.

For full descriptions of the pin functions, see the *Pin Attributes* and *Signal Descriptions* sections.

6.1 Pin Diagrams

For full pin configuration and functions for each package option, refer to Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) and Signal Descriptions

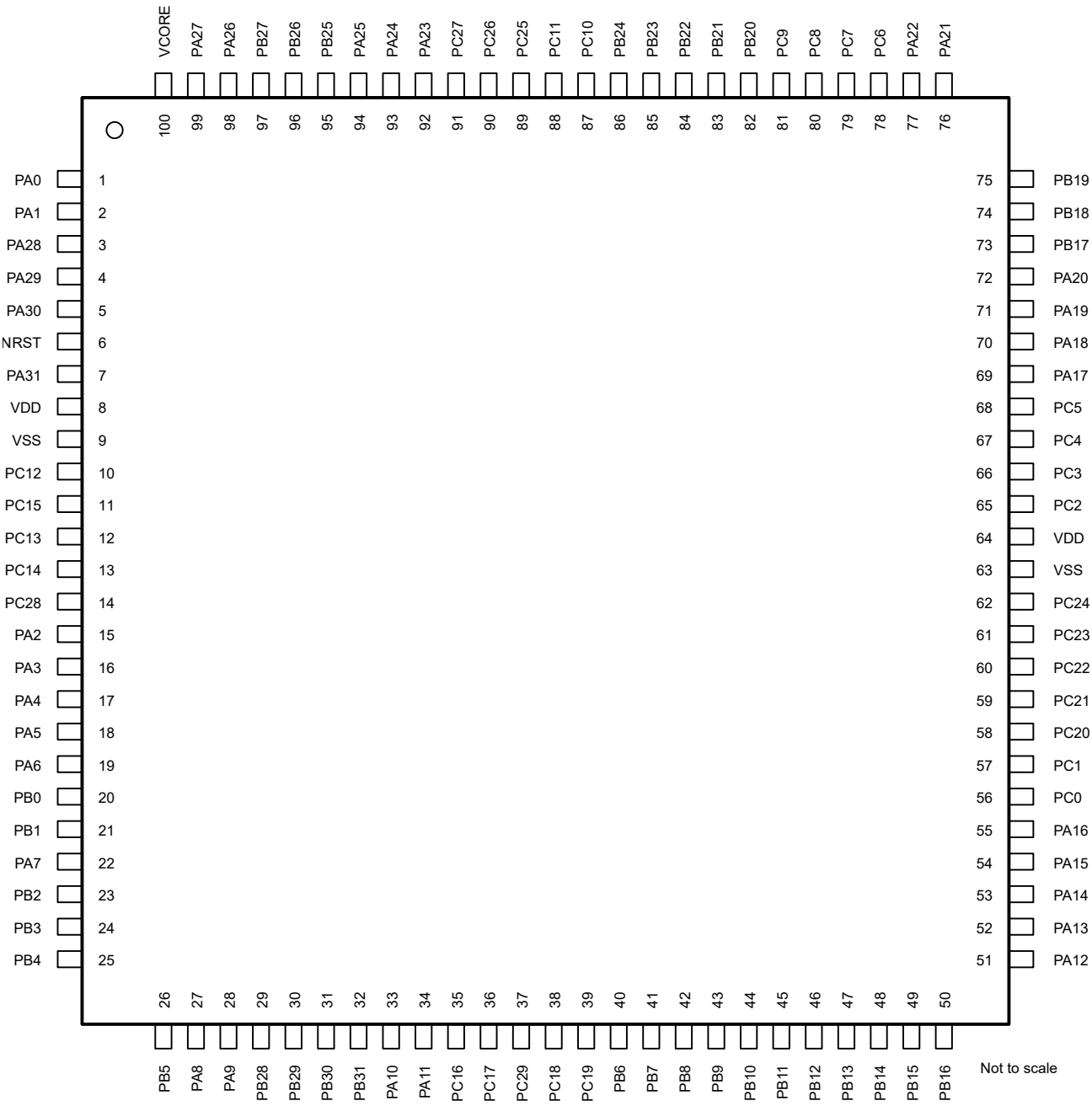


Figure 6-1. 100-pin PZ (0.5mm) (LQFP) Package Diagram

ADVANCE INFORMATION

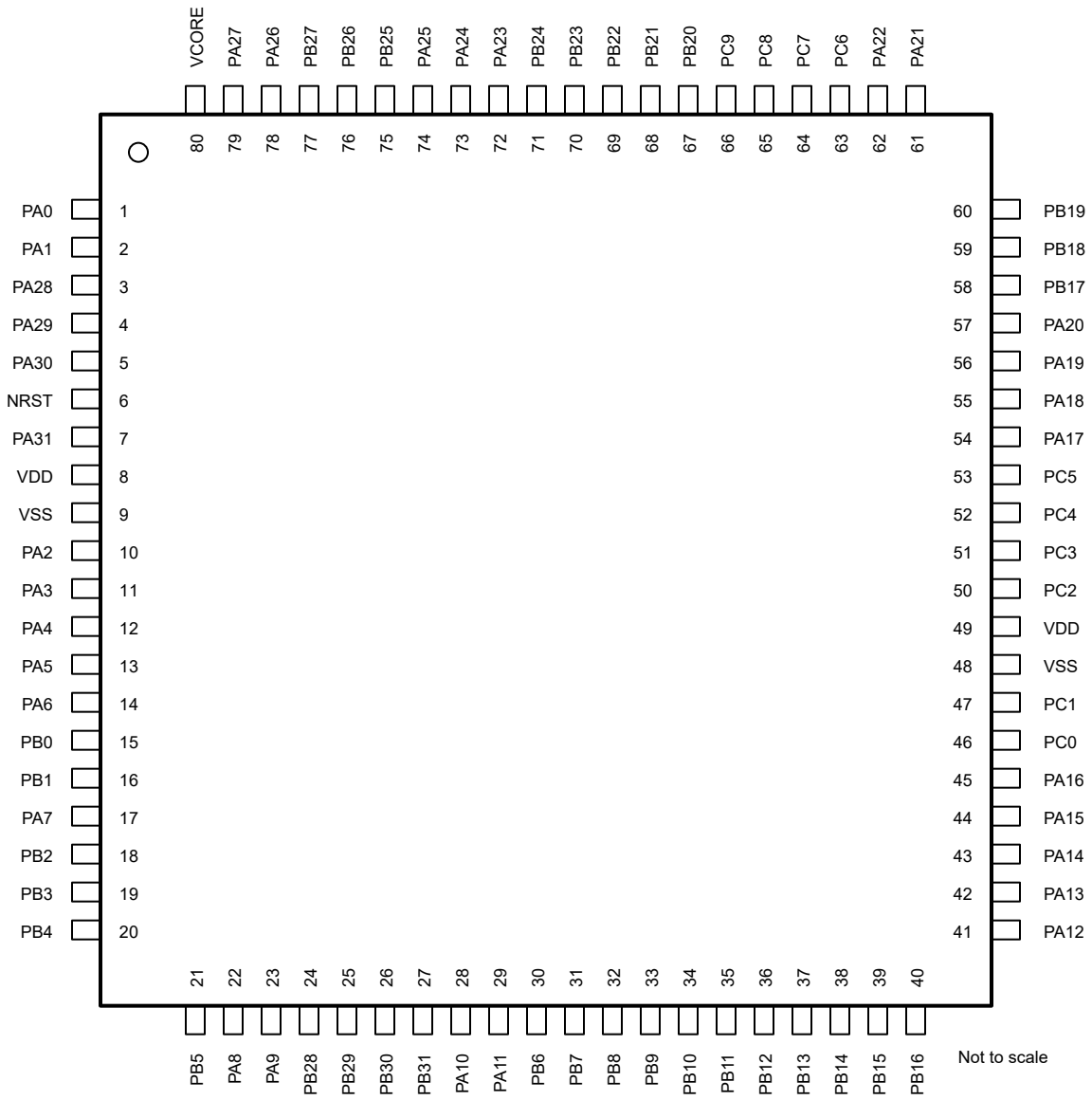


Figure 6-2. 80-pin PN (0.5mm) (LQFP) Package Diagram

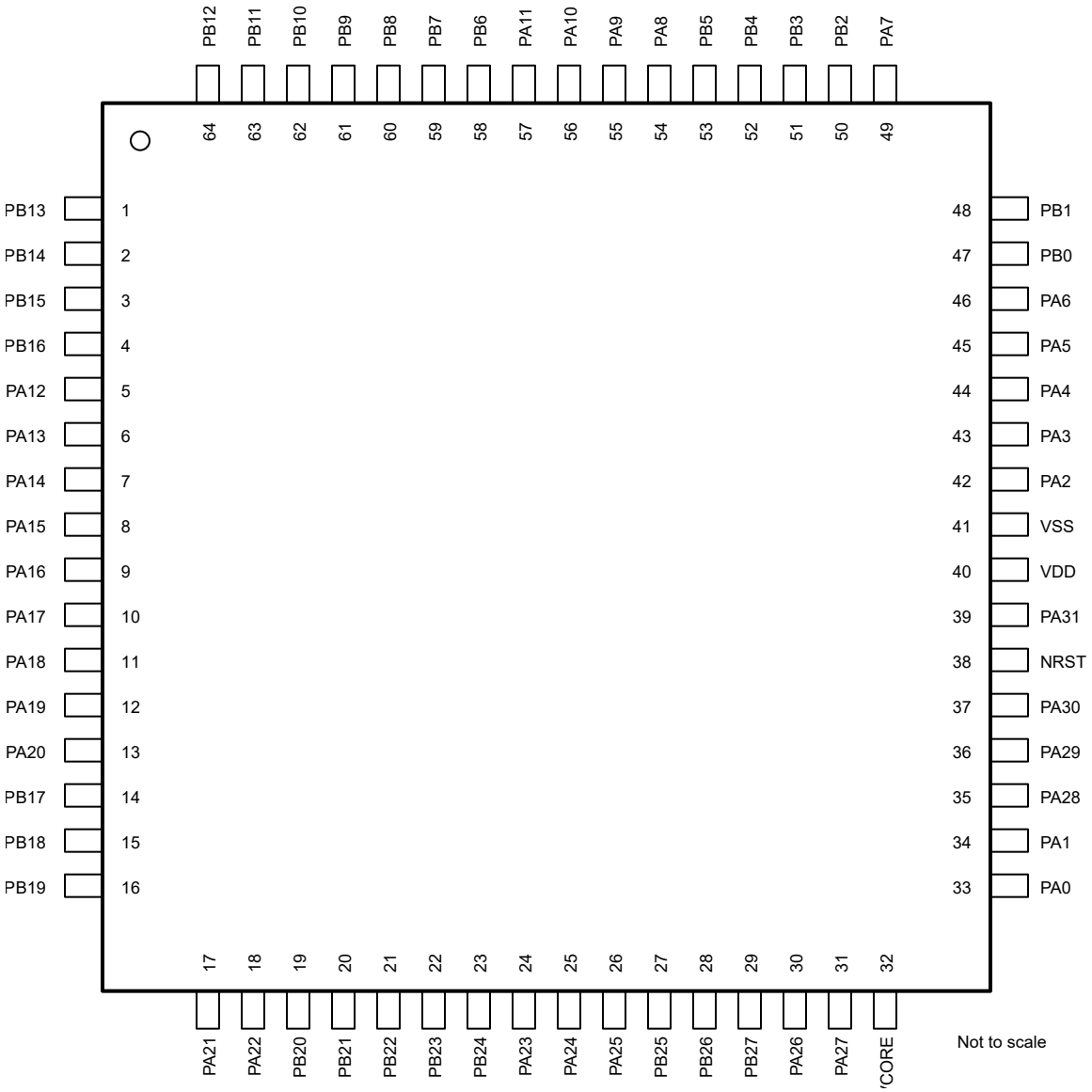


Figure 6-3. 64-pin PM (0.5mm) (LQFP) Package Diagram

ADVANCE INFORMATION

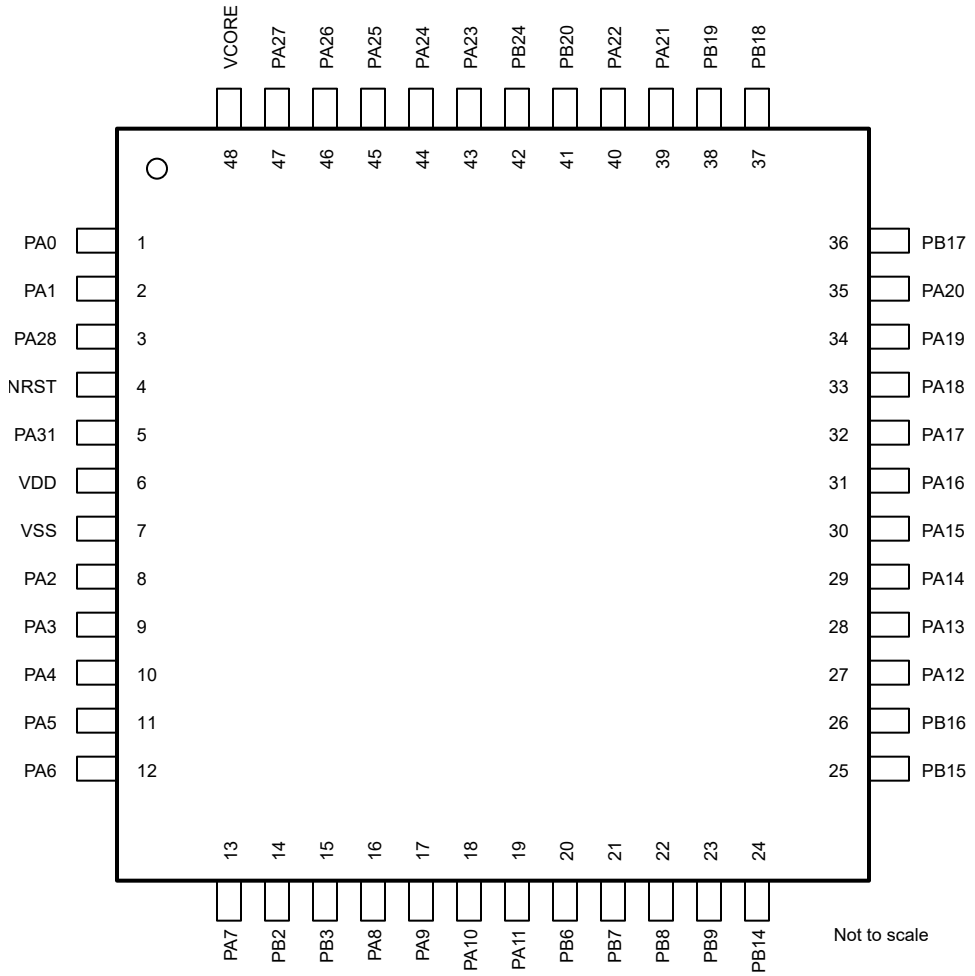


Figure 6-4. 48-pin PT (0.5mm) (LQFP) Package Diagram

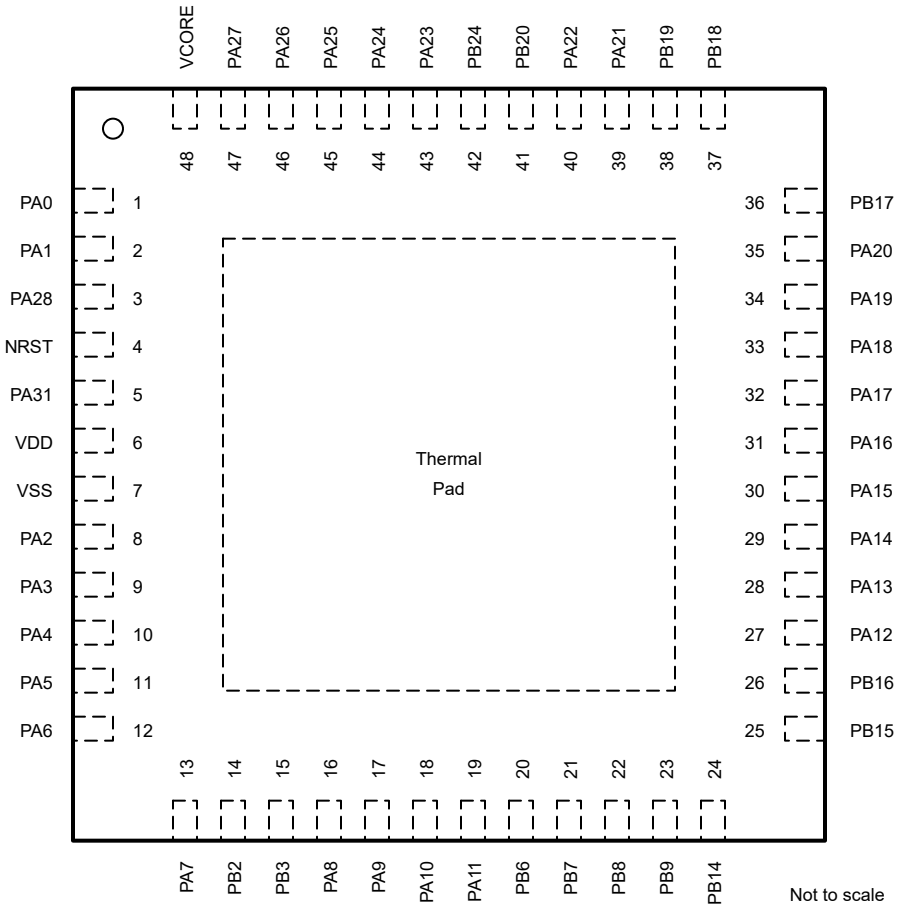


Figure 6-5. 48-pin RGZ (0.5mm) (VQFN) Package Diagram

ADVANCE INFORMATION

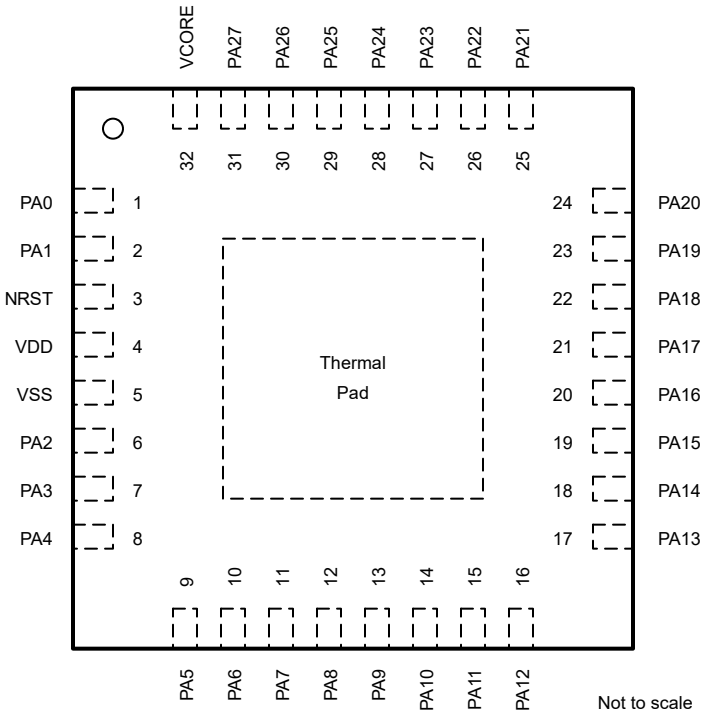


Figure 6-6. 32-pin RHB (0.5mm) (VQFN) Package Diagram

6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired Pin Function using the PINCM.PF control bits. The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. The PINCM.PF and PINCM.PC in IOMUX are recommended to be set to 0 when non-IOMUX managed functions (such as analog connections) are intended to be used on a pin. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin, provided there is no contention between the functions. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-1. Digital IO Features by IO Type

BUFFER TYPE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
SDIO (standard drive)	Y			Y	Y	
SDIO (standard drive) with wake Section 6.2.1	Y			Y	Y	Y
HDIO (High drive)	Y	Y		Y	Y	Y
HSIO (High speed)	Y	Y		Y	Y	
ODIO (5V-tolerant open drain)	Y		Y		Y	Y

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
3	4	4	38	6	6	NRST	NRST	(Non-IOMUX 1) 0	I	RESET
							WAKE	(Non-IOMUX 2) 0	I	
1	1	1	33	1	1	PA0 PINCM1 0x40428000	PA0	1	IO	ODIO (5V-tol)
							UART0_TX	2	O	
							I2C0_SDA	3	IOD	
							TIMA0_C0	4	IO	
							TIMA_FAL1	5	I	
							FCC_IN	6	I	
							TIMG8_C1	7	IO	
							TIMG12_C0	8	IO	
							TIMG0_C0	9	IO	
							UART5_RX	12	I	
							BSLSDA	(Non-IOMUX 1) 0	IOD	
							WAKE	(Non-IOMUX 2) 0	I	
2	2	2	34	2	2	PA1 PINCM2 0x40428004	PA1	1	IO	ODIO (5V-tol)
							UART0_RX	2	I	
							I2C0_SCL	3	IOD	
							TIMA0_C1	4	IO	
							TIMA_FAL2	5	I	
							TIMG8_IDX	6	I	
							TIMG8_C0	7	IO	
							TIMG12_C1	8	IO	
							TIMG0_C1	9	IO	
							SPI0_CS3	10	IO	
							UART5_TX	12	O	
							BSLSCL	(Non-IOMUX 1) 0	IOD	
							WAKE	(Non-IOMUX 2) 0	I	
6	8	8	42	10	15	PA2 PINCM7 0x40428018	PA2	1	IO	SDIO (standard)
							TIMG8_C1	2	IO	
							SPI0_CS0	3	IO	
							TIMG7_C1	4	IO	
							SPI1_CS0	5	IO	
							TIMA0_C3N	6	O	
							TIMA0_C2N	7	O	
							TIMA_FAL0	8	I	
							TIMA_FAL1	9	I	
							UART4_CTS	10	I	
							TIMA0_C0	11	IO	
							SPI2_POCI	12	IO	
							TIMG9_C1	13	IO	
							ROSC	(Non-IOMUX 1) 0	A	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
7	9	9	43	11	16	PA3 PINCM8 0x4042801c	PA3	1	IO	SDIO (standard)
							TIMG8_C0	2	IO	
							SPI0_CS1	3	IO	
							I2C1_SDA	4	IOD	
							TIMA0_C1	5	IO	
							COMP0_OUT	6	O	
							TIMG9_C0	7	IO	
							TIMA0_C2	8	IO	
							UART7_CTS	9	I	
							UART1_TX	10	O	
							SPI0_CS3	11	IO	
							COMP1_OUT	12	O	
							TIMG7_C0	13	IO	
							LFXIN	(Non-IOMUX 1) 0	A	
8	10	10	44	12	17	PA4 PINCM9 0x40428020	PA4	1	IO	SDIO (standard)
							TIMG8_C1	2	IO	
							SPI0_POCI	3	IO	
							I2C1_SCL	4	IOD	
							TIMA0_C1N	5	O	
							LFCLK_IN	6	I	
							TIMG9_IDX	7	I	
							TIMA0_C3	8	IO	
							UART7_RTS	9	O	
							UART1_RX	10	I	
							SPI0_CS0	11	IO	
							SPI2_CS0	12	IO	
							TIMG7_C1	13	IO	
							LFXOUT	(Non-IOMUX 1) 0	A	
9	11	11	45	13	18	PA5 PINCM10 0x40428024	PA5	1	IO	SDIO (standard)
							TIMG8_C0	2	IO	
							SPI0_PICO	3	IO	
							I2C1_SDA	4	IOD	
							TIMG0_C0	5	IO	
							FCC_IN	6	I	
							TIMG6_C0	7	IO	
							TIMA_FAL1	8	I	
							UART0_CTS	9	I	
							UART4_RTS	10	O	
							UART1_TX	11	O	
							SPI2_CS1	12	IO	
							HFXIN	(Non-IOMUX 1) 0	A	

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
10	12	12	46	14	19	PA6 PINCM11 0x40428028	PA6	1	IO	SDIO (standard)
							TIMG8_C1	2	IO	
							SPI0_SCK	3	IO	
							I2C1_SCL	4	IOD	
							TIMG0_C1	5	IO	
							HFCLK_IN	6	I	
							TIMG6_C1	7	IO	
							TIMA_FAL0	8	I	
							UART0_RTS	9	O	
							TIMA0_C2N	10	O	
							UART1_RX	11	I	
							SPI2_CS2	12	IO	
							HFXOUT	(Non-IOMUX 1) 0	A	
11	13	13	49	17	22	PA7 PINCM14 0x40428034	PA7	1	IO	SDIO (standard)
							COMP0_OUT	2	O	
							CLK_OUT	3	O	
							TIMG8_C0	4	IO	
							TIMA0_C2	5	IO	
							TIMG8_IDX	6	I	
							TIMG7_C1	7	IO	
							TIMA0_C1	8	IO	
							SPI0_CS2	9	IO	
							FCC_IN	10	I	
							SPI0_POCI	11	IO	
12	16	16	54	22	27	PA8 PINCM19 0x40428048	PA8	1	IO	SDIO (standard)
							UART1_TX	2	O	
							SPI0_CS0	3	IO	
							I2C0_SDA	4	IOD	
							TIMA0_C0	5	IO	
							TIMA_FAL2	6	I	
							TIMA_FAL0	7	I	
							SPI0_CS3	8	IO	
							TIMG14_C2	9	I	
							HFCLK_IN	10	I	
							UART0_RTS	11	O	
							TIMA1_C0N	12	O	
13	17	17	55	23	28	PA9 PINCM20 0x4042804c	PA9	1	IO	HSIO (High-speed)
							UART1_RX	2	I	
							SPI0_PICO	3	IO	
							I2C0_SCL	4	IOD	
							TIMA0_C0N	5	O	
							CLK_OUT	6	O	
							TIMA0_C1	7	IO	
							RTC_OUT	8	O	
							TIMG14_C3	9	I	
							UART4_RTS	10	O	
							UART0_CTS	11	I	
							TIMA1_C1N	12	O	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
14	18	18	56	28	33	PA10 PINCM21 0x40428050	PA10	1	IO	HDIO (high-drive)
							UART0_TX	2	O	
							SPI0_POCI	3	IO	
							I2C0_SDA	4	IOD	
							TIMA0_C2	5	IO	
							CLK_OUT	6	O	
							TIMG0_C0	7	IO	
							I2C1_SDA	8	IOD	
							TIMG12_C0	9	IO	
							TIMA_FAL1	10	I	
							TIMA1_C0	11	IO	
							SPI2_SCK	12	IO	
							BSLTX	(Non-IOMUX 1) 0	O	
							WAKE	(Non-IOMUX 2) 0	I	
15	19	19	57	29	34	PA11 PINCM22 0x40428054	PA11	1	IO	HDIO (high-drive)
							UART0_RX	2	I	
							SPI0_SCK	3	IO	
							I2C0_SCL	4	IOD	
							TIMA0_C2N	5	O	
							COMP0_OUT	6	O	
							TIMG0_C1	7	IO	
							I2C1_SCL	8	IOD	
							TIMG12_C1	9	IO	
							TIMA_FAL0	10	I	
							TIMA1_C1	11	IO	
							BSLRX	(Non-IOMUX 1) 0	I	
							WAKE	(Non-IOMUX 2) 0	I	
16	27	27	5	41	51	PA12 PINCM34 0x40428084	PA12	1	IO	HSIO (high-speed)
							UART3_CTS	2	I	
							SPI0_SCK	3	IO	
							COMP0_OUT	4	O	
							TIMA0_C3	5	IO	
							FCC_IN	6	I	
							TIMG0_C0	7	IO	
							SPI1_CS1	8	IO	
							SPI0_CS1	9	IO	
							UART7_CTS	10	I	
							UART1_CTS	11	I	
							CAN0_TX	12	O	
							A0_8	(Non-IOMUX 1) 0	A	

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
17	28	28	6	42	52	PA13 PINCM35 0x40428088	PA13	1	IO	HSIO (high-speed)
							UART3_RTS	2	O	
							SPI0_POCI	3	IO	
							UART3_RX	4	I	
							TIMA0_C3N	5	O	
							RTC_OUT	6	O	
							TIMG0_C1	7	IO	
							SPI1_CS0	8	IO	
							SPI0_CS3	9	IO	
							UART7_TX	10	O	
							UART1_RTS	11	O	
							CAN0_RX	12	I	
							A0_9	(Non-IOMUX 1) 0	A	
							COMP0_IN2-	(Non-IOMUX 2) 0	A	
18	29	29	7	43	53	PA14 PINCM36 0x4042808c	PA14	1	IO	HSIO (high-speed)
							UART0_CTS	2	I	
							SPI0_PICO	3	IO	
							UART3_TX	4	O	
							TIMG12_C0	5	IO	
							CLK_OUT	6	O	
							TIMG12_C1	7	IO	
							SPI1_CS2	8	IO	
							SPI0_CS2	9	IO	
							UART7_RX	10	I	
							A0_12	(Non-IOMUX 1) 0	A	
							COMP0_IN2+	(Non-IOMUX 2) 0	A	
19	30	30	8	44	54	PA15 PINCM37 0x40428090	PA15	1	IO	SDIO (standard)
							UART0_RTS	2	O	
							SPI1_CS2	3	IO	
							I2C1_SCL	4	IOD	
							TIMA0_C2	5	IO	
							I2C2_SCL	6	IOD	
							TIMG8_IDX	7	I	
							TIMG12_C0	8	IO	
							TIMA1_C0N	9	O	
							UART7_RTS	10	O	
							TIMA1_C0	11	IO	
							A1_0	(Non-IOMUX 1) 0	A	
							DAD_OUT	(Non-IOMUX 2) 0	I	
							COMP0_IN3+	(Non-IOMUX 3) 0	A	
							COMP1_IN3+	(Non-IOMUX 4) 0	A	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
20	31	31	9	45	55	PA16 PINCM38 0x40428094	PA16	1	IO	SDIO (standard)
							COMP0_OUT	2	O	
							SPI1_POCI	3	IO	
							I2C1_SDA	4	IOD	
							TIMA0_C2N	5	O	
							I2C2_SDA	6	IOD	
							FCC_IN	7	I	
							TIMG12_C1	8	IO	
							COMP2_OUT	9	O	
							UART7_CTS	10	I	
							TIMA1_C1	11	IO	
							TIMA1_C1N	12	O	
							A1_1	(Non-IOMUX 1) 0	A	
21	32	32	10	54	69	PA17 PINCM39 0x40428098	PA17	1	IO	SDIO (standard with wake)
							UART1_TX	2	O	
							SPI1_SCK	3	IO	
							I2C1_SCL	4	IOD	
							TIMA0_C3	5	IO	
							TIMG8_C0	7	IO	
							TIMG12_C0	8	IO	
							SPI0_CS1	9	IO	
							TIMA1_C0	10	IO	
							TIMG7_C0	11	IO	
							WAKE	(Non-IOMUX 1) 0	I	
							A1_2	(Non-IOMUX 2) 0	A	
							COMP0_IN1-	(Non-IOMUX 3) 0	A	
22	33	33	11	55	70	PA18 PINCM40 0x4042809c	PA18	1	IO	SDIO (standard with wake)
							UART1_RX	2	I	
							SPI1_PICO	3	IO	
							I2C1_SDA	4	IOD	
							TIMA0_C3N	5	O	
							TIMG8_C1	7	IO	
							TIMG12_C1	8	IO	
							SPI0_CS0	9	IO	
							TIMA1_C1	10	IO	
							TIMG7_C1	11	IO	
							BSL_invoke	(Non-IOMUX 1) 0	I	
							WAKE	(Non-IOMUX 2) 0	I	
							A1_3	(Non-IOMUX 3) 0	A	
							COMP0_IN1+	(Non-IOMUX 4) 0	A	
23	34	34	12	56	71	PA19 PINCM41 0x404280a0	PA19	1	IO	SDIO (standard)
							SWDIO	2	IO	
							SPI1_POCI	3	IO	
							I2C1_SDA	4	IOD	
							TIMA0_C2	5	IO	
							TIMG0_C0	6	IO	
							A0_13	(Non-IOMUX 1) 0	A	

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
24	35	35	13	57	72	PA20 PINCM42 0x404280a4	PA20	1	IO	SDIO (standard)
							SWCLK	2	I	
							SPI1_SCK	3	IO	
							I2C1_SCL	4	IOD	
							TIMA0_C2N	5	O	
							TIMG0_C1	6	IO	
							A0_14	(Non-IOMUX 1) 0	A	
25	39	39	17	61	76	PA21 PINCM46 0x404280b4	PA21	1	IO	SDIO (standard)
							UART7_TX	2	O	
							SPI0_CS3	3	IO	
							UART1_CTS	4	I	
							TIMA0_C0	5	IO	
							SPI1_CS1	7	IO	
							UART7_CTS	8	I	
							UART4_RTS	9	O	
							TIMG8_C0	10	IO	
							TIMG6_C0	11	IO	
							A1_7	(Non-IOMUX 1) 0	A	
							COMP2_IN1-	(Non-IOMUX 2) 0	A	
							VREF-	(Non-IOMUX 3) 0	A	
26	40	40	18	62	77	PA22 PINCM47 0x404280b8	PA22	1	IO	SDIO (standard)
							UART7_RX	2	I	
							SPI0_CS2	3	IO	
							UART1_RTS	4	O	
							TIMA0_C0N	5	O	
							TIMA0_C1	7	IO	
							CLK_OUT	8	O	
							I2C0_SCL	9	IOD	
							TIMG8_C1	10	IO	
							TIMG6_C1	12	IO	
							A0_7	(Non-IOMUX 1) 0	A	
27	43	43	24	72	92	PA23 PINCM53 0x404280d0	PA23	1	IO	SDIO (standard)
							UART7_TX	2	O	
							SPI0_CS3	3	IO	
							I2C2_SCL	4	IOD	
							TIMA0_C3	5	IO	
							TIMG8_C0	6	IO	
							UART3_CTS	8	I	
							TIMG0_C0	9	IO	
							SPI1_CS1	10	IO	
							TIMG7_C0	11	IO	
							A1_12	(Non-IOMUX 1) 0	A	
							COMP1_IN1-	(Non-IOMUX 2) 0	A	
							VREF+	(Non-IOMUX 3) 0	I	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
28	44	44	25	73	93	PA24 PINCM54 0x404280d4	PA24	1	IO	SDIO (standard)
							UART7_RX	2	I	
							SPI0_CS2	3	IO	
							I2C2_SDA	4	IOD	
							TIMA0_C3N	5	O	
							TIMG8_C1	6	IO	
							TIMA1_C1	7	IO	
							UART3_RTS	8	O	
							TIMG0_C1	9	IO	
							SPI1_CS2	10	IO	
							TIMG7_C1	11	IO	
							A0_3	(Non-IOMUX 1) 0	A	
29	45	45	26	74	94	PA25 PINCM55 0x404280d8	PA25	1	IO	SDIO (standard)
							UART3_RX	2	I	
							SPI1_CS3	3	IO	
							TIMG12_C1	4	IO	
							TIMA0_C3	5	IO	
							TIMA0_C1N	6	O	
							COMP0_OUT	7	O	
							UART7_CTS	8	I	
							UART3_TX	9	O	
							A0_2	(Non-IOMUX 1) 0	A	
30	46	46	30	78	98	PA26 PINCM59 0x404280e8	PA26	1	IO	SDIO (standard)
							UART3_TX	2	O	
							SPI1_CS0	3	IO	
							TIMG8_C0	4	IO	
							TIMA_FAL0	5	I	
							TIMA0_C3N	6	O	
							UART7_RTS	8	O	
							UART3_RX	9	I	
							CAN0_TX	10	O	
							TIMG7_C0	11	IO	
							A0_1	(Non-IOMUX 1) 0	A	
							COMP0_IN0+	(Non-IOMUX 2) 0	A	
31	47	47	31	79	99	PA27 PINCM60 0x404280ec	PA27	1	IO	SDIO (standard)
							UART3_RX	2	I	
							SPI1_CS1	3	IO	
							TIMG8_C1	4	IO	
							TIMA_FAL2	5	I	
							CLK_OUT	6	O	
							RTC_OUT	8	O	
							COMP0_OUT	9	O	
							CAN0_RX	10	I	
							TIMG7_C1	11	IO	
							A0_0	(Non-IOMUX 1) 0	A	
							COMP0_IN0-	(Non-IOMUX 2) 0	A	

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
	3	3	35	3	3	PA28 PINCM3 0x40428008	PA28	1	IO	HDIO (high-drive)
							UART0_TX	2	O	
							I2C0_SDA	3	IOD	
							TIMA0_C3	4	IO	
							TIMA_FAL0	5	I	
							TIMA0_C1	7	IO	
							TIMA1_C0	9	IO	
							TIMG14_C2	10	I	
							TIMG7_C0	11	IO	
							UART5_CTS	12	I	
							WAKE	(Non-IOMUX 1) 0	I	
			36	4	4	PA29 PINCM4 0x4042800c	PA29	1	IO	SDIO (standard)
							I2C1_SCL	2	IOD	
							UART7_RTS	3	O	
							TIMG8_C0	4	IO	
							I2C2_SCL	6	IOD	
							UART0_CTS	7	I	
							SPI0_CS3	8	IO	
							TIMG6_C0	9	IO	
							TIMG14_C3	10	I	
							TIMG14_C0	11	I	
							UART5_RTS	12	O	
			37	5	5	PA30 PINCM5 0x40428010	PA30	1	IO	SDIO (standard)
							I2C1_SDA	2	IOD	
							UART7_CTS	3	I	
							TIMG8_C1	4	IO	
							I2C2_SDA	6	IOD	
							UART0_RTS	7	O	
							SPI0_CS2	8	IO	
							TIMG6_C1	9	IO	
							TIMG14_C1	11	I	
	5	5	39	7	7	PA31 PINCM6 0x40428014	PA31	1	IO	SDIO (standard with wake)
							UART0_RX	2	I	
							I2C0_SCL	3	IOD	
							TIMA0_C3N	4	O	
							TIMG12_C1	5	IO	
							CLK_OUT	6	O	
							SPI0_CS3	8	IO	
							TIMG7_C1	9	IO	
							TIMA1_C1	11	IO	
							WAKE	(Non-IOMUX 1) 0	I	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
							PB0	1	IO	
							UART0_TX	2	O	
							SPI1_CS2	3	IO	
							I2C0_SCL	4	IOD	
						PB0	TIMA0_C2	5	IO	
			47	15	20	PINCM12	TIMG0_C0	6	IO	SDIO (standard)
						0x4042802c	SPI0_CS3	7	IO	
							TIMA1_C0	8	IO	
							TIMG14_C2	9	I	
							SPI2_CS3	12	IO	
							PB1	1	IO	
							UART0_RX	2	I	
							SPI1_CS3	3	IO	
						PB1	I2C0_SDA	4	IOD	
			48	16	21	PINCM13	TIMA0_C2N	5	O	SDIO (standard)
						0x40428030	TIMG0_C1	6	IO	
							SPI0_CS2	7	IO	
							TIMA1_C1	8	IO	
							TIMG14_C3	9	I	
							PB2	1	IO	
							UART3_TX	2	O	
							UART7_CTS	3	I	
							I2C1_SCL	4	IOD	
							TIMA0_C3	5	IO	
						PB2	UART1_CTS	6	I	
	14	14	50	18	23	PINCM15	TIMG14_C0	7	I	SDIO (standard)
						0x40428038	UART7_TX	8	O	
							TIMG12_C0	9	IO	
							HFCLK_IN	10	I	
							SPI0_PICO	11	IO	
							TIMA1_C0	12	IO	
							TIMG6_C0	13	IO	
							PB3	1	IO	
							UART3_RX	2	I	
							UART7_RTS	3	O	
							I2C1_SDA	4	IOD	
							TIMA0_C3N	5	O	
						PB3	UART1_RTS	6	O	
	15	15	51	19	24	PINCM16	TIMG14_C1	7	I	SDIO (standard)
						0x4042803c	UART7_RX	8	I	
							TIMG12_C1	9	IO	
							TIMA0_C0	10	IO	
							SPI0_SCK	11	IO	
							TIMA1_C1	12	IO	
							TIMG6_C1	13	IO	

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
							PB4	1	IO	
							UART1_TX	2	O	
							UART3_CTS	3	I	
						PB4	TIMA0_C1	4	IO	
			52	20	25	PINCM17	TIMA0_C2	5	IO	SDIO (standard)
						0x40428040	TIMG0_C0	6	IO	
							TIMA1_C0	8	IO	
							TIMA1_C0N	11	O	
							SPI2_PICO	12	IO	
							PB5	1	IO	
							UART1_RX	2	I	
							UART3_RTS	3	O	
						PB5	TIMA0_C1N	4	O	
			53	21	26	PINCM18	TIMA0_C2N	5	O	SDIO (standard)
						0x40428044	TIMG0_C1	6	IO	
							TIMA1_C1	8	IO	
							TIMA1_C1N	11	O	
							SPI2_POCI	12	IO	
							PB6	1	IO	
							UART1_TX	2	O	
							SPI1_CS0	3	IO	
							I2C2_SCL	4	IOD	
						PB6	TIMG8_C0	5	IO	
	20	20	58	30	40	PINCM23	UART7_CTS	6	I	SDIO (standard)
						0x40428058	TIMG14_C3	7	I	
							TIMA_FAL2	8	I	
							SPI0_CS1	9	IO	
							TIMG12_C0	10	IO	
							TIMG6_C0	11	IO	
							TIMA1_C0N	12	O	
							PB7	1	IO	
							UART1_RX	2	I	
							SPI1_POCI	3	IO	
							I2C2_SDA	4	IOD	
						PB7	TIMG8_C1	5	IO	
	21	21	59	31	41	PINCM24	UART7_RTS	6	O	SDIO (standard)
						0x4042805c	TIMG9_C0	7	IO	
							SPI0_CS2	9	IO	
							TIMG12_C1	10	IO	
							TIMG6_C1	11	IO	
							TIMA1_C1N	12	O	

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
	22	22	60	32	42	PB8 PINCM25 0x40428060	PB8	1	IO	SDIO (standard)
							UART1_CTS	2	I	
							SPI1_PICO	3	IO	
							I2C2_SCL	4	IOD	
							TIMA0_C0	5	IO	
							COMP0_OUT	6	O	
							TIMG9_IDX	7	I	
							COMP1_OUT	8	O	
	23	23	61	33	43	PB9 PINCM26 0x40428064	PB9	1	IO	SDIO (standard)
							UART1_RTS	2	O	
							SPI1_SCK	3	IO	
							I2C2_SDA	4	IOD	
							TIMA0_C0N	5	O	
							TIMA0_C1	6	IO	
							TIMG9_C1	13	IO	
			62	34	44	PB10 PINCM27 0x40428068	PB10	1	IO	SDIO (standard)
							TIMG0_C0	2	IO	
							TIMG8_C0	3	IO	
							COMP0_OUT	4	O	
							UART4_TX	6	O	
							SPI1_CS3	7	IO	
							TIMG6_C0	9	IO	
							COMP1_OUT	11	O	
			63	35	45	PB11 PINCM28 0x4042806c	PB11	1	IO	SDIO (standard)
							TIMG0_C1	2	IO	
							TIMG8_C1	3	IO	
							CLK_OUT	4	O	
							UART4_RX	6	I	
							SPI1_CS2	7	IO	
							TIMG6_C1	9	IO	
			64	36	46	PB12 PINCM29 0x40428070	PB12	1	IO	SDIO (standard)
							UART3_TX	2	O	
							TIMA0_C2	3	IO	
							TIMA_FAL1	4	I	
							TIMA0_C1	5	IO	
							UART4_CTS	6	I	
							SPI1_CS1	7	IO	
							TIMG14_C0	10	I	
			1	37	47	PB13 PINCM30 0x40428074	PB13	1	IO	SDIO (standard)
							UART3_RX	2	I	
							TIMA0_C3	3	IO	
							TIMG12_C0	4	IO	
							TIMA0_C1N	5	O	
							UART4_RTS	6	O	
							SPI1_CS0	7	IO	
							TIMG14_C1	10	I	

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
	24	24	2	38	48	PB14 PINCM31 0x40428078	PB14	1	IO	SDIO (standard)
							SPI1_CS3	2	IO	
							SPI1_POCI	3	IO	
							TIMG12_C1	4	IO	
							TIMA0_C0	5	IO	
							TIMG8_IDX	6	I	
							SPI0_CS3	7	IO	
	25	25	3	39	49	PB15 PINCM32 0x4042807c	PB15	1	IO	SDIO (standard)
							UART7_TX	2	O	
							SPI1_PICO	3	IO	
							UART3_CTS	4	I	
							TIMG8_C0	5	IO	
							I2C2_SCL	7	IOD	
							TIMG7_C0	11	IO	
	26	26	4	40	50	PB16 PINCM33 0x40428080	PB16	1	IO	SDIO (standard)
							UART7_RX	2	I	
							SPI1_SCK	3	IO	
							UART3_RTS	4	O	
							TIMG8_C1	5	IO	
							I2C2_SDA	7	IOD	
							TIMG7_C1	11	IO	
	36	36	14	58	73	PB17 PINCM43 0x404280a8	PB17	1	IO	SDIO (standard)
							UART7_TX	2	O	
							SPI0_PICO	3	IO	
							I2C0_SCL	4	IOD	
							TIMA0_C2	5	IO	
							TIMG0_C0	6	IO	
							SPI1_CS1	7	IO	
							UART4_TX	8	O	
							TIMG14_C2	9	I	
							TIMA1_C0	11	IO	
							A1_4	(Non-IOMUX 1) 0	A	
							COMP1_IN2-	(Non-IOMUX 2) 0	A	
	37	37	15	59	74	PB18 PINCM44 0x404280ac	PB18	1	IO	SDIO (standard)
							UART7_RX	2	I	
							SPI0_SCK	3	IO	
							I2C0_SDA	4	IOD	
							TIMA0_C2N	5	O	
							TIMG0_C1	6	IO	
							SPI1_CS2	7	IO	
							UART4_RX	8	I	
							TIMG14_C3	9	I	
							TIMA1_C1	11	IO	
							A1_5	(Non-IOMUX 1) 0	A	
							COMP1_IN2+	(Non-IOMUX 2) 0	A	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
	38	38	16	60	75	PB19 PINCM45 0x404280b0	PB19	1	IO	SDIO (standard)
							COMP0_OUT	2	O	
							SPI0_POCI	3	IO	
							TIMG8_C1	4	IO	
							UART0_CTS	5	I	
							COMP2_OUT	6	O	
							TIMG8_IDX	7	I	
							UART7_CTS	8	I	
							UART4_CTS	9	I	
							SPI1_CS3	10	IO	
							TIMG7_C1	11	IO	
							A1_6	(Non-IOMUX 1) 0	A	
							COMP2_IN1+	(Non-IOMUX 2) 0	A	
	41	41	19	67	82	PB20 PINCM48 0x404280bc	PB20	1	IO	SDIO (standard)
							SPI0_CS2	2	IO	
							SPI1_CS0	3	IO	
							TIMG12_C0	4	IO	
							TIMA0_C2	5	IO	
							TIMA_FAL1	6	I	
							TIMA0_C1	7	IO	
							UART7_RTS	8	O	
							I2C0_SDA	9	IOD	
							TIMA1_C1N	10	O	
							A0_6	(Non-IOMUX 1) 0	A	
			20	68	83	PB21 PINCM49 0x404280c0	PB21	1	IO	SDIO (standard)
							UART4_TX	2	O	
							SPI1_POCI	3	IO	
							I2C0_SCL	4	IOD	
							TIMG8_C0	5	IO	
							UART1_TX	6	O	
							CAN1_TX	7	O	
							UART6_RX	9	I	
							A1_8	(Non-IOMUX 1) 0	A	
							COMP2_INO+	(Non-IOMUX 2) 0	A	
			21	69	84	PB22 PINCM50 0x404280c4	PB22	1	IO	SDIO (standard)
							UART4_RX	2	I	
							SPI1_PICO	3	IO	
							I2C0_SDA	4	IOD	
							TIMG8_C1	5	IO	
							UART1_RX	6	I	
							CAN1_RX	7	I	
							UART6_TX	9	O	
							A1_10	(Non-IOMUX 1) 0	A	
							COMP2_IN0-	(Non-IOMUX 2) 0	A	

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
							PB23	1	IO	
							UART1_CTS	2	I	
						PB23	SPI1_SCK	3	IO	
			22	70	85	PINCM51	TIMA_FAL0	4	I	SDIO (standard)
						0x404280c8	COMP0_OUT	5	O	
							UART6_CTS	9	I	
							A1_11	(Non-IOMUX 1) 0	A	
							PB24	1	IO	
							SPI0_CS3	2	IO	
							SPI0_CS1	3	IO	
							TIMG12_C1	4	IO	
							TIMA0_C3	5	IO	
						PB24	TIMA0_C1N	6	O	
	42	42	23	71	86	PINCM52	SPI1_CS1	7	IO	SDIO (standard)
						0x404280cc	UART7_RTS	8	O	
							UART6_RTS	9	O	
							TIMA1_C0N	10	O	
							A0_5	(Non-IOMUX 1) 0	A	
							COMP1_IN1+	(Non-IOMUX 2) 0	A	
							PB25	1	IO	
							UART0_CTS	2	I	
							SPI0_CS0	3	IO	
						PB25	TIMA_FAL0	4	I	
			27	75	95	PINCM56	TIMA_FAL1	5	I	SDIO (standard)
						0x404280dc	TIMA_FAL2	6	I	
							COMP0_OUT	7	O	
							FCC_IN	8	I	
							A0_4	(Non-IOMUX 1) 0	A	
							PB26	1	IO	
							UART0_RTS	2	O	
							SPI0_CS1	3	IO	
							TIMA0_C0	4	IO	
						PB26	TIMA0_C3	5	IO	
			28	76	96	PINCM57	COMP0_OUT	7	O	SDIO (standard)
						0x404280e0	FCC_IN	8	I	
							TIMA1_C0	9	IO	
							TIMG6_C0	11	IO	
							A1_13	(Non-IOMUX 1) 0	A	
							COMP1_IN0+	(Non-IOMUX 2) 0	A	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
							PB27	1	IO	
							COMP0_OUT	2	O	
							SPI1_CS1	3	IO	
							TIMA0_C0N	4	O	
						PB27	TIMA0_C3N	5	O	
			29	77	97	PINCM58	COMP2_OUT	6	O	SDIO (standard)
						0x404280e4	TIMA1_C1	9	IO	
							TIMG6_C1	11	IO	
							A1_14	(Non-IOMUX 1) 0	A	
							COMP1_IN0-	(Non-IOMUX 2) 0	A	
							PB28	1	IO	
							I2C2_SCL	2	IOD	
							SPI1_CS0	3	IO	
						PB28	TIMA_FAL0	4	I	
				24	29	PINCM65	TIMA0_C0	5	IO	SDIO (standard)
						0x40428100	TIMG0_C0	6	IO	
							UART5_RX	7	I	
							TIMG14_C0	10	I	
							UART6_RX	12	I	
							PB29	1	IO	
							I2C2_SDA	2	IOD	
							SPI1_POCI	3	IO	
						PB29	TIMA_FAL1	4	I	
				25	30	PINCM66	TIMA0_C0N	5	O	SDIO (standard)
						0x40428104	TIMG0_C1	6	IO	
							UART5_TX	7	O	
							TIMG9_C0	8	IO	
							TIMG14_C1	10	I	
							UART6_TX	12	O	
							PB30	1	IO	
							UART1_CTS	2	I	
							SPI1_PICO	3	IO	
						PB30	TIMA_FAL2	4	I	
				26	31	PINCM67	TIMA0_C1	5	IO	SDIO (standard)
						0x40428108	UART5_CTS	7	I	
							TIMG9_C1	8	IO	
							TIMG14_C2	9	I	
							UART6_CTS	12	I	
							PB31	1	IO	
							UART1_RTS	2	O	
							SPI1_SCK	3	IO	
						PB31	TIMG8_IDX	4	I	
				27	32	PINCM68	TIMA0_C1N	5	O	SDIO (standard)
						0x4042810c	UART5_RTS	7	O	
							TIMG9_IDX	8	I	
							TIMG14_C3	9	I	
							UART6_RTS	12	O	

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
				46	56	PC0 PINCM74 0x40428124	PC0	1	IO	SDIO (standard)
							UART1_TX	2	O	
							SPI1_CS3	3	IO	
							TIMG8_C0	4	IO	
							TIMA0_C2	5	IO	
				47	57	PC1 PINCM75 0x40428128	PC1	1	IO	SDIO (standard)
							UART1_RX	2	I	
							SPI1_CS2	3	IO	
							TIMG8_C1	4	IO	
							TIMA0_C2N	5	O	
				50	65	PC2 PINCM76 0x4042812c	PC2	1	IO	SDIO (standard)
							I2C2_SCL	2	IOD	
							SPI1_CS0	3	IO	
							TIMA_FAL0	4	I	
							TIMA0_C0	5	IO	
							TIMG0_C0	6	IO	
				51	66	PC3 PINCM77 0x40428130	PC3	1	IO	SDIO (standard)
							I2C2_SDA	2	IOD	
							SPI1_CS1	3	IO	
							TIMA_FAL1	4	I	
							TIMA0_C0N	5	O	
							TIMG0_C1	6	IO	
				52	67	PC4 PINCM78 0x40428134	PC4	1	IO	SDIO (standard)
							UART3_CTS	2	I	
							SPI1_CS2	3	IO	
							TIMA_FAL2	4	I	
							TIMA0_C1	5	IO	
							TIMG14_C2	7	I	
				53	68	PC5 PINCM79 0x40428138	PC5	1	IO	SDIO (standard)
							UART3_RTS	2	O	
							SPI1_CS3	3	IO	
							TIMG8_IDX	4	I	
							TIMA0_C1N	5	O	
							TIMG14_C3	7	I	
				63	78	PC6 PINCM84 0x4042814c	PC6	1	IO	SDIO (standard)
							UART3_TX	2	O	
							SPI0_CS1	3	IO	
							TIMG8_C0	4	IO	
							TIMA0_C0	5	IO	
				64	79	PC7 PINCM85 0x40428150	PC7	1	IO	SDIO (standard)
							UART3_RX	2	I	
							SPI0_CS0	3	IO	
							TIMG8_C1	4	IO	
							TIMA0_C0N	5	O	
				65	80	PC8 PINCM86 0x40428154	PC8	1	IO	SDIO (standard)
							UART3_CTS	2	I	
							SPI1_CS2	3	IO	
							TIMA0_C1	5	IO	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
				66	81	PC9 PINCM87 0x40428158	PC9	1	IO	SDIO (standard)
							UART3_RTS	2	O	
							SPI1_CS1	3	IO	
							TIMA0_C1N	5	O	
					87	PC10 PINCM88 0x4042815c	PC10	1	IO	SDIO (standard)
							TIMG9_C0	7	IO	
							UART6_RX	8	I	
					88	PC11 PINCM89 0x40428160	PC11	1	IO	SDIO (standard)
							TIMG9_C1	7	IO	
							UART6_TX	8	O	
					10	PC12 PINCM61 0x404280f0	PC12	1	IO	SDIO (standard)
					12	PC13 PINCM62 0x404280f4	PC13	1	IO	SDIO (standard)
							SPI2_PICO	12	IO	
					13	PC14 PINCM63 0x404280f8	PC14	1	IO	SDIO (standard)
							TIMG9_C1	7	IO	
							SPI2_SCK	12	IO	
					11	PC15 PINCM64 0x404280fc	PC15	1	IO	SDIO (standard)
					35	PC16 PINCM69 0x40428110	PC16	1	IO	SDIO (standard)
					36	PC17 PINCM70 0x40428114	PC17	1	IO	SDIO (standard)
							TIMG14_C2	7	I	
					38	PC18 PINCM71 0x40428118	PC18	1	IO	SDIO (standard)
					39	PC19 PINCM72 0x4042811c	PC19	1	IO	SDIO (standard)
							TIMG9_C1	7	IO	
					58	PC20 PINCM73 0x40428120	PC20	1	IO	SDIO (standard)
					59	PC21 PINCM80 0x4042813c	PC21	1	IO	SDIO (standard)
							CAN1_TX	7	O	
					60	PC22 PINCM81 0x40428140	PC22	1	IO	SDIO (standard)
							CAN1_RX	7	I	
					61	PC23 PINCM82 0x40428144	PC23	1	IO	SDIO (standard)
					62	PC24 PINCM83 0x40428148	PC24	1	IO	SDIO (standard)
					89	PC25 PINCM90 0x40428164	PC25	1	IO	SDIO (standard)
							TIMG9_IDX	7	I	
							UART6_CTS	8	I	

Table 6-2. Pin Attributes (PN, RHB, PZ, RGZ, PM, PT Packages) (continued)

RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
					90	PC26 PINCM91 0x40428168	PC26	1	IO	SDIO (standard)
							CAN1_TX	7	O	
							UART6_RTS	8	O	
					91	PC27 PINCM92 0x4042816c	PC27	1	IO	SDIO (standard)
							CAN1_RX	7	I	
					14	PC28 PINCM93 0x40428170	PC28	1	IO	SDIO (standard)
							UART5_RX	7	I	
					37	PC29 PINCM94 0x40428174	PC29	1	IO	SDIO (standard)
							UART5_TX	7	O	
32	48	48	32	80	100	VCORE	VCORE	(Non-IOMUX 1) 0	PWR	PWR
4	6	6	40	49, 8	64, 8	VDD	VDD	(Non-IOMUX 1) 0	PWR	PWR
5	7	7	41	48, 9	63, 9	VSS	VSS	(Non-IOMUX 1) 0	PWR	PWR

6.3 Signal Descriptions

Many MSPM0 signals are made available on multiple device pins. The following list describes the column headers:

1. **SIGNAL NAME**: The name of the signal which can be connected to one of the specified pins.
2. **PIN TYPE**: The signal direction and signal type:
   - I = Input
   - O = Output
   - IO = Input, output, or simultaneous input and output
   - ID = Input with open-drain behavior
   - OD = Output with open-drain behavior
   - IOD = Input, output, or simultaneous input and output with open-drain behavior
   - A = Analog
   - PWR = Power function
3. **DESCRIPTION**: A description of the signal.
4. **PIN**: Associated pin number.

For additional information on the pin multiplexing scheme, refer to the IOMUX chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

Note

The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
A0_0	A	ADC0 analog input channel 0	31	47	47	31	79	99
A0_1	A	ADC0 analog input channel 1	30	46	46	30	78	98
A0_2	A	ADC0 analog input channel 2	29	45	45	26	74	94
A0_3	A	ADC0 analog input channel 3	28	44	44	25	73	93
A0_4	A	ADC0 analog input channel 4				27	75	95

ADVANCE INFORMATION

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
A0_5	A	ADC0 analog input channel 5		42	42	23	71	86
A0_6	A	ADC0 analog input channel 6		41	41	19	67	82
A0_7	A	ADC0 analog input channel 7	26	40	40	18	62	77
A0_8	A	ADC0 analog input channel 8	16	27	27	5	41	51
A0_9	A	ADC0 analog input channel 9	17	28	28	6	42	52
A0_12	A	ADC0 analog input channel 12	18	29	29	7	43	53
A0_13	A	ADC0 analog input channel 13	23	34	34	12	56	71
A0_14	A	ADC0 analog input channel 14	24	35	35	13	57	72
A1_0	A	ADC1 analog input channel 0	19	30	30	8	44	54
A1_1	A	ADC1 analog input channel 1	20	31	31	9	45	55
A1_2	A	ADC1 analog input channel 2	21	32	32	10	54	69
A1_3	A	ADC1 analog input channel 3	22	33	33	11	55	70
A1_4	A	ADC1 analog input channel 4		36	36	14	58	73
A1_5	A	ADC1 analog input channel 5		37	37	15	59	74
A1_6	A	ADC1 analog input channel 6		38	38	16	60	75
A1_7	A	ADC1 analog input channel 7	25	39	39	17	61	76
A1_8	A	ADC1 analog input channel 8				20	68	83
A1_10	A	ADC1 analog input channel 10				21	69	84
A1_11	A	ADC1 analog input channel 11				22	70	85
A1_12	A	ADC1 analog input channel 12	27	43	43	24	72	92
A1_13	A	ADC1 analog input channel 13				28	76	96
A1_14	A	ADC1 analog input channel 14				29	77	97

Table 6-4. Bootstrap Loader (BSL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
BSLRX	I	BSL UART receive signal (RXD)	15	19	19	57	29	34
BSLSCL	IOD	BSL I2C clock signal (SCL)	2	2	2	34	2	2
BSLSDA	IOD	BSL I2C data signal (SDA)	1	1	1	33	1	1
BSLTX	O	BSL UART transmit signal (TXD)	14	18	18	56	28	33
BSL_invoke	I	BSL invoke signal (if BSL is enabled, must be HIGH during BOOTRST for a BSL entry, and LOW during BOOTRST to prevent BSL entry)	22	33	33	11	55	70

Table 6-5. Clock Module (CKM) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
CLK_OUT	O	CLK_OUT digital clock output from the PMCU	11, 13, 14, 18, 26, 31	13, 17, 18, 29, 40, 47, 5	13, 17, 18, 29, 40, 47, 5	18, 31, 39, 49, 55, 56, 63, 7	17, 23, 28, 35, 43, 62, 7, 79	22, 28, 33, 45, 53, 7, 77, 99
FCC_IN	I	Frequency clock counter (FCC) input signal	1, 11, 16, 20, 9	1, 11, 13, 27, 31	1, 11, 13, 27, 31	27, 28, 33, 45, 49, 5, 9	1, 13, 17, 41, 45, 75, 76	1, 18, 22, 51, 55, 95, 96
HFCLK_IN	I	High frequency clock digital clock input signal	10, 12	12, 14, 16	12, 14, 16	46, 50, 54	14, 18, 22	19, 23, 27

Table 6-5. Clock Module (CKM) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
HFXIN	A	High frequency crystal oscillator (HFXT) signal	9	11	11	45	13	18
HFXOUT	A	High frequency crystal oscillator (HFXT) signal	10	12	12	46	14	19
LFCLK_IN	I	Low frequency clock digital clock input signal	8	10	10	44	12	17
LFXIN	A	Low frequency crystal oscillator (LFXT) signal	7	9	9	43	11	16
LFXOUT	A	Low frequency crystal oscillator (LFXT) signal	8	10	10	44	12	17
ROSC	A	SYSOSC frequency correction loop (FCL) external resistor signal	6	8	8	42	10	15

Table 6-6. Comparator (COMP) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
COMP0_OUT	O	COMP0 digital output signal	11, 15, 16, 20, 29, 31, 7	13, 19, 22, 27, 31, 38, 45, 47, 9	13, 19, 22, 27, 31, 38, 45, 47, 9	16, 22, 26, 27, 28, 29, 31, 43, 49, 5, 57, 60, 62, 9	11, 17, 29, 32, 34, 41, 45, 60, 70, 74, 75, 76, 77, 79	16, 22, 34, 42, 44, 51, 55, 75, 85, 94, 95, 96, 97, 99
COMP1_OUT	O	COMP1 digital output signal	7	22, 9	22, 9	43, 60, 62	11, 32, 34	16, 42, 44
COMP2_OUT	O	COMP2 digital output signal	20	31, 38	31, 38	16, 29, 9	45, 60, 77	55, 75, 97
COMP0_IN0+	A	COMP0 non-inverting input channel 0	30	46	46	30	78	98
COMP0_IN0-	A	COMP0 inverting input channel 0	31	47	47	31	79	99
COMP0_IN1+	A	COMP0 non-inverting input channel 1	22	33	33	11	55	70
COMP0_IN1-	A	COMP0 inverting input channel 1	21	32	32	10	54	69
COMP0_IN2+	A	COMP0 non-inverting input channel 2	18	29	29	7	43	53
COMP0_IN2-	A	COMP0 inverting input channel 2	17	28	28	6	42	52
COMP0_IN3+	A	COMP0 non-inverting input channel 3	19	30	30	8	44	54
COMP1_IN0+	A	COMP1 non-inverting input channel 0				28	76	96
COMP1_IN0-	A	COMP1 inverting input channel 0				29	77	97
COMP1_IN1+	A	COMP1 non-inverting input channel 1		42	42	23	71	86
COMP1_IN1-	A	COMP1 inverting input channel 1	27	43	43	24	72	92
COMP1_IN2+	A	COMP1 non-inverting input channel 2		37	37	15	59	74
COMP1_IN2-	A	COMP1 inverting input channel 2		36	36	14	58	73
COMP1_IN3+	A	COMP1 non-inverting input channel 3	19	30	30	8	44	54
COMP2_IN0+	A	COMP2 non-inverting input channel 0				20	68	83
COMP2_IN0-	A	COMP2 inverting input channel 0				21	69	84
COMP2_IN1+	A	COMP2 non-inverting input channel 1		38	38	16	60	75
COMP2_IN1-	A	COMP2 inverting input channel 1	25	39	39	17	61	76

Table 6-7. Controller Area Network (CAN) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
CAN0_RX	I	CAN0 receive signal (TXD)	17, 31	28, 47	28, 47	31, 6	42, 79	52, 99

ADVANCE INFORMATION

Table 6-7. Controller Area Network (CAN) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
CAN0_TX	O	CAN0 transmit signal (TXD)	16, 30	27, 46	27, 46	30, 5	41, 78	51, 98
CAN1_RX	I	CAN1 receive signal (TXD)				21	69	60, 84, 91
CAN1_TX	O	CAN1 transmit signal (TXD)				20	68	59, 83, 90

Table 6-8. Digital to Analog Converter (DAC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
DAC_OUT	O	DAC output	19	30	30	8	44	54

Table 6-9. General Purpose Input Output Module Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
PA0	IO	GPIO port A input/output 0	1	1	1	33	1	1
PA1	IO	GPIO port A input/output 1	2	2	2	34	2	2
PA2	IO	GPIO port A input/output 2	6	8	8	42	10	15
PA3	IO	GPIO port A input/output 3	7	9	9	43	11	16
PA4	IO	GPIO port A input/output 4	8	10	10	44	12	17
PA5	IO	GPIO port A input/output 5	9	11	11	45	13	18
PA6	IO	GPIO port A input/output 6	10	12	12	46	14	19
PA7	IO	GPIO port A input/output 7	11	13	13	49	17	22
PA8	IO	GPIO port A input/output 8	12	16	16	54	22	27
PA9	IO	GPIO port A input/output 9	13	17	17	55	23	28
PA10	IO	GPIO port A input/output 10	14	18	18	56	28	33
PA11	IO	GPIO port A input/output 11	15	19	19	57	29	34
PA12	IO	GPIO port A input/output 12	16	27	27	5	41	51
PA13	IO	GPIO port A input/output 13	17	28	28	6	42	52
PA14	IO	GPIO port A input/output 14	18	29	29	7	43	53
PA15	IO	GPIO port A input/output 15	19	30	30	8	44	54
PA16	IO	GPIO port A input/output 16	20	31	31	9	45	55
PA17	IO	GPIO port A input/output 17	21	32	32	10	54	69
PA18	IO	GPIO port A input/output 18	22	33	33	11	55	70
PA19	IO	GPIO port A input/output 19	23	34	34	12	56	71
PA20	IO	GPIO port A input/output 20	24	35	35	13	57	72
PA21	IO	GPIO port A input/output 21	25	39	39	17	61	76
PA22	IO	GPIO port A input/output 22	26	40	40	18	62	77
PA23	IO	GPIO port A input/output 23	27	43	43	24	72	92
PA24	IO	GPIO port A input/output 24	28	44	44	25	73	93
PA25	IO	GPIO port A input/output 25	29	45	45	26	74	94
PA26	IO	GPIO port A input/output 26	30	46	46	30	78	98
PA27	IO	GPIO port A input/output 27	31	47	47	31	79	99
PA28	IO	GPIO port A input/output 28		3	3	35	3	3
PA29	IO	GPIO port A input/output 29				36	4	4
PA30	IO	GPIO port A input/output 30				37	5	5
PA31	IO	GPIO port A input/output 31		5	5	39	7	7

ADVANCE INFORMATION

Table 6-9. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
PB0	IO	GPIO port B input/output 0				47	15	20
PB1	IO	GPIO port B input/output 1				48	16	21
PB2	IO	GPIO port B input/output 2		14	14	50	18	23
PB3	IO	GPIO port B input/output 3		15	15	51	19	24
PB4	IO	GPIO port B input/output 4				52	20	25
PB5	IO	GPIO port B input/output 5				53	21	26
PB6	IO	GPIO port B input/output 6		20	20	58	30	40
PB7	IO	GPIO port B input/output 7		21	21	59	31	41
PB8	IO	GPIO port B input/output 8		22	22	60	32	42
PB9	IO	GPIO port B input/output 9		23	23	61	33	43
PB10	IO	GPIO port B input/output 10				62	34	44
PB11	IO	GPIO port B input/output 11				63	35	45
PB12	IO	GPIO port B input/output 12				64	36	46
PB13	IO	GPIO port B input/output 13				1	37	47
PB14	IO	GPIO port B input/output 14		24	24	2	38	48
PB15	IO	GPIO port B input/output 15		25	25	3	39	49
PB16	IO	GPIO port B input/output 16		26	26	4	40	50
PB17	IO	GPIO port B input/output 17		36	36	14	58	73
PB18	IO	GPIO port B input/output 18		37	37	15	59	74
PB19	IO	GPIO port B input/output 19		38	38	16	60	75
PB20	IO	GPIO port B input/output 20		41	41	19	67	82
PB21	IO	GPIO port B input/output 21				20	68	83
PB22	IO	GPIO port B input/output 22				21	69	84
PB23	IO	GPIO port B input/output 23				22	70	85
PB24	IO	GPIO port B input/output 24		42	42	23	71	86
PB25	IO	GPIO port B input/output 25				27	75	95
PB26	IO	GPIO port B input/output 26				28	76	96
PB27	IO	GPIO port B input/output 27				29	77	97
PB28	IO	GPIO port B input/output 28					24	29
PB29	IO	GPIO port B input/output 29					25	30
PB30	IO	GPIO port B input/output 30					26	31
PB31	IO	GPIO port B input/output 31					27	32
PC0	IO	GPIO port C input/output 0					46	56
PC1	IO	GPIO port C input/output 1					47	57
PC2	IO	GPIO port C input/output 2					50	65
PC3	IO	GPIO port C input/output 3					51	66
PC4	IO	GPIO port C input/output 4					52	67
PC5	IO	GPIO port C input/output 5					53	68
PC6	IO	GPIO port C input/output 6					63	78
PC7	IO	GPIO port C input/output 7					64	79
PC8	IO	GPIO port C input/output 8					65	80
PC9	IO	GPIO port C input/output 9					66	81
PC10	IO	GPIO port C input/output 10						87
PC11	IO	GPIO port C input/output 11						88

ADVANCE INFORMATION

Table 6-9. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
PC12	IO	GPIO port C input/output 12						10
PC13	IO	GPIO port C input/output 13						12
PC14	IO	GPIO port C input/output 14						13
PC15	IO	GPIO port C input/output 15						11
PC16	IO	GPIO port C input/output 16						35
PC17	IO	GPIO port C input/output 17						36
PC18	IO	GPIO port C input/output 18						38
PC19	IO	GPIO port C input/output 19						39
PC20	IO	GPIO port C input/output 20						58
PC21	IO	GPIO port C input/output 21						59
PC22	IO	GPIO port C input/output 22						60
PC23	IO	GPIO port C input/output 23						61
PC24	IO	GPIO port C input/output 24						62
PC25	IO	GPIO port C input/output 25						89
PC26	IO	GPIO port C input/output 26						90
PC27	IO	GPIO port C input/output 27						91
PC28	IO	GPIO port C input/output 28						14
PC29	IO	GPIO port C input/output 29						37

Table 6-10. I2C Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
I2C0_SCL	IOD	I2C0 serial clock signal (SCL)	13, 15, 2, 26	17, 19, 2, 36, 40, 5	17, 19, 2, 36, 40, 5	14, 18, 20, 34, 39, 47, 55, 57	15, 2, 23, 29, 58, 62, 68, 7	2, 20, 28, 34, 7, 73, 77, 83
I2C0_SDA	IOD	I2C0 serial data signal (SDA)	1, 12, 14	1, 16, 18, 3, 37, 41	1, 16, 18, 3, 37, 41	15, 19, 21, 33, 35, 48, 54, 56	1, 16, 22, 28, 3, 59, 67, 69	1, 21, 27, 3, 33, 74, 82, 84
I2C1_SCL	IOD	I2C1 serial clock signal (SCL)	10, 15, 19, 21, 24, 8	10, 12, 14, 19, 30, 32, 35	10, 12, 14, 19, 30, 32, 35	10, 13, 36, 44, 46, 50, 57, 8	12, 14, 18, 29, 4, 44, 54, 57	17, 19, 23, 34, 4, 54, 69, 72
I2C1_SDA	IOD	I2C1 serial data signal (SDA)	14, 20, 22, 23, 7, 9	11, 15, 18, 31, 33, 34, 9	11, 15, 18, 31, 33, 34, 9	11, 12, 37, 43, 45, 51, 56, 9	11, 13, 19, 28, 45, 5, 55, 56	16, 18, 24, 33, 5, 55, 70, 71
I2C2_SCL	IOD	I2C2 serial clock signal (SCL)	19, 27	20, 22, 25, 30, 43	20, 22, 25, 30, 43	24, 3, 36, 58, 60, 8	24, 30, 32, 39, 4, 44, 50, 72	29, 4, 40, 42, 49, 54, 65, 92
I2C2_SDA	IOD	I2C2 serial data signal (SDA)	20, 28	21, 23, 26, 31, 44	21, 23, 26, 31, 44	25, 37, 4, 59, 61, 9	25, 31, 33, 40, 45, 5, 51, 73	30, 41, 43, 5, 50, 55, 66, 93

Table 6-11. IOMUX Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
WAKE	I	Input signal to wake the device from SHUTDOWN mode	1, 14, 15, 2, 21, 22, 3	1, 18, 19, 2, 3, 32, 33, 4, 5	1, 18, 19, 2, 3, 32, 33, 4, 5	10, 11, 33, 34, 35, 38, 39, 56, 57	1, 2, 28, 29, 3, 54, 55, 6, 7	1, 2, 3, 33, 34, 6, 69, 7, 70

Table 6-12. Power Management Unit (PMU) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
VCORE	PWR	VCORE capacitor connection	32	48	48	32	80	100
VDD	PWR	VDD supply	4	6	6	40	49, 8	64, 8
VSS	PWR	VSS (ground)	5	7	7	41	48, 9	63, 9

Table 6-13. Real-time Clock (RTC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
RTC_OUT	O	Real-time clock output signal	13, 17, 31	17, 28, 47	17, 28, 47	31, 55, 6	23, 42, 79	28, 52, 99

Table 6-14. Serial Peripheral Interface (SPI) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
SPI0_PICO	IO	SPI0 peripheral in controller out signal	13, 18, 9	11, 14, 17, 29, 36	11, 14, 17, 29, 36	14, 45, 50, 55, 7	13, 18, 23, 43, 58	18, 23, 28, 53, 73
SPI0_POCI	IO	SPI0 peripheral out controller in signal	11, 14, 17, 8	10, 13, 18, 28, 38	10, 13, 18, 28, 38	16, 44, 49, 56, 6	12, 17, 28, 42, 60	17, 22, 33, 52, 75
SPI0_SCK	IO	SPI0 serial clock	10, 15, 16	12, 15, 19, 27, 37	12, 15, 19, 27, 37	15, 46, 5, 51, 57	14, 19, 29, 41, 59	19, 24, 34, 51, 74
SPI1_PICO	IO	SPI1 peripheral in controller out signal	22	22, 25, 33	22, 25, 33	11, 21, 3, 60	26, 32, 39, 55, 69	31, 42, 49, 70, 84
SPI1_POCI	IO	SPI1 peripheral out controller in signal	20, 23	21, 24, 31, 34	21, 24, 31, 34	12, 2, 20, 59, 9	25, 31, 38, 45, 56, 68	30, 41, 48, 55, 71, 83
SPI1_SCK	IO	SPI1 serial clock	21, 24	23, 26, 32, 35	23, 26, 32, 35	10, 13, 22, 4, 61	27, 33, 40, 54, 57, 70	32, 43, 50, 69, 72, 85
SPI2_PICO	IO	SPI2 peripheral in controller out signal				52	20	12, 25
SPI2_POCI	IO	SPI2 peripheral out controller in signal	6	8	8	42, 53	10, 21	15, 26
SPI2_SCK	IO	SPI2 serial clock	14	18	18	56	28	13, 33
SPI0_CS0	IO	SPI0 chip select 0 signal	12, 22, 6, 8	10, 16, 33, 8	10, 16, 33, 8	11, 27, 42, 44, 54	10, 12, 22, 55, 64, 75	15, 17, 27, 70, 79, 95
SPI0_CS1	IO	SPI0 chip select 1 signal	16, 21, 7	20, 27, 32, 42, 9	20, 27, 32, 42, 9	10, 23, 28, 43, 5, 58	11, 30, 41, 54, 63, 71, 76	16, 40, 51, 69, 78, 86, 96

ADVANCE INFORMATION

Table 6-14. Serial Peripheral Interface (SPI) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
SPI0_CS2	IO	SPI0 chip select 2 signal	11, 18, 26, 28	13, 21, 29, 40, 41, 44	13, 21, 29, 40, 41, 44	18, 19, 25, 37, 48, 49, 59, 7	16, 17, 31, 43, 5, 62, 67, 73	21, 22, 41, 5, 53, 77, 82, 93
SPI0_CS3	IO	SPI0 chip select 3 signal	12, 17, 2, 25, 27, 7	16, 2, 24, 28, 39, 42, 43, 5, 9	16, 2, 24, 28, 39, 42, 43, 5, 9	17, 2, 23, 24, 34, 36, 39, 43, 47, 54, 6	11, 15, 2, 22, 38, 4, 42, 61, 7, 71, 72	16, 2, 20, 27, 4, 48, 52, 7, 76, 86, 92
SPI1_CS0	IO	SPI1 chip select 0 signal	17, 30, 6	20, 28, 41, 46, 8	20, 28, 41, 46, 8	1, 19, 30, 42, 58, 6	10, 24, 30, 37, 42, 50, 67, 78	15, 29, 40, 47, 52, 65, 82, 98
SPI1_CS1	IO	SPI1 chip select 1 signal	16, 25, 27, 31	27, 36, 39, 42, 43, 47	27, 36, 39, 42, 43, 47	14, 17, 23, 24, 29, 31, 5, 64	36, 41, 51, 58, 61, 66, 71, 72, 77, 79	46, 51, 66, 73, 76, 81, 86, 92, 97, 99
SPI1_CS2	IO	SPI1 chip select 2 signal	18, 19, 28	29, 30, 37, 44	29, 30, 37, 44	15, 25, 47, 63, 7, 8	15, 35, 43, 44, 47, 52, 59, 65, 73	20, 45, 53, 54, 57, 67, 74, 80, 93
SPI1_CS3	IO	SPI1 chip select 3 signal	29	24, 38, 45	24, 38, 45	16, 2, 26, 48, 62	16, 34, 38, 46, 53, 60, 74	21, 44, 48, 56, 68, 75, 94
SPI2_CS0	IO	SPI2 chip select 0 signal	8	10	10	44	12	17
SPI2_CS1	IO	SPI2 chip select 1 signal	9	11	11	45	13	18
SPI2_CS2	IO	SPI2 chip select 2 signal	10	12	12	46	14	19
SPI2_CS3	IO	SPI2 chip select 3 signal				47	15	20

Table 6-15. Serial Wire Debug (SWD) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
SWCLK	I	Serial wire debug interface clock input signal	24	35	35	13	57	72
SWDIO	IO	Serial wire debug interface data input/ output signal	23	34	34	12	56	71

Table 6-16. System Controller (SYSCTL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
NRST	I	Active-low reset signal (must be logic high for the device to start)	3	4	4	38	6	6

Table 6-17. Timer (TIMx) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
TIMA0_C0	IO	TIMA0 capture/compare 0 signal	1, 12, 25, 6	1, 15, 16, 22, 24, 39, 8	1, 15, 16, 22, 24, 39, 8	17, 2, 28, 33, 42, 51, 54, 60	1, 10, 19, 22, 24, 32, 38, 50, 61, 63, 76	1, 15, 24, 27, 29, 42, 48, 65, 76, 78, 96
TIMA0_C1	IO	TIMA0 capture/compare 1 signal	11, 13, 2, 26, 7	13, 17, 2, 23, 3, 40, 41, 9	13, 17, 2, 23, 3, 40, 41, 9	18, 19, 34, 35, 43, 49, 52, 55, 61, 64	11, 17, 2, 20, 23, 26, 3, 33, 36, 52, 62, 65, 67	16, 2, 22, 25, 28, 3, 31, 43, 46, 67, 77, 80, 82
TIMA0_C2	IO	TIMA0 capture/compare 2 signal	11, 14, 19, 23, 7	13, 18, 30, 34, 36, 41, 9	13, 18, 30, 34, 36, 41, 9	12, 14, 19, 43, 47, 49, 52, 56, 64, 8	11, 15, 17, 20, 28, 36, 44, 46, 56, 58, 67	16, 20, 22, 25, 33, 46, 54, 56, 71, 73, 82
TIMA0_C3	IO	TIMA0 capture/compare 3 signal	16, 21, 27, 29, 8	10, 14, 27, 3, 32, 42, 43, 45	10, 14, 27, 3, 32, 42, 43, 45	1, 10, 23, 24, 26, 28, 35, 44, 5, 50	12, 18, 3, 37, 41, 54, 71, 72, 74, 76	17, 23, 3, 47, 51, 69, 86, 92, 94, 96
TIMA0_C0N	O	TIMA0 capture/compare 0 complementary output	13, 26	17, 23, 40	17, 23, 40	18, 29, 55, 61	23, 25, 33, 51, 62, 64, 77	28, 30, 43, 66, 77, 79, 97
TIMA0_C1N	O	TIMA0 capture/compare 1 complementary output	29, 8	10, 42, 45	10, 42, 45	1, 23, 26, 44, 53	12, 21, 27, 37, 53, 66, 71, 74	17, 26, 32, 47, 68, 81, 86, 94
TIMA0_C2N	O	TIMA0 capture/compare 2 complementary output	10, 15, 20, 24, 6	12, 19, 31, 35, 37, 8	12, 19, 31, 35, 37, 8	13, 15, 42, 46, 48, 53, 57, 9	10, 14, 16, 21, 29, 45, 47, 57, 59	15, 19, 21, 26, 34, 55, 57, 72, 74
TIMA0_C3N	O	TIMA0 capture/compare 3 complementary output	17, 22, 28, 30, 6	15, 28, 33, 44, 46, 5, 8	15, 28, 33, 44, 46, 5, 8	11, 25, 29, 30, 39, 42, 51, 6	10, 19, 42, 55, 7, 73, 77, 78	15, 24, 52, 7, 70, 93, 97, 98
TIMA1_C0	IO	TIMA1 capture/compare 0 signal	14, 19, 21	14, 18, 3, 30, 32, 36	14, 18, 3, 30, 32, 36	10, 14, 28, 35, 47, 50, 52, 56, 8	15, 18, 20, 28, 3, 44, 54, 58, 76	20, 23, 25, 3, 33, 54, 69, 73, 96
TIMA1_C1	IO	TIMA1 capture/compare 1 signal	15, 20, 22, 28	15, 19, 31, 33, 37, 44, 5	15, 19, 31, 33, 37, 44, 5	11, 15, 25, 29, 39, 48, 51, 53, 57, 9	16, 19, 21, 29, 45, 55, 59, 7, 73, 77	21, 24, 26, 34, 55, 7, 70, 74, 93, 97
TIMA1_C0N	O	TIMA1 capture/compare 0 complementary output	12, 19	16, 20, 30, 42	16, 20, 30, 42	23, 52, 54, 58, 8	20, 22, 30, 44, 71	25, 27, 40, 54, 86
TIMA1_C1N	O	TIMA1 capture/compare 1 complementary output	13, 20	17, 21, 31, 41	17, 21, 31, 41	19, 53, 55, 59, 9	21, 23, 31, 45, 67	26, 28, 41, 55, 82

ADVANCE INFORMATION

Table 6-17. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
TIMA_FAL0	I	Timer fault input 0	10, 12, 15, 30, 6	12, 16, 19, 3, 46, 8	12, 16, 19, 3, 46, 8	22, 27, 30, 35, 42, 46, 54, 57	10, 14, 22, 24, 29, 3, 50, 70, 75, 78	15, 19, 27, 29, 3, 34, 65, 85, 95, 98
TIMA_FAL1	I	Timer fault input 1	1, 14, 6, 9	1, 11, 18, 41, 8	1, 11, 18, 41, 8	19, 27, 33, 42, 45, 56, 64	1, 10, 13, 25, 28, 36, 51, 67, 75	1, 15, 18, 30, 33, 46, 66, 82, 95
TIMA_FAL2	I	Timer fault input 2	12, 2, 31	16, 2, 20, 47	16, 2, 20, 47	27, 31, 34, 54, 58	2, 22, 26, 30, 52, 75, 79	2, 27, 31, 40, 67, 95, 99
TIMG8_IDX	I	TIMG8 quadrature encoder index pulse signal	11, 19, 2	13, 2, 24, 30, 38	13, 2, 24, 30, 38	16, 2, 34, 49, 8	17, 2, 27, 38, 44, 53, 60	2, 22, 32, 48, 54, 68, 75
TIMG9_IDX	I	TIMG9 quadrature encoder index pulse signal	8	10, 22	10, 22	44, 60	12, 27, 32	17, 32, 42, 89
TIMG0_C0	IO	TIMG0 capture/compare 0 signal	1, 14, 16, 23, 27, 9	1, 11, 18, 27, 34, 36, 43	1, 11, 18, 27, 34, 36, 43	12, 14, 24, 33, 45, 47, 5, 52, 56, 62	1, 13, 15, 20, 24, 28, 34, 41, 50, 56, 58, 72	1, 18, 20, 25, 29, 33, 44, 51, 65, 71, 73, 92
TIMG0_C1	IO	TIMG0 capture/compare 1 signal	10, 15, 17, 2, 24, 28	12, 19, 2, 28, 35, 37, 44	12, 19, 2, 28, 35, 37, 44	13, 15, 25, 34, 46, 48, 53, 57, 6, 63	14, 16, 2, 21, 25, 29, 35, 42, 51, 57, 59, 73	19, 2, 21, 26, 30, 34, 45, 52, 66, 72, 74, 93
TIMG12_C0	IO	TIMG12 capture/compare 0 signal	1, 14, 18, 19, 21	1, 14, 18, 20, 29, 30, 32, 41	1, 14, 18, 20, 29, 30, 32, 41	1, 10, 19, 33, 50, 56, 58, 7, 8	1, 18, 28, 30, 37, 43, 44, 54, 67	1, 23, 33, 40, 47, 53, 54, 69, 82
TIMG12_C1	IO	TIMG12 capture/compare 1 signal	15, 18, 2, 20, 22, 29	15, 19, 2, 21, 24, 29, 31, 33, 42, 45, 5	15, 19, 2, 21, 24, 29, 31, 33, 42, 45, 5	11, 2, 23, 26, 34, 39, 51, 57, 59, 7, 9	19, 2, 29, 31, 38, 43, 45, 55, 7, 71, 74	2, 24, 34, 41, 48, 53, 55, 7, 70, 86, 94
TIMG14_C0	I	TIMG14 capture/compare 0 signal		14	14	36, 50, 64	18, 24, 36, 4	23, 29, 4, 46
TIMG14_C1	I	TIMG14 capture/compare 1 signal		15	15	1, 37, 51	19, 25, 37, 5	24, 30, 47, 5
TIMG14_C2	I	TIMG14 capture/compare 2 signal	12	16, 3, 36	16, 3, 36	14, 35, 47, 54	15, 22, 26, 3, 52, 58	20, 27, 3, 31, 36, 67, 73
TIMG14_C3	I	TIMG14 capture/compare 3 signal	13	17, 20, 37	17, 20, 37	15, 36, 48, 55, 58	16, 23, 27, 30, 4, 53, 59	21, 28, 32, 4, 40, 68, 74
TIMG6_C0	IO	TIMG6 capture/compare 0 signal	25, 9	11, 14, 20, 39	11, 14, 20, 39	17, 28, 36, 45, 50, 58, 62	13, 18, 30, 34, 4, 61, 76	18, 23, 4, 40, 44, 76, 96

Table 6-17. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
TIMG6_C1	IO	TIMG6 capture/compare 1 signal	10, 26	12, 15, 21, 40	12, 15, 21, 40	18, 29, 37, 46, 51, 59, 63	14, 19, 31, 35, 5, 62, 77	19, 24, 41, 45, 5, 77, 97
TIMG7_C0	IO	TIMG7 capture/compare 0 signal	21, 27, 30, 7	25, 3, 32, 43, 46, 9	25, 3, 32, 43, 46, 9	10, 24, 3, 30, 35, 43	11, 3, 39, 54, 72, 78	16, 3, 49, 69, 92, 98
TIMG7_C1	IO	TIMG7 capture/compare 1 signal	11, 22, 28, 31, 6, 8	10, 13, 26, 33, 38, 44, 47, 5, 8	10, 13, 26, 33, 38, 44, 47, 5, 8	11, 16, 25, 31, 39, 4, 42, 44, 49	10, 12, 17, 40, 55, 60, 7, 73, 79	15, 17, 22, 50, 7, 70, 75, 93, 99
TIMG8_C0	IO	TIMG8 capture/compare 0 signal	11, 2, 21, 25, 27, 30, 7, 9	11, 13, 2, 20, 25, 32, 39, 43, 46, 9	11, 13, 2, 20, 25, 32, 39, 43, 46, 9	10, 17, 20, 24, 3, 30, 34, 36, 43, 45, 49, 58, 62	11, 13, 17, 2, 30, 34, 39, 4, 46, 54, 61, 63, 68, 72, 78	16, 18, 2, 22, 4, 40, 44, 49, 56, 69, 76, 78, 83, 92, 98
TIMG8_C1	IO	TIMG8 capture/compare 1 signal	1, 10, 22, 26, 28, 31, 6, 8	1, 10, 12, 21, 26, 33, 38, 40, 44, 47, 8	1, 10, 12, 21, 26, 33, 38, 40, 44, 47, 8	11, 16, 18, 21, 25, 31, 33, 37, 4, 42, 44, 46, 59, 63	1, 10, 12, 14, 31, 35, 40, 47, 5, 55, 60, 62, 64, 69, 73, 79	1, 15, 17, 19, 41, 45, 5, 50, 57, 70, 75, 77, 79, 84, 93, 99
TIMG9_C0	IO	TIMG9 capture/compare 0 signal	7	21, 9	21, 9	43, 59	11, 25, 31	16, 30, 41, 87
TIMG9_C1	IO	TIMG9 capture/compare 1 signal	6	23, 8	23, 8	42, 61	10, 26, 33	13, 15, 31, 39, 43, 88

Table 6-18. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
UART0_CTS	I	UART0 clear to send signal	13, 18, 9	11, 17, 29, 38	11, 17, 29, 38	16, 27, 36, 45, 55, 7	13, 23, 4, 43, 60, 75	18, 28, 4, 53, 75, 95
UART0_RTS	O	UART0 ready to send signal	10, 12, 19	12, 16, 30	12, 16, 30	28, 37, 46, 54, 8	14, 22, 44, 5, 76	19, 27, 5, 54, 96
UART0_RX	I	UART0 receive signal (RXD)	15, 2	19, 2, 5	19, 2, 5	34, 39, 48, 57	16, 2, 29, 7	2, 21, 34, 7
UART0_TX	O	UART0 transmit signal (TXD)	1, 14	1, 18, 3	1, 18, 3	33, 35, 47, 56	1, 15, 28, 3	1, 20, 3, 33
UART1_CTS	I	UART1 clear to send signal	16, 25	14, 22, 27, 39	14, 22, 27, 39	17, 22, 5, 50, 60	18, 26, 32, 41, 61, 70	23, 31, 42, 51, 76, 85
UART1_RTS	O	UART1 ready to send signal	17, 26	15, 23, 28, 40	15, 23, 28, 40	18, 51, 6, 61	19, 27, 33, 42, 62	24, 32, 43, 52, 77
UART1_RX	I	UART1 receive signal (RXD)	10, 13, 22, 8	10, 12, 17, 21, 33	10, 12, 17, 21, 33	11, 21, 44, 46, 53, 55, 59	12, 14, 21, 23, 31, 47, 55, 69	17, 19, 26, 28, 41, 57, 70, 84

ADVANCE INFORMATION

Table 6-18. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
UART1_TX	O	UART1 transmit signal (TXD)	12, 21, 7, 9	11, 16, 20, 32, 9	11, 16, 20, 32, 9	10, 20, 43, 45, 52, 54, 58	11, 13, 20, 22, 30, 46, 54, 68	16, 18, 25, 27, 40, 56, 69, 83
UART3_CTS	I	UART3 clear to send signal	16, 27	25, 27, 43	25, 27, 43	24, 3, 5, 52	20, 39, 41, 52, 65, 72	25, 49, 51, 67, 80, 92
UART3_RTS	O	UART3 ready to send signal	17, 28	26, 28, 44	26, 28, 44	25, 4, 53, 6	21, 40, 42, 53, 66, 73	26, 50, 52, 68, 81, 93
UART3_RX	I	UART3 receive signal (RXD)	17, 29, 30, 31	15, 28, 45, 46, 47	15, 28, 45, 46, 47	1, 26, 30, 31, 51, 6	19, 37, 42, 64, 74, 78, 79	24, 47, 52, 79, 94, 98, 99
UART3_TX	O	UART3 transmit signal (TXD)	18, 29, 30	14, 29, 45, 46	14, 29, 45, 46	26, 30, 50, 64, 7	18, 36, 43, 63, 74, 78	23, 46, 53, 78, 94, 98
UART4_CTS	I	UART4 clear to send signal	6	38, 8	38, 8	16, 42, 64	10, 36, 60	15, 46, 75
UART4_RTS	O	UART4 ready to send signal	13, 25, 9	11, 17, 39	11, 17, 39	1, 17, 45, 55	13, 23, 37, 61	18, 28, 47, 76
UART4_RX	I	UART4 receive signal (RXD)		37	37	15, 21, 63	35, 59, 69	45, 74, 84
UART4_TX	O	UART4 transmit signal (TXD)		36	36	14, 20, 62	34, 58, 68	44, 73, 83
UART5_CTS	I	UART5 clear to send signal		3	3	35	26, 3	3, 31
UART5_RTS	O	UART5 ready to send signal				36	27, 4	32, 4
UART5_RX	I	UART5 receive signal (RXD)	1	1	1	33	1, 24	1, 14, 29
UART5_TX	O	UART5 transmit signal (TXD)	2	2	2	34	2, 25	2, 30, 37
UART6_CTS	I	UART6 clear to send signal				22	26, 70	31, 85, 89
UART6_RTS	O	UART6 ready to send signal		42	42	23	27, 71	32, 86, 90
UART6_RX	I	UART6 receive signal (RXD)				20	24, 68	29, 83, 87
UART6_TX	O	UART6 transmit signal (TXD)				21	25, 69	30, 84, 88
UART7_CTS	I	UART7 clear to send signal	16, 20, 25, 29, 7	14, 20, 27, 31, 38, 39, 45, 9	14, 20, 27, 31, 38, 39, 45, 9	16, 17, 26, 37, 43, 5, 50, 58, 9	11, 18, 30, 41, 45, 5, 60, 61, 74	16, 23, 40, 5, 51, 55, 75, 76, 94
UART7_RTS	O	UART7 ready to send signal	19, 30, 8	10, 15, 21, 30, 41, 42, 46	10, 15, 21, 30, 41, 42, 46	19, 23, 30, 36, 44, 51, 59, 8	12, 19, 31, 4, 44, 67, 71, 78	17, 24, 4, 41, 54, 82, 86, 98
UART7_RX	I	UART7 receive signal (RXD)	18, 26, 28	15, 26, 29, 37, 40, 44	15, 26, 29, 37, 40, 44	15, 18, 25, 4, 51, 7	19, 40, 43, 59, 62, 73	24, 50, 53, 74, 77, 93
UART7_TX	O	UART7 transmit signal (TXD)	17, 25, 27	14, 25, 28, 36, 39, 43	14, 25, 28, 36, 39, 43	14, 17, 24, 3, 50, 6	18, 39, 42, 58, 61, 72	23, 49, 52, 73, 76, 92

Table 6-19. Voltage Reference Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PZ PIN
VREF+	A	Voltage reference positive input	27	43	43	24	72	92
VREF-	A	Voltage reference negative input	25	39	39	17	61	76

6.4 Connections for Unused Pins

Table 6-20 lists the correct termination of unused pins.

Table 6-20. Connection of Unused Pins

PIN (1)	POTENTIAL	COMMENT
PAx, PBx, PCx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup/ pulldown resistor.
NRST	VCC	NRST is an active-low reset signal; it must be pulled high to VCC or the device will not start, for more information refer to Section 9.1

(1) Any unused pin with a function that is shared with general-purpose I/O should follow the "PAx and PBx" unused pin connection guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	–0.3	4.1	V
V_I	Input voltage	Applied to any 5V tolerant open-drain pins	–0.3	5.5	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current into VDD pin (source)	-40°C ≤ Tj ≤ 130°C, VDD>=2.7V		80	mA
	Current into VDD pin (source)	-40°C ≤ Tj ≤ 85°C, VDD>=2.7V		100	mA
I_{VSS}	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 130°C, VDD>=2.7V		80	mA
	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 85°C, VDD>=2.7V		100	mA
I_{IO}	Current of SDIO pin	Current sunk or sourced by SDIO pin, VDD>=2.7V		6	mA
	Current of HS_IO pin	Current sunk or sourced by HSIO pin, VDD>=2.7V		6	mA
	Current of HDIO pin	Current sunk or sourced by HDIO pin		20	mA
	Current of ODIO pin	Current sunk by ODIO pin		20	mA
I_D	Supported diode current	Diode current at any device pin (excluding Open Drain IO)	-2	2	mA
T_J	Junction temperature	Junction temperature	-40	130	°C
T_{stg}	Storage temperature	Storage temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC-Q100-002	±2000	V
		Charged device model (CDM), per AEC-Q100-011 , All pins	±500	V
		Charged device model (CDM), per AEC-Q100-011 , Corner pins	±750	V

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
VCORE	Voltage on VCORE pin (2)		1.35		V
C_{VDD}	Capacitor connected between VDD and VSS (1)		10		uF
C_{VCORE}	Capacitor connected between VCORE and VSS (1) (2)		470		nF
$f_{MCLK (PD1 bus clock)}$	MCLK, CPUCLK frequency with 2 flash wait states (3)			80	MHz
	MCLK, CPUCLK frequency with 1 flash wait state (3)			48	
	MCLK, CPUCLK frequency with 0 flash wait states (3)			24	
$f_{ULPCLK (PD0 bus clock)}$	ULPCLK frequency			40	MHz

(1) Connect C_{VDD} and C_{VCORE} between VDD/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD} and C_{VCORE}.
(2) The VCORE pin must only be connected to C_{VCORE}. Do not supply any voltage or apply any external load to the VCORE pin.

ADVANCE INFORMATION

(3) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software unless MCLK is sourced from a high speed clock source (HSCLK sourced from HFCLK or SYSPLL).

7.4 Thermal Information

THERMAL METRIC(1)		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-100 (PZ)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		TBD	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-80 (PN)	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		TBD	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-64 (PM)	44.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		38.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		21.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		21.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		7.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-48 (PT)	69.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		32.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		2.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		32.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-48 (RGZ)	30.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		20.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		12.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		12.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		4.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-32 (RHB)	32.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		23.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		13.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		13.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode													
IDD_{RUN}	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from flash	80MHz	9.6		9.7		10		10.4		11.1		mA
		48MHz	6.2		6.3		6.6		6.9		7.6		
	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	4.6		4.7		5		5.3		6.1		
		4MHz	0.9		1		1.2		1.6		2.3		
	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from SRAM	80MHz	9.2		9.4		9.7		10		10.8		
		48MHz	6		6.1		6.4		6.7		7.5		
	MCLK=SYSOSC, CoreMark, execute from SRAM	32MHz	4.2		4.3		4.6		4.9		5.7		
		4MHz	0.9		0.9		1.2		1.6		2.3		
IDD_{RUN}, perMHz	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from flash	80MHz	120		121		125		130		139		uA/MHz
	MCLK=SYSPLL, SYSPLLREF=SYSOSC, While(1), execute from flash	80MHz	59	TBD	60	TBD	63	TBD	68	TBD	77	TBD	
SLEEP Mode													
IDD_{SLEEP}	MCLK=SYSPLL, SYSPLLREF=SYSOSC, CPU is halted	80MHz	2891	TBD	2967	TBD	3256	TBD	3590	TBD	4353	TBD	uA
		48MHz	2160	TBD	2228	TBD	2516	TBD	2854	TBD	3607	TBD	
	MCLK=SYSOSC, CPU is halted	32MHz	1686	TBD	1747	TBD	2029	TBD	2368	TBD	3127	TBD	
		4MHz	562	TBD	614	TBD	893	TBD	1232	TBD	1981	TBD	

7.5.2 STOP/STANDBY Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
IDD_{STOP0}	SYSOSC=32MHz, USE4MHZSTOP=0, DISABLESTOP=0	4MHz	425	TBD	429	TBD	434	TBD	439	TBD	453	TBD	uA
IDD_{STOP1}	SYSOSC=4MHz, USE4MHZSTOP=1, DISABLESTOP=0		213	TBD	218	TBD	223	TBD	229	TBD	244	TBD	
IDD_{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	54	TBD	56	TBD	60	TBD	65	TBD	79	TBD	
STANDBY Mode													
IDD_{STBY0}	LFCLK=LFXT, STOPCLKSTBY=0, RTC enabled	32kHz	2	TBD	2.3	TBD	5	TBD	10	TBD	25	TBD	uA
IDD_{STBY1}	LFCLK=LFOSC, STOPCLKSTBY=1, RTC enabled		1.5	TBD	1.7	TBD	5	TBD	9	TBD	24	TBD	
	LFCLK=LFXT, STOPCLKSTBY=1, RTC enabled		1.5	TBD	1.8	TBD	5	TBD	9	TBD	24	TBD	
	LFCLK=LFXT, STOPCLKSTBY=1, GPIOA enabled		1.5	TBD	1.7	TBD	5	TBD	9	TBD	24	TBD	

ADVANCE INFORMATION

7.5.3 SHUTDOWN Mode

All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{SHDN}	Supply current in SHUTDOWN mode	3.3V	54		93		523		1220		3430		nA

7.6 Power Supply Sequencing

7.6.1 Power Supply Ramp

Figure 7-1 gives the relationship of POR- POR+, BOR0-, and BOR0+ during power-up and power-down.

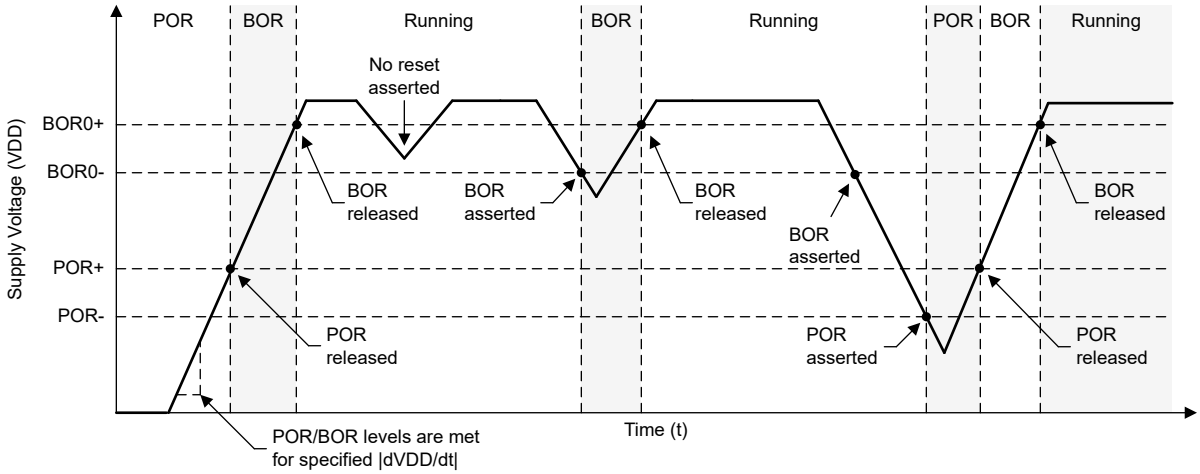


Figure 7-1. Power Cycle POR/BOR Conditions - VDD

7.6.2 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling (2)			0.01	
		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising (1)	0.91	1.30	1.5	V
V_{POR-}		Falling (1)	0.87	1.25	1.48	V
$V_{HYS, POR}$	POR hysteresis		30	58	74	mV
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	-40°C ≤ Tj ≤ 30°C Cold start, rising (1)	1.45	1.54	1.62	V
		30°C ≤ Tj ≤ 85°C Cold start, rising (1)	1.48	1.56	1.64	
		85°C ≤ Tj ≤ 130°C Cold start, rising (1)	1.48	1.57	1.66	
V_{BOR0+}		Rising (1) (2)	1.56	1.59	1.62	
V_{BOR0-}		Falling (1) (2)	1.55	1.58	1.61	
$V_{BOR0, STBY}$		STANDBY mode (1)	1.51	1.56	1.61	
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (1) (2)	2.13	2.17	2.21	V
V_{BOR1-}		Falling (1) (2)	2.10	2.14	2.18	
$V_{BOR1, STBY}$		STANDBY mode (1)	2.06	2.13	2.20	

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (1) (2)	2.73	2.77	2.82	V
V_{BOR2-}		Falling (1) (2)	2.7	2.74	2.79	
$V_{BOR2, STBY}$		STANDBY mode (1)	2.62	2.71	2.8	
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (1) (2)	2.88	2.96	3.04	V
V_{BOR3-}		Falling (1) (2)	2.85	2.93	3.01	
$V_{BOR3, STBY}$		STANDBY mode (1)	2.82	2.92	3.02	
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0 (1)		15	21	mV
		Levels 1-3 (1)		34	40	
$T_{PD, BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			5	us
		STANDBY mode			100	us

(1) |dVDD/dt| ≤ 3V/s
(2) Device operating in RUN, SLEEP, or STOP mode.

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		1.62		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
$NWEC_{(LOWER)}$	Erase/program cycle endurance (Data Flash Bank and first 16kB of Flash Bank 0) (1)		100			k cycles
$NWEC_{(UPPER)}$	Erase/program cycle endurance (remaining flash) (1)		10			k cycles
$NE_{(MAX)}$	Total erase operations before failure (2)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase (3)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C <= Tj <= 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C <= Tj <= 105°C	11.4			years
Program and Erase Timing						
$t_{PROG (WORD, 64)}$	Program time for flash word (4) (6)			50	275	µs
$t_{PROG (SEC, 64)}$	Program time for 1kB sector (5) (6)			6.4		ms
$t_{ERASE (SEC)}$	Sector erase time	≤2k erase/program cycles, T_j≥25°C		4	20	ms
$t_{ERASE (SEC)}$	Sector erase time	≤10k erase/program cycles, T_j≥25°C		20	150	ms
$t_{ERASE (SEC)}$	Sector erase time	<10k erase/program cycles		20	200	ms
$t_{ERASE (BANK)}$	Bank erase time	<10k erase/program cycles		22	220	ms

(1) The entire Data Flash Bank and lower 16kB of Flash Bank 0 address space support higher erase/program endurance to enable EEPROM emulation applications.
(2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
(3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.

ADVANCE INFORMATION

(4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
(5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
(6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=3.3V, T_a=25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE, SLEEP1}$	Wakeup time from SLEEP1 to RUN (1)			1.6		us
$t_{WAKE, SLEEP2}$	Wakeup time from SLEEP2 to RUN (1)			2.2		us
$t_{WAKE, STANDBY0}$	Wakeup time from STANDBY0 to RUN (1)			10.4		us
$t_{WAKE, STANDBY1}$	Wakeup time from STANDBY1 to RUN (1)			10.4		us
$t_{WAKE, STOP0}$	Wakeup time from STOP0 to RUN (SYSOSC enabled) (1)			7.6		us
$t_{WAKE, STOP1}$	Wakeup time from STOP1 to RUN (SYSOSC enabled) (1)			9.6		us
$t_{WAKE, STOP2}$	Wakeup time from STOP2 to RUN (SYSOSC disabled) (1)			8.4		
$t_{WAKEUP, SHDN}$	Wakeup time from SHUTDOWN to RUN (2)	Fast boot enabled		306		us
		Fast boot disabled		314		
Asynchronous Fast Clock Request Timing						
$t_{DELAY, SLEEP1}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP1		0.34		us
$t_{DELAY, SLEEP2}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP2		0.94		us
$t_{DELAY, STANDBY0}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY0		3		us
$t_{DELAY, STANDBY1}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY1		3.1		us
$t_{DELAY, STOP0}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP0		0.1		us
$t_{DELAY, STOP1}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP1		2.4		us
$t_{DELAY, STOP2}$	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP2		0.9		us
Startup Timing						
$t_{START, RESET}$	Device cold startup time from reset/ power-up (3)	Fast boot enabled		300		us
		Fast boot disabled		350		
NRST Timing						
$t_{RST, BOOTRST}$	Pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		1.5		us
		ULPCLK=32kHz		29		
$t_{RST, POR}$	Pulse length on NRST pin to generate POR			1		s

(1) The wake-up time is measured from the edge of an external wake-up signal (GPIO wake-up event) to the time that the first instruction of the user program is executed, with glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1) .
(2) The wake-up time is measured from the edge of an external wake-up signal (IOMUX wake-up event) to the time that first instruction of the user program is executed.

ADVANCE INFORMATION

(3) The start-up time is measured from the time that VDD crosses VBOR0- (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32		MHz
		SYSOSCCFG.FREQ=01		4		
	User trimmed SYSOSC frequency	SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=10		24		
		SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=01		16		
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled and an ideal ROSC resistor is assumed (1) (2)	SETUSEFCL=1, T_a = 25 ℃	-0.41		0.58	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 85 ℃	-0.80		0.93	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 105 ℃	-0.80		1.1	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃	-0.80		1.3	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is enabled with R_{OSC} resistor put at R_{OSC} pin, for factory trimmed frequencies(1)	SETUSEFCL=1, T_a = 25 ℃, ±0.1% ±25ppm R_{OSC}	-0.5		0.7	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 85 ℃, ±0.1% ±25ppm R_{OSC}	-1.1		1.2	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 105 ℃, ±0.1% ±25ppm R_{OSC}	-1.1		1.4	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃, ±0.1% ±25ppm R_{OSC}	-1.1		1.7	
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used (4)	SETUSEFCL=1 -40 ℃ ≤ T_a ≤ 125 ℃	-2		1.8	%
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 ℃ ≤ T_a ≤ 125 ℃	-2.6		1.8	%
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, for factory trimmed frequencies, 4MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=01, -40 ℃ ≤ T_a ≤ 125 ℃	-2.7		2.3	
f_{SYSOSC}	External resistor put between ROSC pin and VSS (1)	SETUSEFCL=1		100		kΩ
f_{SYSOSC}	Settling time to target accuracy (3)	SETUSEFCL=1, ±0.1% 25ppm R_{OSC} (1)			30	us
f_{SYSOSC}	f_{SYSOSC} additional undershoot accuracy during t_{settle} (3)	SETUSEFCL=1, ±0.1% 25ppm R_{OSC} (1)	-16			%

(1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an external reference resistor (R_{OSC}) which must be connected between the device ROSC pin and VSS when using the FCL. Accuracies are shown for a ±0.1% ±25ppm R_{OSC}; relaxed tolerance resistors may also be used (with reduced SYSOSC accuracy). See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy for various R_{OSC} accuracies. R_{OSC} does not need to be populated if the FCL is not enabled.

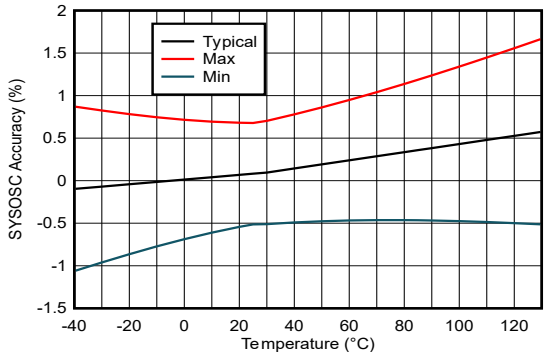
(2) Represents the device accuracy only. The tolerance and temperature drift of the ROSC resistor used must be combined with this spec to determine final accuracy. Performance for a ±0.1% ±25ppm R_{OSC} is given as a reference point.

(3) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to $f_{settle,SYSOSC}$ for the time $t_{settle,SYSOSC}$, after which the target accuracy is achieved.

(4) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.

ADVANCE INFORMATION

7.9.2 SYSOSC Typical Frequency Accuracy



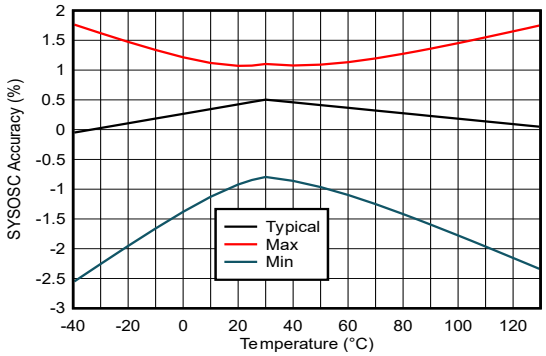


Figure 7-2. SYSOSC Accuracy with FCL On (32MHz) Figure 7-3. SYSOSC Accuracy with FCL Off (32MHz)

FCL-on accuracy is based on a 0.1% tolerance 25 ppm/°C ROSC resistor.

7.9.3 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 °C ≤ T_a ≤ 125 °C	–5		5	%
		-40 °C ≤ T_a ≤ 85 °C	–3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start, LFOSC}$	LFOSC start-up time			1		ms

7.9.4 System Phase Lock Loop (SYSPLL)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SYSPLLREF}$	SYSPLL reference frequency range		4		48	MHz
f_{VCO}	VCO output frequency		80		400	MHz
f_{SYSPLL}	SYSPLL output frequency range (1)	SYSPLLCLK0, SYSPLLCLK1	2.5		200	MHz
		SYSPLLCLK2X	10		400	
DC_{PLL}	SYSPLL output duty cycle	$f_{SYSPLLREF}$=32MHz, f_{VCO}=160MHz	45		55	%
$Jitter_{SYSPLL}$	SYSPLL RMS cycle-to-cycle jitter	$f_{SYSPLLREF}$=32MHz, f_{VCO}=160MHz		60		ps
	SYSPLL RMS period jitter			45		
I_{SYSPLL}	SYSPLL current consumption	$f_{SYSPLLREF}$=32MHz, f_{VCO}=160MHz		322		uA
$t_{start, SYSPLL}$	SYSPLL start-up time	$f_{SYSPLLREF}$=32MHz, f_{VCO}=160MHz, ±0.5% accuracy		14	24	us

(1) The SYSPLL may support higher output frequencies than the device clock system supports. Ensure that the device maximum frequency specifications are not violated when configuring the SYSPLL output frequencies.

7.9.5 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency crystal oscillator (LFXT)						
f_{LFXT}	LFXT frequency			32768		Hz
DC_{LFXT}	LFXT duty cycle		30		70	%
OA_{LFXT}	LFXT crystal oscillation allowance			419		kΩ

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, LFXT}$	LFXT start-up time			1000		ms
I_{LFXT}	LFXT current consumption	XT1DRIVE=0, LOWCAP=1		200		nA
Low frequency digital clock input (LFCLK_IN)						
f_{LFIN}	LFCLK_IN frequency (2)	SETUSEEXLF=1	29491	32768	36045	Hz
DC_{LFIN}	LFCLK_IN duty cycle (2)	SETUSEEXLF=1	40		60	%
LFCLK Monitor						
$f_{FAULTLF}$	LFCLK monitor fault frequency (3)	MONITOR=1	2800	4200	8400	Hz

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{LFXIN} \times C_{LFXOUT}/(C_{LFXIN}+C_{LFXOUT})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.
(2) The digital clock input (LFCLK_IN) accepts a logic level square wave clock.
(3) The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.

7.9.6 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High frequency crystal oscillator (HFXT)						
f_{HFXT}	HFXT frequency	HFXTRSEL=00	4		8	MHz
		HFXTRSEL=01	8.01		16	
		HFXTRSEL=10	16.01		32	
		HFXTRSEL=11	32.01		48	
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=00	40		65	%
		HFXTRSEL=01	40		60	
		HFXTRSEL=10	40		60	
		HFXTRSEL=11	40		60	
OA_{HFXT}	HFXT crystal oscillation allowance	HFXTRSEL=00 (4 to 8MHz range)		2		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, HFXT}$	HFXT start-up time (2)	HFXTRSEL=11, 32MHz crystal		0.5		ms
I_{HFXT}	HFXT current consumption(2)	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		100		uA
		f_{HFXT}=48MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		
High frequency digital clock input (HFCLK_IN)						
f_{HFIN}	HFCLK_IN frequency (3)	USEEXTHFCLK=1	4		48	MHz
DC_{HFIN}	HFCLK_IN duty cycle (3)	USEEXTHFCLK=1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{HFXIN} \times C_{HFXOUT}/(C_{HFXIN}+C_{HFXOUT})$, where C_{HFXIN} and C_{HFXOUT} are the total capacitance at HFXIN and HFXOUT, respectively.
(2) The HFXT startup time ($t_{start, HFXT}$) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the HFXT section of the MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual.Current consumption increases with higher RSEL and start up time is decreases with higher RSEL.
(3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

ADVANCE INFORMATION

7.10 Digital IO

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	ODIO (1)	VDD≥1.62V	0.7*VDD		5.5	V
			VDD≥2.7V	2		5.5	V
		All I/O except ODIO & Reset	VDD≥1.62V	0.7*VDD		VDD+0.3	V
V_{IL}	Low level input voltage	ODIO	VDD≥1.62V	-0.3		0.3*VDD	V
			VDD≥2.7V	-0.3		0.8	V
		All I/O except ODIO & Reset	VDD≥1.62V	-0.3		0.3*VDD	V
V_{HYS}	Hysteresis	ODIO		0.05*VDD			V
		All I/O except ODIO		0.1*VDD			V
I_{lkg}	High-Z leakage current (All packages except PZ, PN, PM)	SDIO(2) (3)	1.62V ≤ VDD ≤ 3.6V, -40 °C ≤ T_a ≤ 125 °C			50(4)	nA
	High-Z leakage current (PZ, PN, PM package)	SDIO(2) (3)	1.62V ≤ VDD ≤ 3.6V, -40 °C ≤ T_a ≤ 85 °C			70(4)	nA
			1.62V ≤ VDD ≤ 3.6V, -40 °C ≤ T_a ≤ 125 °C			400(4)	nA
R_{PU}	Pull up resistance	All I/O except ODIO	VIN = VSS		40		kΩ
R_{PD}	Pull down resistance		VIN = VDD		40		kΩ
C_I	Input capacitance		VDD = 3.3V		5		pF
V_{OH}	High level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤25 °C	VDD-0.4			V
			VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤130 °C	VDD-0.45			
		HSIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_j≤25 °C	VDD-0.4			
			VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_j≤130 °C	VDD-0.45			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤25 °C	VDD-0.4			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤130 °C	VDD-0.45			
		HDIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=20mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=10mA	VDD-0.4			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA	VDD-0.4			

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_J≤25 °C			0.4	V
			VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_J≤130 °C			0.45	V
		HSIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_J≤25 °C			0.4	
			VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_J≤130 °C			0.45	
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_J≤25 °C			0.4	
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_J≤130 °C			0.45	
		HDIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=20mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=10mA			0.4	
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA			0.4	
		ODIO	VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA -40 °C ≤T_J≤25 °C			0.4	V
			VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA -40 °C ≤T_J≤130 °C			0.45	V

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(4) This value is for SDIO not muxed with any analog inputs. If the SDIO is muxed with analog inputs then the leakage can be higher.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO	VDD ≥ 1.71V, C_L= 20pF			16	MHz
			VDD ≥ 2.7V, CL= 20pF			32	
		HSIO	VDD ≥ 1.71V, DRV = 0, CL= 20pF			16	
			VDD ≥ 1.71V, DRV = 1, CL= 20pF			24	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			32	
			VDD ≥ 2.7V, DRV = 1, CL= 20pF			40	
		HDIO	VDD ≥ 1.71V, DRV = 0, CL= 20pF			16	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			20	
		ODIO	VDD ≥ 1.71V, FM^+, CL= 20pF - 100pF			1	
t_r,t_f	Output rise/fall time	All output ports except ODIO	VDD ≥ 1.71V			0.3*f_{max}	s

ADVANCE INFORMATION

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM+, CL= 20pF-100pF	20*VDD/5.5		120	ns

7.11 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is LFCLK		0.8		uA
		MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 4MHz		10.6		
$t_{START,VBST}$	VBOOST startup time			12	20	us

7.12 ADC

7.12.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
		V_{R+} sourced from external reference pin (VREF+)	1.4		VDD	V
		V_{R+} sourced from internal reference (VREF)		VREF		V
V_{R-}	Negative ADC reference voltage			0		V
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode)			4	Msps
		RES = 0x1 (10-bit mode)			4	
		RES = 0x2 (8-bit mode) , SCOMP = 2			5.3	
$I_{(ADC)}$	Operating supply current into VDD terminal	F_S = 4MSPS, V_{R+} = VDD		1.75(2)		mA
$C_{S/H}$	ADC sample-and-hold capacitance			3.3		pF
Rin	ADC input resistance			0.5		kΩ
ENOB	Effective number of bits	External reference (3)	10.9	11.1		bit
		External reference (3), HW Averaging Enabled, 16 Samples and 2-bit shift	12.3	12.5		
		Internal reference, V_{R+} = VREF = 2.5V (VRSEL = 4h)(5)	9.9	10.8		
		Internal reference, V_{R+} = VREF = 2.5V (VRSEL = 2h)		9.2		
SNR	Signal-to-noise ratio	External reference (3)		68		dB
		External reference (3), HW Averaging Enabled, 16 Samples and 2-bit shift		78		
		Internal reference, V_{R+} = VREF = 2.5V (VRSEL = 4h)(5)		66		
		Internal reference, V_{R+} = VREF = 2.5V (VRSEL = 2h)		57		
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference (3), VDD = $VDD_{(min)}$ to $VDD_{(max)}$		62		dB
		VDD = $VDD_{(min)}$ to $VDD_{(max)}$ Internal reference, V_{R+} = VREF = 2.5V		60		
$PSRR_{AC}$	Power supply rejection ratio, AC	External reference (3), ΔVDD = 0.1V at 1 kHz		61		dB
		ΔVDD = 0.1V at 1 kHz Internal reference, V_{R+} = VREF = 2.5V		52		
T_{wakeup}	ADC Wakeup Time	Assumes internal reference is active			5	us
$V_{SupplyMon}$	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor (4) (6)	-1.5		1.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference (VREF) supply current is not included in current consumption parameter $I_{(ADC)}$.

ADVANCE INFORMATION

(3) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 3.3V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin
(4) Analog power supply monitor. Analog input on channel 15 is disconnected and is internally connected to the voltage divider which is VDD/3.
(5) Please note that to achieve this ENOB using internal reference VREF, VRSEL bit in MEMCTL register needs to be set to 4h. This will set the REFN as VREF- and REFP as VREF+. In this configuration ,no external connections can be made on the VREF- and VREF+ pins. The REFN pin should be connected to device ground.
(6) Characterized using external reference (VREFSEL = 1)

7.12.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency		4		48	MHz
$t_{ADC\ trigger}$	Software trigger minimum width		3			ADCCLK cycles
t_{Sample}	Sampling time	12-bit mode, R_S = 50Ω, C_{pext} = 10pF	62.5			ns
t_{Sample_DAC}	Sampling time with DAC as input (1)		0.5			µs
$t_{Sample\_SupplyMon}$	Sample time with Supply Monitor (VDD/3)		5			µs

(1) Only applies for devices with DAC

7.12.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (INL)	External reference (2)	-2		2	LSB
E_D	Differential linearity error (DNL) Guaranteed no missing codes	External reference (2)	-1		1	LSB
E_O	Offset error	Internal or External reference (2)	-2		2	mV
E_G	Gain error	External reference, VRSEL = 1h (2)	-3		3	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{(E_I^2 + |E_O|^2 + E_G^2)}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate
(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD and V_{R-} = VSS = 0V, external 1uF cap on VREF+ pin.

7.12.4 Typical Connection Diagram

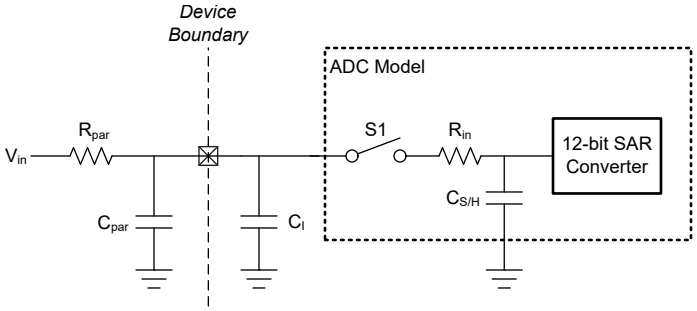


Figure 7-4. ADC Input Network

1. Refer to Electrical Characteristics for the values of R_{in} and $C_{S/H}$
2. Refer to *Digital IO Electrical Characteristics* for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. Tau = $(R_{par} + R_{in})^* C_{S/H} + R_{par}^*(C_{par} + C_I)$
2. K= $\ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I)/C_{S/H})$
3. T (Min sampling time) = K*Tau

ADVANCE INFORMATION

7.13 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (1)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h(External/ Internal reference), V_{R+} = VREF = 1.4V (BUFCONFIG =1), cap=1uF on VREF+, ADC t_{Sample}=10µs	27	30	33	℃
TS_c	Temperature coefficient	-40℃ ≤ T_j ≤ 130℃	-2.1	-2	-1.9	mV/℃
$t_{SET, TS}$	Temperature sensor settling time (2)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL= 0h (VDD = 3.3V), ADC CHANNEL=11			10	us

(1) Higher absolute accuracy may be achieved through user calibration. Please refer to temperature sensor chapter in detailed description section.
(2) This is the minimum required ADC sampling time when measuring the temperature sensor.

7.14 VREF

7.14.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 0	2.7			V
		BUFCONFIG = 1	1.62			
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.38	1.4	1.42	V
		BUFCONFIG = 0	2.46	2.5	2.54	

7.14.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load		166	330	µA
I_{Drive}	VREF output drive strength (1)	Drive strength supported on VREF+ device pin			100	µA
I_{SC}	VREF short circuit current				100	mA
TC_{VREF}	Temperature coefficient of VREF (Bandgap+VRBUF) (2)	BUFCONFIG = {1}			75	ppm/°C
TC_{VREF}	Temperature coefficient of VREF (Bandgap+VRBUF) (2)	BUFCONFIG = {0}			75	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25℃			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.7V to VDDmax, BUFCONFIG = 1	60	70		dB
		VDD = 2.7V to VDDmax, BUFCONFIG = 0	50	60		
V_{noise}	RMS noise at VREF output (0.1 Hz to 100MHz)	BUFCONFIG = 1		500		µVrms
		BUFCONFIG = 0		900		
C_{VREF}	Recommended VREF decoupling capacitor on VREF+ pin (3) (4) (5)		0.7	1	1.15	µF
$T_{startup}$	VREF startup time	BUFCONFIG = {0, 1} , VDD = 2.8 V, C_{VREF} = 1µF			200	µS
$T_{refresh}$	VREF External capacitor refresh time		31.25			

(1) The specified MAX output drive strength is supported regardless of which peripherals are being used in the device.
(2) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.
(3) Decoupling capacitor (C_{VREF}) is required when using the internal voltage reference VREF and should be connected from the VREF+ pin to VREF-/GND. When using the VREF+/- pins to supply an external reference, a decoupling capacitor value should be selected based on the external reference source.
(4) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable
(5) The VREF module should only be enabled when C_{VREF} is connected and should not be enabled otherwise.

7.15 Comparator (COMP)

7.15.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator Electrical Characteristics						
Vcm	Common mode input range		0		VDD	V
V_{offset}	Input offset voltage		-20		20	mV
V_{hys}	DC input hysteresis	HYST=00h		0.4		mV
		HYST=01h		10		
		HYST=02h		20		
		HYST=03h		30		
t_{PD_ls}	Propagation delay, response time	Output Filter off, Overdrive = 100 mV, High Speed Mode		32	50	ns
		Output Filter off, Overdrive = 100 mV, Low Power Mode		1.2	4	µs
t_{en}	Comparator enable time	Startup time to reach propagation delay specification, High Speed Mode (comparator only)			5	µs
		Startup time to reach propagation delay specification, Low Power Mode (comparator only)			10	µs
I_{comp}	Comparator current consumption.	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode		130	200	µA
		Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode		0.85	2.7	µA
		Vcm = VDD/2, 100mV overdrive, comparator only. High Speed Mode		120	180	µA
		Vcm = VDD/2, 100mV overdrive, comparator only, Low Power Mode		0.7	2.1	µA
I_{comp}	Comparator +VREF current consumption in low power	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, Internal VREF is reference for DAC, Low Power Mode. VREF registers SHCYCLE=0xC0, HCYCLE=0xC0, SHMODE=1		2.5		uA
8-bit DAC Electrical Characteristics						
V_{dac}	DAC output range		0		VDD	V
$V_{dac\text{-}code}$	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, code n = 0 to 255		VIN × (n+1) / 256		V
INL	Integral nonlinearity of 8-bit DAC		-1		1	LSB
DNL	Differential nonlinearity of 8-bit DAC		-1		1	LSB
Gain error	Gain error of 8-bitDAC	Reference voltage = VDD	-2		2	% of FSR
Offset error	Offset error of 8-bit DAC		-5		5	mV
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB		1.5		µs

7.16 DAC

7.16.1 DAC_Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	VDD, External, Internal(1.4V, 2.5V)	1.4		VDD	V
I_{DAC}	DAC current consumption from VDD	VREF= VDD, No load, DAC code = 0x800		400		µA

ADVANCE INFORMATION

7.16.2 DAC Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage range	No load, Vref = VDD, DATA = 0x0			20	mV
V_O	Output voltage range	No load, Vref = VDD, DATA = 0xFFF	VDD-0.05	VDD-0.01	VDD	V
V_O	Output voltage range	R_{load} = 3.3kΩ, Vref = VDD, DATA = 0x0			0.13	V
V_O	Output voltage range	R_{load} = 3.3kΩ, Vref = VDD, DATA = 0xFFF	VDD-0.13	VDD-0.1	VDD	V
$C_{L(DAC)}$	Load capacitance				100	pF
$I_{L(DAC)}$	Load current		-1		1	mA
$R_{OUT(DAC)}$	Output resistance	R_{load} = 3.3kΩ, Vref = VDD, V_O = 0.3V to Vdd-0.3V		1.2	10	Ω

7.16.3 DAC Dynamic Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	DATA = 0x80 → 0xF7F → 0x80, Vref = external reference		5.5		V/µs
GE	Glitch energy	DATA = 0x800 → 0x7FF → 0x800, Vref = external reference		1.2		nV-s
PSRR_DC	Power supply rejection ratio, DC	ΔVDD = 100 mV, DATA = 0xFFF, Vref = external reference		79.5		dB
PSRR_AC	Power supply rejection ratio, AC	ΔVDD = 100mV at 100kHz, DATA = 0xFFF, Vref = external reference		25.7		dB
SNR	Signal-to-noise ratio	Vref = external reference, 4kHz input with 1Msps sampling rate(1)		80.9		dB
THD	Total harmonic distortion	Vref = external reference, 4kHz input with 1Msps sampling rate(1)		71.5		dB
SINAD	Signal-to-noise and distortion	Vref = external reference, 4kHz input with 1Msps sampling rate(1)		71.1		dB
ENOB	Effective number of bits	Vref = external reference, 4kHz input with 1Msps sampling rate(1)		11.5		bits

(1) A low pass filter with 300 Hz to 4 kHz pass band connected at DAC output pin.

7.16.4 DAC Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				12		bits
DNL	Differential nonlinearity	Vref = internal or external or VDD reference(1)	-1		1	LSB
INL	Integral nonlinearity	Vref = internal or external or VDD reference(1)	-4		4	LSB
E_G	Gain error	Vref = internal or external or VDD reference(1)	-2	-0.5	2	%FSR
E_O	Offset error	Vref = internal or external reference or vdd, With calibration (1)	-2	0.5	2	mV
E_O	Offset error	Vref = internal or external or VDD reference, without calibration (1)	-20		20	mV
t_{cal}	Time for offset calibration		1.3			ms

(1) DAC valid output range is 0.3 to VDD-0.3

7.16.5 DAC Timing Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ON,12b}$	Turn on time from off state (VREF ready)	DATA = 0xFFF, Error < ±2 LSB, Vref = internal reference		4.5	6.9	µs
$t_{S(FS)}$	Full scale settling time	DATA = 0x1EC->0xFFF->0x1EC, Error< ±2 LSB, Vref = internal reference		0.8	1	µs

7.17 I2C

7.17.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0	2	32	8	32	20	32	MHz

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency		0.025	0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9		0.45	us

7.17.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.17.3 I²C Timing Diagram

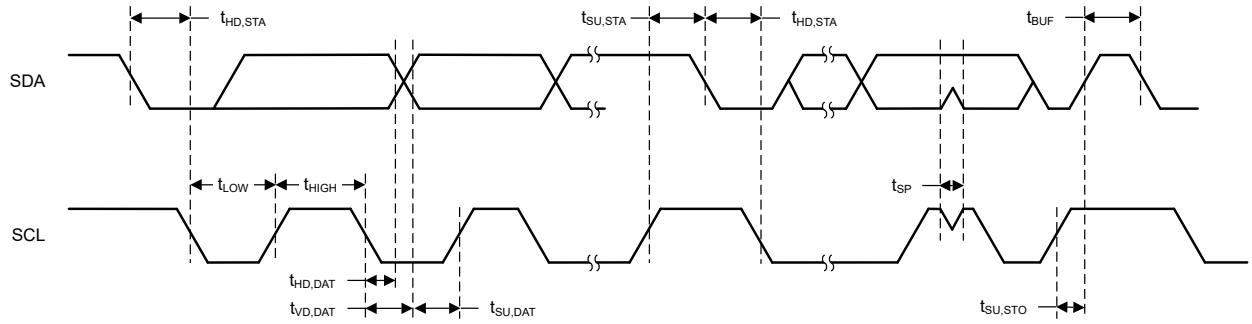


Figure 7-5. I2C Timing Diagram

7.18 SPI

7.18.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	Clock max speed >= 32MHz 1.62 < VDD < 3.6V Peripheral or Controller mode			16	MHz
f_{SPI}	SPI clock frequency	Clock max speed >= 48MHz 1.62 < VDD < 2.7V Peripheral or Controller mode with High speed IO			24	MHz

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SPI}	SPI clock frequency	Clock max speed >= 64MHz 2.7 < VDD < 3.6V Peripheral or Controller mode with High speed IO			32	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						
$t_{SCLK\_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=0	1 SPI Clock			
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=1	1/2 SPI Clock			
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1 SPI Clock			
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1/2 SPI Clock	
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high inpedance				1 SPI Clock	
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, delayed sampling enabled	1			ns
$t_{SU.CI}$	POCI input data setup time (1)	1.62 < VDD < 2.7V, delayed sampling enabled	1			ns
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, no delayed sampling	29			ns
$t_{SU.CI}$	POCI input data setup time (1)	1.62 < VDD < 2.7V, no delayed sampling	37			ns
$t_{HD.CI}$	POCI input data hold time	delayed sampling enabled	24			ns
$t_{HD.CI}$	POCI input data hold time	no delayed sampling	0			ns
$t_{VALID.CO}$	PICO output data valid time (2)				10	ns
$t_{HD.CO}$	PICO output data hold time (3)		6			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock		11			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out				26	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance				26	ns
$t_{SU.PI}$	PICO input data setup time		7			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
$t_{VALID.PO}$	POCI output data valid time(2)	2.7 < VDD < 3.6V			25	ns
$t_{VALID.PO}$	POCI output data valid time(2)	1.62 < VDD < 2.7V			31	ns
$t_{HD.PO}$	POCI output data hold time(3)		5			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

ADVANCE INFORMATION

7.18.2 SPI Timing Diagram

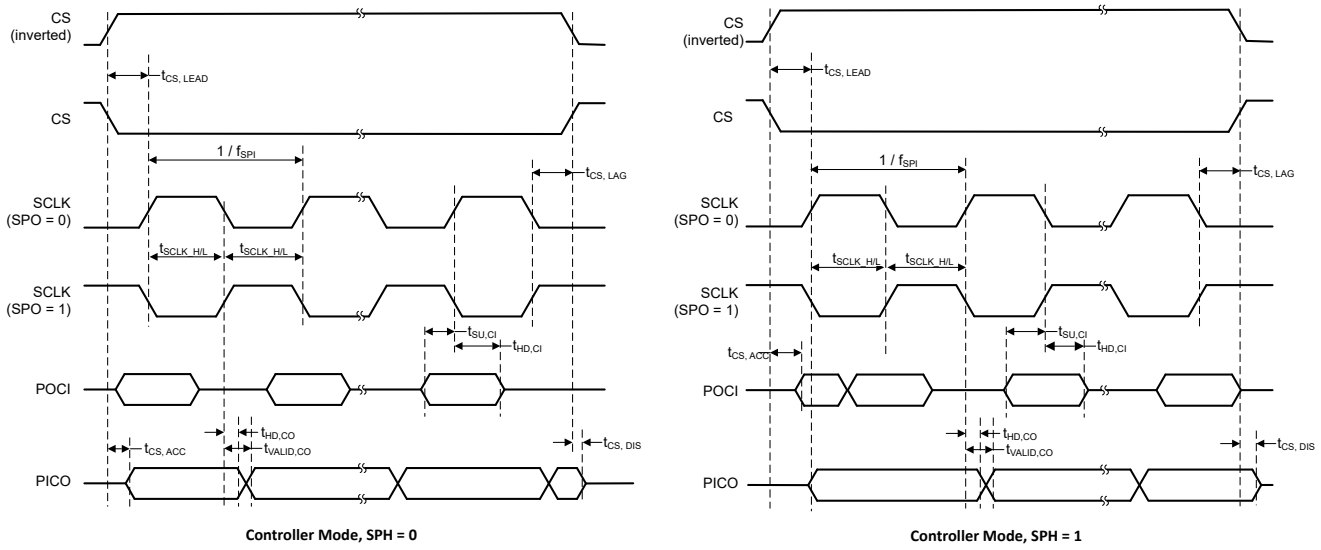


Figure 7-6. SPI timing diagram - Controller Mode

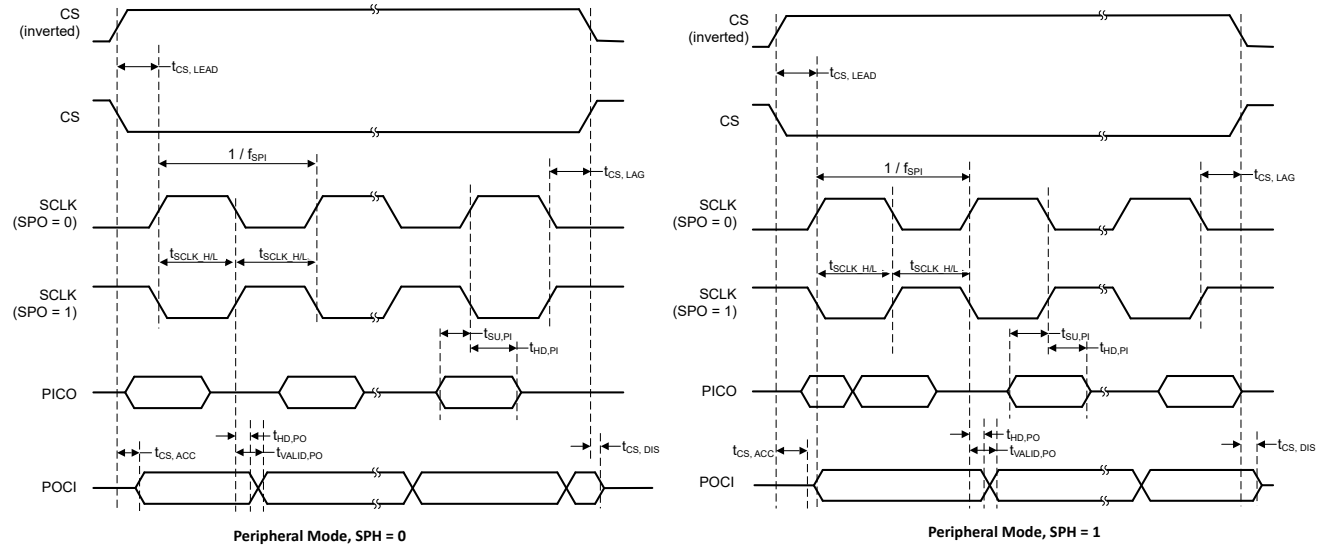


Figure 7-7. SPI timing diagram - Peripheral Mode

7.19 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency	UART in Power Domain1			80	MHz
f_{UART}	UART input clock frequency	UART in Power Domain0			40	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain1			10	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain0			5	MHz

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.20 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{res}	Timer resolution time	$f_{TIMxCLK}$ = 32MHz	31.25			ns
			1			$t_{TIMxCLK}$
t_{res}	Timer resolution time	TIMx in Power Domain 1, $f_{TIMxCLK}$ = 80MHz	12.5			ns
		TIMx in Power Domain 0, $f_{TIMxCLK}$ = 40MHz	25			ns
			1			$t_{TIMxCLK}$

7.21 TRNG

7.21.1 TRNG Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TRNG_{IACT}$	TRNG active current	TRNG clock = 20MHz		115		µA

7.21.2 TRNG Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TRNGCLK_F$	TRNG input clock frequency		9.5	10	25	MHz
$TRNG_{STARTUP}$	TRNG startup time			520		µs
$TRNG_{LAT32}$	Latency to generate 32 random bits	Decimation ratio = 4, TRNG clock = 20MHz		6.4		µs
$TRNG_{LAT256}$	Latency to generate 256 random bits	Decimation ratio = 4, TRNG clock = 20MHz		51.2		µs

7.22 Emulation and Debug

7.22.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz

8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.1 Functional Block Diagram

MSPM0Gx51x Functional Block Diagram shows the MSPM0Gx51x functional block diagram.

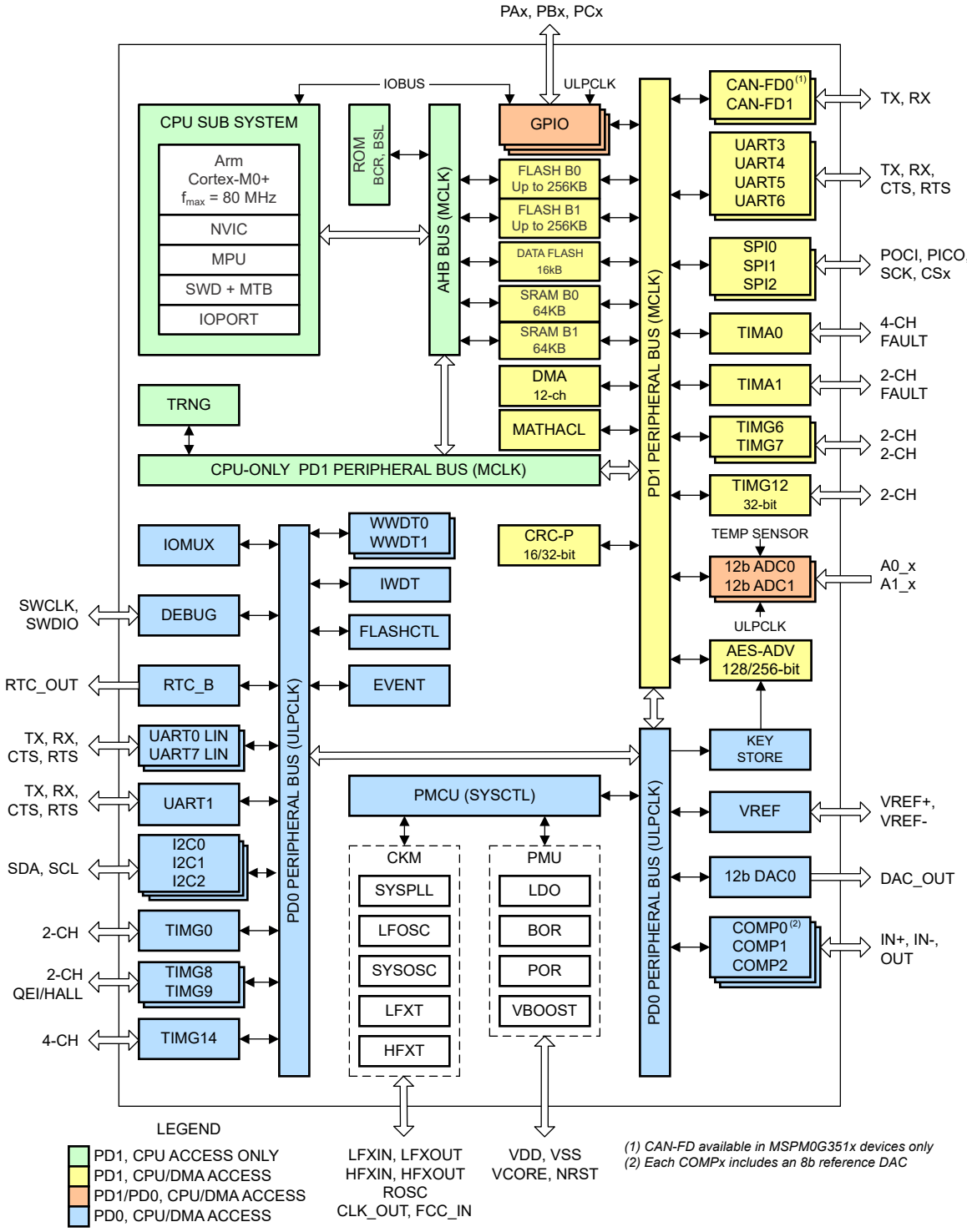


Figure 8-1. MSPM0Gx51x Functional Block Diagram

8.2 CPU

The CPU sub system (MCPUSS) implements an ARM Cortex-M0+ CPU, an instruction pre-fetch/cache, a system timer, a memory protection unit, and interrupt management features. The ARM Cortex-M0+ is a cost-optimized, 32-bit CPU which delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- ARM Cortex-M0+ CPU supporting clock frequencies from 32kHz to 80MHz
  - ARMv6-M Thumb instruction set (little endian) with single-cycle 32x32 multiply instruction
  - Single-cycle access to GPIO registers via ARM single-cycle IO port
- Pre-fetch logic to improve sequential code execution, and I-cache with 4 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Memory protection unit (MPU) with 8 programmable regions
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail-chaining
- Interrupt groups for expanding the total interrupt sources, with jump index for low interrupt latency

8.3 Operating Modes

MSPM0G MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (e.g. RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0G devices implement two power domains: PD1 (for the CPU, memories, and high performance peripherals), and PD0 (for low speed, low power peripherals). PD1 is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 is always powered in RUN, SLEEP, STOP, and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode.

8.3.1 Functionality by Operating Mode (MSPM0Gx51x)

Supported functionality in each operating mode is given in Table 8-1.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but it is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 8-1. Supported Functionality by Operating Mode

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
Oscillators	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT[1]	EN	DIS	DIS	DIS	OFF
	LFOSC or LFXT	EN (LFOSC or LFXT)											OFF
	HFXT	OPT	DIS	DIS	OPT	DIS	DIS	DIS	DIS	DIS	DIS	DIS	OFF
	SYSPLL	OPT	DIS	DIS	OPT	DIS	DIS	DIS	DIS	DIS	DIS	DIS	OFF

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 8-1. Supported Functionality by Operating Mode (continued)

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
Clocks	CPUCLK	80 MHz	32 kHz	32 kHz	DIS								OFF
	MCLK to PD1	80 MHz	32 kHz	32 kHz	80 MHz	32 kHz	32 kHz	DIS					OFF
	ULPCLK to PD0	40 MHz	32 kHz	32 kHz	40 MHz	32 kHz	32 kHz	4 MHz (1)	4 MHz	32 kHz		DIS	OFF
	ULPCLK to TIMG0, TIMG8, TIMG9, TIMG14	40 MHz	32 kHz	32 kHz	40 MHz	32 kHz	32 kHz	4 MHz (1)	4 MHz	32 kHz			OFF
	RTCCLK	32 kHz											OFF
	MFCLK	OPT	DIS		OPT	DIS		OPT		DIS			OFF
	MFPCLK	OPT	DIS		OPT	DIS		OPT		DIS			OFF
	LFCLK	32 kHz										DIS	OFF
	LFCLK to TIMG0, TIMG8, TIMG9, TIMG14	32 kHz											OFF
	LFCLK Monitor	OPT											OFF
	MCLK Monitor	OPT										DIS	OFF
PMU	POR monitor	EN											
	BOR monitor	EN											OFF
	Core regulator	FULL DRIVE						REDUCED DRIVE			LOW DRIVE		OFF
Core Functions	CPU	EN			DIS								OFF
	DMA	OPT						DIS (triggers supported)					OFF
	Flash	EN						DIS					OFF
	SRAM (Bank 0)	EN						DIS					OFF
	SRAM (Bank 1)	OPT						DIS / OFF			OFF		
PD1 Peripherals	CRC	OPT						DIS					OFF
	UART3, UART4, UART5, UART6	OPT						DIS					OFF
	SPI0, SPI1, SPI2	OPT						DIS					OFF
	MATHACL	OPT						OFF					
	AESADV	OPT						OFF					
	MCAN0, MCAN1	OPT						OFF					
	TIMA0, TIMA1	OPT						OFF					
	TIMG0, TIMG6, TIMG7, TIMG12	OPT						OFF					

Table 8-1. Supported Functionality by Operating Mode (continued)

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
PD0 Peripherals	TIMG0, TIMG8, TIMG9, TIMG14	OPT											OFF
	RTC_B	OPT											OFF
	UART0, UART1, UART7	OPT										OPT(2)	OFF
	I2C0, I2C1, I2C2	OPT										OPT(2)	OFF
	GPIOA, GPIOB(3)	OPT										OPT(2)	OFF
	WWDT0, WWDT1	OPT										DIS	OFF
	IWDT	OPT											OFF
Analog	TRNG	OPT						OFF					
	ADC0, ADC1(3)	OPT								NS (triggers supported)			OFF
	DAC0	OPT								NS			OFF
	COMP0, COMP1, COMP2	OPT	OPT (ULP)		OPT	OPT (ULP)		OPT		OPT (ULP)			OFF
	VREF	OPT											OFF
	Temperature Sensor	OPT									OFF		
IOMUX and IO Wakeup		EN											DIS w/ WAKE
Wake Sources		N/A			ANY IRQ			PD0 IRQ					IOMUX, NRST, SWD

(1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCLK remains at 32 kHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCLK remains at 32 kHz as it was in RUN2.
(2) When using the STANDBY1 policy for STANDBY, only TIMG0, TIMG8, and the RTC are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.
(3) For ADCx and GPIO Ports A and B, the digital logic is in PD0 and the register interface is in PD1. These peripherals support fast single-cycle register access when PD1 is active and also support basic operation down to STANDBY mode where PD0 is still active.

8.4 Security

This PSA-L1 certified device offers several security features, including:

- Debug security
- Device identify
- Crypto acceleration
- True random number generation
- Flash write-erase protection
- Flash read-execute protection
- Flash IP protection
- SRAM write-execute mutual exclusion
- Secure boot
- Secure firmware update

ADVANCE INFORMATION

- Secure key storage
- Customer secure code
- Hardware monotonic counter

For more details, see the Security chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.5 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brown-out reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.6 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32KHz)
- **SYSOSC**: Internal high-frequency oscillator (4MHz or 32MHz with factory trim, 16MHz or 24MHz with user trim)
- **LFXT/LFCKIN** : low-frequency external crystal oscillator or digital clock input (32KHz)
- **HFXT/HFCKIN**: high-frequency external crystal oscillator or digital clock input (4 to 48MHz)
- **SYSPLL**: system phase locked loop with 3 outputs (32 to 80MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **MFPCLK**: 4MHz fixed mid-frequency precision clock, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High speed clock derived from HFCLK or the SYSPLL, available in RUN and SLEEP mode
- **CANCLK**: CAN functional clock, derived from HFCLK or SYSPLL

For more details, see the CKM chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.7 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 12 independent DMA transfer channels
  - 6 full-feature channel (DMA0-DMA5), supporting repeated transfer modes
  - 6 basic channels (DMA6-DMA11) supporting single transfer modes
- Configurable DMA channel priorities
- Byte (8 bit), short word (16 bit), word (32 bit), long word (64 bit) and quad word (128 bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications
- Gather mode

Table 8-2 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-2. DMA Trigger Mapping

DMACTL.DMATSEL	Trigger Source	DMACTL.DMATSEL	Trigger Source
0	Software	17	SPI2 Publisher 2
1	Generic Subscriber (FSUB_0)	18	UART3 Publisher 1
2	Generic Subscriber (FSUB_1)	19	UART3 Publisher 2
3	AESADV Publisher 1	20	UART4 Publisher 1
4	AESADV Publisher 2	21	UART4 Publisher 2
5	DAC0 Publisher 2	22	UART5 Publisher 1
6	I2C0 Publisher 1	23	UART5 Publisher 2
7	I2C0 Publisher 2	24	UART6 Publisher 1
8	I2C1 Publisher 1	25	UART6 Publisher 2
9	I2C1 Publisher 2	26	UART0 Publisher 1
10	I2C2 Publisher 1	27	UART0 Publisher 2
11	I2C2 Publisher 2	28	UART7 Publisher 1
12	SPI0 Publisher 1	29	UART7 Publisher 2
13	SPI0 Publisher 2	30	UART1 Publisher 1
14	SPI1 Publisher 1	31	UART1 Publisher 2
15	SPI1 Publisher 2	32	ADC0 DMA Trigger
16	SPI2 Publisher 1	33	ADC1 DMA Trigger

For more details, see the DMA chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.8 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA, or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) which are interconnected through an event fabric containing a combination of static and programmable routes.

Events which are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: RTC interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)

ADVANCE INFORMATION

– Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

Refer to Event chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for more information.

Table 8-3. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 1
4	Generic event channel 4 selected	1 : 1
5	Generic event channel 5 selected	1 : 1
6	Generic event channel 6 selected	1 : 1
7	Generic event channel 7 selected	1 : 1
8	Generic event channel 8 selected	1 : 1
9	Generic event channel 9 selected	1 : 1
10	Generic event channel 10 selected	1 : 1
11	Generic event channel 11 selected	1 : 1
12	Generic event channel 12 selected	1 : 2 (splitter)
13	Generic event channel 13 selected	1 : 2 (splitter)
14	Generic event channel 14 selected	1 : 2 (splitter)
15	Generic event channel 15 selected	1 : 2 (splitter)

8.9 Memory

8.9.1 Memory Organization

Table 8-4 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* .

Table 8-4. Memory Organization

MEMORY REGION	SUBREGION	MSPM0G1518, MSPM0G3518	MSPM0G1519, MSPM0G3519
Code (Flash Bank 0)	MAIN ECC Corrected	128KB	256KB
		0x0000.0000 to 0x0001.FFFF	0x0000.0000 to 0x0003.FFFF
	MAIN ECC Uncorrected	0x0040.0000 to 0x0041.FFFF	0x0040.0000 to 0x0043.FFFF
	Flash ECC code	0x0080.0000 to 0x0081.FFFF	0x0080.0000 to 0x0083.FFFF
Code (Flash Bank 1)	MAIN ECC Corrected	128KB	256KB
		0x0002.0000 to 0x0003.FFFF	0x0004.0000 to 0x0007.FFFF
	MAIN ECC Uncorrected	0x0042.0000 to 0x0043.FFFF	0x0044.0000 to 0x0047.FFFF
	Flash ECC code	0x0082.0000 to 0x0083.FFFF	0x0084.0000 to 0x0087.FFFF

Table 8-4. Memory Organization (continued)

MEMORY REGION	SUBREGION	MSPM0G1518, MSPM0G3518	MSPM0G1519, MSPM0G3519
Data Flash Bank	Data Flash ECC Corrected	16KB	16KB
		0x41D0.0000 to 0x41D0.3FFF	0x41D0.0000 to 0x41D0.3FFF
	Data Flash Unchecked	0x41E0.0000 to 0x41E0.3FFF	0x41E0.0000 to 0x41E0.3FFF
	Data Flash ECC code	0x41F0.0000 to 0x41F0.3FFF	0x41F0.0000 to 0x41F0.3FFF
SRAM (Bank 0)	SRAM ECC Corrected	64KB	64KB
		0x2000.0000 to 0x2000.FFFF	0x2000.0000 to 0x2000.FFFF
	SRAM Parity Checked	0x2010.0000 to 0x2010.FFFF	0x2010.0000 to 0x2010.FFFF
	SRAM Unchecked	0x2020.0000 to 0x2020.FFFF	0x2020.0000 to 0x2020.FFFF
	SRAM ECC code	0x2030.0000 to 0x2030.FFFF	0x2030.0000 to 0x2030.FFFF
SRAM (Bank 1)	SRAM Unchecked	64KB	64KB
		0x2021.0000 to 0x2021.FFFF	0x2021.0000 to 0x2021.FFFF
Peripheral	Peripherals	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF
	NONMAIN Corrected	2KB	2KB
		0x41C0.0000 to 0x41C0.07FF	0x41C0.0000 to 0x41C0.07FF
	NONMAIN Uncorrected	0x41C1.0000 to 0x41C1.07FF	0x41C1.0000 to 0x41C1.07FF
	NONMAIN ECC code	0x41C2.0000 to 0x41C2.07FF	0x41C2.0000 to 0x41C2.07FF
	FACTORY Corrected	512Bytes	512Bytes
		0x41C4.0000 to 0x41C4.01FF	0x41C4.0000 to 0x41C4.01FF
	FACTORY Uncorrected	0x41C5.0000 to 0x41C5.01FF	0x41C5.0000 to 0x41C5.01FF
	FACTORY ECC code	0x41C6.0000 to 0x41C6.01FF	0x41C6.0000 to 0x41C6.01FF
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

ADVANCE INFORMATION

8.9.2 Peripheral File Map

Table 8-5 lists the available peripherals and the register base address for each.

Table 8-5. Peripherals Summary

Peripheral Name	Base Address	Size
ADC0	0x40000000	0x2000
ADC1	0x40002000	0x2000
COMP0	0x40008000	0x2000
COMP1	0x4000A000	0x2000
COMP2	0x4000C000	0x2000
DAC0	0x40018000	0x2000
VREF	0x40030000	0x2000
WWDT0	0x40080000	0x2000
WWDT1	0x40082000	0x2000
TIMG0	0x40084000	0x2000
TIMG8	0x40090000	0x2000
TIMG9	0x40092000	0x2000

Table 8-5. Peripherals Summary (continued)

Peripheral Name	Base Address	Size
RTC_B	0x40094000	0x2000
TIMG14	0x40096000	0x2000
GPIOA	0x400A0000	0x2000
GPIOB	0x400A2000	0x2000
GPIOC	0x400A4000	0x2000
KEYSTORE	0x400AC000	0x2000
SYSCTL	0x400AF000	0x4000
DEBUGSS	0x400C7000	0x2000
EVENT	0x400C9000	0x3000
NVM	0x400CD000	0x2000
I2C0	0x400F0000	0x2000
I2C1	0x400F2000	0x2000
I2C2	0x400F4000	0x2000
UART1	0x40100000	0x2000
UART0	0x40108000	0x2000
UART7	0x4010A000	0x2000
MCPUSS	0x40400000	0x2000
MTB	0x40402000	0x1000
MTBRAM	0x40403000	0x0020
MATHACL	0x40410000	0x2000
IOMUX	0x40428000	0x2000
DMA	0x4042A000	0x2000
CRC	0x40440000	0x2000
AESADV	0x40442000	0x2000
TRNG	0x40444000	0x2000
SPI0	0x40468000	0x2000
SPI1	0x4046A000	0x2000
SPI2	0x4046C000	0x2000
UART3	0x40500000	0x2000
UART4	0x40502000	0x2000
UART5	0x40504000	0x2000
UART6	0x40506000	0x2000
MCAN0	0x40508000	0x8000
MCAN1	0x40510000	0x8000
ADC0 (1)	0x40556000	0x2000
ADC1 (1)	0x40558000	0x2000
TIMA0	0x40860000	0x2000

Table 8-5. Peripherals Summary (continued)

Peripheral Name	Base Address	Size
TIMA1	0x40862000	0x2000
TIMG6	0x40868000	0x2000
TIMG7	0x4086A000	0x2000
TIMG12	0x40870000	0x2000

(1) Aliased region of ADC0 and ADC1 memory-mapped registers

8.9.3 Peripheral Interrupt Vector

Table 8-6 shows the IRQ number and the interrupt group number for each periperals in this device.

Table 8-6. Interrupt vector number

Peripheral Name	NVIC IRQ	Group IIDX
WWDT0	0	0
WWDT1	0	1
DEBUGSS	0	2
FLASHCTL	0	3
EVENT SUB PORT 0	0	4
EVENT SUB PORT 1	0	5
SYSCTL	0	6
GPIOA	1	0
GPIOB	1	1
COMP0	1	2
COMP1	1	3
COMP2	1	4
TRNG	1	5
GPIOC	1	6
TIMG8	2	-
UART3	3	-
ADC0	4	-
ADC1	5	-
CANFD0	6	-
DAC0	7	-
TIMG9	8	-
SPI0	9	-
SPI1	10	-
SPI2	11	-
CANFD1	12	-
UART1	13	-
UART4	14	-
UART0	15	-
TIMG0	16	-
TIMG6	17	-
TIMA0	18	-
TIMA1	19	-
TIMG7	20	-
TIMG12	21	-
TIMG14	22	-
UART5	23	-
I2C0	24	-
I2C1	25	-
I2C2	26	-
UART7	27	-
AESADV	28	-
UART6	29	-

Table 8-6. Interrupt vector number (continued)

Peripheral Name	NVIC IRQ	Group IIDX
RTC_B	30	-
DMA0	31	-

8.10 Flash Memory

A dual bank of non-volatile flash memory (up to 256kB/512kB total) and a separate data flash bank (16kB) is provided for storing executable program code and application data.

Key features of the flash include:

- Hardware ECC protection (encode and decode) with single bit error correction and double bit error detection
- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1kB sector sizes (minimum erase resolution of 1kB)
- Up to 100,000 program/erase cycles on the lower 32kB of the flash memory (and data flash bank), with up to 10,000 program/erase cycles on the remaining flash memory (devices with 32kB support 100,000 cycles on the entire flash memory)
- Bank address swap for in-system, over-the-air (OTA) firmware updates

For a complete description of the flash memory, see the NVM chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.11 SRAM

MSPM0 MCUs include a low power, high performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. MSPM0 MCUs also provides up to 128KB SRAM. SRAM memory may be used for storing volatile information such as the call stack, heap, global data, and code.

The SRAM memory content is split into two banks of 64kB each. SRAM (Bank 0) provides 64kB of ECC or parity protected SRAM and is always available in run, sleep, stop, and standby operating modes. SRAM (Bank 1) provides 64kB which does not include ECC protection or parity and can be selectively enabled or disabled through BANKOFF1 bit in SRAMCFG register in SYSCTL. When enabled, SRAM (Bank 1) is available in run, sleep, and stop modes. SRAM (Bank 1) can be powered off in STOP mode by configuring the BANKSTOP1 bit in SRAMCFG register in SYSCTL. SRAM contents for both banks are lost in shutdown mode.

A write protection mechanism is provided to allow the application to prevent unintended modifications to the SRAM memory. Write protection is useful when placing executable code into SRAM as it provides a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

Please note that if the DMA controller is to be configured for DMA transfers which access the SRAM, the ECC protected SRAM address region must not be used by the DMA or the CPU. In cases where the DMA must access SRAM, configure the DMA and CPU to use only the parity checked SRAM address region or the unchecked SRAM address region.

8.12 GPIO

The general purpose input/output (GPIO) peripheral provides the user with a means to write data out and read data in to and from the device pins. Through the use of the Port A, Port B, and Port C GPIO peripherals, these devices support up to 93 GPIO pins.

The key features of the GPIO module include:

- 0 wait state MMR access from CPU
- Set/Clear/Toggle multiple bits without the need of a read-modify-write construct in software
- GPIOs with "Standard with Wake" drive functionality able to wake the device from SHUTDOWN mode
- User controlled input filtering
- GPIO "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port

ADVANCE INFORMATION

For more details, see the GPIO chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.13 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.14 ADC

Both 12-bit analog-to-digital converter (ADC) modules in these devices, ADC0 and ADC1, support fast 12-bit conversions with single-ended inputs and simultaneous sampling operation.

ADC features include:

- 12-bit output resolution at 4Msps with greater than 11 ENOB
- HW averaging enables 14-bit effective resolution at 250ksps
- Up to 27 total external input channels with individual result storage registers
- Internal channels for temperature sensing and supply monitoring
- Software selectable reference:
  - Configurable internal reference voltage of 1.4V and 2.5V (requires decoupling capacitor on VREF+/- pins)
  - MCU supply voltage (VDD)
  - External reference supplied to the ADC through the VREF+/- pins
- Operates in RUN, SLEEP, and STOP modes

Table 8-7 shows the ADC channel mapping in the device.

Table 8-7. ADC Channel Mapping

CHANNEL[0:7]	SIGNAL NAME(2)		CHANNEL[8:15]	SIGNAL NAME(1) (2)	
	ADC0	ADC1		ADC0	ADC1
0	A0_0	A1_0 / DAC_OUT[3]	8	A0_8	A1_8
1	A0_1	A1_1	9	A0_9	-
2	A0_2	A1_2	10	-	A1_10
3	A0_3	A1_3	11	*Temperature Sensor*	A1_11
4	A0_4	A1_4	12	A0_12	A1_12 / VREF+
5	A0_5	A1_5	13	A0_13	A1_13
6	A0_6	A1_6	14	A0_14	A1_14
7	A0_7	A1_7 / VREF-	15	*Supply/Battery Monitor*	*Supply/Battery Monitor*

(1) *Italicized* signal names are purely internal to the device. These signals are used for internal peripheral interconnections.
(2) For more information about device analog connections please refer to Section 8.33
(3) When DAC_OUT is used, A1_0 cannot be used to sample external signals. Avoid using external circuitry on the PA15 pin when using DAC_OUT.

For more details, see the ADC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.15 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4-V internal VREF at the factory trim temperature (TS_{TRIM}).

The ADC and VREF configuration for the above measurement is as the following: RES=0 (12-bit mode), VRSEL=0h (VDD), BUFCONFIG=1h (1.4V VREF), ADC t_{Sample}=10µs. This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature.

See the temperature sensor section of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for guidance on estimating the device temperature with the factory trim value.

8.16 VREF

The shared voltage reference module (VREF) in these devices contain a configurable voltage reference buffer which allows users to supply a stable reference to on-board analog peripherals. It also supports bringing in an external reference for applications where higher accuracy is required.

VREF features include:

- 1.4V and 2.5V user-selectable internal references
- Internal reference supports full speed ADC operation
- Support for bringing in an external reference on VREF+/- device pins
- Requires a decoupling capacitor placed on VREF+/- pins for proper operation. See VREF for more details.

For more details, see the VREF chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.17 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. It supports the following key features:

- Programmable hysteresis
- Programmable reference voltage:
  - External reference voltage (VREF IO)
  - Internal reference voltage (1.4V, 2.5V)
  - Integrated 8-bit reference DAC
- Configurable operation modes:
  - High-speed mode
  - Low-power mode
- Programmable output glitch filter delay
- Supports 6 blanking sources from TIMx instances (see Table 8-8)
- Device wakeup from all low power modes using comparator output
- Output connected to advanced timer fault handling mechanism
- Selection of comparator channel inputs from device pins or internal analog module (see Table 8-9, Table 8-10 and Table 8-11)

Table 8-8. COMP Blanking Source Table

CTL2.BLANKSRC	BLANKING SOURCE
1	TIMA0.CC2
2	TIMA0.CC3
3	TIMA1.CC1
4	TIMG12.CC1
5	TIMG6.CC1
6	TIMG7.CC1

ADVANCE INFORMATION

Table 8-9. COMP0 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP0_IN0+	COMP0_IN0-
0x1	COMP0_IN1+	COMP0_IN1-
0x2	COMP0_IN2+	COMP0_IN2-
0x3	DAC_OUT / COMP0_IN3+(1)	-
0x5	-	Temperature Sensor
0x7	COMP1 positive terminal signal	-

Table 8-10. COMP1 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP1_IN0+	COMP1_IN0-
0x1	COMP1_IN1+	COMP1_IN1- / VREF+
0x2	COMP1_IN2+	COMP1_IN2-
0x3	DAC_OUT / COMP1_IN3+(1)	-
0x7	COMP0 positive terminal signal	-

Table 8-11. COMP2 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP2_IN0+	COMP2_IN0-
0x1	COMP2_IN1+	COMP2_IN1- / VREF-

(1) The connection to COMP0/1_IN3+ and DAC_OUT connects using the PA15 pin. When connecting DAC_OUT to COMP0/1_IN3+, avoid using external circuitry on the PA15 pin.

For more information about device analog connections, see Section 8.33.

For more details, see the COMP chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.18 DAC

The 12-bit buffered digital-to-analog converter (DAC) in these devices converts a digital input value into an analog voltage to a buffered output channel and it supports the following key features:

- Up to 1Msps output sampling rate
- 8-bit or 12-bit voltage-output resolution
- Self-calibration option for offset error correction
- Straight binary or twos-complement data format
- Integrated sample time generator for generation of predefined sampling rates
- Integrated FIFO and support DMA operation
- One hardware trigger from event fabric for conversion
- Programmable voltage reference options:
  - Supply voltage (VDD)
  - External reference voltage (VREF IO)
  - Internal reference voltage (1.4V, 2.5V)

For more information about device analog connections, see Section 8.33.

For more details, see the DAC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.19 TRNG

The true random number generator (TRNG) utilizes an internal circuit to generate 32-bit random numbers. The TRNG is intended to be used as a source to a deterministic random number generator (DRNG) to build a FIPS-140-2 compliant system. Key features of the TRNG include:

- Generation of 32-bit random numbers
- A new 32-bit number may be generated every 32 * 4 = 128 TRNG clock cycles
- Built-in health tests
- Available in RUN and SLEEP modes

For more details, see the TRNG chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.20 AESADV

The AES advanced (AESADV) accelerator module performs encryption and decryption of 128-bit data blocks with a 128-bit or 256-bit key in hardware according to the advanced encryption standard (AES). AES is a symmetric-key block cipher algorithm specified in FIPS PUB 197.

The AESADV accelerator features include:

- AES operation with 128-bit and 256-bit keys
- Key scheduling in hardware
- Enc/decrypt only modes: CBC, CFB-1, CFB-8, CFB-128, OFB-128, CTR/ICM
- Authentication only modes: CBC-MAC, CMAC
- AES-CCM
- AES-GCM
- AES-CCM and AES-GCM modes support continuation with hold/resume of payload data
- 32-bit word access to provide key data, input data, and output data
- AESADV ready interrupt
- DMA triggers for input/output data
- Supported in RUN and SLEEP (see the *Operating Modes* section of the device technical reference manual)

For more details, see the AESADV chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.21 Keystore

The Keystore controller provides secure management of the Advanced Encryption Engine (AES) keys. The use-model of the keystore controller is to securely deposit keys into it during the execution of customer secure code, and have the AES engine access them subsequently in a secure manner without leaking any key data to observers. Both 128 and 256-bit keys can be stored in the keystore's key slots. The keystore and its interaction with the AES engine are designed for secure operation including thwarting partial key modification attacks.

For more details, see the KEYSTORE chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.22 CRC-P

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal
- Support for custom polynomials

For more details, see the CRC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* .

8.23 MATHACL

The math accelerator (MATHACL) is a collection of hardware accelerated 32-bit math functions to improve system computational throughput. The MATHACL offloads mathematical calculations performed by the CPU to improve efficiency and CoreMark performance.

The following hardware functions are available in the MATHACL:

- Sine/Cosine (SINCOS)
- Arc tangent (ATAN2)
- Square root (SQRT)
- Division (DIV)
- Multiply with 32-bit result (MPY32)
- Square with 32-bit result (SQUARE32)
- Multiply with 64-bit result (MPY64)
- Square with 64-bit result (SQUARE64)
- Multiply-accumulate (MAC)
- Square-accumulate (SAC)

For more details, see the MATHACL chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.24 UART

The UART peripherals (UART0-UART1, UART3-UART7) provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity -bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8 or 3
  - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs support DAM data transfer
- Support transmit and receive loopback mode operation
- See Table 8-12 for detail information on supported protocols

Table 8-12. UART Features

UART Features	UART0, UART7 (Extend)	UART1, UART2 (Main, low-power)	UART3-UART6 (Main)
Active in Stop and Standby Mode	Yes	Yes	-
Separate transmit and receive FIFOs	Yes	Yes	Yes
Support hardware flow control	Yes	Yes	Yes
Support 9-bit configuration	Yes	Yes	Yes
Support LIN mode	Yes	-	-
Support DALI	Yes	-	-
Support IrDA	Yes	-	-
Support ISO7816 Smart Card	Yes	-	-
Support Manchester coding	Yes	-	-

For more details, see the UART chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.25 I2C

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching

- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
  - Supported on open drain IOs (ODIO) and high-drive (HDIO) IOs only
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- Wakeup from low power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression
- 8-entry transmit and receive FIFOs

For more details, see the I2C chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.26 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to 32Mbits/s in both controller and peripheral mode [1]
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode) and 7 bits to 16 bit(peripheral mode)
- Supports PACKEN feature that allows the packing of 2 16 bit FIFO entries into a 32-bitvalue to improve CPU performance
- Transmit and receive FIFOs (4 entries each with 16 bits per entry) supporting DMA data transfer
- Supports TI mode, Motorola mode and National Microwire format

For more details, see the SPI chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.27 CAN-FD

The controller area network (CAN) controller enables communication with a CAN2.0A, CAN2.0B, or CAN-FD bus and is compliant to ISO 11898-1:2015 standard supporting up to 5M bit/s bit rate. Key features of the CAN-FD peripheral include:

- Full support for 64-byte CAN-FD frames
- Dedicated 1kB message SRAM with ECC
- Configurable transmit FIFO, transmit queue and event FIFO (up to 32 elements)
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs (up to 64 elements each)
- Up to 128 filter elements
- Two interrupt lines
- Power-down and wake-up support
- Timestamp counter

For more details, see the CAN-FD chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.28 Low-Frequency Sub System (LFSS)

The Low-Frequency Sub-System (LFSS) is a sub-system which combines several functional peripherals under one shared subsystem. These peripherals are clocked by the low freqency clock (LFCLK) or need to be active during low power modes. The LFCLK has a typical frequency of 32kHz and is mainly intended for long-term timekeeping.

LFSS in this device contains following components:

- RTC_B with additional prescalar extension and timestamp captures
- An asynchronous IWDT_B

[1] Only SPI signals on HSIO pins support data rate > 16 Mbits/s; see *Pin Diagrams* for HSIO pins.

ADVANCE INFORMATION

For more details, see the LFSS chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.29 RTC_B

The RTC_B instance of the real-time clock operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. The RTC_B provides common key features in relation to the Low-Frequency Sub System (LFSS).

Common key features of the RTC_B include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format
- Leap-year handling
- One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128 Hz
- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5 Hz
- Calibration for crystal offset error (up to +/- 240ppm)
- Compensation for temperature drift (up to +/- 240ppm)
- RTC clock output to pin for calibration

Table 8-13 shows the RTC features supported in this device.

Table 8-13. RTC_B Key Features

RTC Features	RTC_B
Power enable register	-
Real-time clock and calendar mode providing seconds, minutes, hours, day of week, day of month, and year	Yes
Selectable binary or binary-coded decimal (BCD) format	Yes
Leap-year correction (valid for year 1901 through 2099)	Yes
Two customizable calendar alarm interrupts based on minute, hour, day of the week, and day of the month	Yes
Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon	Yes
Periodic interrupt to wake at 4096, 2048, 1024, 512, 256, or 128Hz	Yes
Periodic interrupt to wake at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz	Yes
Interrupt capability down to STANDBY mode with STOPCLKSTBY	Yes
Calibration for crystal offset error and crystal temperature drift (up to ±240 ppm total)	Yes
RTC clock output to pin for calibration (GPIO)	Yes
RTC clock output to pin for calibration (TIO)	-
Three -bit prescaler for heartbeat function with interrupt generation	-
RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz or 1Hz	-
RTC time stamp capture upon detection of a timer stamp event, including: • TIO event • VDD fail event	-
RTC counter lock function	-

For more details, see the RTC chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.30 IWDT_B

The independent watchdog timer (IWDT) in the LFSS is a device-independent supervisor which monitors code execution and overall hang up scenarios of the device. Due to the nature of LFSS, this IWDT has its own system independent clock source. If the application software does not successfully reset the watchdog within the programmed time, the watchdog generates a POR reset to the device.

Key features of the IWDT include:

- A 25-bit counter
- Counter driven from LFOSC (fixed 32kHz clock path) with a programmable clock divider
- Eight selectable watchdog timer periods (2ms to 2hr)

For more details, see the IWDT chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.31 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.32 Timers (TIMx)

There are two timer peripherals in these devices support that following key features: TIMGx (general-purpose timer) and TIMAx (advanced timer). TIMGx is a subset of TIMAx, which means common features between timer instances are software compatible. For specific configurations, see Table 8-14:

Specific features for the general-purpose timer **(TIMGx)** include:

- 16-/32-bit up, down, up-down or down-up counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow CC register available in TIMG6, TIMG7 and TIMG12
- Shadow register for load available in TIMG6, TIMG7
- Support quadrature encoder interface (QEI) and Hall sensor input logic available in TIMG8, TIMG9
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability

Specific features for the advanced timer **(TIMAx)** include:

- 16-bit down or up-down counter, with repeat-reload mode
- Selectable and configurable clock source

ADVANCE INFORMATION

- 8-bit programmable prescaler to divide the counter clock frequency
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow register for load and CC register available in both TIMA0 and TIMA1
- Complementary output PWM with programmable dead band insertion
- Asymmetric PWM
- Configurable fault handling mechanism for
  - Fast PWM responses (<40ns) to external fault inputs or comparator events
  - Outputting signals in a safe user-defined state when a latched fault condition has occurred
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt and DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Table 8-14. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEADBAND	FAULT	QEI
TIMG0	PD0	16 bit	8 bit	–	2	–	–	–	–	–	–
TIMG6	PD1	16 bit	8 bit	–	2	–	–	–	–	–	–
TIMG7	PD1	16 bit	8 bit	–	2	–	Yes	Yes	–	–	–
TIMG8	PD0	16 bit	8 bit	–	2	–	–	–	–	–	Yes
TIMG9	PD0	16 bit	8 bit	–	2	–	–	–	–	–	Yes
TIMG12	PD1	32bit	–	–	2	–	–	Yes	–	–	–
TIMG14	PD0	16 bit	8 bit	–	4	–	–	–	–	–	–
TIMA0	PD1	16 bit	8 bit	8 bit	4	Yes	Yes	Yes	Yes	Yes	–
TIMA1	PD1	16 bit	8 bit	8 bit	2	Yes	Yes	Yes	Yes	Yes	–

For more details, see the TIMx chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

8.33 Device Analog Connections

Figure 8-2 shows the internal analog connection of the device.

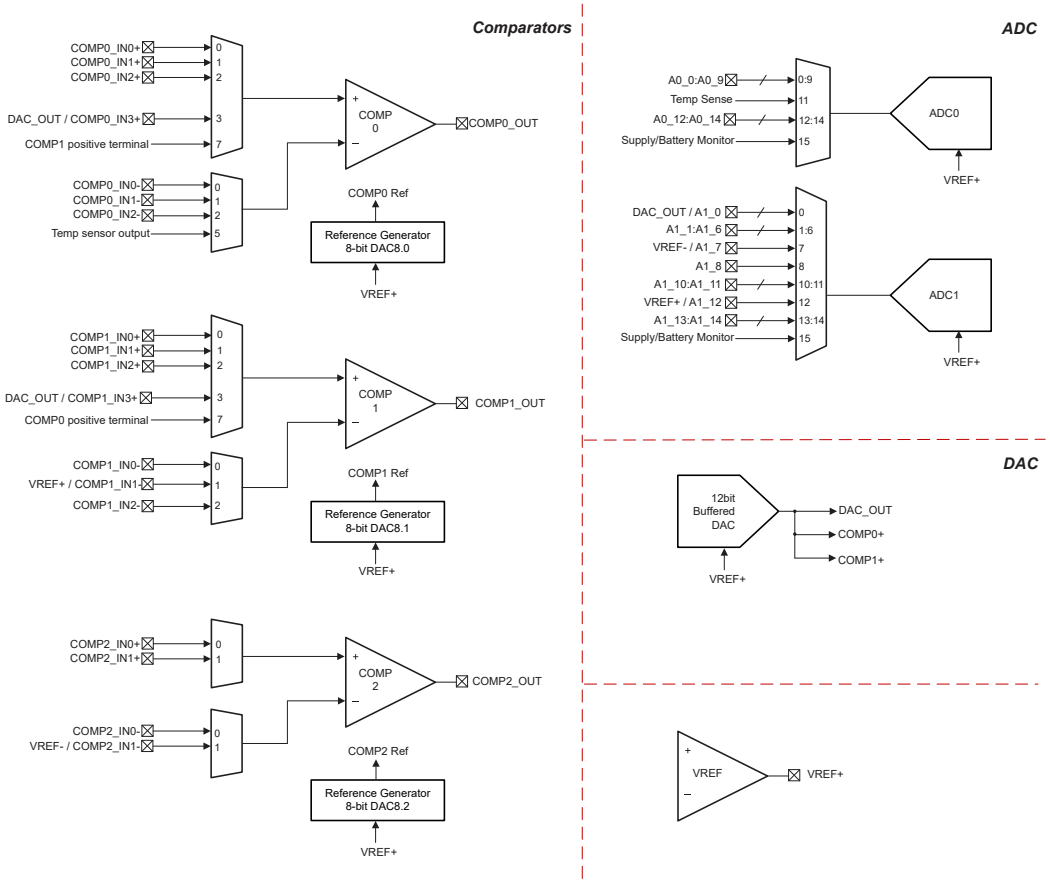


Figure 8-2. Device Analog Connection

Note

Enabling DAC_OUT connects to PA15 therefore it is not recommended to have any external signal on PA15 when using DAC_OUT.

ADVANCE INFORMATION

ADVANCE INFORMATION

8.34 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-3. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

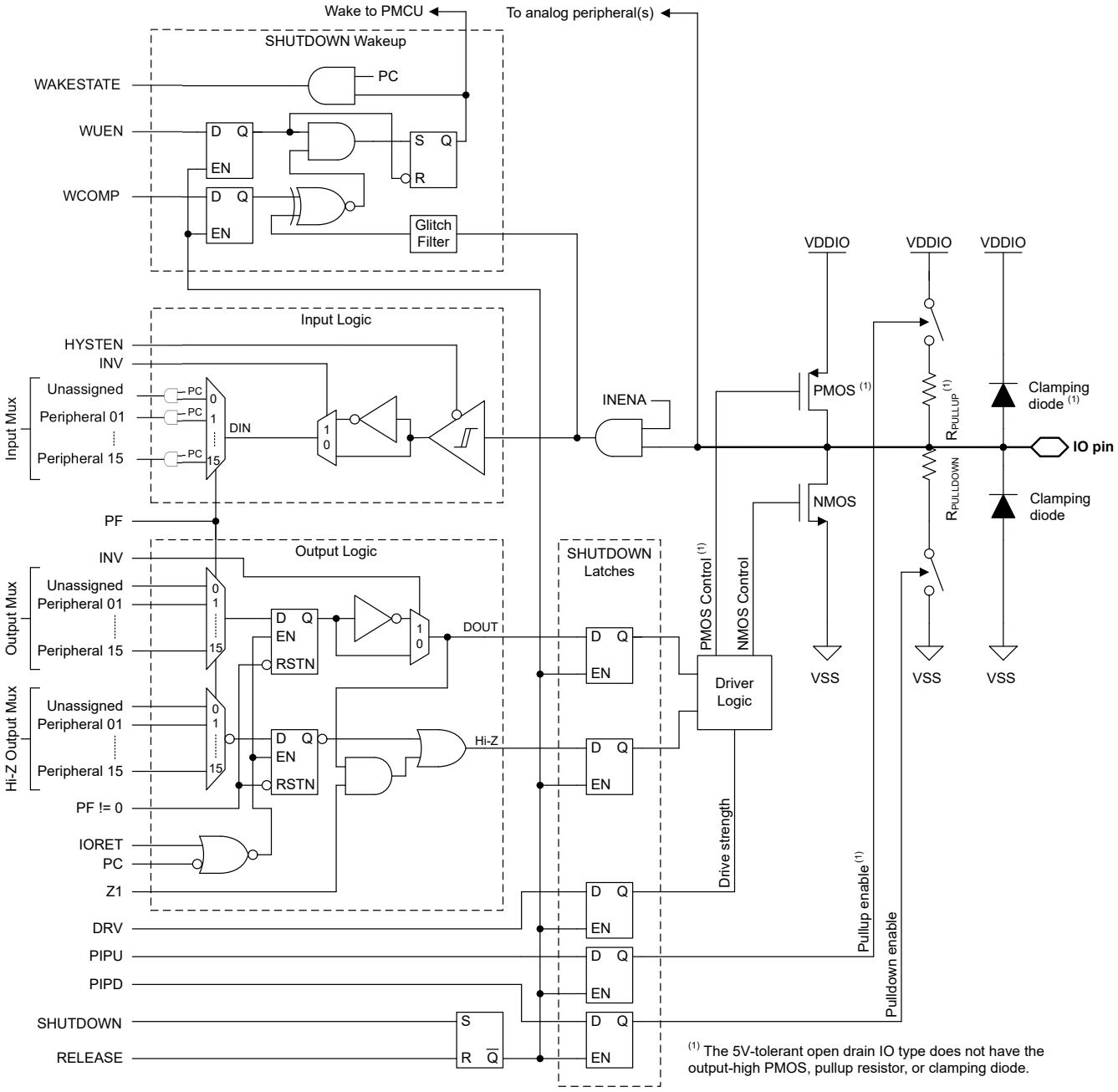


Figure 8-3. Superset Input/Output Diagram

8.35 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an ARM compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality offered on MSPM0 devices, see the DEBUG chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual*.

Table 8-15. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

8.36 Boot Strap Loader (BSL)

The boot strap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART or I2C serial interface. Access to the device memory and configuration through the BSL is protected by a 256 bit user-defined password, and it is possible to completely disable the BSL in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSLRX and BSLTX signals (for UART), or the BSLSCL and BSLSDA signals (for I^2C). Additionally, one or two additional pins (BSL_invoke and NRST) may be used for controlled invokation of the bootloader by an external host.

If enabled, the BSL may be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device will verify the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI will invoke the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL may be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 8-16. BSL Pin Requirements and Functions

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSLRX	Required for UART	UART receive signal (RXD), an input
BSLTX	Required for UART	UART transmit signal (TXD) an output
BSLSCL	Required for I2C	I^2C BSL clock signal (SCL)
BSLSDA	Required for I2C	I^2C BSL data signal (SDA)
BSL_invoke	Optional	Active-high digital input used to start the BSL during boot
NRST	Optional	Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke)

For a complete description of the BSL functionality and command set, see the MSPM0 boot strap loader user's guide.

8.37 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Please

ADVANCE INFORMATION

refer to Factory Constants chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for more information.

Table 8-17. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	PARTNUM	MANUFACTURER
MSPM0G1518, MSPM0G3518	0xBBA9	0x17
MSPM0G1519, MSPM0G3519	0xBBA9	0x17

Table 8-18. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	Part	Variant
MSPM0G1518SPMR	0x2120	0x13
MSPM0G1518SPNR	0x2120	0x16
MSPM0G1518SPTR	0x2120	0x12
MSPM0G1518SPZR	0x2120	0x18
MSPM0G1518SRGZR	0x2120	0x11
MSPM0G1518SRHBR	0x2120	0x10
MSPM0G1519SPMR	0x2407	0x13
MSPM0G1519SPNR	0x2407	0x16
MSPM0G1519SPTR	0x2407	0x12
MSPM0G1519SPZR	0x2407	0x18
MSPM0G1519SRGZR	0x2407	0x11
MSPM0G1519SRHBR	0x2407	0x10
MSPM0G3518SPMR	0x1205	0x13
MSPM0G3518SPNR	0x1205	0x15
MSPM0G3518SPTR	0x1205	0x12
MSPM0G3518SPZR	0x1205	0x16
MSPM0G3518SRGZR	0x1205	0x11
MSPM0G3518SRHBR	0x1205	0x10
MSPM0G3519SPMR	0x1508	0x13
MSPM0G3519SPNR	0x1508	0x15
MSPM0G3519SPTR	0x1508	0x12
MSPM0G3519SPZR	0x1508	0x16
MSPM0G3519SRGZR	0x1508	0x11
MSPM0G3519SRHBR	0x1508	0x10

ADVANCE INFORMATION

8.38 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region, refer to Device Factory Constants section, which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to Factory Constants chapter of the *MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual* for more information.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 10.4)

9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10µF and a 0.1µF low-ESR ceramic decoupling capacitor across the VDD and VSS pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The 10µF bulk decoupling capacitor is a recommended value for most applications, but this capacitance may be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

The NRST reset pin must be pulled up to VDD (supply level) for the device to release from RESET state and start the boot process. TI recommends connecting an external 47kΩ pullup resistor with a 10nF pulldown capacitor for most applications, enabling the NRST pin to be controlled by another device or a debug probe.

The SYSOSC frequency correction loop (FCL) circuit utilizes an external 100kΩ with 0.1% tolerance resistor with a temperature coefficient (TCR) of 25ppm/C or better populated between the ROSC pin and VSS. This resistor establishes a reference current to stabilize the SYSOSC frequency through a correction loop. This resistor is required if the FCL feature is used for higher accuracy, and it is not required if the SYSOSC FCL is not enabled. When the FCL mode is not used, the PA2 pin may be used as a digital input/output pin.

A 0.47µF tank capacitor is required for the VCORE pin and must be placed close to the device with minimum distance to the device ground. Do not connect other circuits to the VCORE pin.

For the 5V-tolerant open drain (ODIO), a pullup resistor is required to output high for I2C and UART functions, as the open drain IO only implement a low-side NMOS driver and no high-side PMOS driver. The 5V-tolerant open drain IO are fail-safe and may have a voltage present even if VDD is not supplied.

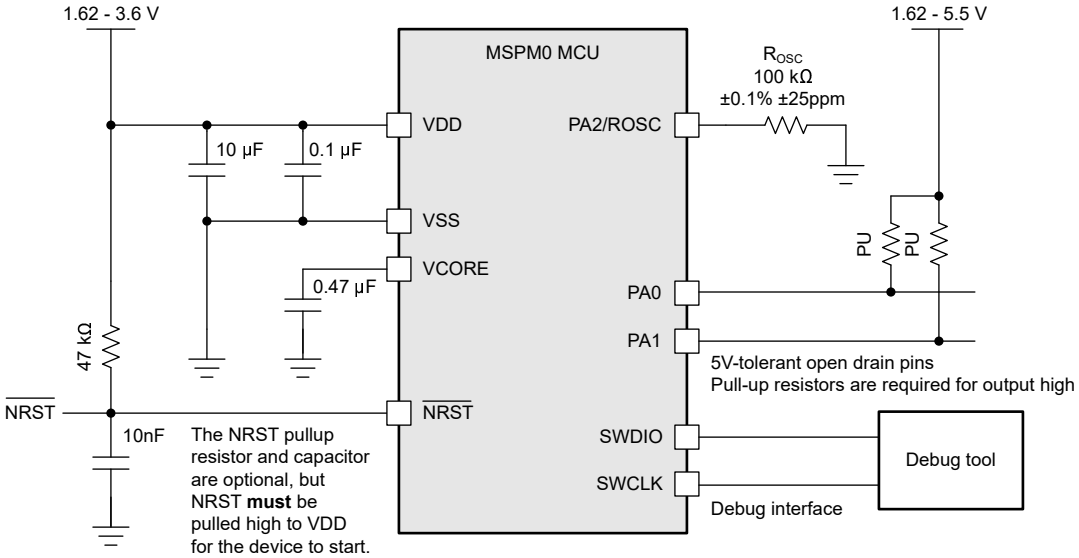


Figure 9-1. Basic Application Schematic

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with development, visit the Texas Instruments *Arm Cortex-M0+ MCUs* page.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. . Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

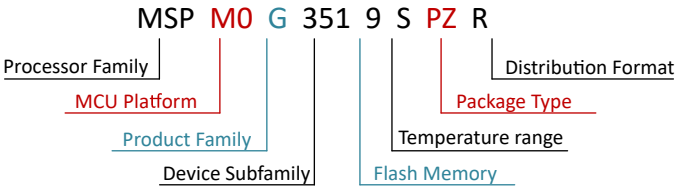


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X= Experimental silicon
MCU Platform	M0 = Arm based 32-bit M0+
Product Family	G = 80MHz frequency
Device Subfamily	351 = 2x ADC, 3x COMP, 2x CAN-FD 151 = 2x ADC, 3x COMP
Flash Memory	8 = 256KB 9= 512KB
Temperature Range	
Package Type	See the Device Comparison section and https://www.ti.com/packaging
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray

ADVANCE INFORMATION

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

10.3 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0G3519	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/ EnergyTrace. The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Developer Zone	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE ,in TI Cloud Tools or a standalone version. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler toolchains

Code Composer Studio™ (CCS)	Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. CCS is completely free to use and is available on Eclipse and Theia frameworks.
IAR Embedded Workbench® IDE	IAR Embedded Workbench for Arm delivers a complete development toolchain for building and debugging embedded applications for MSPM0.The included IAR C/C++ Compiler generates highly optimized code for your application, and the C-SPY Debugger is a fully integrated debugger for source and disassembly level debugging with support for complex code and data breakpoint.
Keil® MDK IDE	Arm Keil MDK is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications for MSPM0.Keil MDK includes a fully integrated debugger for source and disassembly level debugging.MDK provides full CMSIS compliance.
TI Arm-Clang	TI Arm Clang is included in Code Composer Studio.
GNU Arm Embedded Toolchain	The MSPM0 SDK supports development using the open-source Arm GNU Toolchain.Arm GCC is supported by Code Composer Studio (CCS).

ADVANCE INFORMATION

10.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual	This manual describes the modules and peripherals of the MSPM0G family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different devices. Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

LaunchPad™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XMSPM0G1519SRGZR	ACTIVE	VQFN	RGZ	48	4000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSPM0G1519SRHBR	ACTIVE	VQFN	RHB	32	5000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSPM0G3519SPMR	ACTIVE	LQFP	PM	64	1000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSPM0G3519SPNR	ACTIVE	LQFP	PN	80	1000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSPM0G3519SPZR	ACTIVE	LQFP	PZ	100	1000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSPM0G3519SRGZR	ACTIVE	VQFN	RGZ	48	4000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSPM0G3519SRHBR	ACTIVE	VQFN	RHB	32	5000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

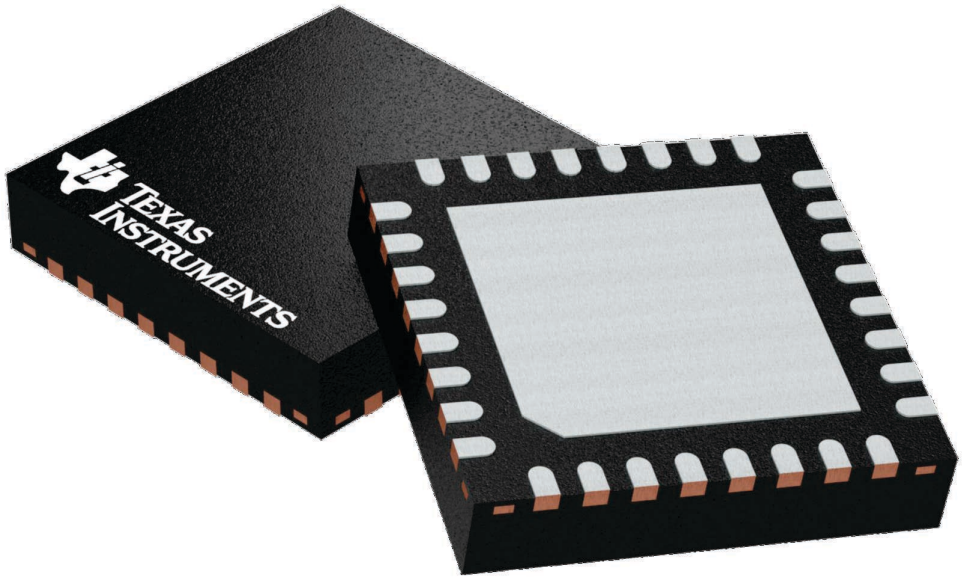
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

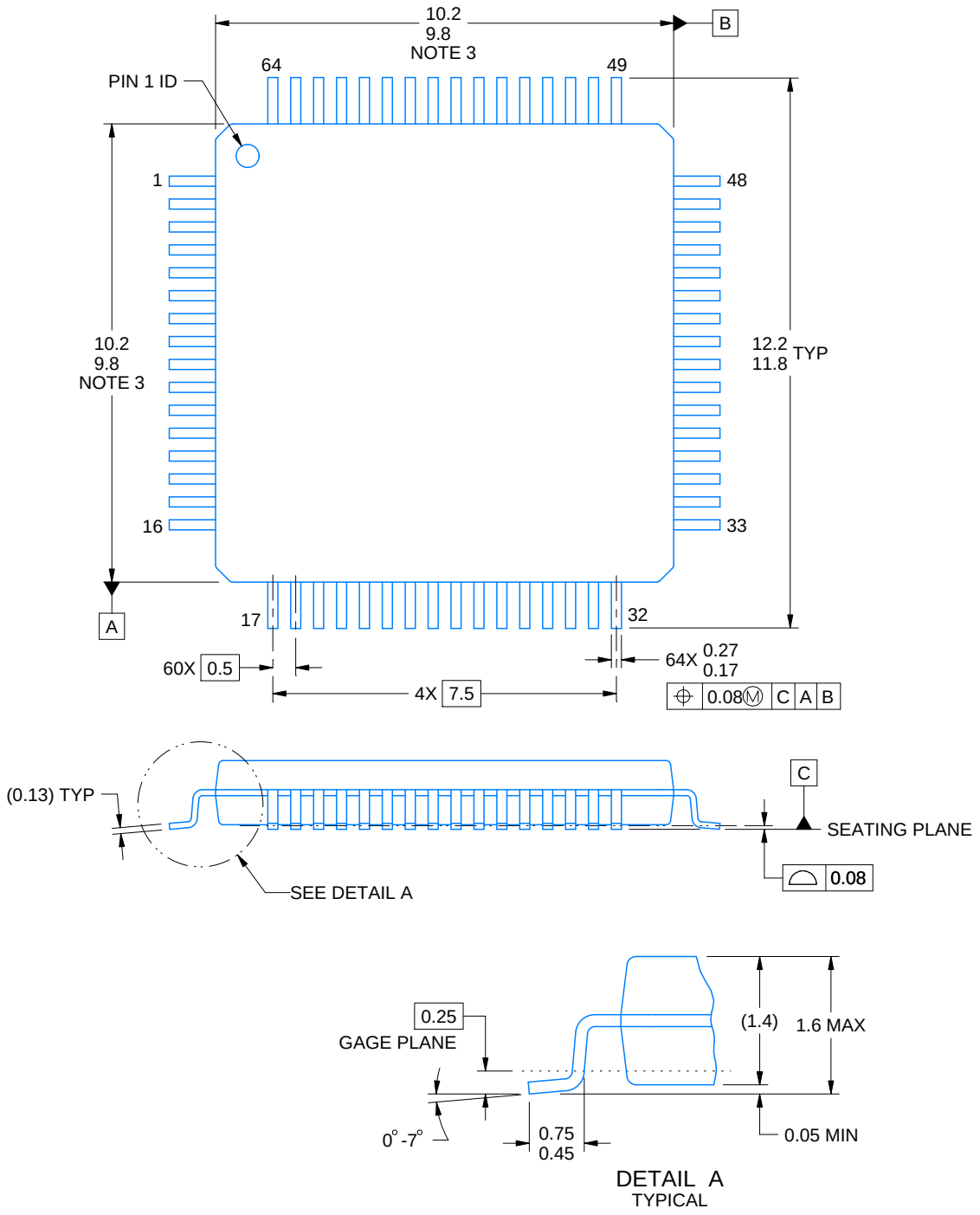
4224745/A

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

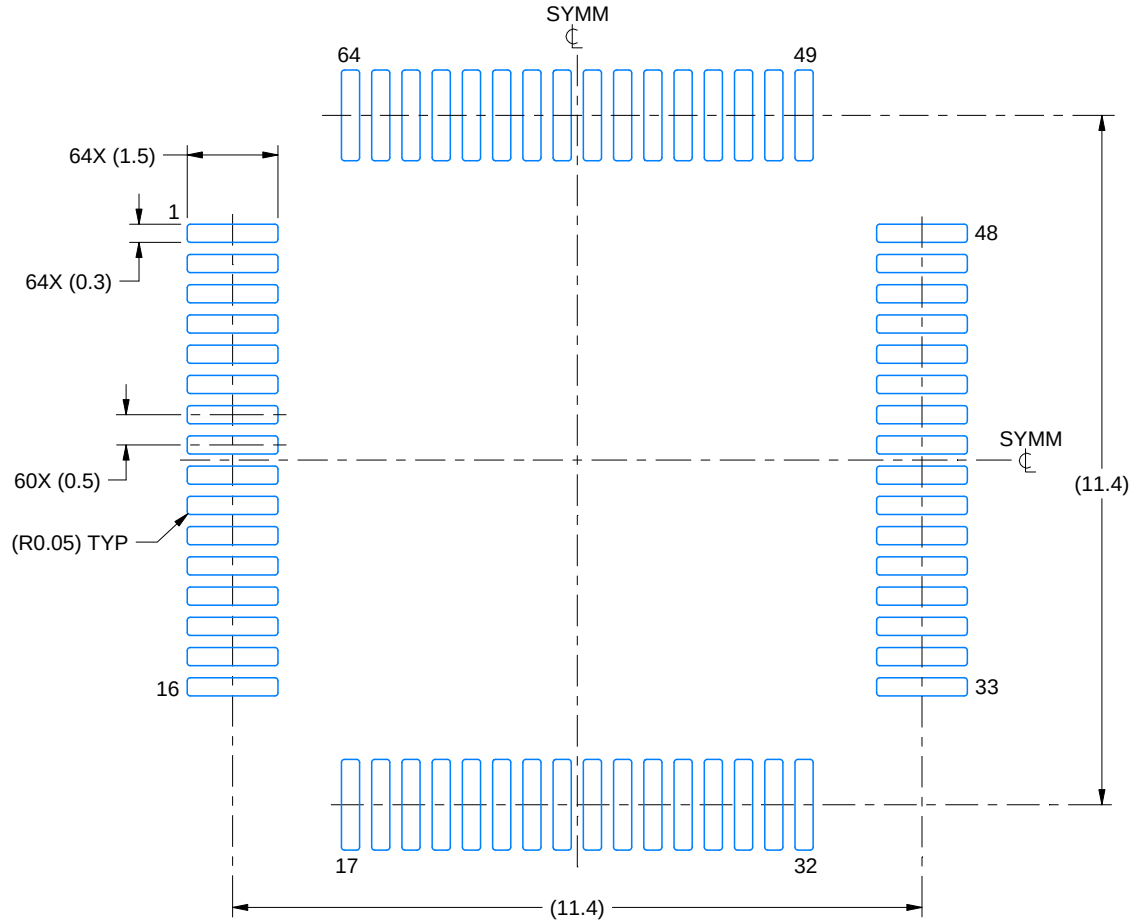
PLASTIC QUAD FLATPACK



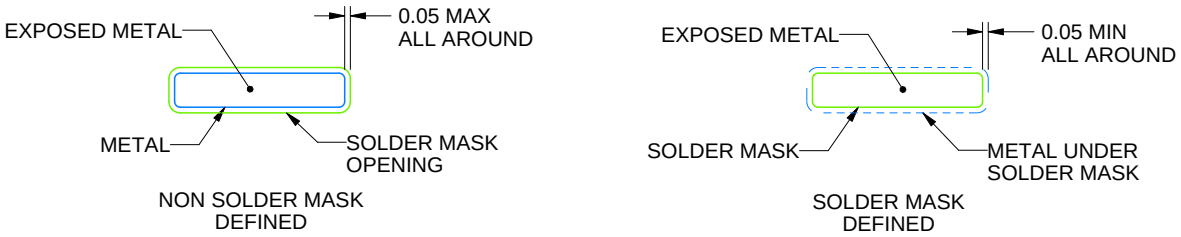
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

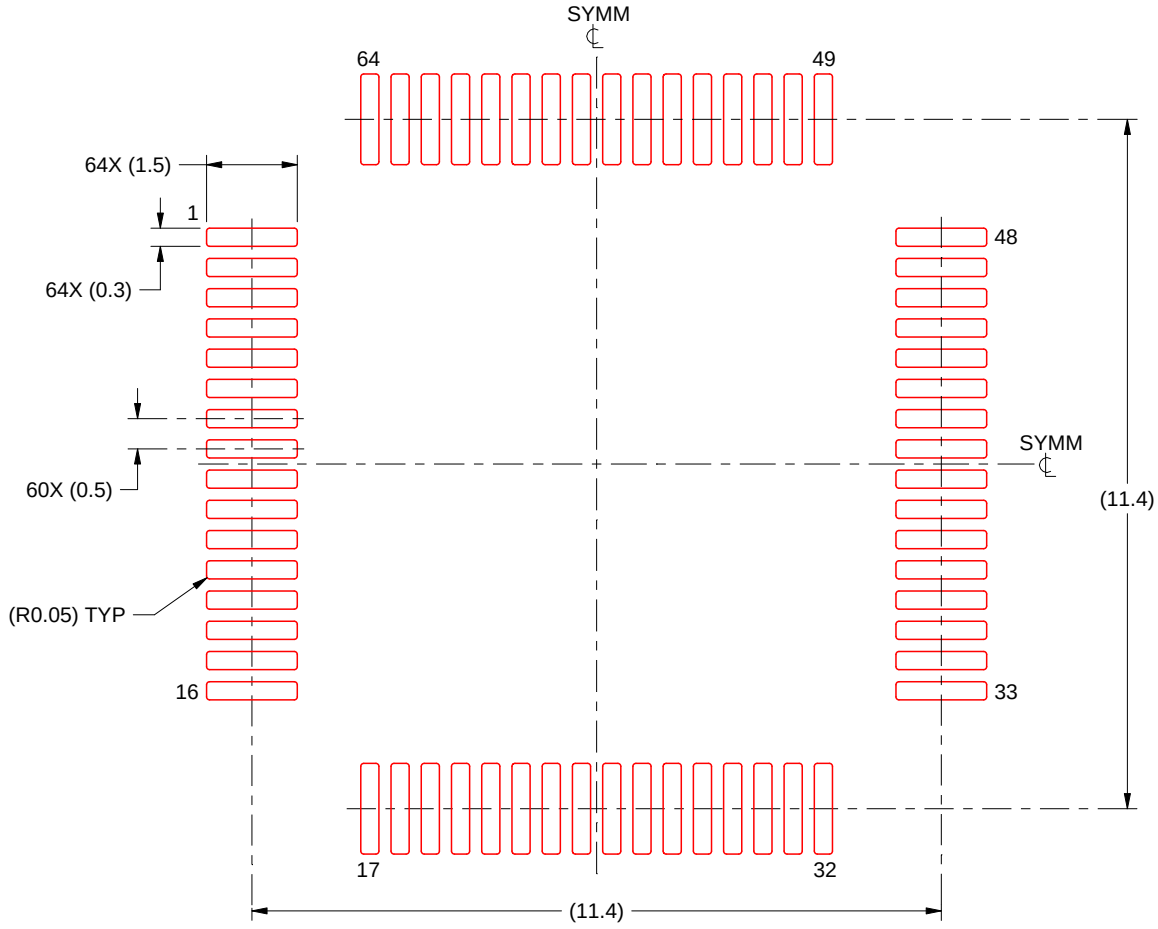


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

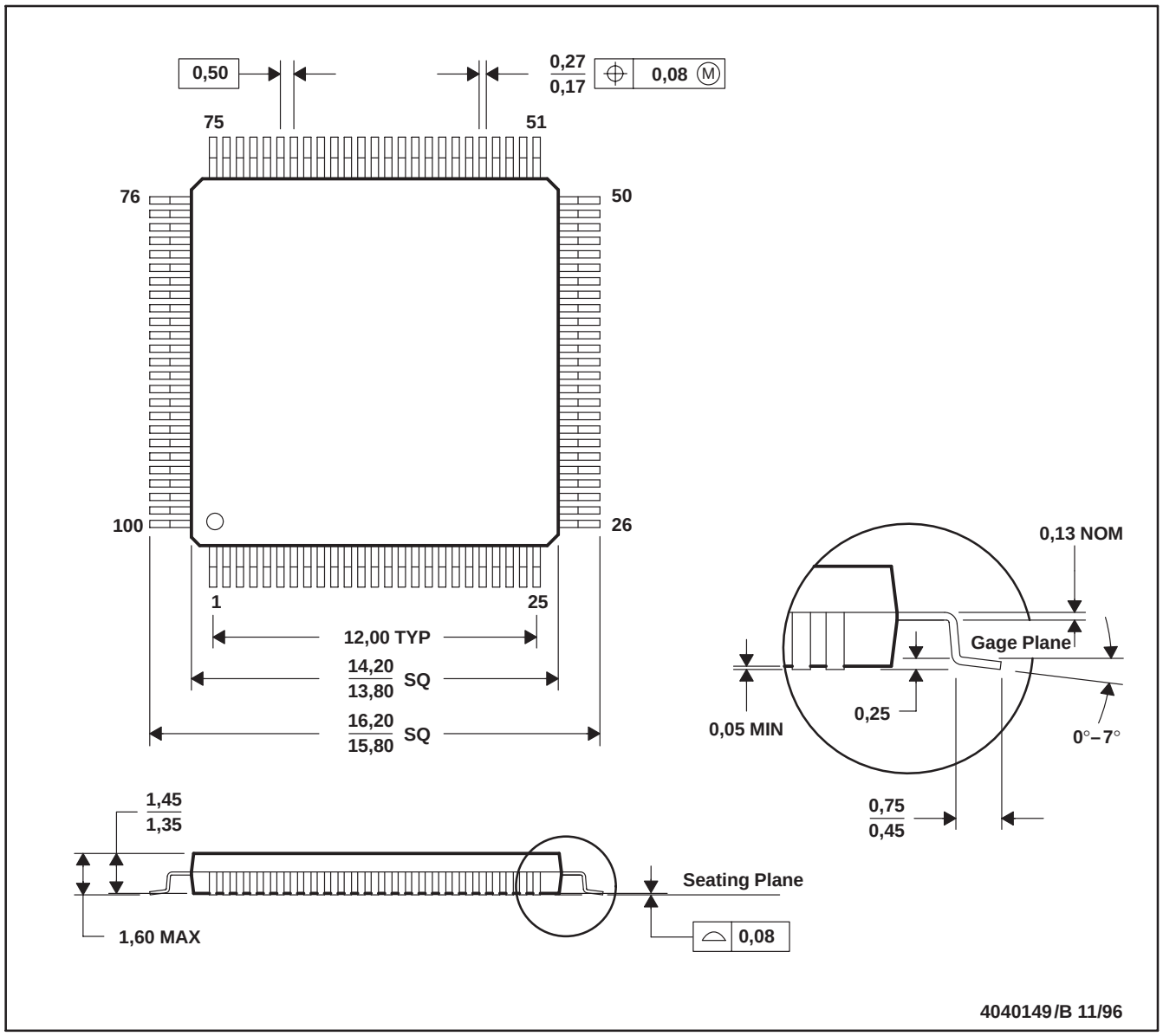
4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

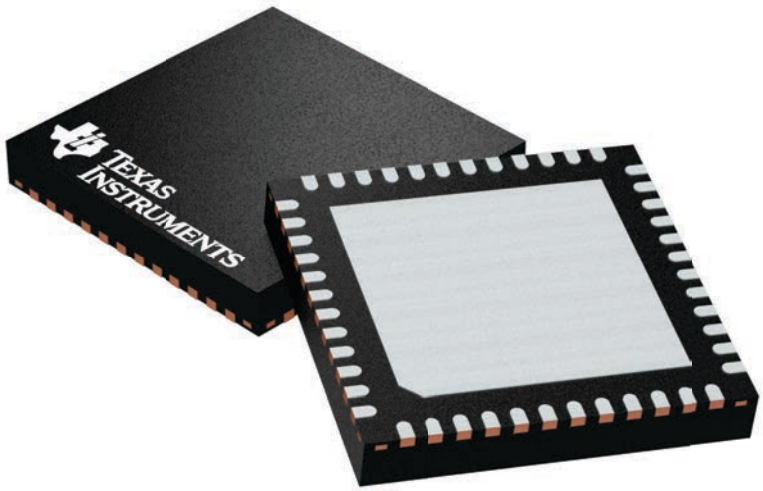
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

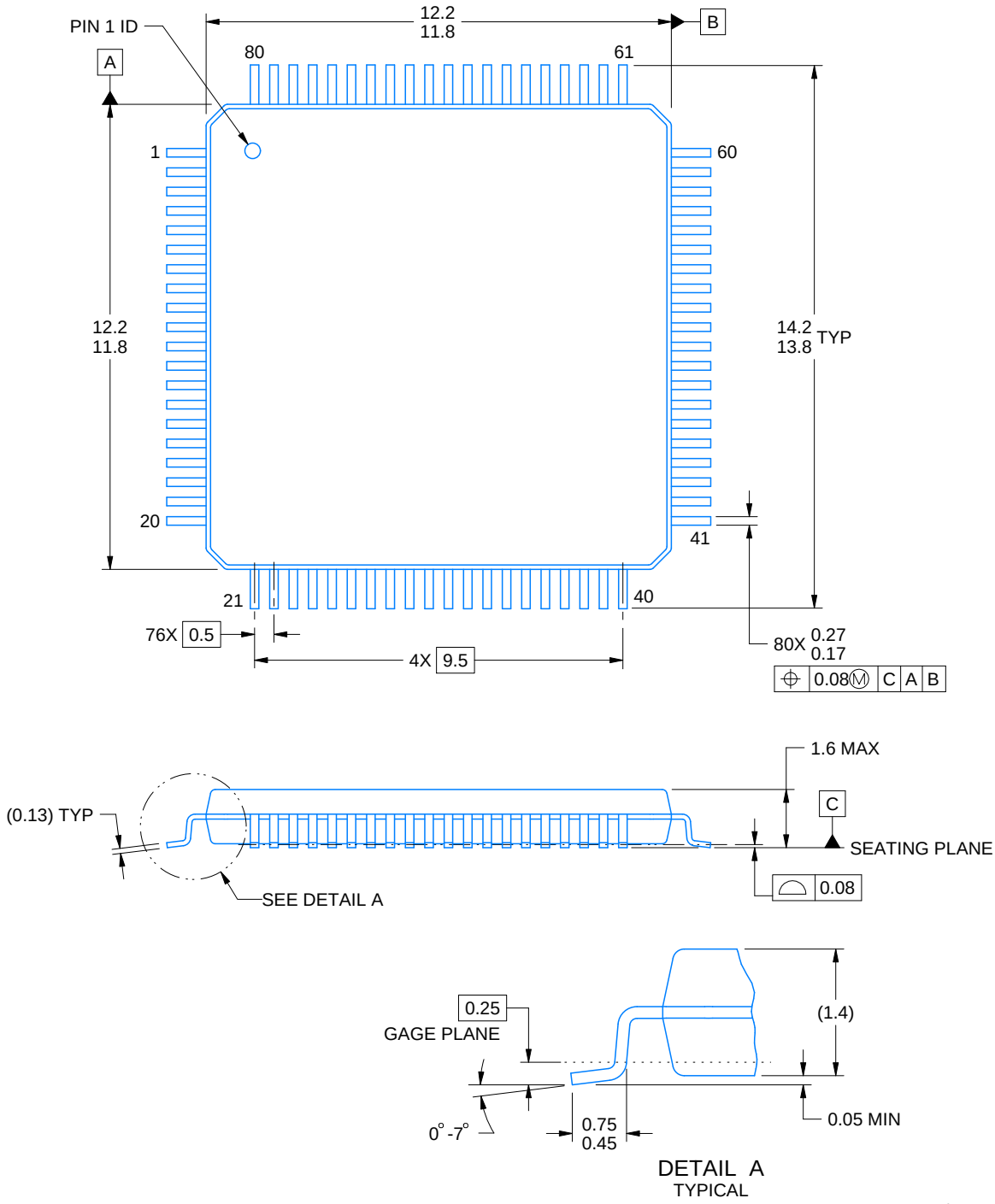
4224671/A

PACKAGE OUTLINE

PN0080A

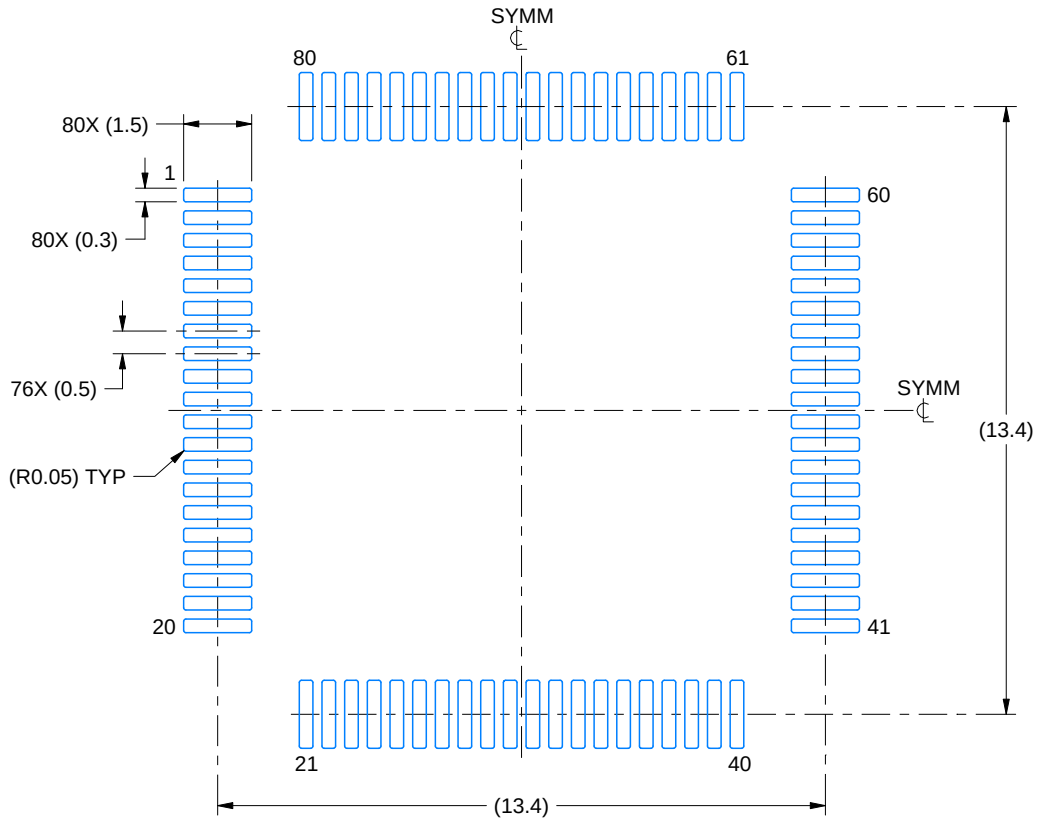
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

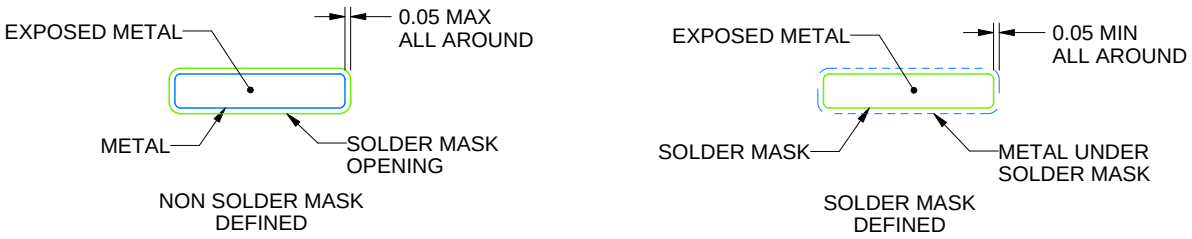


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

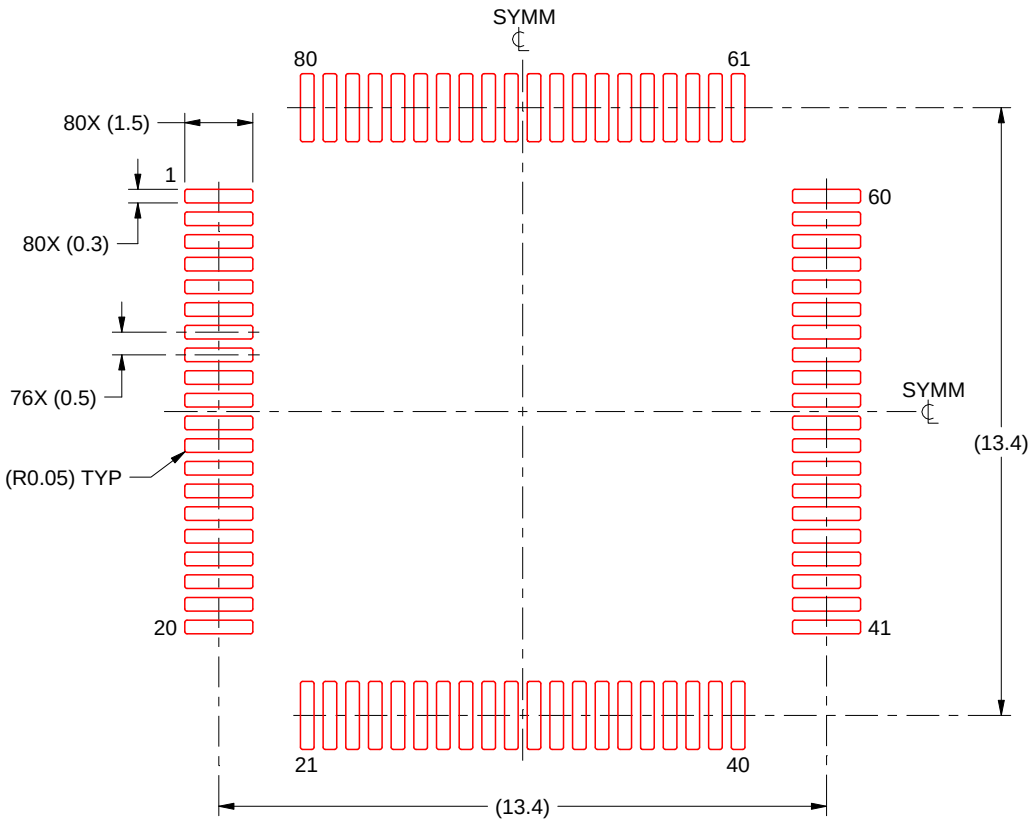


SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265