

SINGLE-SUPPLY RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

Check for Samples: [OPA340-EP](#)

FEATURES

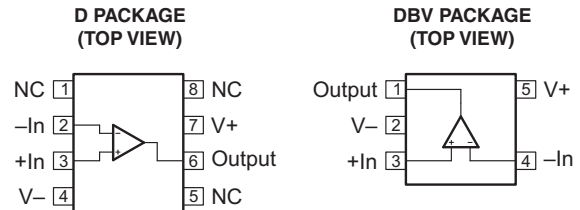
- Rail-to-Rail Input
- Rail-to-Rail Output (Within 1 mV)
- Wide Bandwidth: 5.5 MHz
- High Slew Rate: 6 V/ μ s
- Low THD+Noise: 0.0007% ($f = 1$ kHz)
- Low Quiescent Current: 750 μ A/channel
- Single, Dual, and Quad Versions

APPLICATIONS

- Driving Analog-to-Digital (A/D) Converters
- PCMCIA Cards
- Data Acquisition
- Process Control
- Audio Processing
- Communications
- Active Filters
- Test Equipment

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military ($-55^{\circ}\text{C}/125^{\circ}\text{C}$) Temperature Range⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



NC – No internal connection

(1) Additional temperature ranges are available - contact factory

DESCRIPTION

The OPA340 rail-to-rail CMOS operational amplifier is optimized for low-voltage, single-supply operation. Rail-to-rail input/output and high-speed operation make it ideal for driving sampling analog-to-digital (A/D) converters. The OPA340 is also well-suited for general purpose and audio applications as well as providing current/voltage conversion at the output of digital-to-analog (D/A) converters.

The OPA340 operates on a single supply as low as 2.7 V with an input common-mode voltage range that extends 500 mV below ground and 500 mV above the positive supply. Output voltage swing is to within 1 mV of the supply rails with a 100-k Ω load. It offers excellent dynamic response (BW = 5.5 MHz, SR = 6 V/ μ s), yet quiescent current is only 750 μ A.

The surface mount package options are SOIC-8 or SOT23-5. Both are specified from -55°C to 125°C . A SPICE macromodel is available for design analysis.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D (8 pin)	Reel of 2500	OPA340MDREP ⁽³⁾	PREVIEW
	SOT23-5 – DBV	Reel of 250	OPA340MDBVTEP	CVS

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) Product preview. Contact your TI sales representative for availability.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V _S	Supply voltage	5.5 V
V _I	Signal input voltage ⁽²⁾	(V _–) – 0.5 V to (V ₊) + 0.5 V
V _O	Signal input current ⁽²⁾	10 mA
	Output short-circuit ⁽³⁾	Continuous
T _A	Operating free-air temperature range	–55°C to 125°C
T _{stg}	Storage temperature range	–55°C to 125°C
T _J	Operating virtual-junction temperature	150°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: $V_S = 2.7\text{ V to }5\text{ V}$

Over specified temperature range ($T_A = -55^\circ\text{C to }125^\circ\text{C}$), $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$ (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Input offset voltage	V_{OS} $V_S = 5\text{ V}$		± 150	± 500	μV
				± 1600	μV
vs temperature	dV_{OS}/dT $T_A = 25^\circ\text{C}$		± 2.5		$\mu\text{V}/^\circ\text{C}$
vs power supply	PSRR $T_A = \text{Full range}$		30	150	$\mu\text{V}/\text{V}$
Channel separation, dc	$V_S = 2.7\text{ V to }5.5\text{ V}$, $V_{CM} = 0\text{ V}$		0.2		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT					
Input bias current	I_B		± 0.2	± 500	pA
Input offset current	I_{OS}		± 0.2	± 600	pA
NOISE					
Input voltage noise, $f = 0.1\text{ kHz to }50\text{ kHz}$			8		μVrms
Input voltage noise density, $f = 1\text{ kHz}$	e_n		25		$\text{nV}/\sqrt{\text{Hz}}$
Current noise density, $f = 1\text{ kHz}$	i_n		3		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE					
Common-mode voltage range	V_{CM}	-0.3		$(V+) + 0.3$	V
Common-mode rejection ratio	CMRR	$-0.3\text{ V} < V_{CM} < (V+) - 1.8\text{ V}$	78	92	dB
		$T_A = 25^\circ\text{C}$	75		dB
		$T_A = \text{Full range}$	70	84	dB
		$V_S = 5\text{ V}$, $-0.3\text{ V} < V_{CM} < 5.3\text{ V}$	64		dB
		$T_A = 25^\circ\text{C}$	66	80	dB
		$T_A = \text{Full range}$			
		$V_S = 2.7\text{ V}$, $-0.3\text{ V} < V_{CM} < 3\text{ V}$			
		$T_A = 25^\circ\text{C}$			
INPUT IMPEDANCE					
Differential			$10^{13} \parallel 3$		$\Omega \parallel \text{pF}$
Common-mode			$10^{13} \parallel 6$		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN					
Open-loop voltage gain	A_{OL}	$R_L = 100\text{ k}\Omega$, $10\text{ mV} < V_O < (V+) - 10\text{ mV}$	103	124	dB
		$R_L = 10\text{ k}\Omega$, $70\text{ mV} < V_O < (V+) - 70\text{ mV}$	98	120	dB
		$R_L = 2\text{ k}\Omega$, $250\text{ mV} < V_O < (V+) - 250\text{ mV}$	92	114	dB
FREQUENCY RESPONSE					
Gain-bandwidth product	GBW	$G = 1$		5.5	MHz
Slew rate	SR	$V_S = 5\text{ V}$, $G = 1$, $C_L = 100\text{ pF}$		6	$\text{V}/\mu\text{s}$
Settling time, 0.1%		$V_S = 5\text{ V}$, 2-V Step, $C_L = 100\text{ pF}$		1	μs
Settling time, 0.01%		$V_S = 5\text{ V}$, 2-V Step, $C_L = 100\text{ pF}$		1.6	μs
Overload recovery time		$V_{IN} \cdot G = V_S$		0.2	μs
Total harmonic distortion + noise	THD+N	$V_S = 5\text{ V}$, $V_O = 3\text{ V}_{PP}$ ⁽¹⁾ , $G = 1$, $f = 1\text{ kHz}$		0.0007	%

(1) $V_{OUT} = 0.25\text{ V to }3.25\text{ V}$

ELECTRICAL CHARACTERISTICS: $V_S = 2.7\text{ V to }5\text{ V}$ (continued)

Over specified temperature range ($T_A = -55^\circ\text{C to }125^\circ\text{C}$), $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$ (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT					
Voltage output swing from rail ⁽²⁾	$R_L = 100\text{ k}\Omega$, $A_{OL} \geq 104\text{ dB}$		1	10	mV
	$R_L = 10\text{ k}\Omega$, $A_{OL} \geq 98\text{ dB}$		10	70	mV
	$R_L = 2\text{ k}\Omega$, $A_{OL} \geq 92\text{ dB}$		40	250	mV
Short-circuit current	I_{SC}		± 50		mA
Capacitive load drive	C_{LOAD}	See Typical Characteristics			
POWER SUPPLY					
Specified voltage range	V_S	2.7		5	V
Operating voltage range			2.5 to 5.5		V
Quiescent current (per amplifier)	I_Q	$I_O = 0$, $V_S = 5\text{ V}$			
			750	950	μA
				1300	μA
TEMPERATURE RANGE					
Specified range		-55		125	$^\circ\text{C}$
Storage range		-55		125	$^\circ\text{C}$
Thermal resistance	θ_{JA}				
DBV (5 pin) package			200		$^\circ\text{C/W}$
D (8 pin) package			150		$^\circ\text{C/W}$

(2) Output voltage swings are measured between the output and power supply rails.

TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

OPEN-LOOP GAIN/PHASE vs FREQUENCY

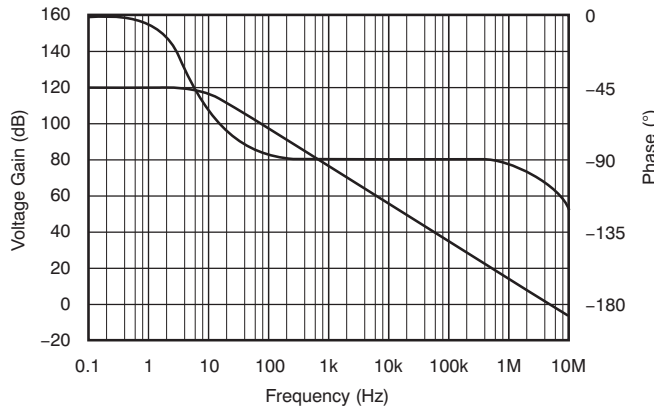


Figure 1.

POWER-SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY

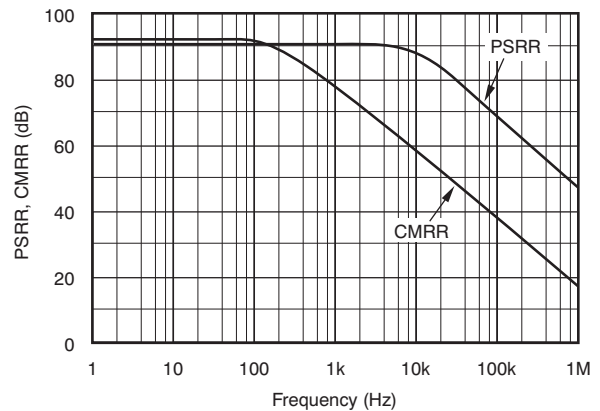


Figure 2.

INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY

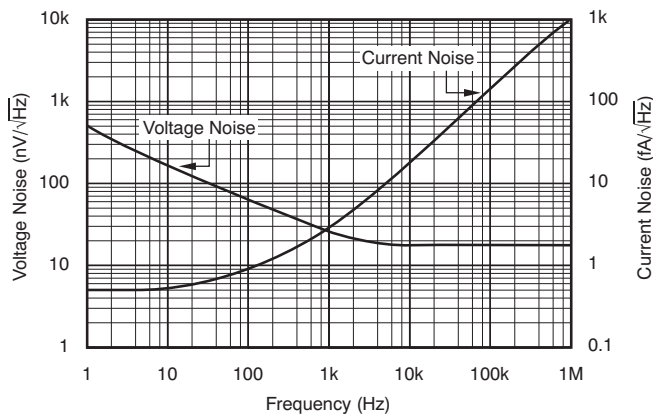


Figure 3.

CHANNEL SEPARATION vs FREQUENCY

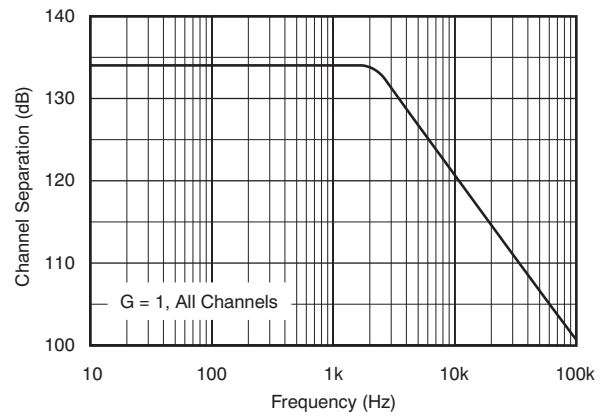


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

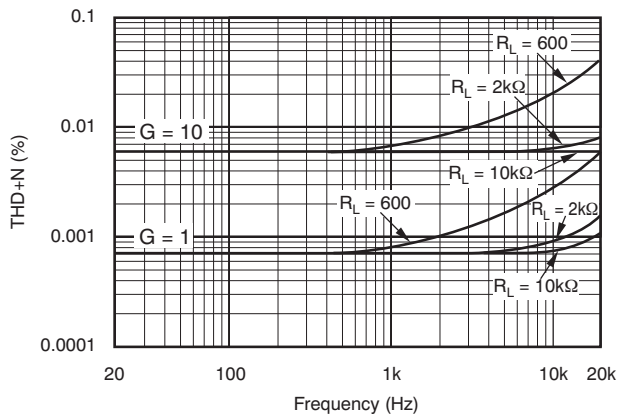


Figure 5.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

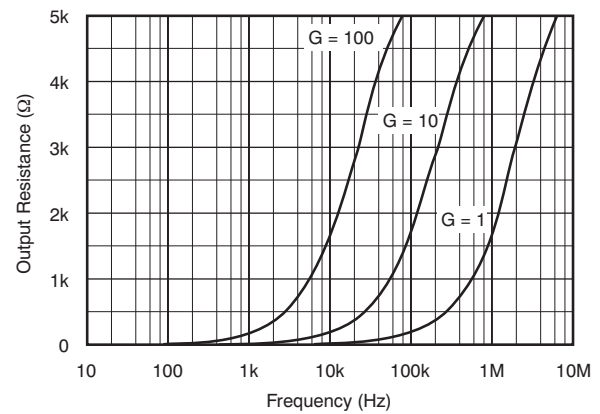


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

OPEN-LOOP GAIN AND POWER-SUPPLY REJECTION vs TEMPERATURE

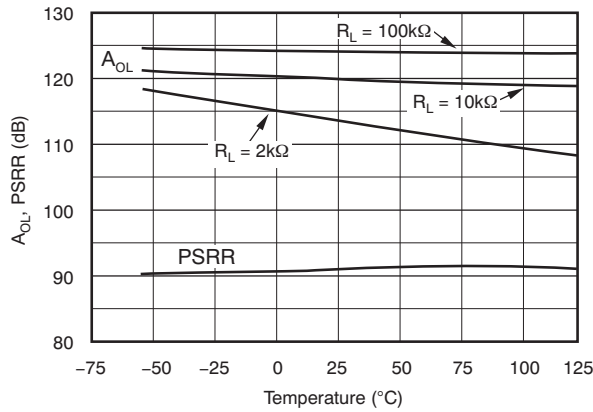


Figure 7.

COMMON-MODE REJECTION vs TEMPERATURE

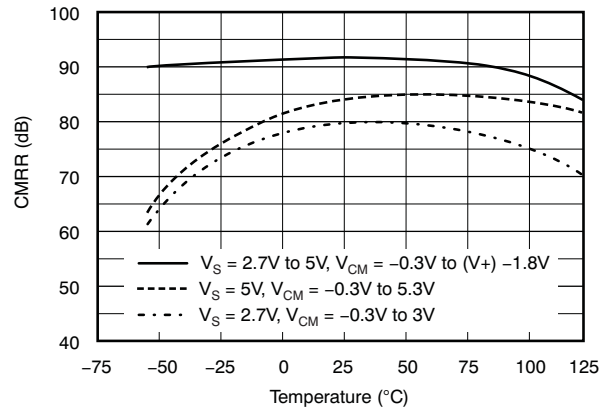


Figure 8.

QUIESCENT CURRENT vs TEMPERATURE

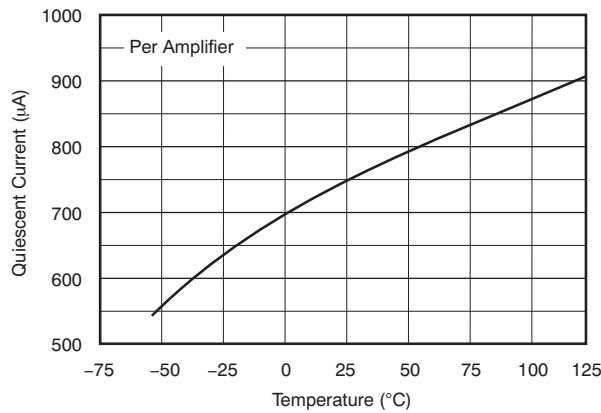


Figure 9.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

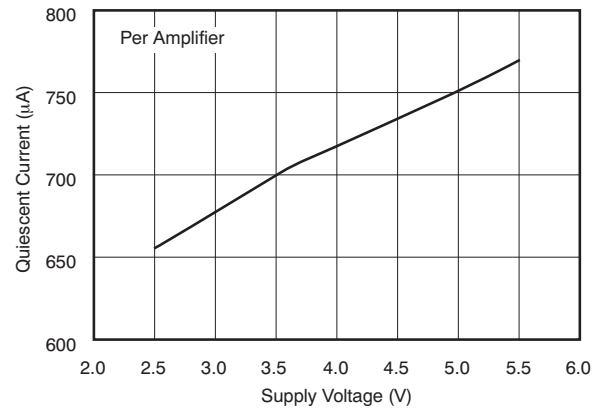


Figure 10.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

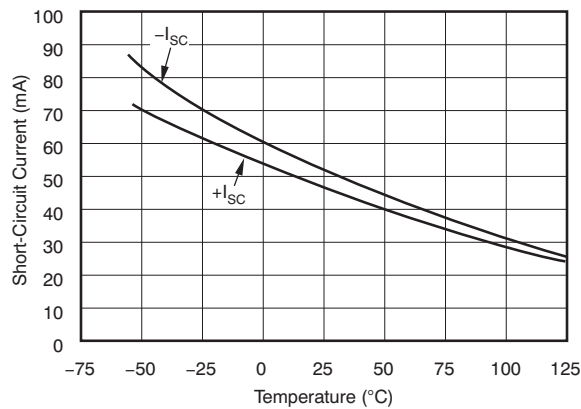


Figure 11.

SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE

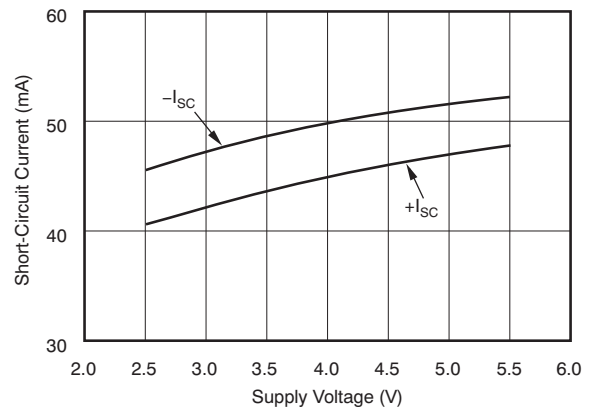


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

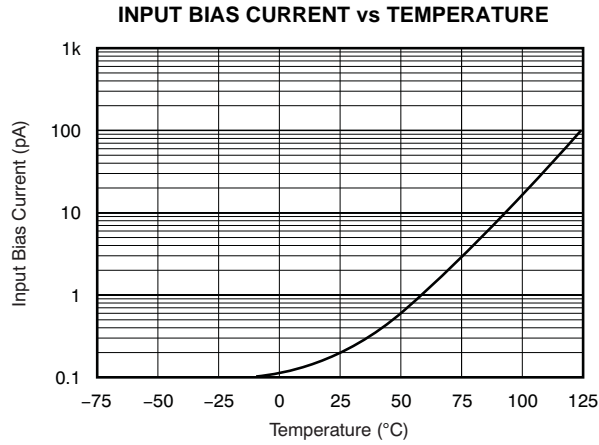


Figure 13.

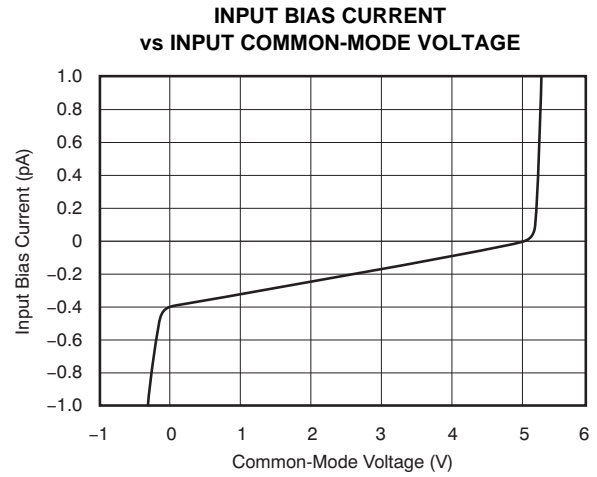


Figure 14.

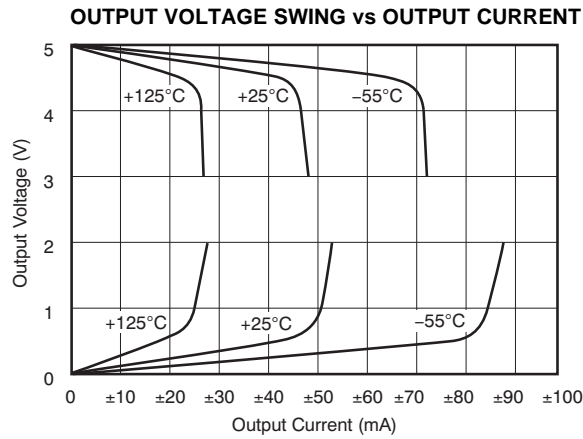


Figure 15.

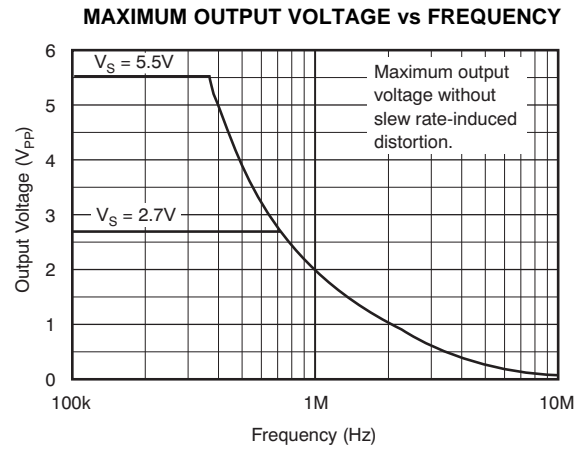


Figure 16.

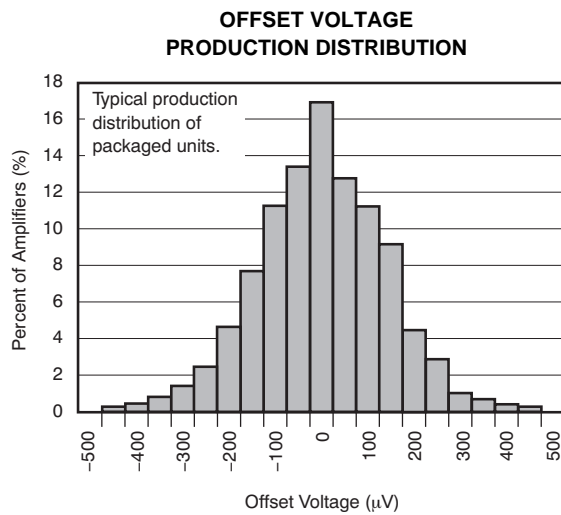


Figure 17.

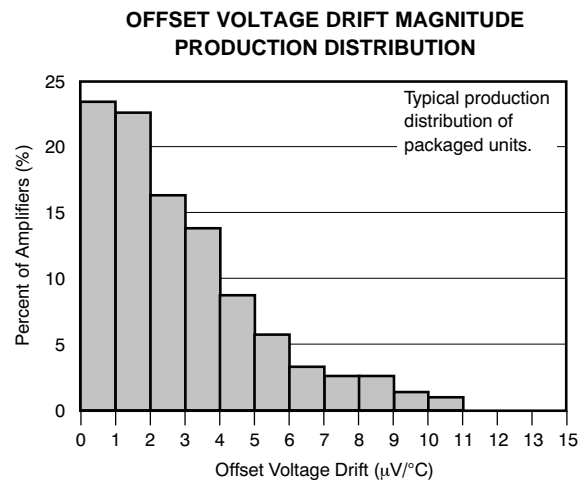


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

SMALL-SIGNAL STEP RESPONSE
 $C_L = 100\text{pF}$

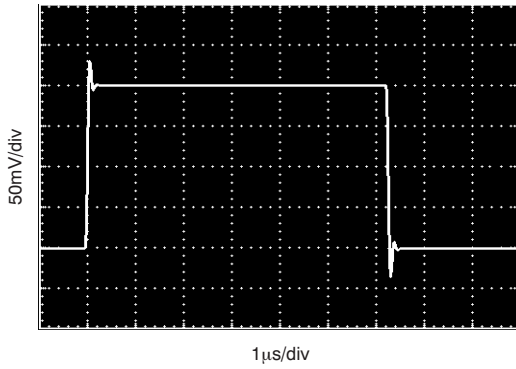


Figure 19.

LARGE-SIGNAL STEP RESPONSE
 $C_L = 100\text{pF}$

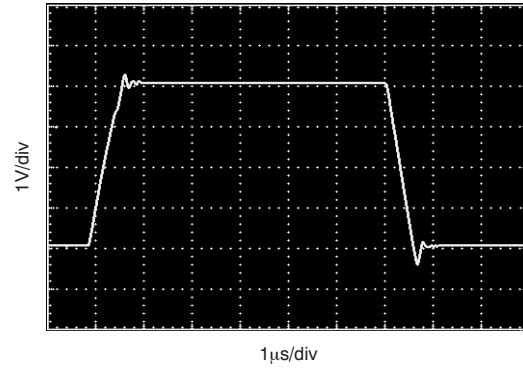


Figure 20.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

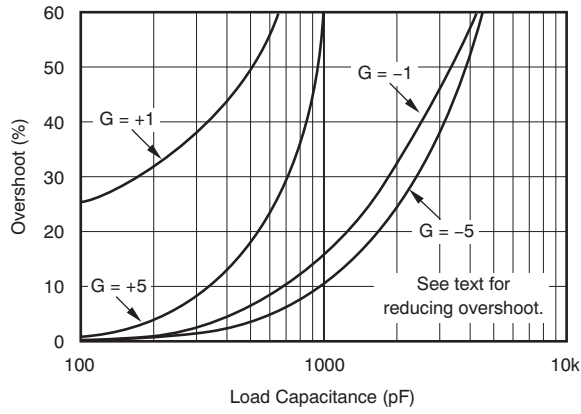


Figure 21.

SETTLING TIME vs CLOSED-LOOP GAIN

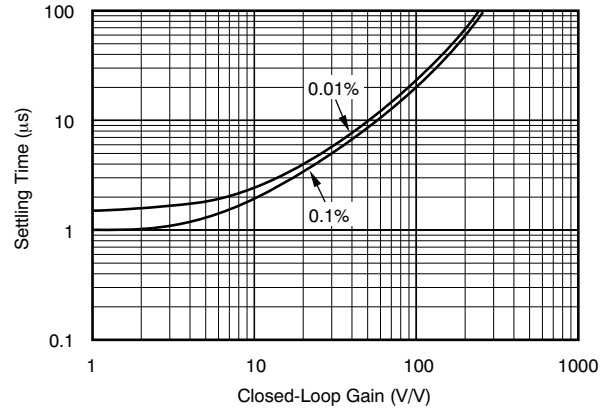


Figure 22.

APPLICATION INFORMATION

The OPA340 is fabricated on a state-of-the-art 0.6-micron CMOS process. It is unity-gain stable and suitable for a wide range of general-purpose applications. Rail-to-rail input/output makes it ideal for driving sampling A/D converters. In addition, excellent ac performance makes it well-suited for audio applications. The class AB output stage is capable of driving 600- Ω loads connected to any point between V_+ and ground.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. [Figure 23](#) shows the input and output waveforms for the OPA340 in unity-gain configuration. Operation is from a single 5-V supply with a 10-k Ω load connected to $V_S/2$. The input is a 5- V_{PP} sinusoid. Output voltage is approximately 4.98 V_{PP} .

Power-supply pins should be bypassed with 0.01- μ F ceramic capacitors.

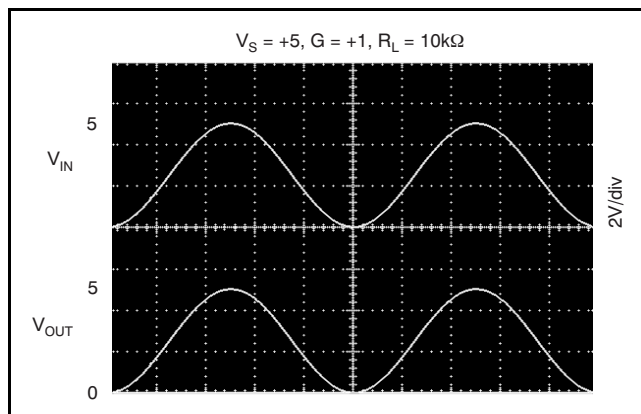


Figure 23. Rail-to-Rail Input and Output

Operating Voltage

The OPA340 is fully specified from 2.7 V to 5 V. Parameters are ensured over the specified supply range—a unique feature of the OPA340 series. In addition, many specifications apply from -55°C to

125°C . Most behavior remains nearly unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltages or temperature are shown in [Typical Characteristics](#).

Rail-to-Rail Input

The input common-mode voltage range of the OPA340 extends 500 mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair (as shown in [Figure 24](#)). The N-channel pair is active for input voltages close to the positive rail, typically $(V_+) - 1.3\text{ V}$ to 500 mV above the positive supply, while the P-channel pair is on for inputs from 500 mV below the negative supply to approximately $(V_+) - 1.3\text{ V}$. There is a small transition region, typically $(V_+) - 1.5\text{ V}$ to $(V_+) - 1.1\text{ V}$, in which both pairs are on. This 400-mV transition region can vary $\pm 300\text{ mV}$ with process variation. Thus, the transition region (both stages on) can range from $(V_+) - 1.8\text{ V}$ to $(V_+) - 1.4\text{ V}$ on the low end, up to $(V_+) - 1.2\text{ V}$ to $(V_+) - 0.8\text{ V}$ on the high end.

The OPA340 is laser-trimmed to reduce the offset voltage difference between the N-channel and P-channel input stages, resulting in improved common-mode rejection and a smooth transition between the N-channel pair and the P-channel pair. However, within the 400-mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage. Normally, input bias current is approximately 200 fA; however, input voltages exceeding the power supplies by more than 500 mV can cause excessive current to flow in or out of the input pins. Momentary voltages greater than 500 mV beyond the power supply can be tolerated if the current on the input pins is limited to 10 mA. This is easily accomplished with an input resistor, as shown in [Figure 25](#). Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required.

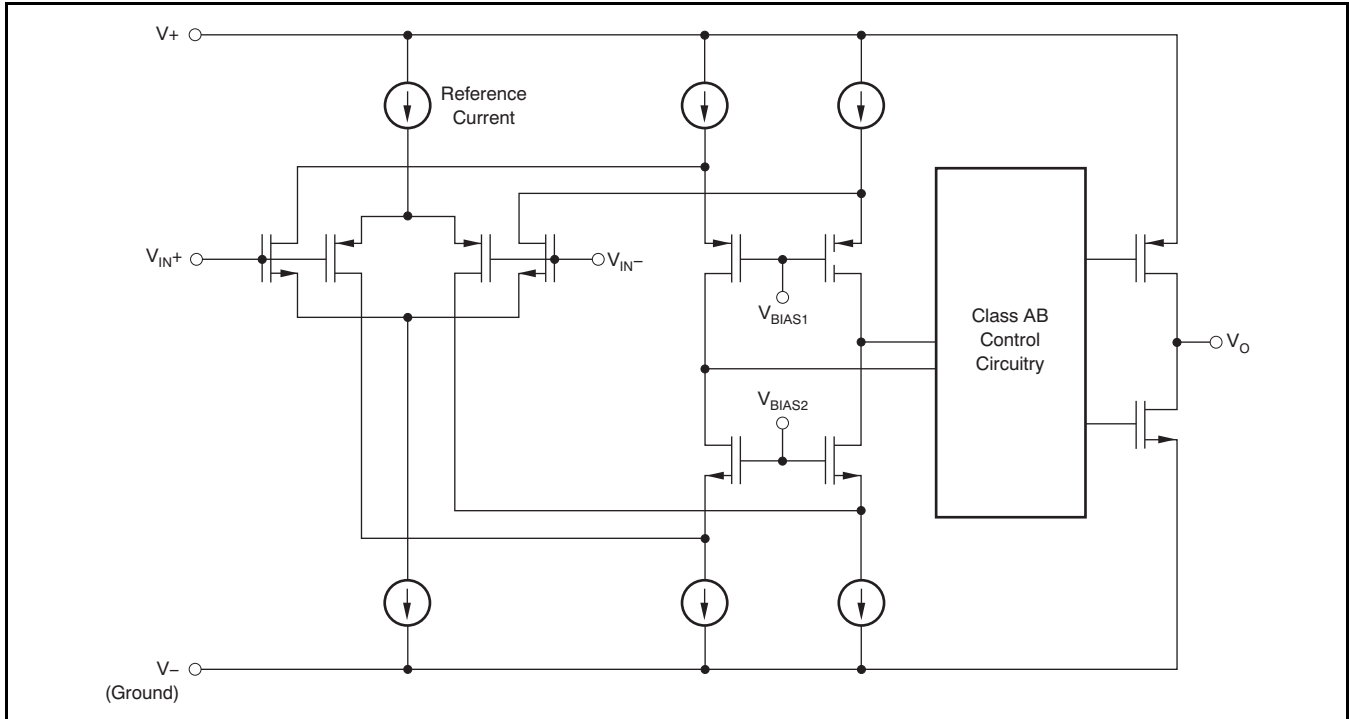


Figure 24. Simplified Schematic

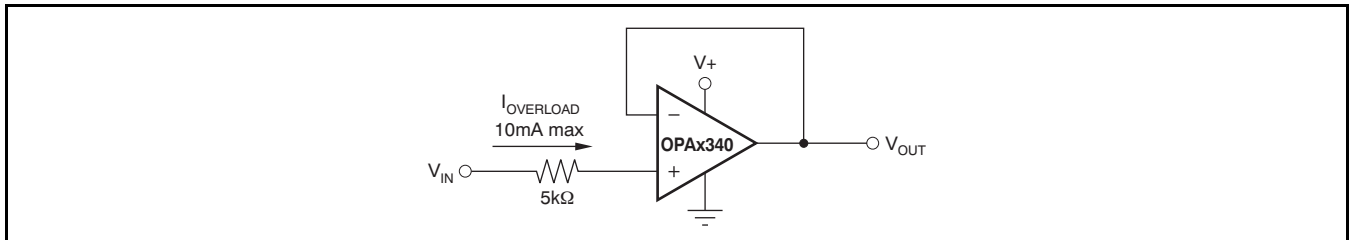


Figure 25. Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (> 50 kΩ), the output voltage is typically a few millivolts from the supply rails. With

moderate resistive loads (2 kΩ to 50 kΩ), the output can swing to within a few tens of millivolts from the supply rails and maintain high open-loop gain. See the typical characteristic curve [Output Voltage Swing vs Output Current](#).

CAPACITIVE LOAD AND STABILITY

The OPA340 can drive a wide range of capacitive loads. However, all operational amplifiers under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An operational amplifier in unity gain configuration is most susceptible to the effects of capacitive load. The capacitive load reacts with the operational amplifier's output resistance, along with any additional load resistance, to create a pole in the small-signal response which degrades the phase margin. In unity gain, OPA340 series operational amplifiers perform well, with a pure capacitive load up to approximately 1000 pF. Increasing gain enhances the amplifier's ability to drive more capacitance. See the typical performance curve [Small-Signal Overshoot vs Capacitive Load](#).

One method of improving capacitive load drive in the unity gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in [Figure 26](#). This significantly reduces ringing with large capacitive loads. However, if there is a resistive load in parallel with the capacitive load, it creates a voltage divider introducing a dc error at the output and slightly reduces output swing. This error may be insignificant. For example, with $R_L = 10\text{ k}\Omega$ and $R_S = 20\ \Omega$, there is only approximately 0.2% error at the output.

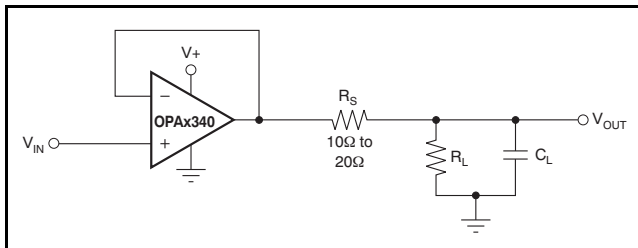


Figure 26. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

DRIVING A/D CONVERTERS

The OPA340 is optimized for driving medium speed (up to 100 kHz) sampling A/D converters. However, it also offers excellent performance for higher speed converters. The OPA340 provides an effective means of buffering the A/D converter's input capacitance and resulting charge injection while providing signal gain. [Figure 27](#) and [Figure 28](#) show the OPA340 driving an [ADS7816](#). The [ADS7816](#) is a 12-bit, micro-power sampling converter in the tiny MSOP-8 package. When used with the miniature package options of the OPA340 series, the combination is ideal for space-limited and low-power applications. For further information consult the [ADS7816 data sheet](#). With the OPA340 in a noninverting configuration, an RC network at the amplifier's output can be used to filter high-frequency noise in the signal (see [Figure 27](#)). In the inverting configuration, filtering may be accomplished with a capacitor across the feedback resistor (see [Figure 28](#)).

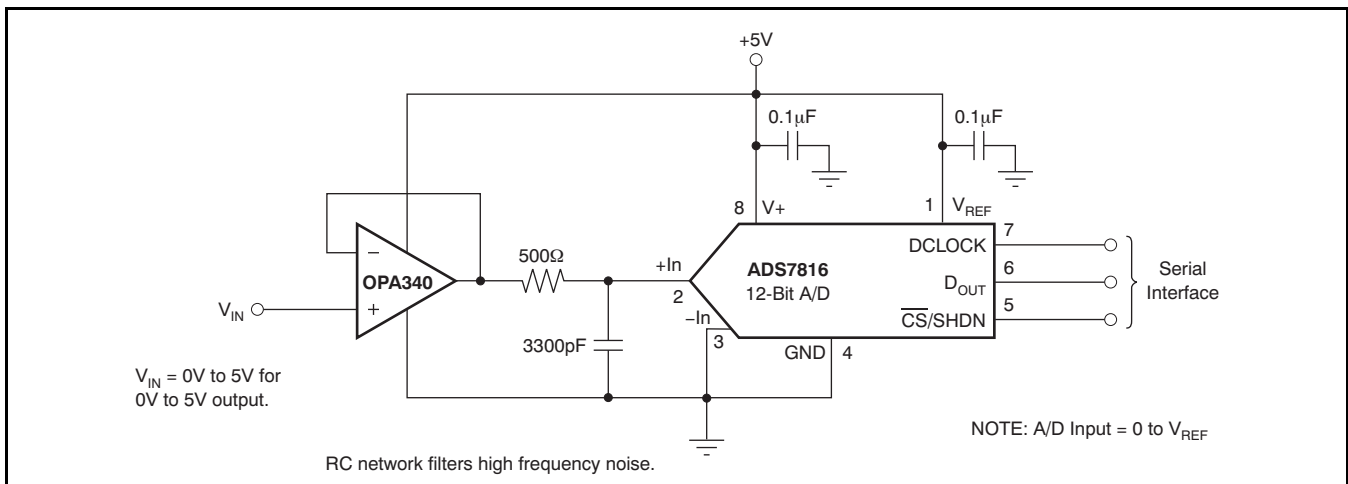


Figure 27. OPA340 in Noninverting Configuration Driving ADS7816

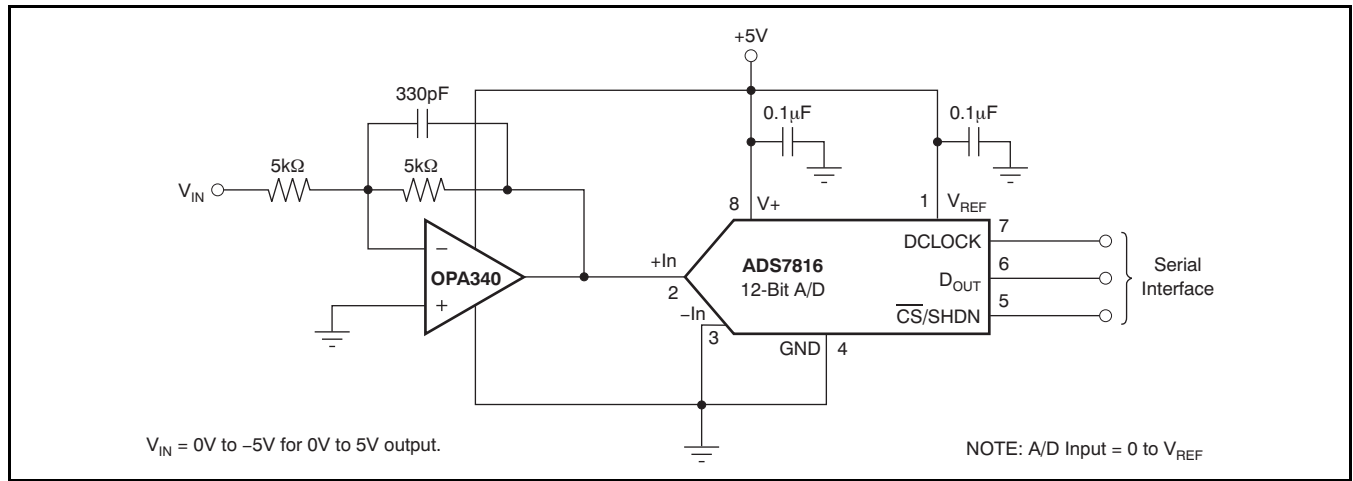


Figure 28. OPA340 in Inverting Configuration Driving ADS7816

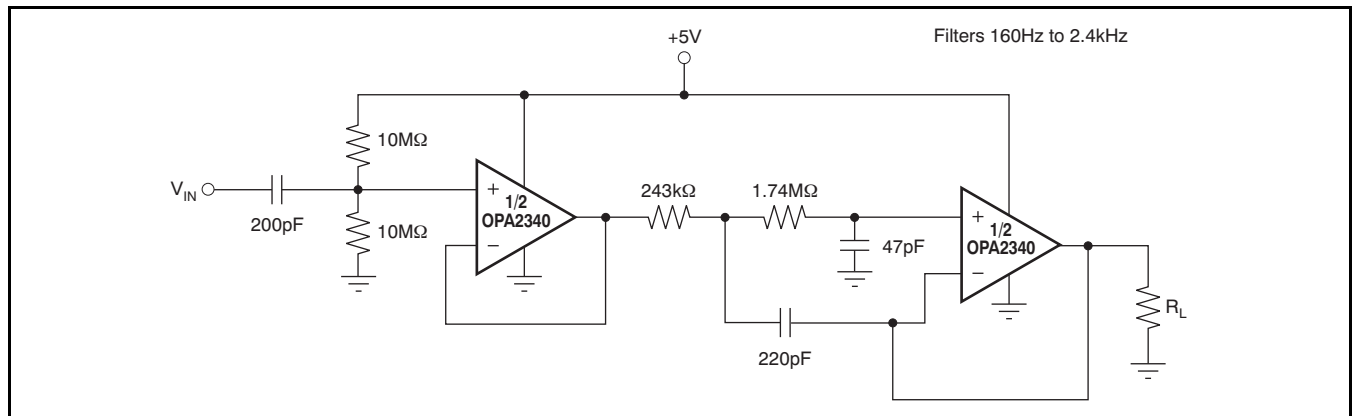


Figure 29. Speech Bandpass Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA340MDBVTEP	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	CVS	Samples
V62/08618-01XE	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	CVS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA340-EP :

- Catalog: [OPA340](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA340MDBVTEP	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA340MDBVTEP	SOT-23	DBV	5	250	213.0	191.0	35.0

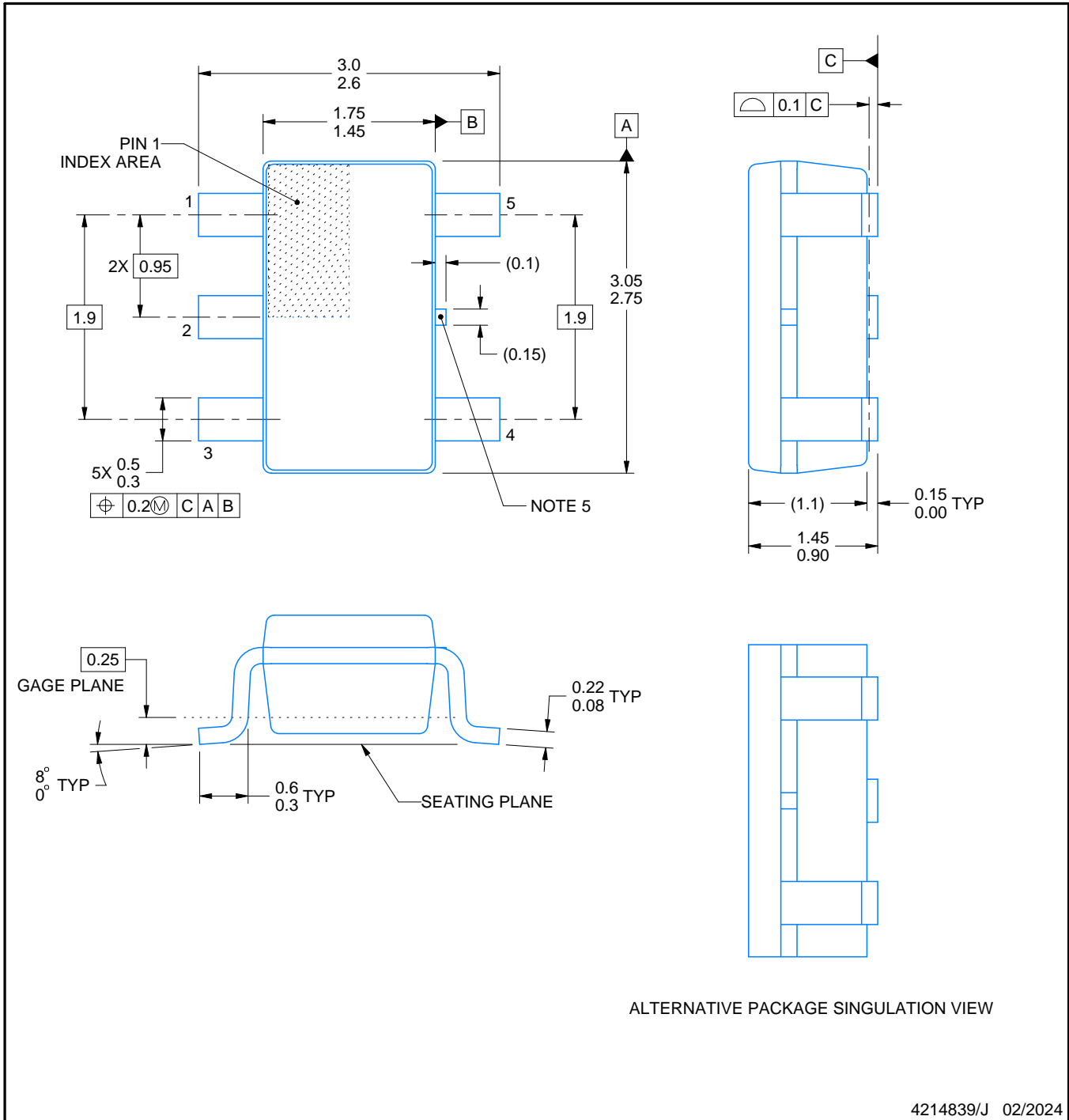
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/J 02/2024

NOTES:

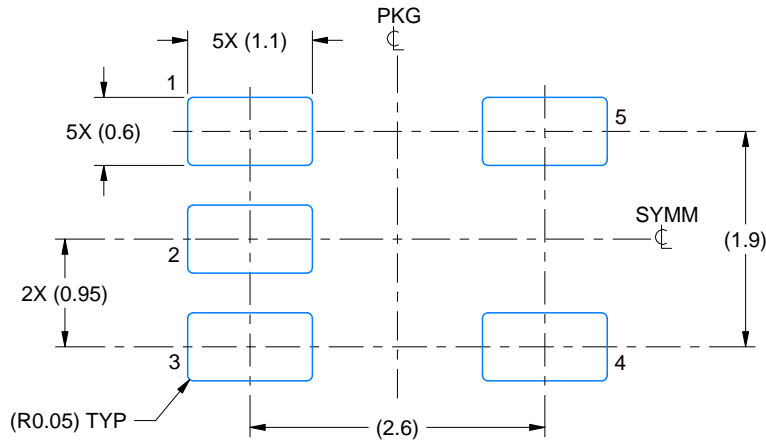
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

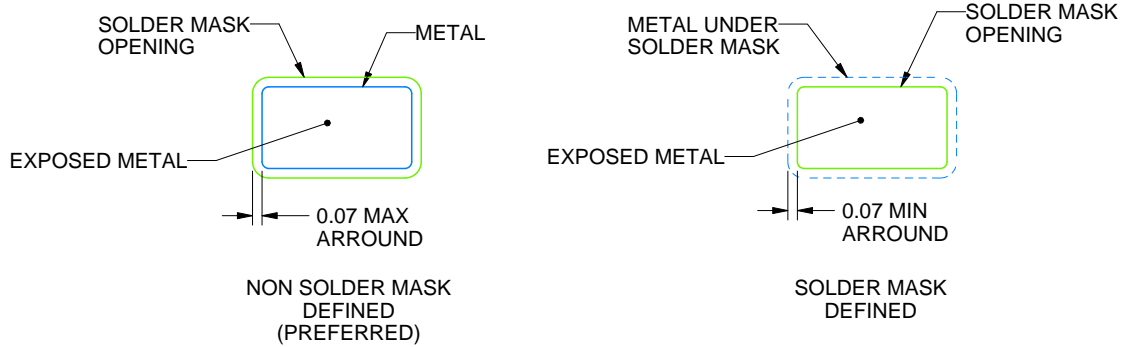
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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