Quad, Low-Power, Current-Feedback Operational Amplifier

FEATURES

- MINIMAL BANDWIDTH CHANGE VERSUS GAIN
- 170MHz BANDWIDTH AT G = +2
- > 120MHz BANDWIDTH TO GAIN > +10
- LOW DISTORTION: < –78dBc at 5MHz
- HIGH OUTPUT CURRENT: 120mA
- SINGLE +5V TO +12V SUPPLY OPERATION
- DUAL ±2.5 TO ±6.0V SUPPLY OPERATION
- LOW SUPPLY CURRENT: 1.7mA/ch

APPLICATIONS

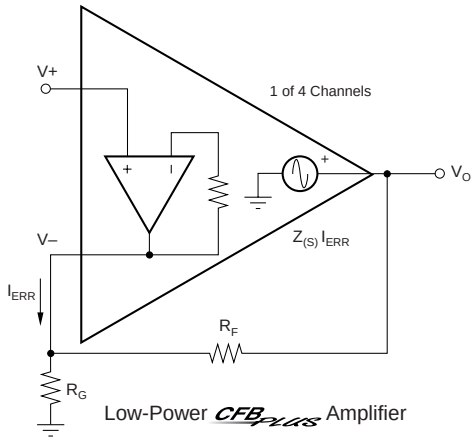
- LOW-POWER BROADCAST VIDEO DRIVERS
- EQUALIZING FILTERS
- SAW FILTER HIGH-GAIN POST AMPLIFIERS
- MULTICHANNEL SUMMING AMPLIFIERS
- WIDEBAND DIFFERENTIAL CHANNELS
- ANALOG-TO-DIGITAL CONVERTERS INPUT DRIVERS
- MULTIPLE POLE ACTIVE FILTERS
- OPA4658 LOW-POWER UPGRADE

DESCRIPTION

The OPA4684 provides a new level of performance in low-power, wideband, current-feedback (CFB) amplifiers. This CFB_{PLUS} amplifier is among the first to use an internally closed-loop input buffer stage that enhances performance significantly over earlier low-power CFB amplifiers. This new architecture provides many of the benefits of a more ideal CFB amplifier while retaining the benefits of very low power operation. The closed-loop input stage buffer gives a very low and linearized impedance path at the inverting input to sense the feedback error current. This improved inverting input impedance retains exceptional bandwidth to much higher gains and improves harmonic distortion over earlier solutions limited by inverting input linearity. Beyond simple high-gain applications, the OPA4684 CFB_{PLUS} amplifier permits the gain setting element to be set with considerable freedom from amplifier bandwidth interaction. This allows frequency response peaking elements to be added, multiple input inverting summing circuits to have greater bandwidth, and low-power line drivers to meet the demanding requirements of studio cameras and broadcast video.

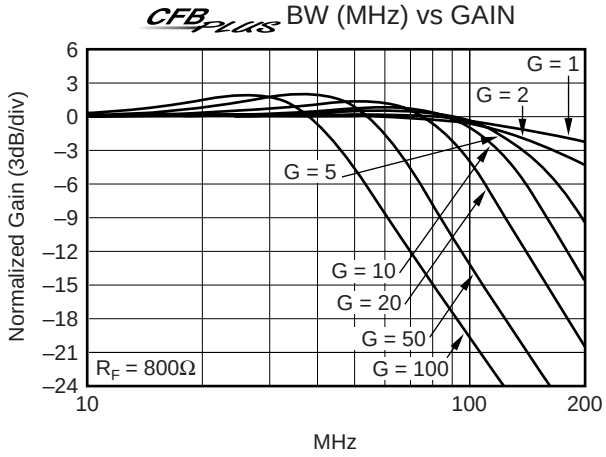
The output capability of the OPA4684 also sets a new mark in performance for low-power current-feedback amplifiers. Delivering a full $\pm 4V_{PP}$ swing on ±5V supplies, the OPA4684 also has the output current to support > ±3V swing into 50Ω. This minimal output headroom requirement is complemented by a similar 1.2V input stage headroom giving exceptional capability for single +5V operation.

The OPA4684's low 6.8mA supply current is precisely trimmed at 25°C. This trim, along with low shift over temperature and supply voltage, gives a very robust design over a wide range of operating conditions.



Low-Power CFB_{PLUS} Amplifier

(patented design)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS[1]

Power Supply	$\pm 6.5V_{DC}$
Internal Power Dissipation	See Thermal Information
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: ID, IDBV	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating: HBM	2000V
CDM	1500V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

OPA4684 RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	FEATURES
OPA683	OPA2683	—	Very Low-Power CFB_{PLUS}
OPA684	OPA2684	OPA3684	Low-Power CFB_{PLUS}
OPA691	OPA2691	OPA3691	High Slew Rate CFB
OPA695	—	—	> 500MHz CFB

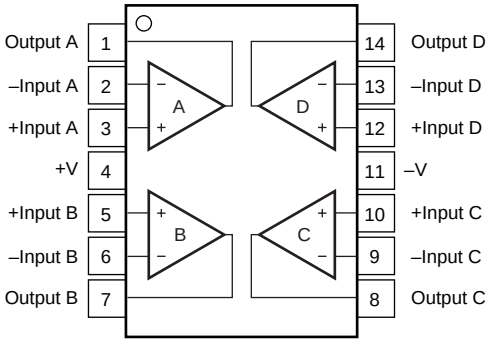
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA4684	SO-14	D	–40°C to +85°C	OPA4684	OPA4684ID	Rails, 58
"	"	"	"	"	OPA4684IDR	Tape and Reel, 2500
OPA4684	TSSOP-14	PW	–40°C to +85°C	OPA4684	OPA4684IPWT	Tape and Reel, 250
"	"	"	"	"	OPA4684IPWR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATION

Top View **SO, TSSOP**



OPA4684

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_F = 800\Omega$, $R_L = 100\Omega$, and G = +2, (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA4684ID, IPW						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[1]	0°C to 70°C[2]	–40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth ($V_O = 0.5V_{PP}$)	G = +1, $R_F = 800\Omega$	250				MHz	typ	C
	G = +2, $R_F = 800\Omega$	170	120	118	117	MHz	min	B
	G = +5, $R_F = 800\Omega$	138				MHz	typ	C
	G = +10, $R_F = 800\Omega$	120				MHz	typ	C
	G = +20, $R_F = 800\Omega$	95				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O = 0.5V_{PP}$, $R_F = 800\Omega$	19	16	14	14	MHz	min	B
Peaking at a Gain of +1	$R_F = 800\Omega$, $V_O = 0.5V_{PP}$	1.4	4.8	5.9	6.3	dB	max	B
Large-Signal Bandwidth	G = +2, $V_O = 4V_{PP}$	90				MHz	typ	C
Slew Rate	G = –1, V_O = 4V Step	780	675	650	575	V/µs	min	B
	G = +2, V_O = 4V Step	750	680	660	650	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	3				ns	typ	C
	G = +2, V_O = 4VStep	6.8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	–67	–59	–59	–58	dBc	max	B
	$R_L \geq 1k\Omega$	–82	–66	–65	–65	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–70	–66	–65	–65	dBc	max	B
	$R_L \geq 1k\Omega$	–84	–82	–81	–81	dBc	max	B
Input Voltage Noise	f > 1MHz	3.7	4.1	4.2	4.4	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	9.4	11	12	12.5	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	17	18	18.5	19	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, $V_O = 1.4V_{PP}$, $R_L = 150\Omega$	0.04				%	typ	C
Differential Phase	G = +2, NTSC, $V_O = 1.4V_{PP}$, $R_L = 150\Omega$	0.02				deg	typ	C
All Hostile Crosstalk, Input-Referred	3 Channels Driven at 5MHz, $1V_{PP}$ 4th Channel Measured	–52				dB	typ	C
DC PERFORMANCE[4]								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = 0V, $R_L = 1k\Omega$	355	**160**	155	153	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±1.5	**±4.0**	±4.6	±4.8	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	±5.0	**±13**	±14.5	±15	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			±25	±30	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±5.0	**±17**	±18.5	±19.5	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			±35	±40	nA°/C	max	B
INPUT								
Common-Mode Input Range[5] (CMIR)		±3.75	**±3.65**	±3.65	±3.6	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V	60	**53**	52	52	dB	min	A
Noninverting Input Impedance		50 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop, DC	4.0				Ω	typ	C
OUTPUT								
Voltage Output Swing	1kΩ Load	±4.1	**±3.9**	±3.9	±3.8	V	min	A
Current Output, Sourcing	V_O = 0	160	**120**	115	110	mA	min	A
Current Output, Sinking	V_O = 0	–120	**–100**	–95	–90	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.006				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Minimum Operating Voltage Range		±1.4				V	min	C
Max Quiescent Current	V_S = ±5V/per Channel	1.7	**1.8**	1.9	1.95	mA	max	A
Min Quiescent Current	V_S = ±5V/per Channel	1.7	**1.6**	1.55	1.45	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input-Referred	60	**54**	53	53	dB	typ	A
TEMPERATURE RANGE								
Specification: ID, IPW		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-14		100				°C/W	typ	C
PW TSSOP-14		110				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C tested specifications. (2) Junction temperature = ambient at low temperature limit, junction temperature = ambient +7°C at high temperature limit for over temperature tested specifications. (3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 1kΩ, R_L = 100Ω to V_S/2, and G = +2, (see Figure 3 for AC performance only), unless otherwise noted.

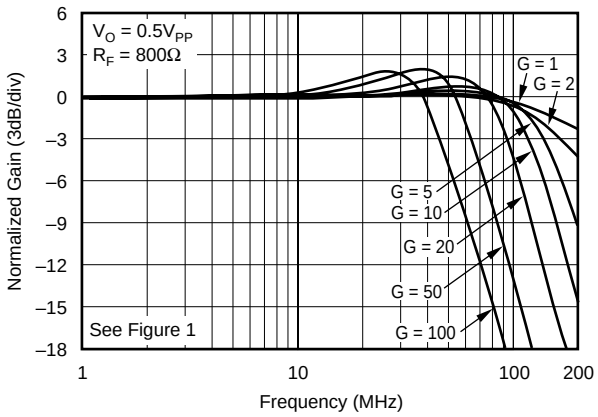
PARAMETER	CONDITIONS	OPA4684ID, IPW						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 3)								
Small-Signal Bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 1.3kΩ	140				MHz	typ	C
	G = +2, R_F = 1.3kΩ	110	86	85	82	MHz	min	B
	G = +5, R_F = 1.3kΩ	100				MHz	min	C
	G = +10, R_F = 1.3kΩ	90				MHz	typ	C
	G = +20, R_F = 1.3kΩ	75				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5Vp-p, R_F = 1.3kΩ	21	12	11	10	MHz	min	B
Peaking at a Gain of +1	R_F = 1.3kΩ, V_O < 0.5V_{PP}	0.5	2.6	3.4	3.7	dB	max	B
Large-Signal Bandwidth	G = 2, V_O = 2V_{PP}	86				MHz	typ	C
Slew Rate	G = 2, V_O = 2V Step	300	300	290	280	V/µs	min	B
	G = 2, V_O = 0.5V Step	4.3				ns	typ	C
Rise-and-Fall Time	G = 2, V_O = 2VStep	5.3				ns	typ	C
Harmonic Distortion	G = 2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω to V_S/2	–65	–60	–59	–59	dBc	max	B
	R_L ≥ 1kΩ to V_S/2	–84	–62	–61	–61	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–65	–64	–63	–63	dBc	max	B
	R_L ≥ 1kΩ to V_S/2	–74	–70	–70	–69	dBc	max	B
Input Voltage Noise	f > 1MHz	3.7	4.1	4.2	4.4	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	9.4	11	12	12.5	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	17	18	18.5	19	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, V_O = 1.4V_{PP}, R_L = 150Ω	0.04				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4V_{PP}, R_L = 150Ω	0.07				deg	typ	C
All Hostile X-Talk, Input-Referred	3-Channels Driven at 5MHz, 1V_{PP} 4th Channel Measured	–52				dB	typ	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = V_S/2, R_L = 1kΩ to V_S/2	355	**160**	155	153	kΩ	min	A
Input Offset Voltage	V_{CM} = V_S/2	±1.0	**±3.5**	±4.1	±4.3	mV	max	A
Average Offset Voltage Drift	V_{CM} = V_S/2			±12	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = V_S/2	±5	**±13**	±14.5	±15	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = V_S/2			±25	±30	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = V_S/2	±5	**±13**	±14.5	±16	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = V_S/2			±25	±30	nA°/C	max	B
INPUT								
Least Positive Input Voltage(5)		1.25	**1.32**	1.35	1.38	V	max	A
Most Positive Input Voltage(5)		3.75	**3.68**	3.65	3.62	V	min	A
Common-Mode Refection Ratio (CMRR)	V_{CM} = V_S/2	58	**51**	50	50	dB	min	A
Noninverting Input Impedance		50 || 1				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop	5				Ω	typ	C
OUTPUT								
Most Positive Output Voltage	R_L = 1kΩ to V_S/2	4.10	**3.9**	3.9	3.8	V	min	A
Least Positive Output Voltage	R_L = 1kΩ to V_S/2	0.9	**1.1**	1.1	1.2	V	max	A
Current Output, Sourcing	V_O = V_S/2	80	**65**	60	55	mA	min	A
Current Output, Sinking	V_O = V_S/2	70	**55**	50	45	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.006				Ω	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Max Single-Supply Operating Voltage			**12**	12	12	V	max	A
Min Single-Supply Operating Voltage		2.8				V	min	C
Max Quiescent Current	V_S = +5V/per Channel	1.45	**1.55**	1.55	1.55	mA	max	A
Min Quiescent Current	V_S = +5V/per Channel	1.45	**1.30**	1.20	1.15	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	58				dB	typ	C
TEMPERATURE RANGE								
Specification: ID, IPW		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA} Junction-to-Ambient								
D SO-14		100				°C/W	typ	C
PW TSSOP-14		110				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C tested specifications. (2) Junction temperature = ambient at low temperature limit, junction temperature = ambient +3°C at high temperature limit for over temperature tested specifications. (3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

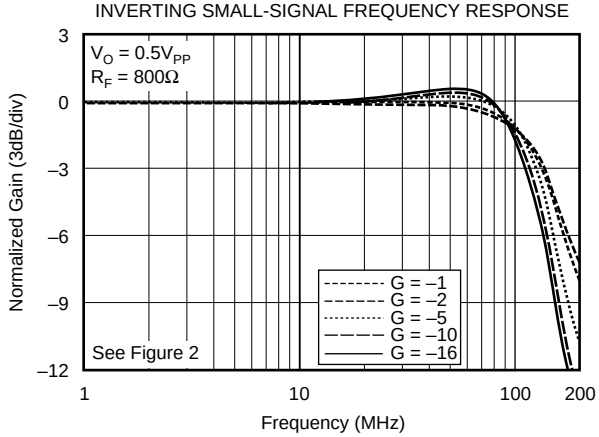
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

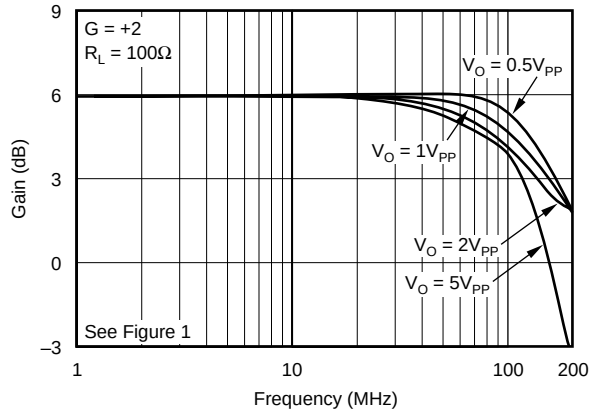
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



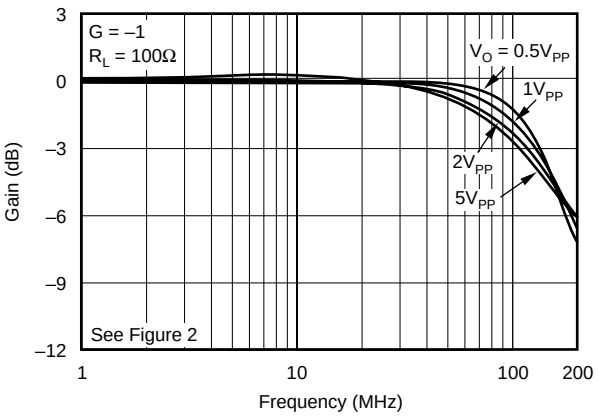
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



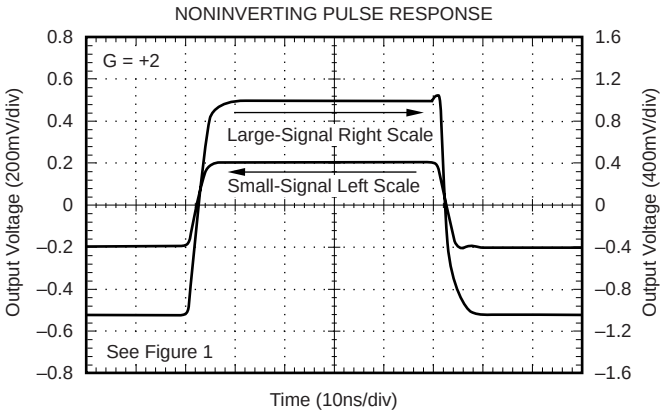
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



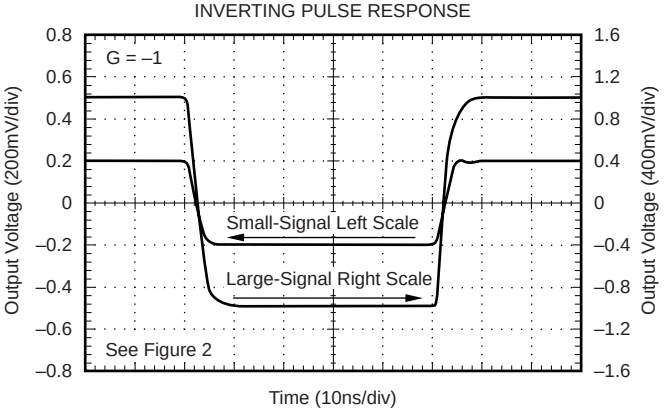
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



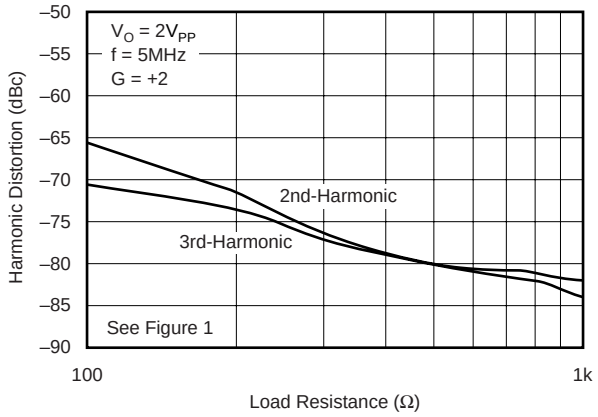
INVERTING PULSE RESPONSE



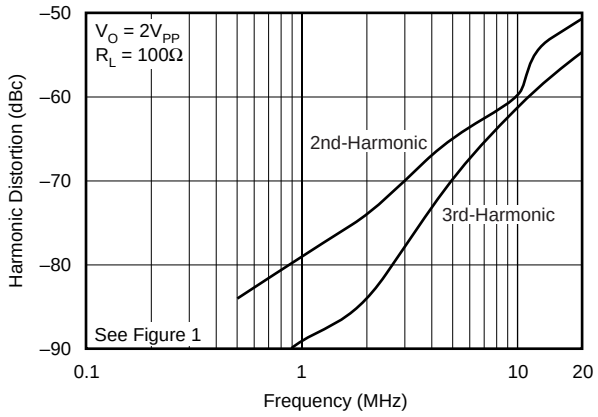
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

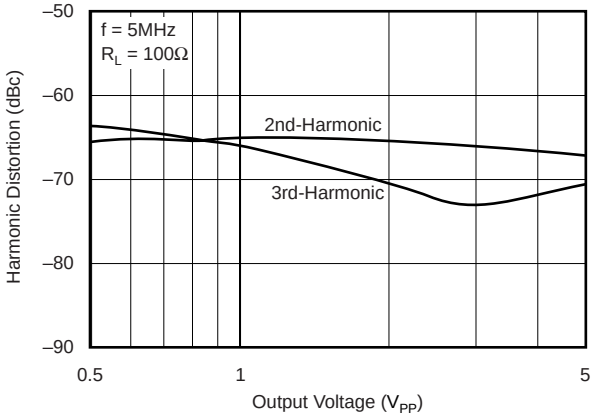
HARMONIC DISTORTION vs LOAD RESISTANCE



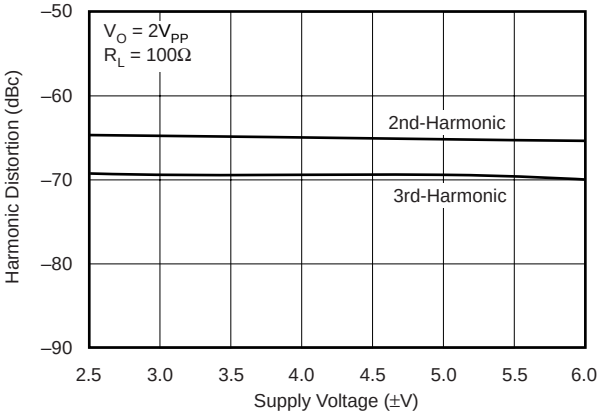
HARMONIC DISTORTION vs FREQUENCY



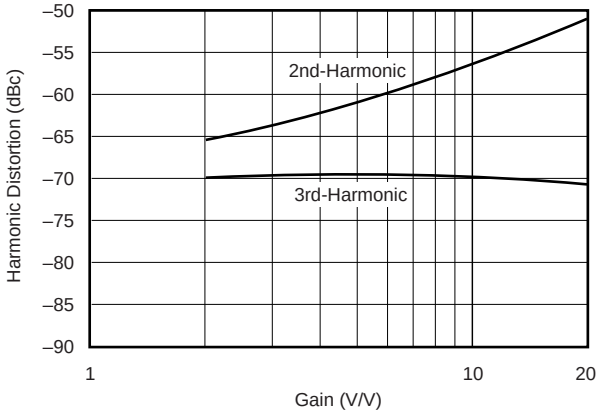
HARMONIC DISTORTION vs OUTPUT VOLTAGE



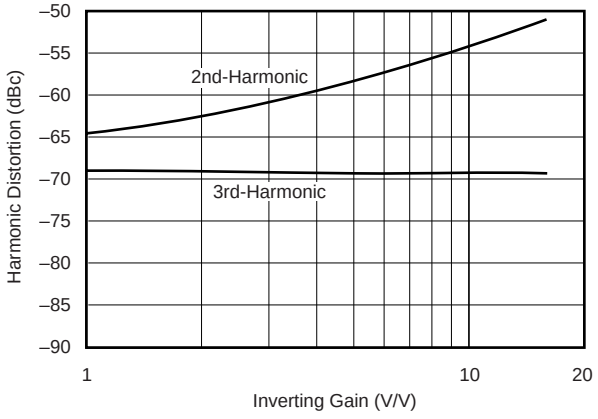
5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



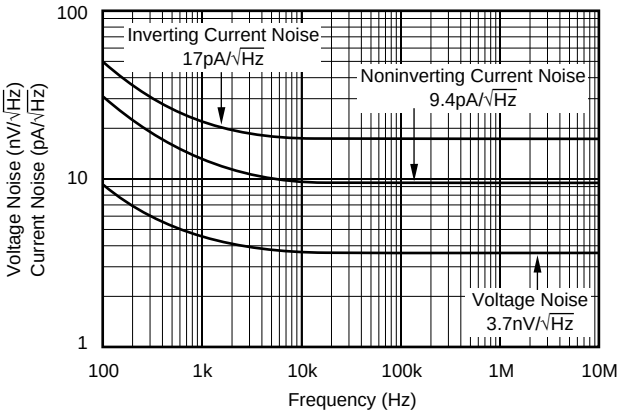
HARMONIC DISTORTION vs INVERTING GAIN



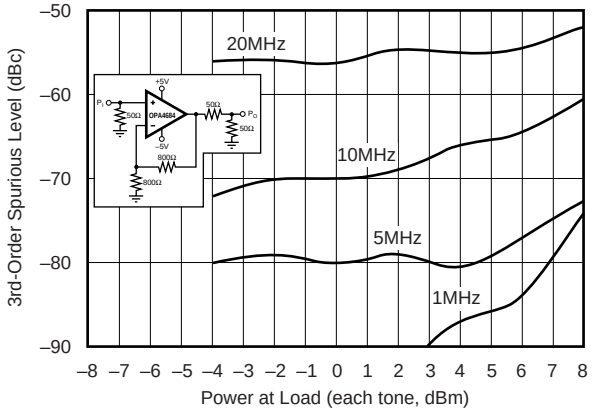
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

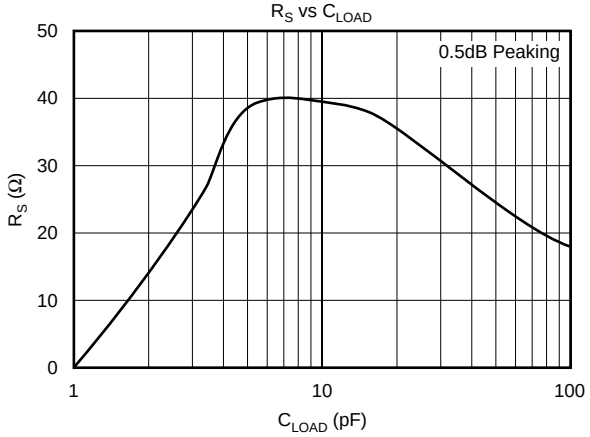
INPUT VOLTAGE AND CURRENT NOISE DENSITY



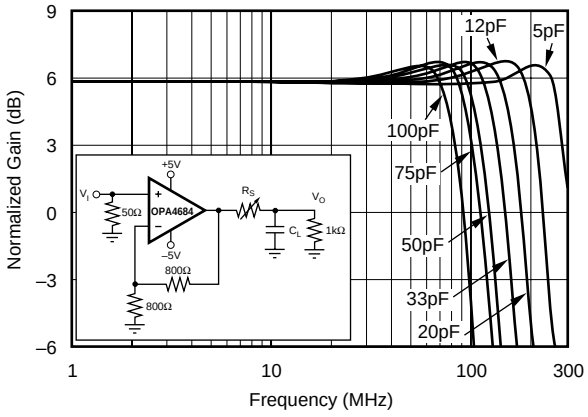
2-TONE, 3RD-ORDER
INTERMODULATION DISTORTION



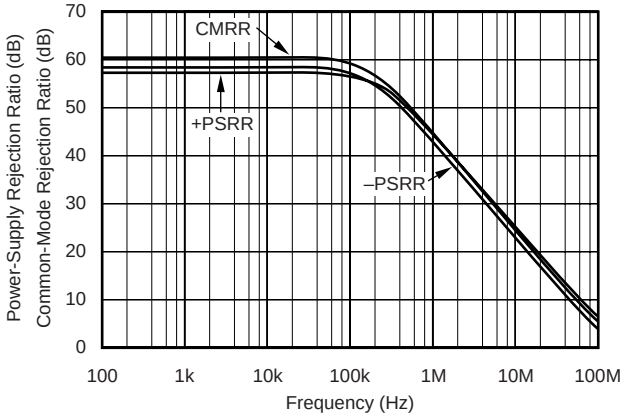
R_S vs C_{LOAD}



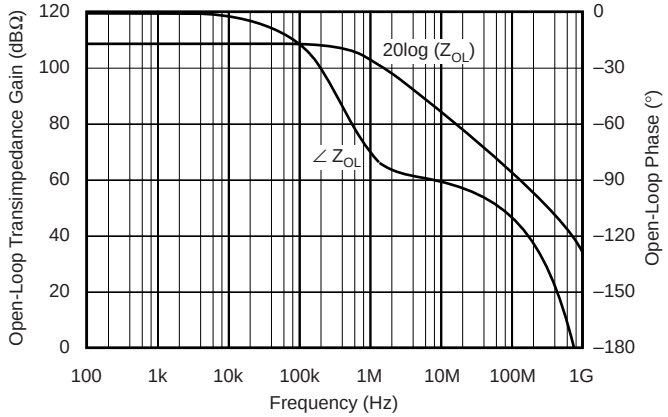
SMALL-SIGNAL BANDWIDTH vs C_{LOAD}



CMRR and PSRR vs FREQUENCY



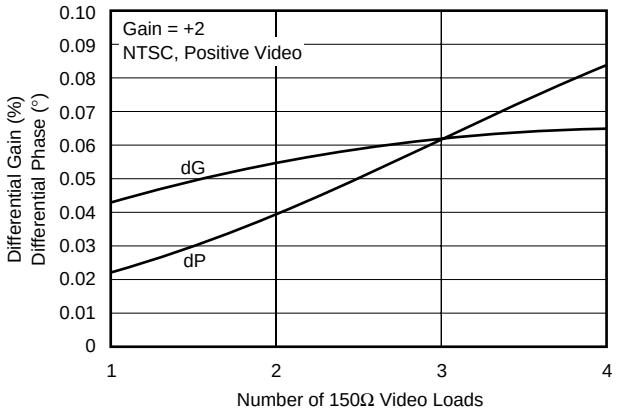
OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE



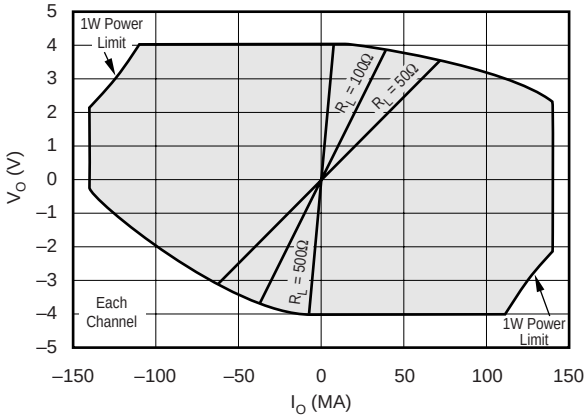
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

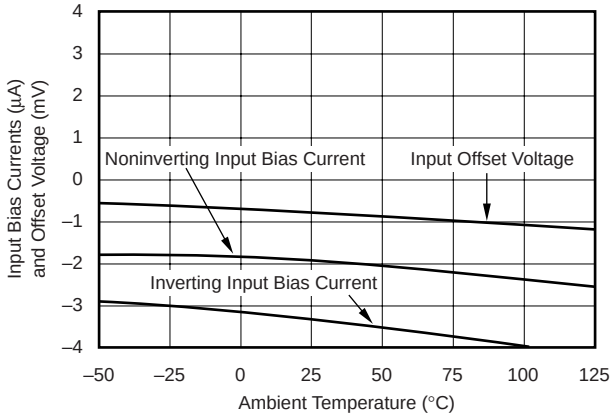
COMPOSITE VIDEO DIFFERENTIAL GAIN/PHASE



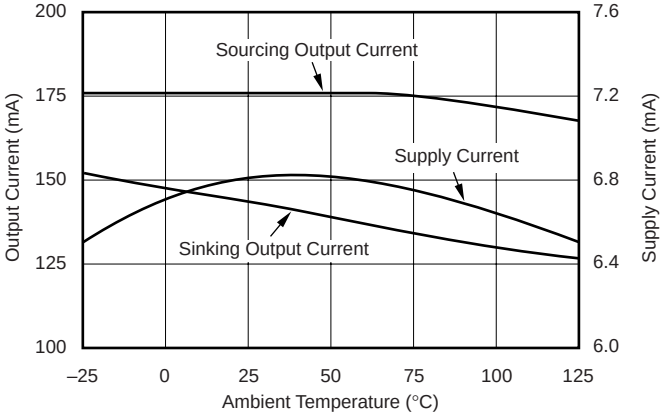
OUTPUT CURRENT AND VOLTAGE LIMITATIONS



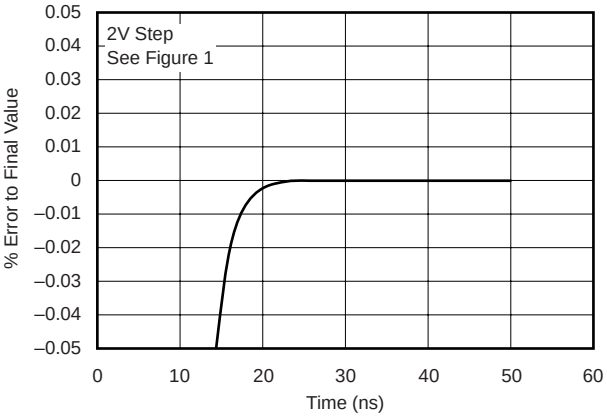
TYPICAL DC DRIFT OVER AMBIENT TEMPERATURE



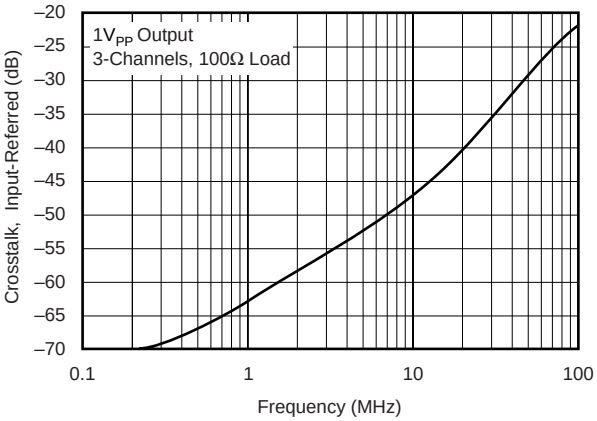
SUPPLY AND OUTPUT CURRENT
vs AMBIENT TEMPERATURE



SETTLING TIME



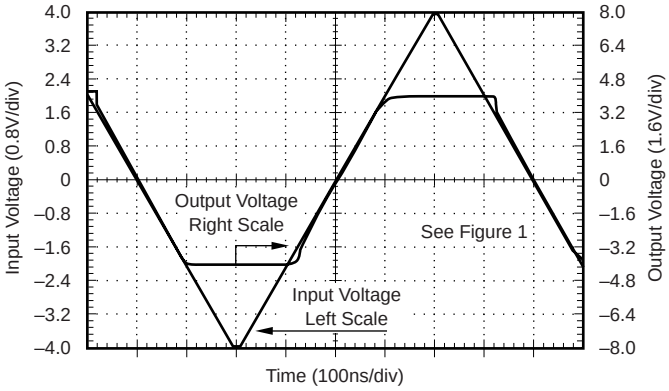
ALL HOSTILE CROSSTALK



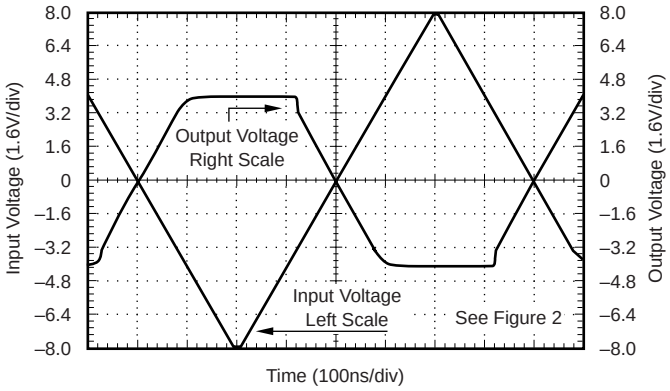
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

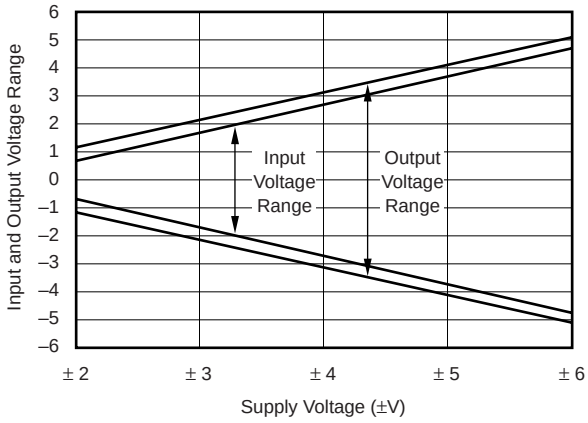
NONINVERTING OVERDRIVE RECOVERY



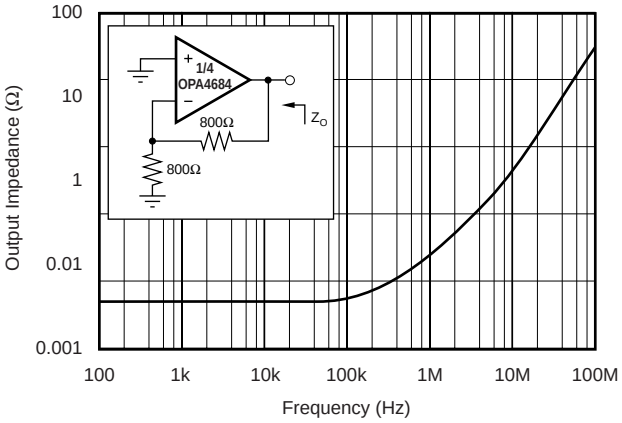
INVERTING OVERDRIVE RECOVERY



INPUT AND OUTPUT RANGE vs SUPPLY VOLTAGE



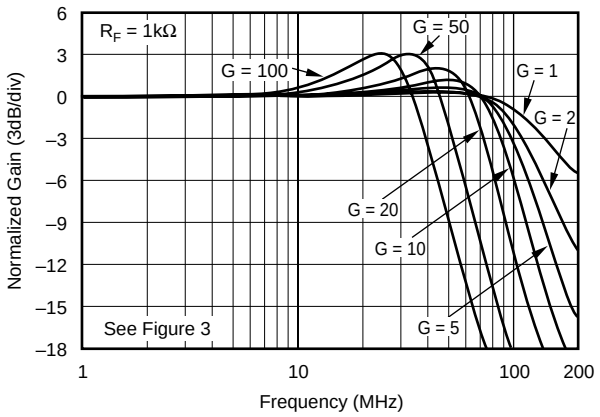
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



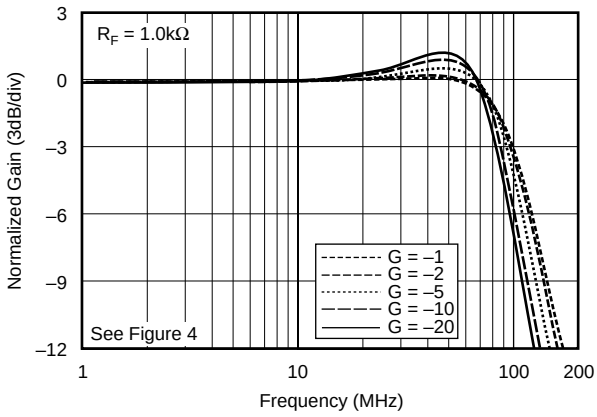
TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +2, R_F = 1kΩ, and R_L = 100Ω to V_S/2, unless otherwise noted.

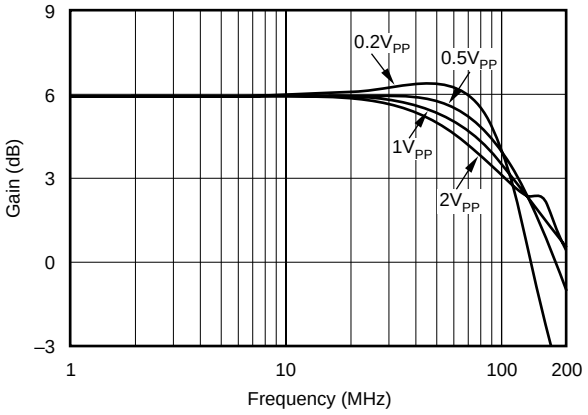
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



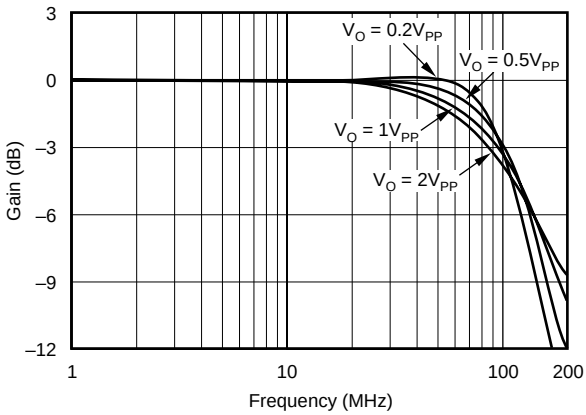
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



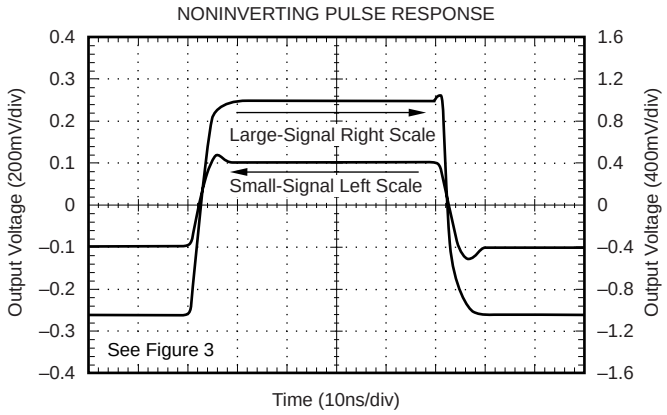
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



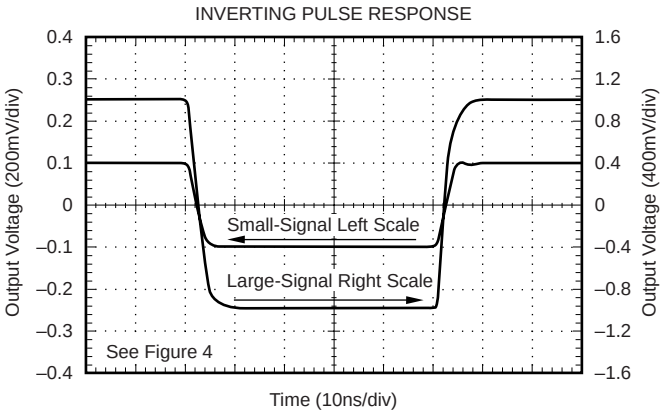
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



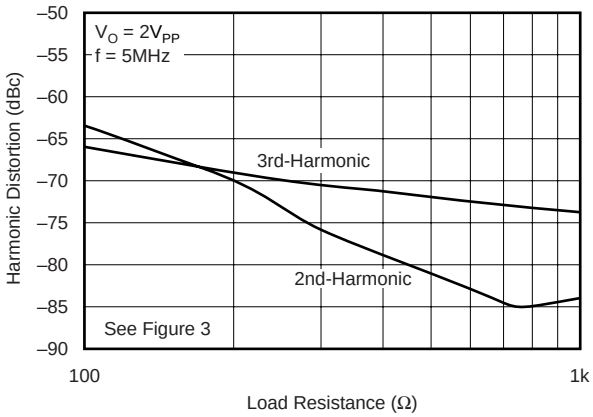
INVERTING PULSE RESPONSE



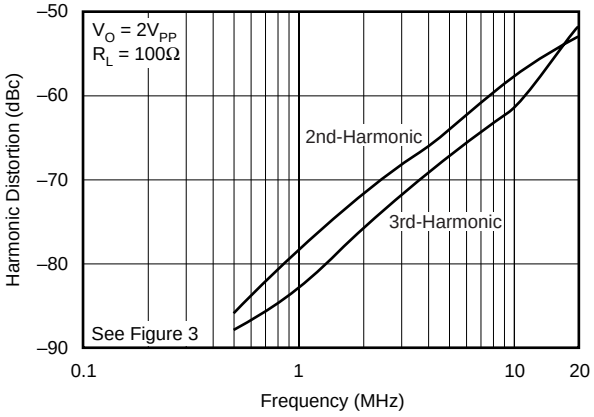
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

At T_A = +25°C, G = +2, R_F = 1kΩ, and R_L = 100Ω to V_S/2, unless otherwise noted.

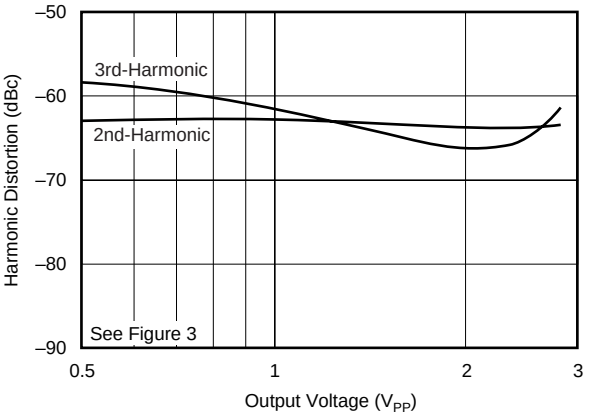
HARMONIC DISTORTION vs LOAD RESISTANCE



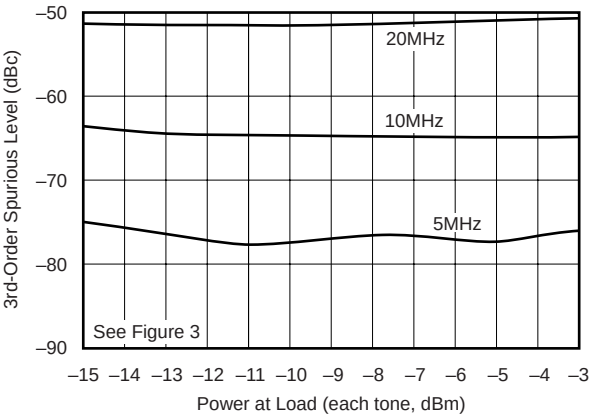
HARMONIC DISTORTION vs FREQUENCY



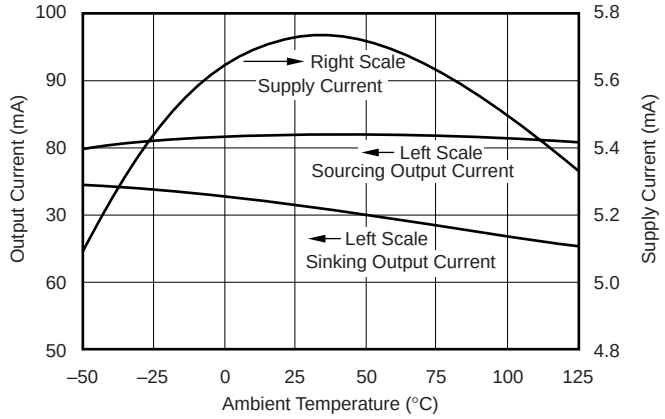
HARMONIC DISTORTION vs OUTPUT VOLTAGE



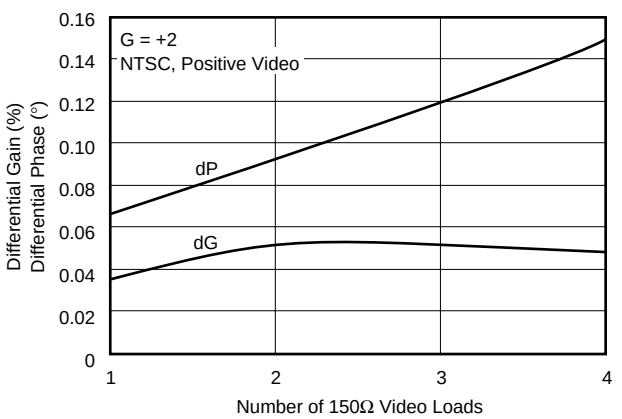
2-TONE, 3RD-ORDER
INTERMODULATION DISTORTION



SUPPLY AND OUTPUT CURRENT
vs TEMPERATURE



COMPOSITE VIDEO DIFFERENTIAL GAIN/PHASE



APPLICATIONS INFORMATION

LOW-POWER CURRENT-FEEDBACK OPERATION

The quad-channel OPA4684 gives a new level of performance in low-power current-feedback op amps. Using a new input stage buffer architecture, the OPA4684 CFB_{PLUS} amplifier holds nearly constant AC performance over a wide gain range. This closed-loop internal buffer gives a very low and linearized impedance at the inverting node, isolating the amplifier's AC performance from gain element variations. This low impedance allows both the bandwidth and distortion to remain nearly constant over gain, moving closer to the ideal current feedback performance of gain bandwidth independence. This low-power amplifier also delivers exceptional output power—its ±4V swing on ±5V supplies with > 100mA output drive gives excellent performance into standard video loads or doubly-terminated 50Ω cables. Single +5V supply operation is also supported with similar bandwidths but with reduced output power capability. For lower quiescent power in a CFB_{PLUS} amplifier, consider the OPA683 family; for higher output power, consider the OPA691 family.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit used as the basis of the ±5V Electrical and Typical Characteristics for each channel. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 1600Ω = 94Ω. Gain changes are most easily accomplished by simply resetting the R_G value, holding R_F constant at its recommended value of 800Ω.

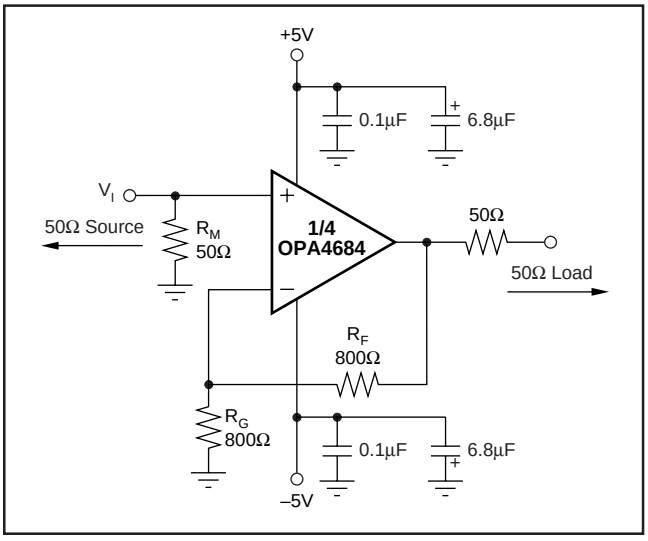


FIGURE 1. DC-Coupled, G = +2V/V, Bipolar Supply Specifications and Test Circuit.

Figure 2 shows the DC-coupled, gain of –1V/V, dual power-supply circuit used as the basis of the Inverting Typical Characteristics for each channel. Inverting operation offers several performance benefits. Since there is no common-mode signal across the input stage, the slew rate for inverting operation is typically higher and the distortion performance is slightly improved. An additional input resistor, R_M, is included in Figure 2 to set the input impedance equal to 50Ω. The parallel combination of R_M and R_G set the input impedance. As the desired gain increases for the inverting configuration, R_G is adjusted to achieved the desired gain, while R_M is also adjusted to hold a 50Ω input match. A point will be reached where R_G will equal 50Ω, R_M is removed, and the input match is set by R_G only. With R_G fixed to achieve an input match to 50Ω, increasing R_F will increase the gain. This will, however, quickly reduce the achievable bandwidth as the feedback resistor increases from its recommended value of 800Ω. If the source does not require an input match to 50Ω, either adjust R_M to get the desired load, or remove R_M and allow the R_G resistor alone provide the input load.

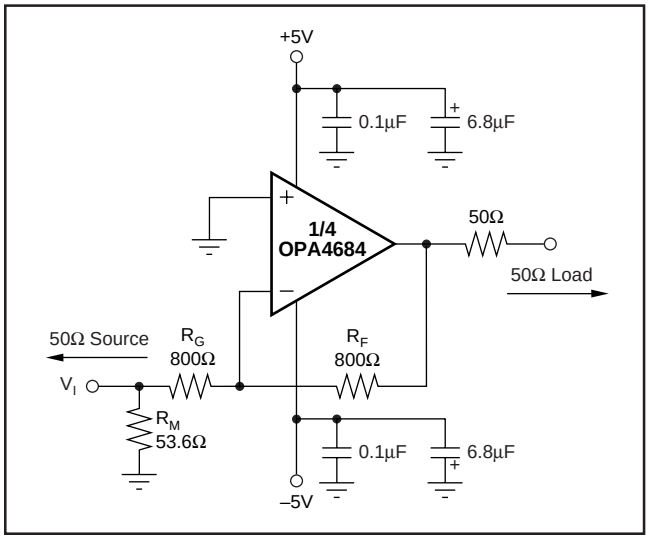


FIGURE 2. DC-Coupled, G = –1V/V, Bipolar Supply Specifications and Test Circuit.

These circuits show ±5V operation. The same circuits can be applied with bipolar supplies from ±2.5V to ±6V. Internal supply independent biasing gives nearly the same performance for the OPA4684 over this wide range of supplies. Generally, the optimum feedback resistor value (for nominally flat frequency response at G = +2) will increase in value as the total supply voltage across the OPA4684 is reduced.

See Figure 3 for the AC-coupled, single +5V supply, gain of +2V/V circuit configuration used as a basis for the +5V only Electrical and Typical Characteristics for each channel. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 10kΩ resistors) to the noninverting input. The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.25V of either supply pin, giving a $2.5V_{PP}$ input signal range centered between the supply pins. The input impedance of Figure 3 is set to give a 50Ω input match. If the source does not require a 50Ω match, remove this and drive

directly into the blocking capacitor. The source will then see the 5kΩ load of the biasing network as a load. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1, which puts the noninverting input DC bias voltage (2.5V) on the output as well. The feedback resistor value has been adjusted from the bipolar ±5V supply condition to re-optimize for a flat frequency response in +5V only, gain of +2, operation. On a single +5V supply, the output voltage can swing to within 1.0V of either supply pin while delivering more than 70mA output current—easily giving a $3V_{PP}$ output swing into 100Ω (8dBm maximum at the matched 50Ω load). The circuit of Figure 3 shows a blocking capacitor driving into a 50Ω output resistor, then into a 50Ω load. Alternatively, the blocking capacitor could be removed if the load is tied to a supply midpoint or to ground if the DC current required by the load is acceptable.

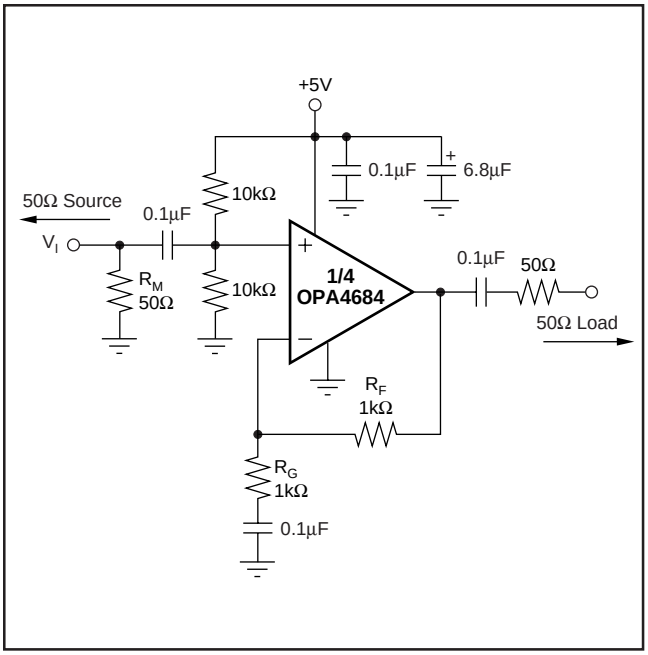


FIGURE 3. AC-Coupled, G = +2V/V, Single-Supply Specifications and Test Circuit.

Figure 4 shows the AC-coupled, single +5V supply, gain of –1V/V circuit configuration used as a basis for the inverting +5V only Typical Characteristics for each channel. In this case, the midpoint DC bias on the noninverting input is also decoupled with an additional 0.1µF capacitor. This reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5V bias on the noninverting input pin appears on the inverting input pin and, since R_G is DC-blocked by the input capacitor, will also appear at the output pin. One advantage to inverting operation is that since there is no signal swing across the input stage, higher slew rates and operation to even lower supply voltages is possible. To retain a $1V_{PP}$ output capability, operation down to a 3V supply is allowed. At a +3V supply, the input stage is saturated, but for the inverting configuration of a current-feedback amplifier, wideband operation is retained even under this condition.

The circuits of Figure 3 and 4 show single-supply operation at +5V. These same circuits may be used up to single supplies of +12V with minimal change in the performance of the OPA4684.

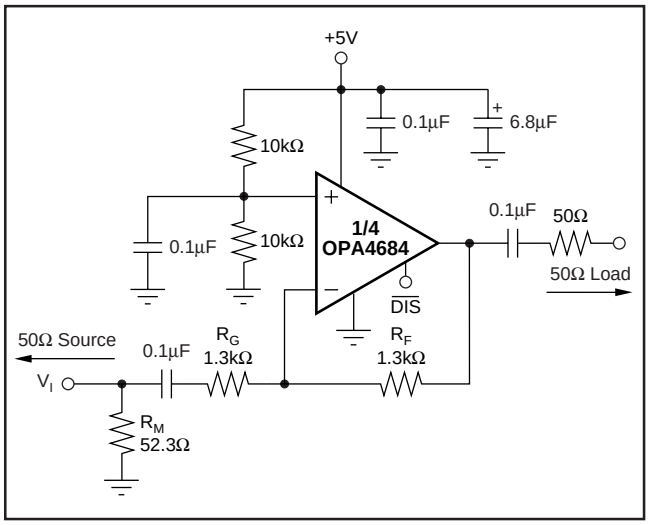


FIGURE 4. AC-Coupled, G = –1V/V, Single-Supply Specifications and Test Circuit.

DIFFERENTIAL INTERFACE APPLICATIONS

Dual and quad op amps are particularly suitable to differential input to differential output applications. Typically, these fall into either analog-to-digital converter (ADC) input interface or line driver applications. Two basic approaches to differential I/O are noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the OPA4684. Each has its advantages and disadvantages. Figure 5 shows a basic starting point for noninverting differential I/O applications.

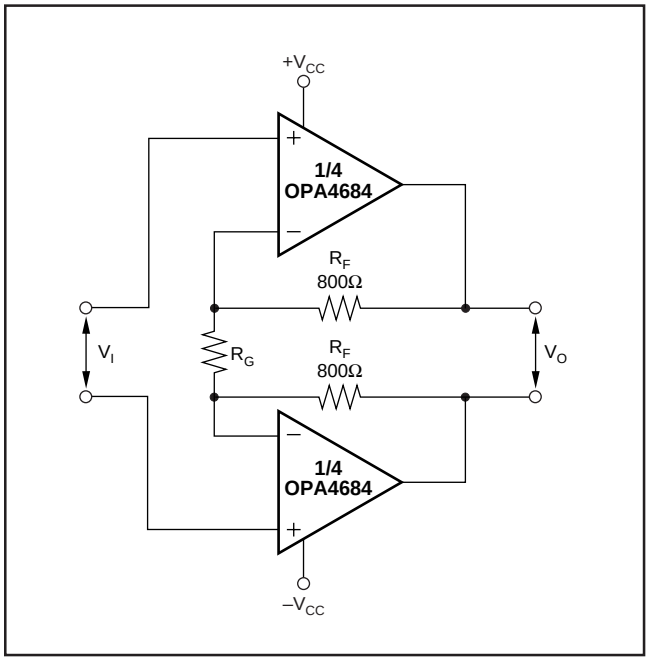


FIGURE 5. Noninverting Differential I/O Amplifier.

This approach provides for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the amplifier gain. The differential signal gain for the circuit of Figure 5 is:

$$V_O/V_I = A_D = 1 + 2 \bullet R_F/R_G$$

Since the OPA4684 is a CFB_{PLUS} amplifier, its bandwidth is principally controlled with the feedback resistor value; Figure 5 shows the recommended value of 800Ω. However, the gain may be adjusted with considerable freedom using just the R_G resistor. In fact, R_G may be a reactive network providing a very isolated shaping to the differential frequency response. Since the inverting inputs of the OPA4684 are very low impedance closed-loop buffer outputs, the R_G element does not interact with the amplifier's bandwidth—wide ranges of resistor values and/or filter elements may be inserted here with minimal amplifier bandwidth interaction.

Various combinations of single-supply or AC-coupled gains can also be delivered using the basic circuit of Figure 5. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1 since an equal DC voltage at each inverting node creates no current through R_G, giving that voltage a common-mode gain of 1 to the output.

Figure 6 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors (R_G) become the input resistance for the source. This provides a better noise performance than the noninverting configuration, but does limit the flexibility in setting the input impedance separately from the gain.

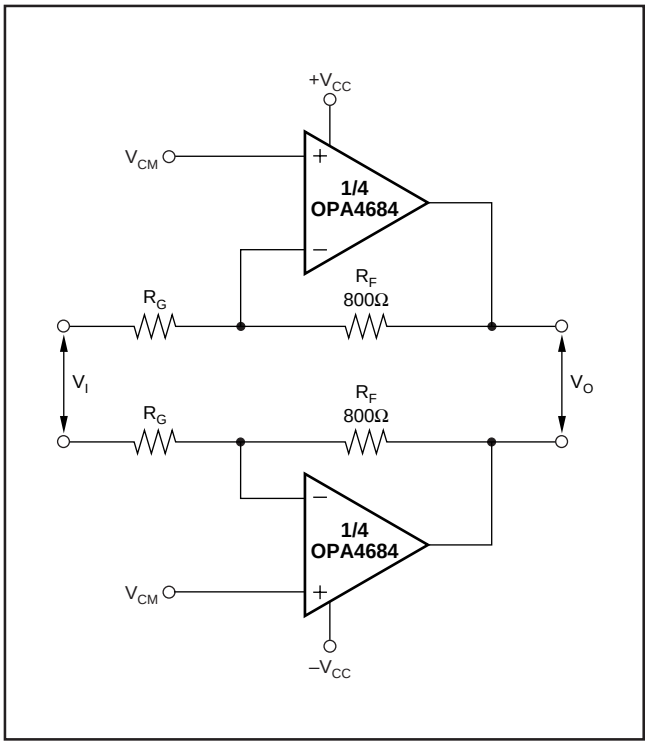


FIGURE 6. Inverting Differential I/O Amplifier.

The two noninverting inputs provide an easy common-mode control input. This is particularly useful if the source is AC-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two noninverting inputs again have a gain of 1 to the output pins, giving an easy common-mode control for single-supply operation. The OPA4684 used in this configuration does constrain the feedback to the 800Ω region for best frequency response. With R_F fixed, the input resistors may be adjusted to the desired gain but will also be changing the input impedance as well. The differential gain for this circuit is:

$$V_O/V_I = -R_F/R_G$$

LOW-POWER VIDEO LINE DRIVER APPLICATIONS

For low-power, video line driving, the OPA4684 provides the output current and linearity to support four channels of either single video lines, or up to four video lines in parallel on each output. Figure 7 shows a typical ±5V supply video line driver application where only one channel is shown and only a single line is being driven. The improved 2nd-harmonic distortion of the CFB_{PLUS} architecture, along with the OPA4684's high output current and voltage, gives exceptional differential gain and phase performance for a low-power solution. As the Typical Characteristics show, a single video load indicates a dG/dP of 0.04%/0.02°. Multiple loads may be driven on each output, with minimal x-talk, while the dG/dP is still < 0.1%/0.1° for up to 4 parallel video loads.

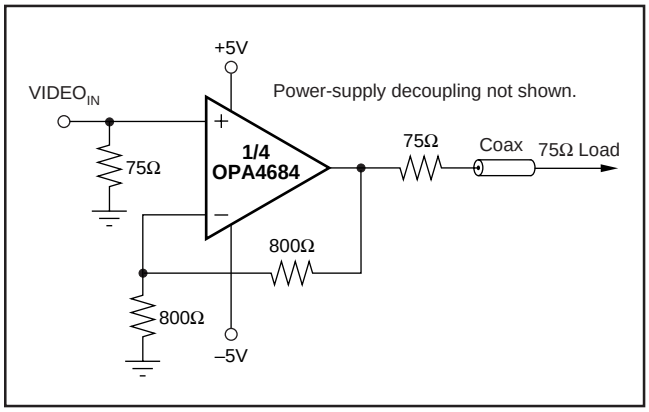


FIGURE 7. Gain of +2 Video Cable Driver.

DC-COUPLED SINGLE-TO-DIFFERENTIAL CONVERSION

The previous differential output circuits were set up to receive a differential input as well as provide a differential output. Figure 8 shows one way to provide a single to differential conversion, with DC coupling, and independent output common-mode control using a quad op amp.

The circuit of Figure 8 provides several useful features for isolating the input signal from the final outputs. Using the first amplifier as a simple noninverting stage gives an independent adjustment on R_I (to set the source loading) while the gain can be easily adjusting in this stage using the R_G resistor. Bandwidth is relatively independent of gain setting in the OPA4684. The next stage allows a separate output common-mode level to be set up. The desired output com-

mon-mode voltage, V_{CM}, is cut in half and applied to the noninverting input of the 2nd stage. The signal path in this stage sees a gain of –1 while this (1/2 • V_{CM}) voltage sees a gain of +2. The output of this 2nd stage is then the original common-mode voltage plus the inverted signal from the output of the first stage. The 2nd stage output appears directly at the output of the noninverting final stage. The inverting node of the inverting output stage is also biased to the common-mode voltage, equal to the common-mode voltage appearing at the output of the 2nd stage, creating no current flow and placing the desired V_{CM} at the output of this stage as well.

LOW-POWER, DIFFERENTIAL I/O, 4th-ORDER ACTIVE FILTER

The OPA4684 can give a very capable gain block for low-power active filters. The quad design lends itself very well to differential active filters. Where the filter topology is looking for a simple gain function to implement the filter, the noninverting configuration is preferred to isolate the filter elements from the gain elements in the design. Figure 9 shows an example of a very low-power, 10MHz, 4th-order Butterworth, low-pass Sallen-Key filter. Often, these filters are designed at an amplifier gain of 1 to minimize amplifier bandwidth interaction with the desired filter shape. Since the OPA4684 shows minimal bandwidth change with gain, this feature would not be a constraint in this design. The example of Figure 9 designs the filter for a differential gain of 4 in each differential stage. This DC-coupled design gives a signal gain of 16V/V in the passband with a f_{-3dB} at 10MHz. The design places the higher Q stage first to allow the lower Q 2nd stage to roll off the peaked noise of the first stage. The resistor values have been adjusted slightly to account for the amplifier group delay.

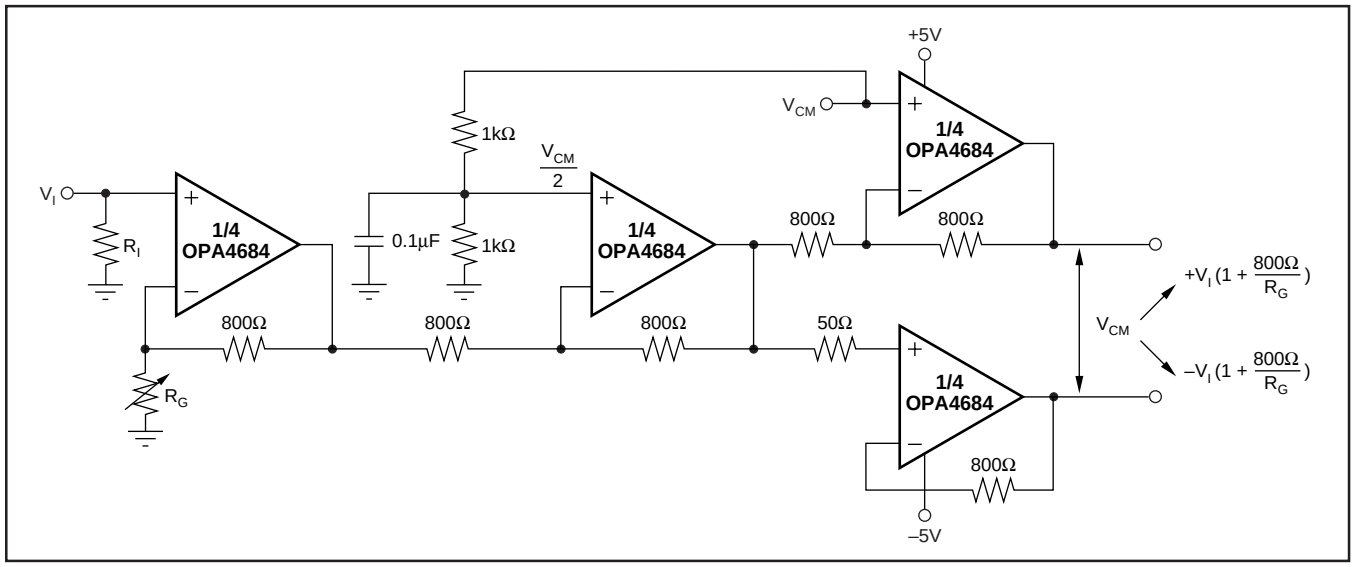


FIGURE 8. High Gain, DC-Coupled, Single to Differential Conversion.

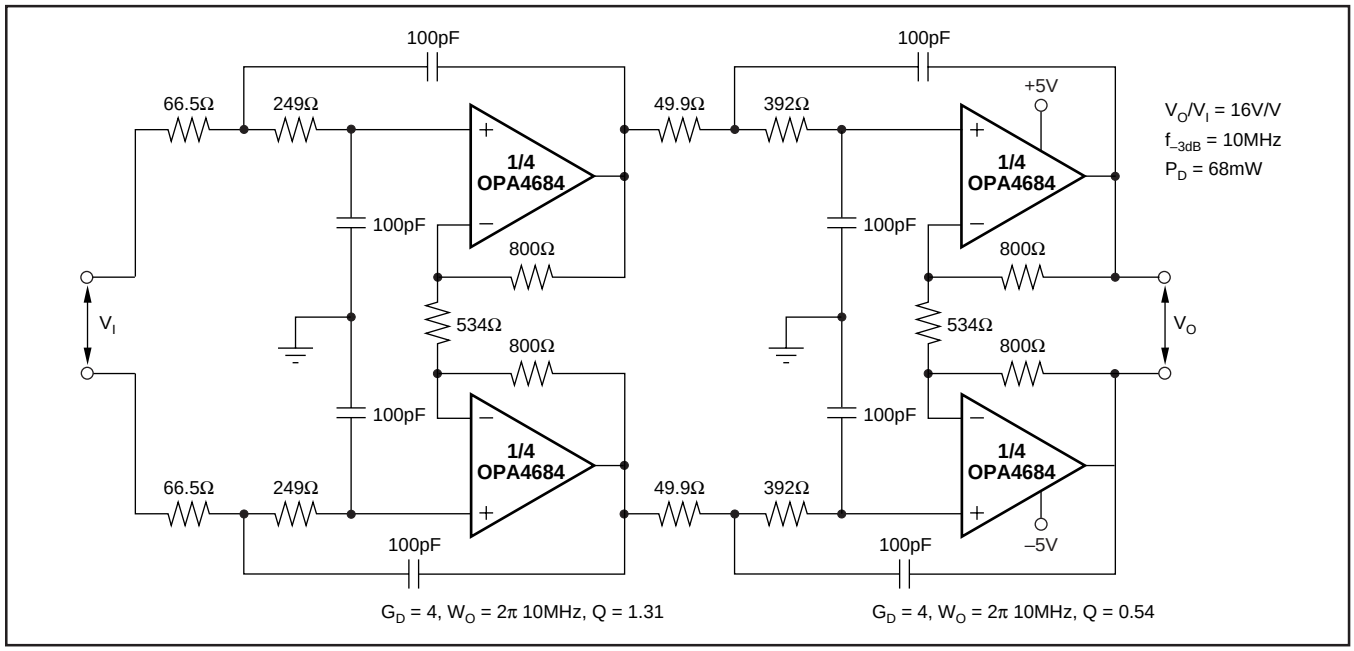


FIGURE 9. Low-Power, Differential I/O, 4th-Order Butterworth Active Filter.

While this circuit is bipolar, using ±5V supplies, it can easily be adapted to single-supply operation. This is typically done by providing a supply midpoint reference at the noninverting inputs then adding DC-blocking caps at each input and in series with the amplifier gain resistor, R_G. This will add two real zeroes in the response, transforming this circuit into a bandpass. Figure 10 shows the frequency response for the filter of Figure 9.

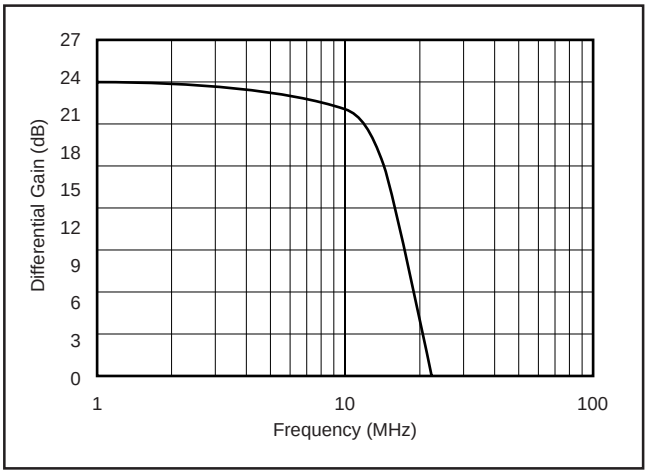


FIGURE 10. Low-Power, Differential 4th-Order, 10MHz Butterworth Response.

LOW-POWER DSL TRANSCEIVER INTERFACE

With four amplifiers available, the quad OPA4684 can meet the needs for both differential driver and receiver in a low-power xDSL line interface design. Figure 11 shows a simplified design example. Two amplifiers are used as a noninverting differential driver while the other two implement the driver echo cancellation and receiver amplifier function. This example shows a single +12V design where the drive side is taking a $2V_{PP}$ maximum input from the transmit filter and providing a differential gain of 7, giving a maximum $14V_{PP}$ differential output swing. This is coupled through 50Ω matching resistors and a 1:1 transformer to give a maximum $7V_{PP}$ on a 100Ω line. This $7V_{PP}$ corresponds to a 10dBm line power with a 3.5 crest factor.

The differential receiver is configured as an inverting summing stage where the outputs of the driver are cancelled prior to appearing at the output of the receive amplifiers. This is done by summing the output voltages for the drive amplifiers and their attenuated and inverted levels (at the transformer input) into the inverting inputs of each receiver amplifier. The resistor values are set in Figure 11 to give perfect drive signal cancellation if the drive signal is attenuated by 1/2, going from the drive amplifier outputs to the transformer input. The signal received through the transformer has a gain of 1 through the receive amplifiers. Higher gain could easily be provided by scaling the resistors summing into the inverting inputs of the receiver amplifiers down while keeping the same ratio between them.

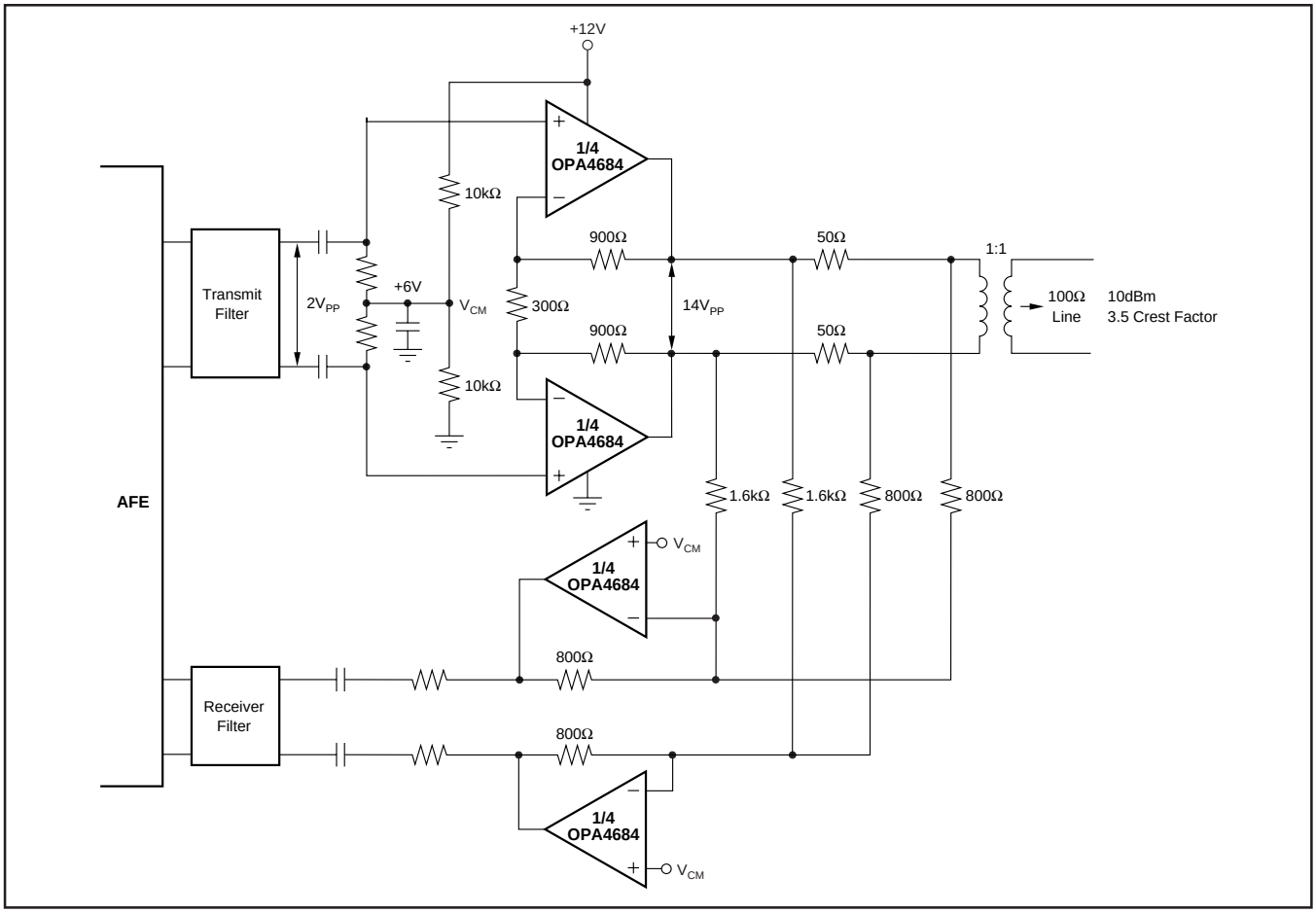


FIGURE 11. Low-Power, XDSL Transceiver Design.

DUAL-CHANNEL, DIFFERENTIAL ADC DRIVER

Where a low-power, single-supply, interface to a differential input +5V ADC is required, the circuit of Figure 12 can provide a high dynamic range, medium gain interface for dual high-performance ADCs. The circuit of Figure 12 uses two amplifiers in the differential inverting configuration. The common-mode voltage is set on the noninverting inputs to the supply midscale. In this example, the input signal is coupled in through a 1:2 transformer. This provides both signal gain, single to differential conversion, and a reduction in noise figure. To show a 50Ω input impedance at the input to the transformer, two 200Ω resistors are required on the transformer secondary. These two resistors are also the amplifier gain elements. Since the same DC voltage appears on both inverting nodes in the circuit of Figure 12, no DC current will flow through the transformer, giving a DC gain of 1 to the output for this common-mode voltage, V_{CM}.

The circuit of Figure 12 is particularly suitable for a moderate resolution dual ADC used as I/Q samplers. The optional 500Ω resistors to ground on each amplifier output can be added to improve the 2nd- and 3rd-harmonic distortion by > 15dB if higher dynamic range is required. Figure 13 shows the harmonic distortion for the circuit of Figure 12 with and without these pull-down resistors. The 5mA added output stage current significantly improves linearity if that is required. The measured 2nd-harmonic distortion is consistently lower than the 3rd-harmonics for this balanced differential design. It is particularly helpful for this low-power design if there are no grounds in the signal path after the low-level signal at the transformer input. The two pull-down resistors do show a signal path ground and should be connected at the same physical point to ground, in order to eliminate imbalanced ground return currents from degrading 2nd-harmonic distortion.

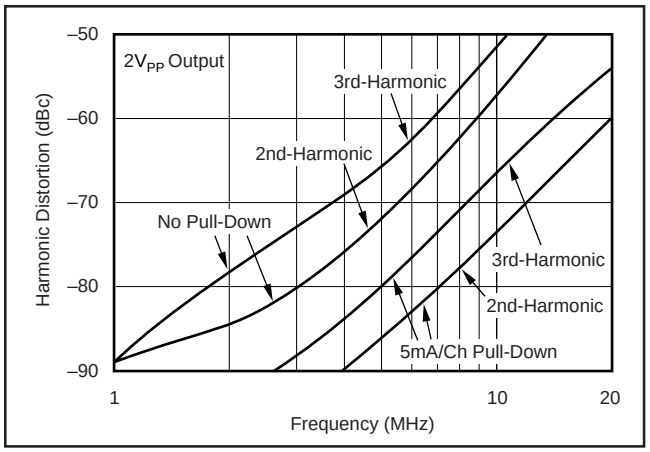


FIGURE 13. Harmonic Distortion vs Frequency.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA4684 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA4684ID	SO-14	DEM-OPA-SO-4A	SBOU016
OPA4684IPW	TSSOP-14	DEM-OPA-TSSOP-4A	SBOU017

TABLE I. Demonstration Fixtures by Package.

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA4684 product folder.

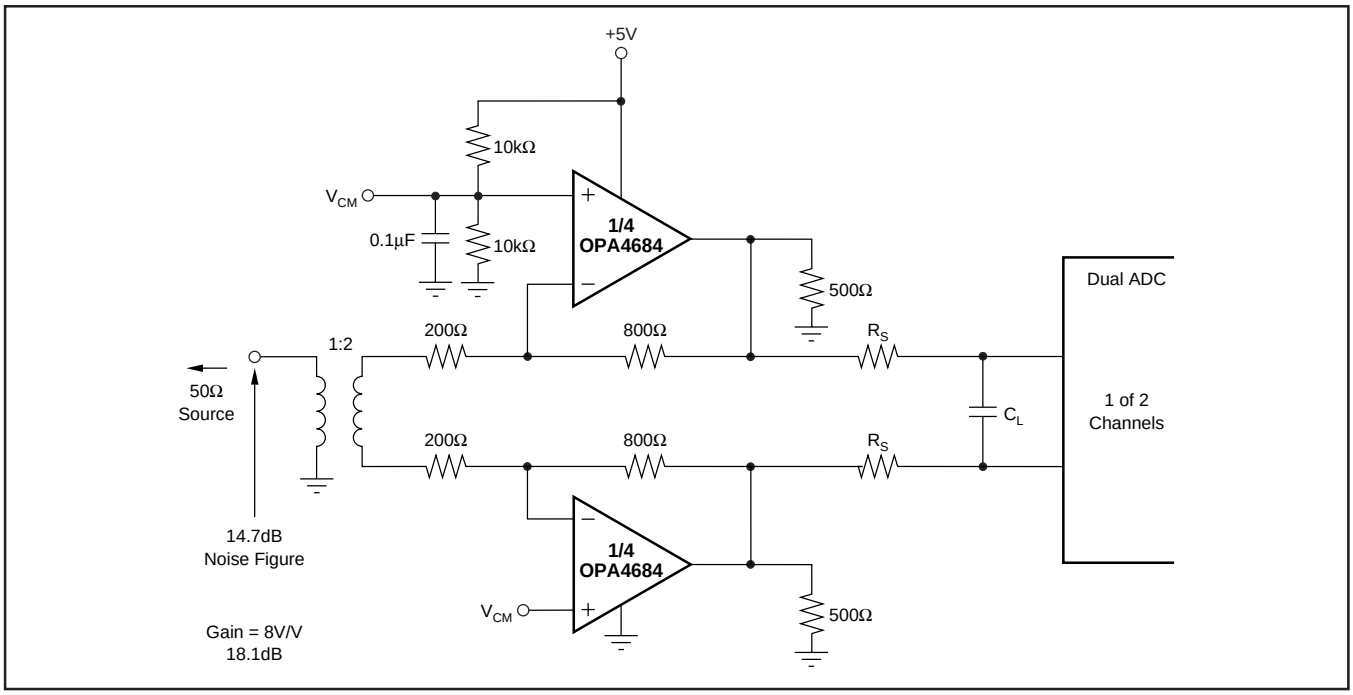


FIGURE 12. Single-Supply Differential ADC Driver (1 of 2 Channels).

MACROMODELS

Computer simulation of circuit performance using SPICE is often useful in predicting the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. Check the TI web site (www.ti.com) for SPICE macromodels within the OPA4684 product folder. These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

Any current-feedback op amp like the OPA4684 can hold high bandwidth over signal-gain settings with the proper adjustment of the external resistor values. A low-power part like the OPA4684 typically shows a larger change in bandwidth due to the significant contribution of the inverting input impedance to loop-gain changes as the signal gain is changed. Figure 14 shows a simplified analysis circuit for any current-feedback amplifier.

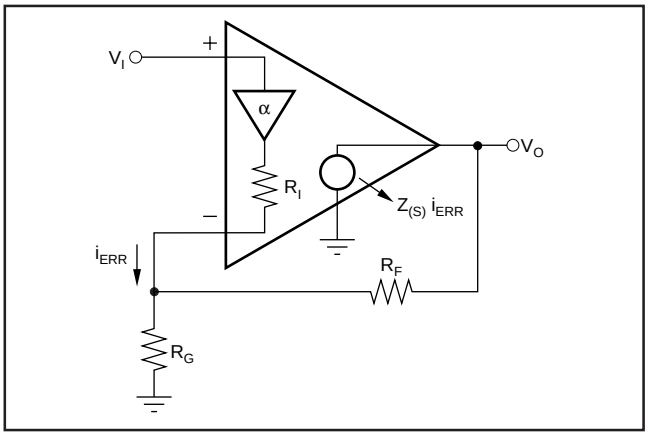


FIGURE 14. Current-Feedback Transfer Function Analysis Circuit.

The key elements of this current-feedback op amp model are:

$\alpha \Rightarrow$ Buffer gain from the noninverting input to the inverting input

$R_I \Rightarrow$ Buffer output impedance

$i_{ERR} \Rightarrow$ Feedback error current signal

$Z_{(S)} \Rightarrow$ Frequency-dependent open-loop transimpedance gain from i_{ERR} to V_O

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single op amp differential amplifier configuration. For the buffer gain $\alpha < 1.0$, the CMRR = $-20 \cdot \log(1 - \alpha)$. The closed-loop input stage buffer used in the OPA4684 gives a buffer gain more closely approaching 1.00; this shows up in a slightly higher CMRR than previous current-feedback op amps.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA4684 reduces this element to approximately 4.0Ω using the local loop gain of the input buffer stage. This significant reduction in output impedance, on very low power, contributes powerfully to extending the bandwidth at higher gains.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency-dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 14 gives Equation 1:

(1)

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F + R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha\, NG}{1+\frac{R_F + R_I\, NG}{Z_{(S)}}}$$

$$\left[NG = \left(1+\frac{R_F}{R_G}\right)\right]$$

This is written in a loop-gain analysis format where the errors arising from a non-infinite open-loop gain are shown in the denominator. If $Z_{(S)}$ were infinite over all frequencies, the denominator of Equation 1 would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 1 determines the frequency response. Equation 2 shows this as the loop-gain equation.

$$\frac{Z_{(S)}}{R_F + R_I\, NG} = \text{Loop Gain} \qquad (2)$$

If $20 \cdot \log(R_F + NG \cdot R_I)$ were drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, $Z_{(S)}$ rolls off to equal the denominator of Equation 2 at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier's closed-loop frequency response given by Equation 1 will start to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage feedback op amp. The difference here is that the total impedance in the denominator of Equation 2 may be controlled somewhat separately from the desired signal gain (or NG).

The OPA4684 is internally compensated to give a maximally flat frequency response for R_F = 800Ω at NG = 2 on ±5V supplies. That optimum value goes to 1.0kΩ on a single +5V supply. Normally, with a current-feedback amplifier, it is

possible to adjust the feedback resistor to hold this bandwidth up as the gain is increased. The CFB_{PLUS} architecture has reduced the contribution of the inverting input impedance to provide exceptional bandwidth to higher gains without adjusting the feedback resistor value. The Typical Characteristics show the small-signal bandwidth over gain with a fixed feedback resistor.

Putting a closed-loop buffer between the noninverting and inverting inputs does bring some added considerations. Since the voltage at the inverting output node is now the output of a locally closed-loop buffer, parasitic external capacitance on this node can cause frequency response peaking for the transfer function from the noninverting input voltage to the inverting node voltage. While it is always important to keep the inverting node capacitance low for any current-feedback op amp, it is critically important for the OPA4684. External layout capacitance in excess of 2pF will start to peak the frequency response. This peaking can be easily reduced by then increasing the feedback resistor value—but it is preferable, from a noise and dynamic range standpoint, to keep that capacitance low, allowing a close to nominal 800Ω feedback resistor for flat frequency response. Very high parasitic capacitance values on the inverting node (> 5pF) can possibly cause input stage oscillation that cannot be filtered by a feedback element adjustment.

At very high gains, 2nd-order effects in the inverting output impedance cause the overall response to peak up. If desired, it is possible to retain a flat frequency response at higher gains by adjusting the feedback resistor to higher values as the gain is increased. Since the exact value of feedback that will give a flat frequency response depends strongly in inverting and output node parasitic capacitance values, it is best to experiment in the specific board with increasing values until the desired flatness (or pulse response shape) is obtained. In general, increasing R_F (and then adjusting R_G to the desired gain) will move towards flattening the response, while decreasing it will extend the bandwidth at the cost of some peaking.

OUTPUT CURRENT AND VOLTAGE

The OPA4684 provides output voltage and current capabilities that can support the needs of driving doubly-terminated 50Ω lines. For a 100Ω load at the gain of +2, (see Figure 1), the total load is the parallel combination of the 100Ω load and the 1.6kΩ total feedback network impedance. This 94Ω load will require no more than 40mA output current to support the ±3.8V minimum output voltage swing specified for 100Ω loads. This is well under the specified minimum +110mA/–90mA output current specifications over the full temperature range.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I product, which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* curve in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA4684's output drive capabilities. Superimposing resistor load lines onto the plot shows the available output voltage and current for specific loads.

The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristic tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem since most applications include a series-matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to a power-supply pin will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small-series resistor in the power-supply leads. This will, under heavy output loads, reduce the available output voltage swing. A 5Ω series resistor in each power-supply lead will limit the internal power dissipation to less than 1W for an output short-circuit while decreasing the available output voltage swing only 0.25V for up to 50mA desired load currents. This slight drop in available swing is more if multiple channels are driving heavy loads simultaneously. Always place the 0.1µF power-supply decoupling capacitors after these supply current limiting resistors, directly on the supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA4684 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S *vs* C_{LOAD} and the resulting frequency response at the load. The 1kΩ resistor shown in parallel with the load capacitor is a measurement path and may be omitted. Parasitic capacitive loads greater than 5pF can begin to degrade the performance of the OPA4684. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA4684 output pin (see the *Board Layout Guidelines* section).

DISTORTION PERFORMANCE

The OPA4684 provides very low distortion in a low-power part. The CFB_{PLUS} architecture also gives two significant areas of distortion improvement. First, in operating regions where the 2nd-harmonic distortion due to output stage nonlinearities is very low (frequencies < 1MHz, low output swings into light loads), the linearization at the inverting node provided by the CFB_{PLUS} design gives 2nd-harmonic distortions that extend into the –90dBc region. Previous current-feedback amplifiers have been limited to approximately –85dBc due to the nonlinearities at the inverting input. The second area of distortion improvement comes in a distortion performance that is largely gain independent. To the extent that the distortion at a particular output power is output stage dependent, 3rd-harmonics particularly, and to a lesser extent 2nd-harmonic distortion, is constant as the gain is increased. This is due to the constant loop gain versus signal gain provided by the CFB_{PLUS} design. As shown in the Typical Characteristic curves, while the 3rd-harmonic is constant with gain, the 2nd-harmonic degrades at higher gains. This is largely due to board parasitic issues. Slightly imbalanced load return currents will couple into the gain resistor to cause a portion of the 2nd-harmonic distortion. At high gains, this imbalance has more gain to the output giving reduced 2nd-harmonic distortion. Differential stages using two of the channels together can reduce this 2nd-harmonic issue enormously getting back to an essentially gain independent distortion.

Relative to alternative amplifiers with < 2mA/ch supply current, the OPA4684 holds much lower distortion at higher frequencies (> 5MHz) and to higher gains. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a lower 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1) this is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. A low-power part like the OPA4684 includes quiescent boost circuits to provide the large-signal bandwidth in the Electrical Characteristics. These act to increase the bias in a very linear fashion only when high slew rate or output power are required. This also acts to actually reduce the distortion slightly at higher output power levels. The Typical Characteristic curves show the 2nd-harmonic holding constant from $500mV_{PP}$ to $5V_{PP}$ outputs while the 3rd-harmonics actually decrease with increasing output power.

The OPA4684 has an extremely low 3rd-order harmonic distortion, particularly for light loads and at lower frequencies. This also gives low 2-tone, 3rd-order intermodulation distortion as shown in the Typical Characteristic curves. Since the OPA4684 includes internal power boost circuits to retain good full-power performance at high frequencies and outputs, it does not show a classical 2-tone, 3rd-order intermodulation intercept characteristic. Instead, it holds relatively low and constant 3rd-order intermodulation spurious levels over power. The Typical Characteristic curves show this spurious level as a dBc below the carrier at fixed center frequencies swept over single-tone power at a matched 50Ω load. These spurious levels drop significantly (> 12dB) for loads lighter than the 100Ω used in the *2-Tone, 3rd-Order Intermodulation Distortion* curve. Converter inputs, for instance, will see < –82dBc 3rd-order spurious to 10MHz for full-scale inputs. For even lower 3rd-order intermodulation distortion to much higher frequencies, consider the OPA2691 dual or OPA691 and OPA695 single-channel current-feedback amplifiers.

NOISE PERFORMANCE

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA4684 offers an excellent balance between voltage and current noise terms to achieve low output noise in a low-power amplifier. The inverting current noise (17pA/$\sqrt{Hz}$) is comparable to most other current-feedback op amps while the input voltage noise (3.7nV/$\sqrt{Hz}$) is lower than any unity-gain stable, comparable slew rate, voltage-feedback op amp. This low input voltage noise was achieved at the price of higher noninverting input current noise (9.4pA/$\sqrt{Hz}$). As long as the AC source impedance looking out of the noninverting node is less than 200Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 15 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

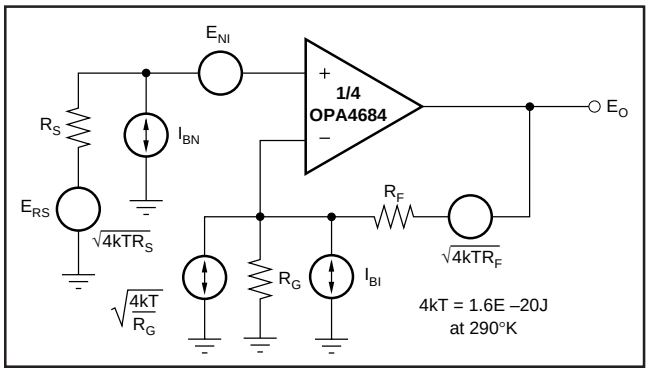


FIGURE 15. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 3 shows the general form for the output noise voltage using the terms presented in Figure 12.

(3)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)G_N^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FG_N}$$

Dividing this expression by the noise gain ($G_N = (1+R_F/R_G)$) will give the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 4.

(4)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{G_N}\right)^2 + \frac{4kTR_F}{G_N}}$$

Evaluating these two equations for the OPA4684 circuit and component values presented in Figure 1 will give a total output spot noise voltage of 16.3nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 8.1nV/$\sqrt{Hz}$. This total input referred spot noise voltage is higher than the 3.7nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. As the gain is increased, this fixed output noise power term contributes less to the total output noise and the total input referred voltage noise given by Equation 3 will approach just the 3.7nV/$\sqrt{Hz}$ of the op amp itself. For example, going to a gain of +20 in the circuit of Figure 1, adjusting only the gain resistor to 42.1Ω, will give a total input referred noise of 3.9nV/$\sqrt{Hz}$. A more complete description of op amp noise analysis can be found in the Texas Instruments application note, AB-103, *Noise Analysis for High Speed Op Amps* (SBOA066), available for download at www.ti.com.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA4684 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high slew rate voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$\pm(NG \bullet V_{OS(MAX)}) + (I_{BN} \bullet R_S/2 \bullet NG) \pm (I_{BI} \bullet R_F)$

where NG = noninverting signal gain

$= \pm(2 \bullet 4.0mV) \pm (13\mu A \bullet 25\Omega \bullet 2) \pm (800\Omega \bullet 17\mu A)$

$= \pm 8mV + 0.65mV \pm 13.6mV$

$= \pm 22.3mV$

While the last term, the inverting bias current error, is dominant in this low-gain circuit, the input offset voltage will become the dominant DC error term as the gain exceeds 5V/V. Where improved DC precision is required in a high-speed amplifier, consider the OPA656 single and OPA4820 quad voltage-feedback amplifiers.

THERMAL ANALYSIS

The OPA4684 will not require external heatsinking or airflow most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, P_{DL} would be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an absolute worst-case example, compute the maximum T_J using an OPA4684IPW (TSSOP-14 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C with all channels driving a grounded 100Ω load to $2.5V_{DC}$.

$P_D = 10V \bullet 7.8mA + 4 \bullet (5^2/(4 \bullet (100\Omega \,||\, 1.6k\Omega))) = 144mW$

Maximum $T_J = +85°C + (0.144W \bullet 110°C/W) = 101°C$.

This maximum operating junction temperature is well below most system level targets. Most applications will be lower than this since an absolute worst-case output stage power was assumed in this calculation with all four channels running maximum output power simultaneously.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA4684 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.01µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) **Careful selection and placement of external components will preserve the high-frequency performance of the OPA4684.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. The quad amplifier pinout allows each output and inverting input to be connected by the feedback element with virtually no trace length. Other network components, such as noninverting input termination resistors, should also be placed close to the package. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing its value will reduce the peaking at higher gains, while decreasing it will give a more peaked frequency response at lower gains. The 800Ω feedback resistor used in the Typical Characteristics at a gain of +2 on ±5V supplies is a good starting point for design. Note that a 800Ω feedback resistor, rather than a direct short, is required for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S *vs* C_{LOAD}. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA4684 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact a higher impedance environment will improve distortion; see the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA4684 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA4684 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S *vs* C_{LOAD}. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) **Socketing a high-speed part like the OPA4684 is not recommended**. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA4684 onto the board.

INPUT AND ESD PROTECTION

The OPA4684 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table where an absolute maximum 13V across the supply pins is reported. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 16.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA4684), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

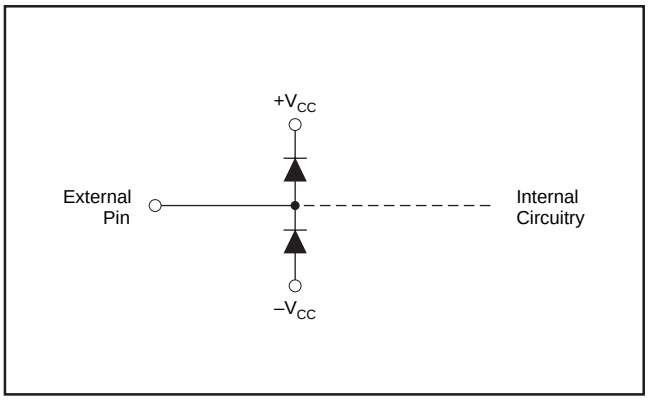


FIGURE 16. Internal ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
7/08	G	2	Abs Max Ratings	Changed Storage Temperature Range from –40°C to +125C to –65°C to +125C.
		3, 4	Electrical Characteristics, Power Supply	Added minimum supply voltage. Changed min and max quiescent current values from total to per channel.
6/06	F	17	Design-In Tools	Demonstration fixture numbers changed.
		24	Applications Information	Added Revision History table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4684ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4684	Samples
OPA4684IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4684	Samples
OPA4684IPWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4684	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA4684 :

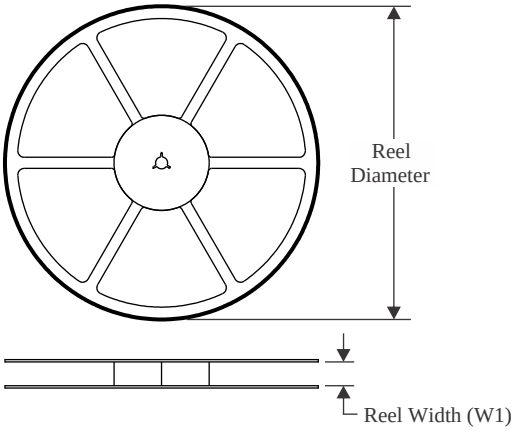
- Military : OPA4684M

NOTE: Qualified Version Definitions:

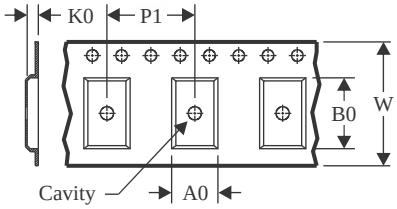
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

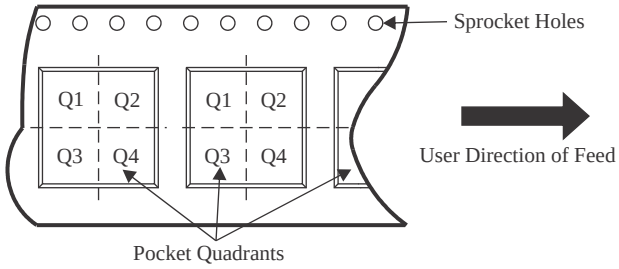


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

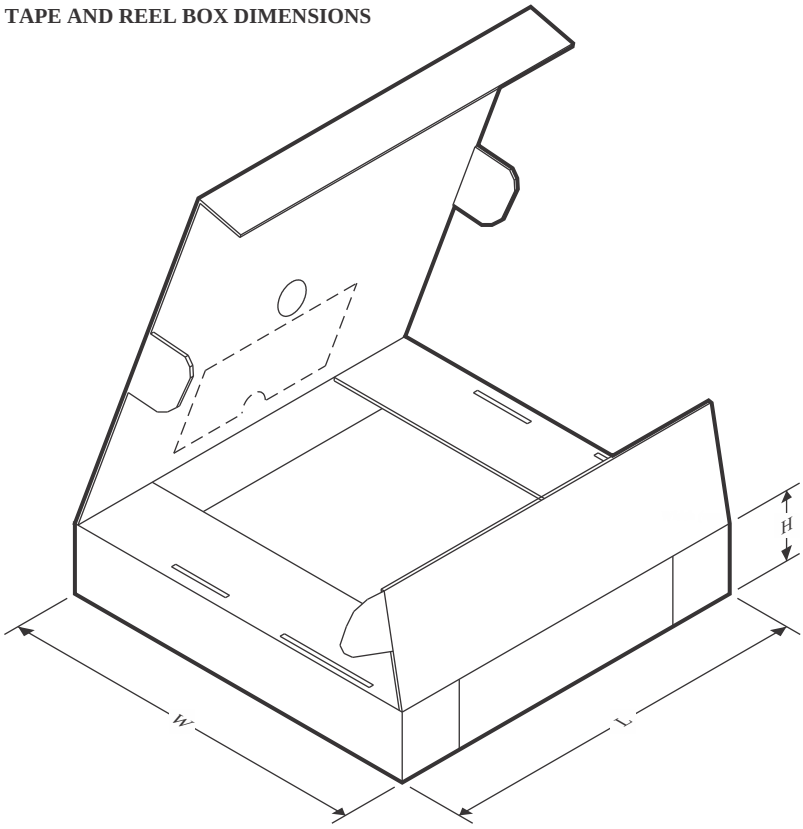
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4684IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4684IPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

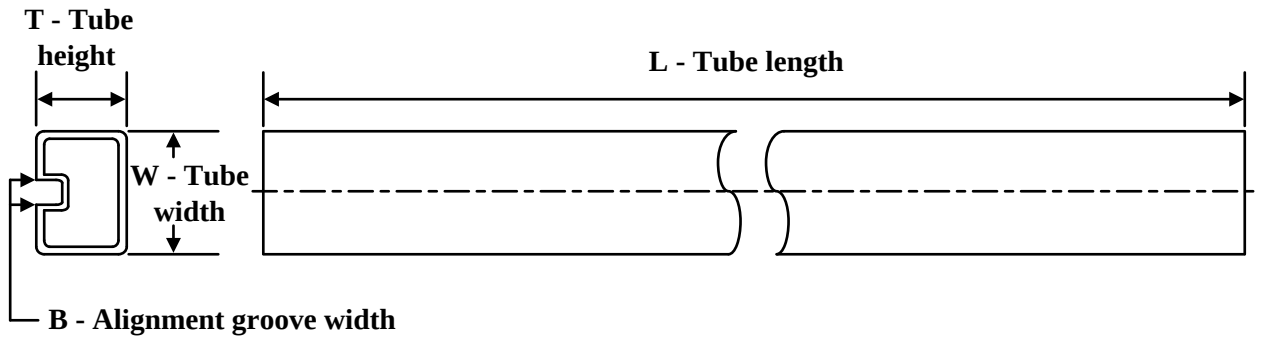
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4684IDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4684IPWT	TSSOP	PW	14	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

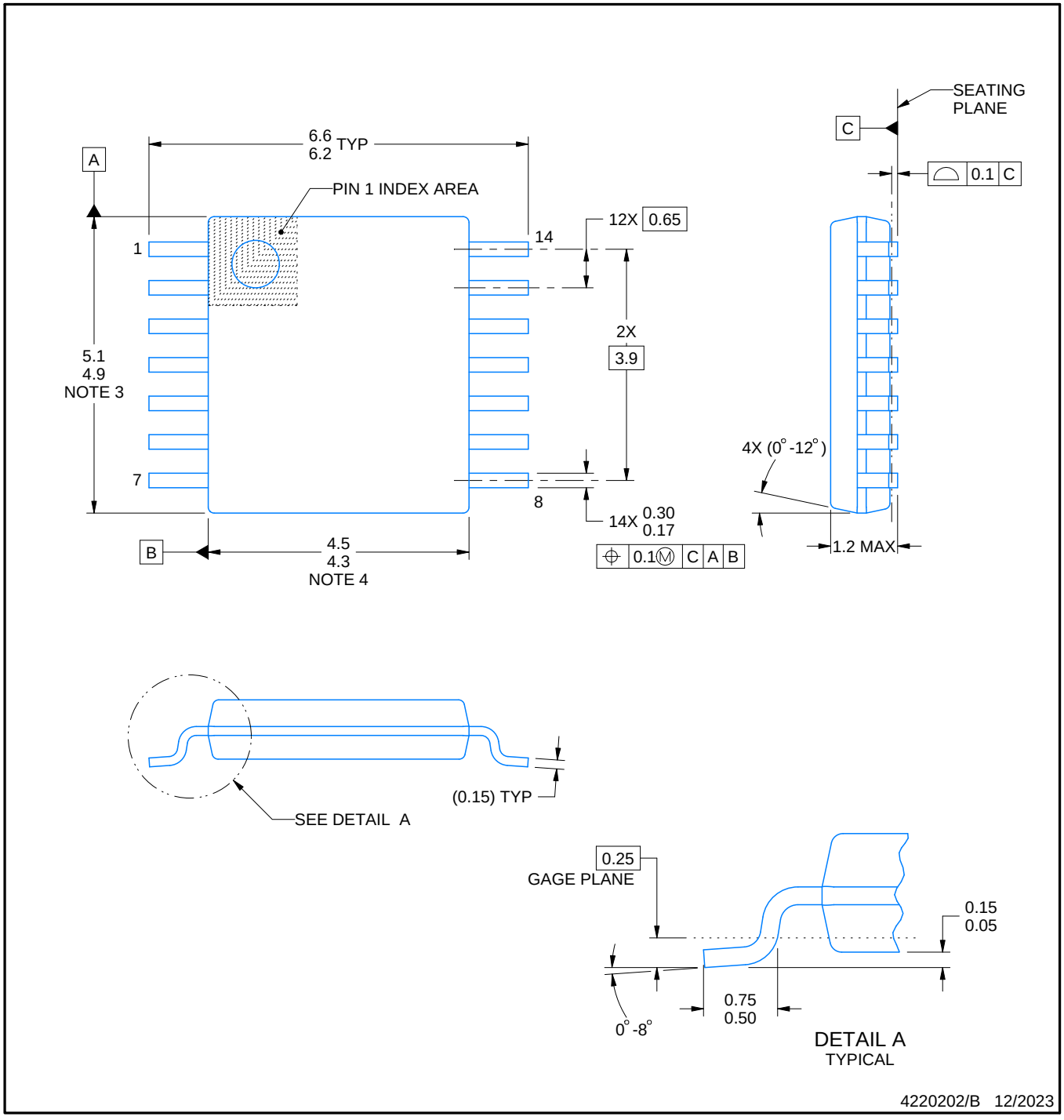
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA4684ID	D	SOIC	14	50	506.6	8	3940	4.32

PACKAGE OUTLINE

PW0014A

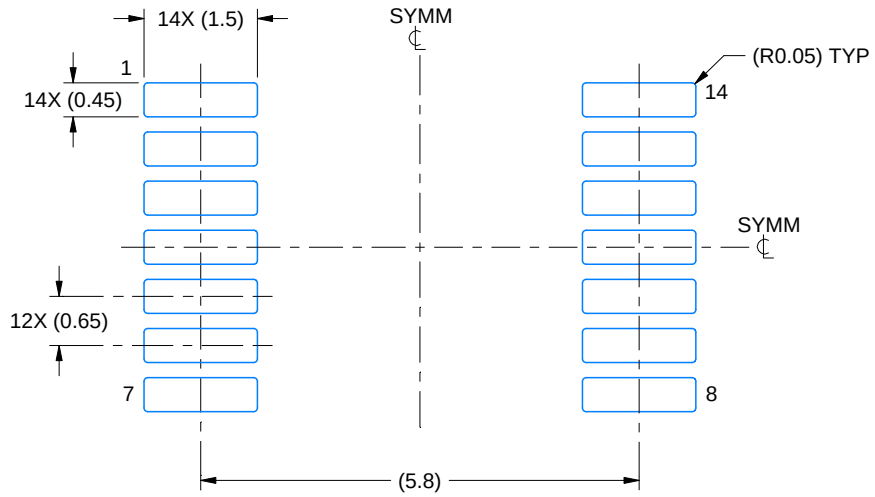
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

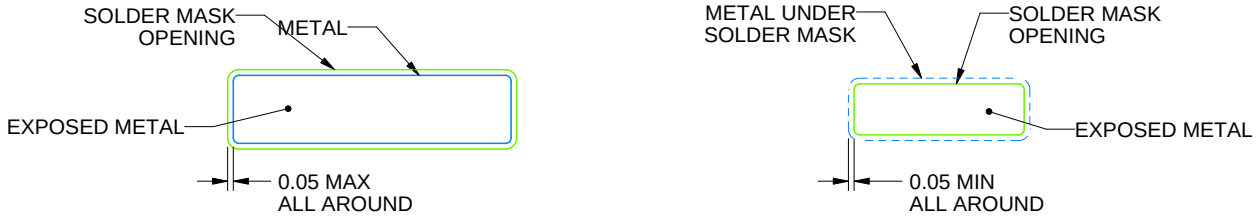


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

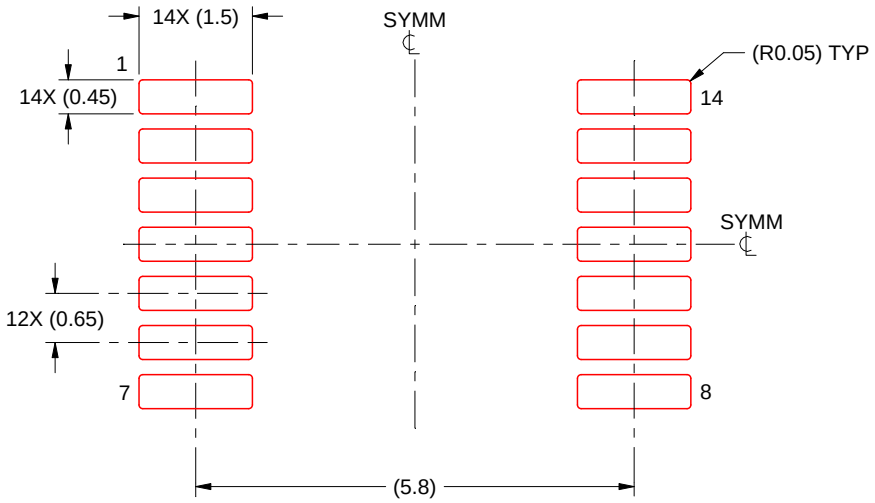


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

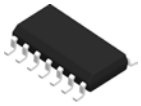


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

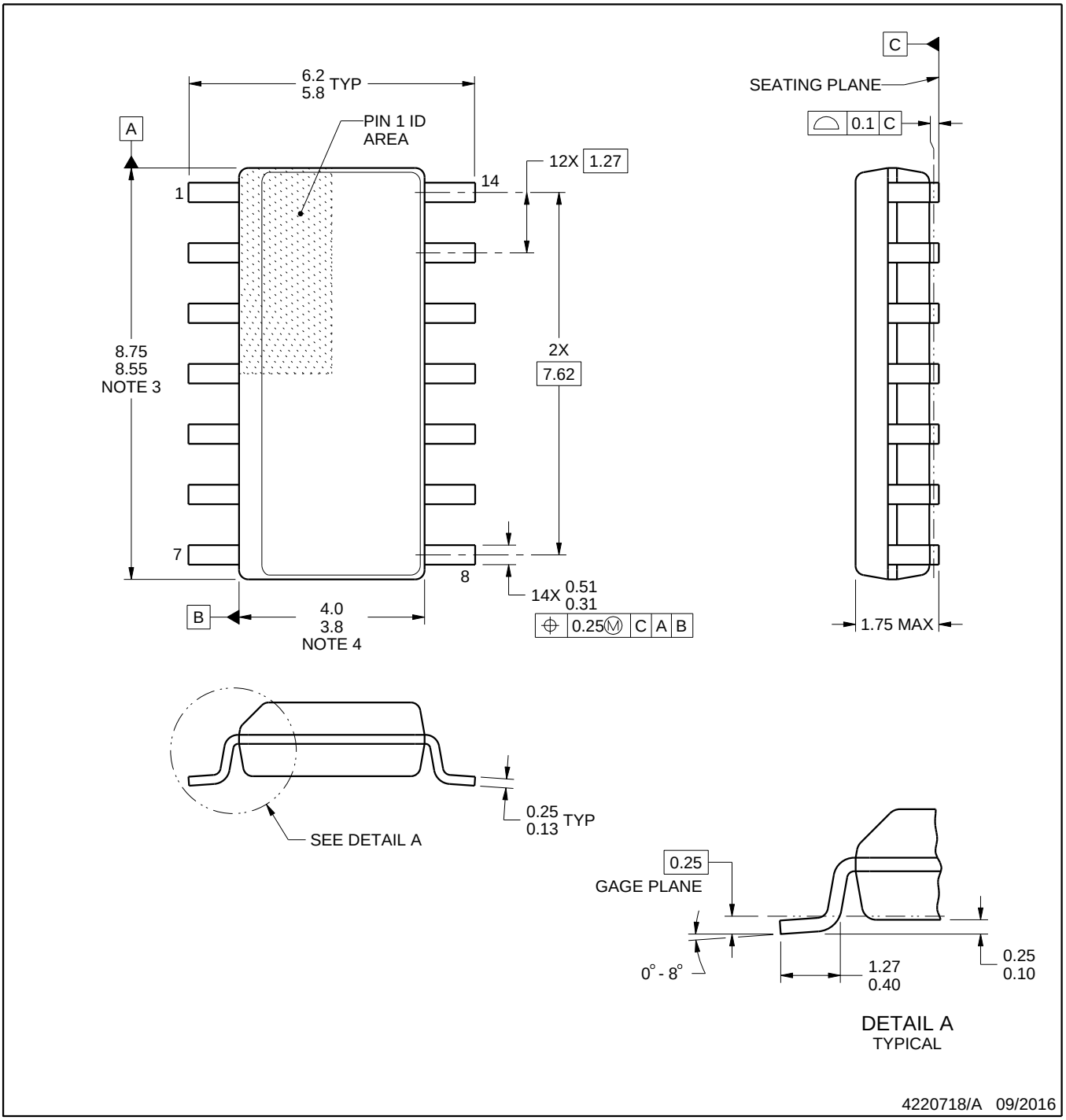


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

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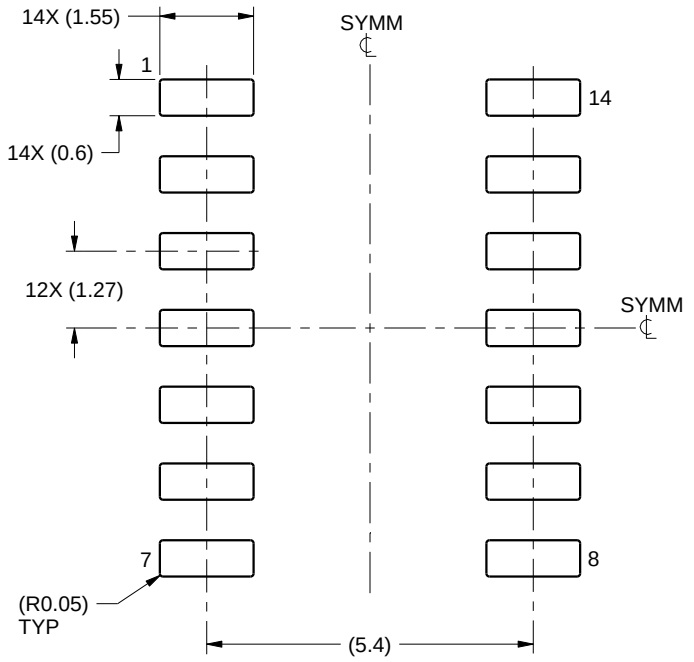
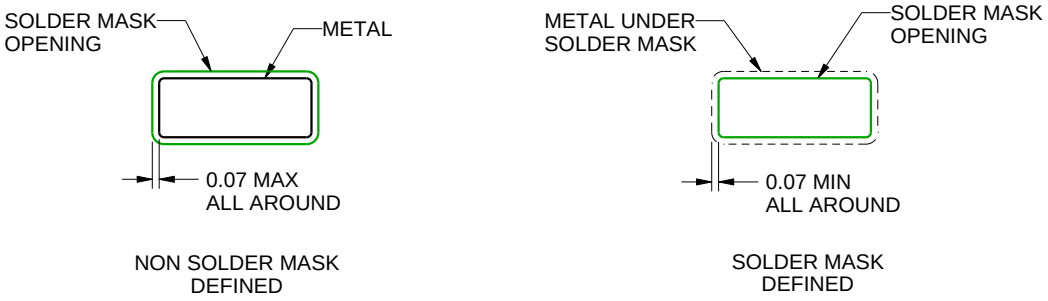
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

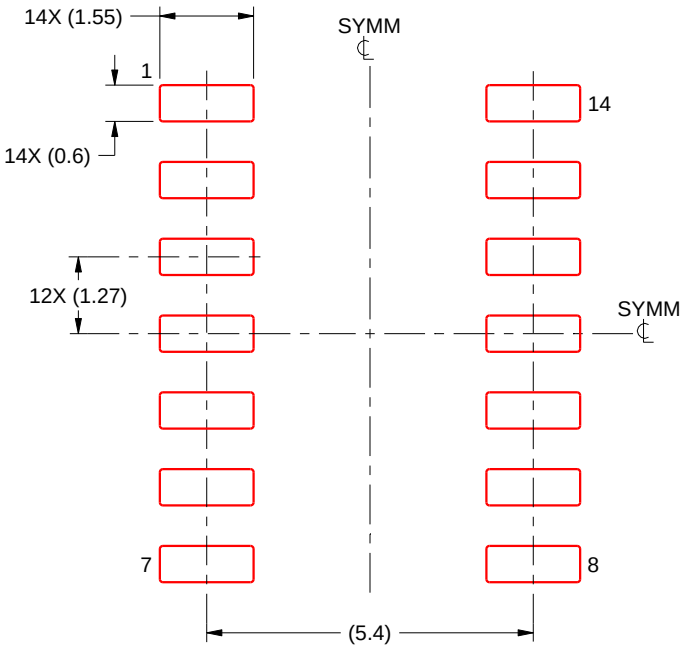
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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