OPAx596 High-Voltage (85V), Low-Power (420µA), High-Slew Rate (100V/µs) Power Amplifier With Mux-Friendly Inputs

1 Features

- High slew rate: 100V/µs
- Low power consumption: 420µA
- Wide power-supply range:
  - ±4V to ±42.5V
  - 8V to 85V
- Mux-friendly inputs
- Rail-to-rail input and out
- Gain bandwidth: 3.75MHz
- Low noise: 12.8nV/√Hz
- Low input bias current: 5pA
- High-output load drive: I_O ±30mA
- Wide temperature range: –40°C to +125°C
- Industry-standard small packages:
  - DBV (5-pin SOT-23)
  - DGK (8-pin VSSOP)

2 Applications

- Semiconductor test
- LCD test
- Programmable dc power supply
- CT and PET scanner
- Source measurement unit (SMU)
- Optical module
- Lab and field Instrumentation

3 Description

The OPA596 and OPA2596 (OPAx596) are high-voltage (85V), high slew rate (100V/µs), micro-power (420µA), unity-gain stable operational amplifiers (op amps).

The OPAx596 enable the next generation of high-voltage systems, such as output load drivers in semiconductor test and digital power supplies by increasing the output voltage of the system though high-gain configurations. Low power consumption and industry-standard small packages allow the device to be used in high-density systems that are size constrained, while reducing the thermal management requirements for the system.

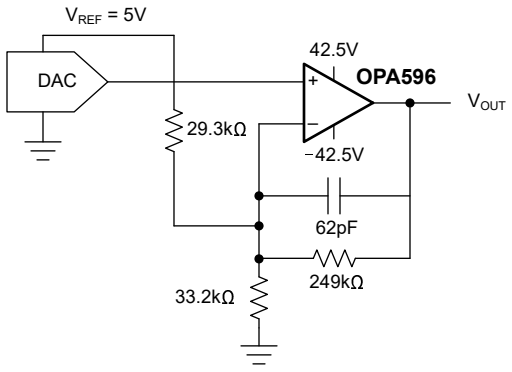
Through proprietary design techniques, the OPAx596 are capable of a very high slew rate with minimal power consumption to improve large-signal settling time and maximize the effective large-signal bandwidth. These devices also offers mux-friendly inputs that enable large differential voltage (up to 85V) and help improve settling behavior when compared to traditional inputs in multiplexed applications.

The OPAx596 are available in industry-standard packages and operates across the temperature range of –40°C to +125°C.

Device Information

PART NUMBER	CHANNELS	PACKAGE(1)
OPA596	Single	DBV (SOT-23, 5)
OPA2596 (2)	Dual	DGK (VSSOP, 8)

(1) For more information, see Section 10.
(2) Preview information.



DAC Output Buffer With Gain

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4 Pin Configuration and Functions

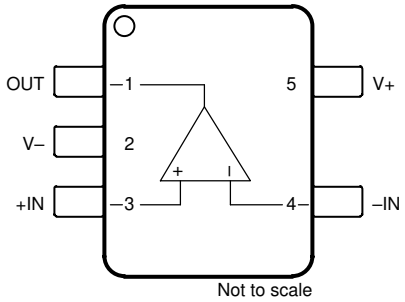

Figure 4-1. OPA596 DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions: OPA596

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	4	Input	Inverting input
OUT	1	Output	Output
V+	5	Power	Positive (highest) power supply
V–	2	Power	Negative (lowest) power supply

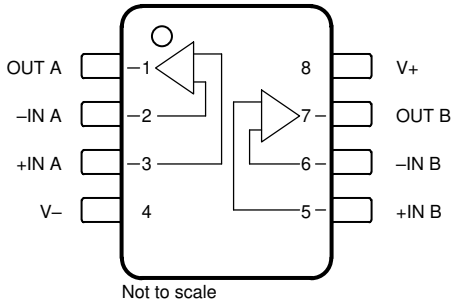

Figure 4-2. OPA2596 DGK Package, 8-Pin VSSOP (Top View)

Table 4-2. Pin Functions: OPA2596

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply		±46.5	V
		Single supply, V_S = (V+) – (V–)		93	
	Signal input pin voltage(2)	Common-mode	(V–) – 0.3	(V+) + 0.3	V
		Differential		(V+) – (V–)	
	Input current, all pins(2)			±10	mA
I_{SC}	Output short circuit(3)			Continuous	
T_J	Junction temperature			150	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
(3) Short-circuit to ground.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Dual supply	±4		±42.5	V
		Single supply	8		85	
T_A	Ambient temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		OPA596 DBV (SOT-23) 5 PINS	OPA2596 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.4	143.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.1	50.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.5	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	42.6	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.2	77.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at V_S = 85V (±42.5V), T_A = 25°C, R_L = 10kΩ to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.2	±1	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±1	±6	µV/°C
PSRR	Power supply rejection ratio	8V ≤ V_S ≤ 85V			±1	±5	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±10	pA
		T_A = –40°C to +85°C				±50	
		T_A = –40°C to +125°C				±1	nA
I_{OS}	Input offset current				±5	±10	pA
		T_A = –40°C to +85°C				±50	
		T_A = –40°C to +125°C				±1	nA
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1.4		μV_{PP}
e_n	Input voltage noise density	f = 100Hz			17.8		nV/√Hz
		f = 1kHz			12.9		
		f = 10kHz			12.8		
i_n	Current noise density	f = 1kHz			10		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	Linear operation		(V–) – 0.1		(V+) – 3.5	V
CMRR	Common-mode rejection	(V–) ≤ V_{CM} ≤ (V+) – 3.5V		126	140		dB
			T_A = –40°C to +125°C	124	140		
INPUT IMPEDANCE							
	Differential				100 || 2.5		MΩ || pF
	Common-mode				10 || 5.5		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 1V < V_O < (V+) – 1.5V, R_L = 10kΩ to mid-supply		134	140		dB
			T_A = –40°C to +125°C	120	140		
		(V–) + 3V < V_O < (V+) – 3.5V, R_L = 2kΩ to mid-supply			126		
			T_A = –40°C to +125°C		126		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = 1			2.25		MHz
		G = 10			3		
		G = 100			3.75		
SR	Slew rate	G = ±1, V_O = 70V step			100		V/µs
t_S	Settling time	To ±0.01%, G = –1, V_O = 10V step, C_L = 100pF			2		µs
	Overload recovery	G = –1			115		ns
THD+N	Total harmonic distortion + noise	G = +1, V_O = 70V_{PP}, f = 1kHz	R_L = 10kΩ		–102		dB
			R_L = 2kΩ		–95		

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5.5 Electrical Characteristics (continued)

at V_S = 85V (±42.5V), T_A = 25°C, R_L = 10kΩ to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing from rail	No load			12	50	mV
		R_L = 10kΩ to mid-supply			100	435	
		R_L = 2kΩ to mid-supply			500	2.05	V
I_{SC}	Output current				±30		mA
C_{LOAD}	Capacitive load drive				1		nF
Z_O	Open-loop output impedance				550		Ω
CURRENT LIMIT							
POWER SUPPLY							
I_Q	Quiescent current	I_O = 0mA			420	490	µA
			T_A = –40°C to +125°C			500	
TEMPERATURE							
	Overtemperature shutdown	Shutdown temperature			185		°C
		Thermal hysteresis			20		

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6 Detailed Description

6.1 Overview

The OPAx596 are low power (420µA), high-slew rate (100V/µs), 85V operational amplifiers (op amps). These op amps uses a proprietary design technique to achieve a very high slew capability with minimal power consumption. The OPAx596 is capable of driving ±30mA of output current and can swing to within 100mV of either power supply rail.

The amplifiers feature state-of-the-art CMOS technology and advanced design features that help achieve outstanding ac performance and enable small package options. The OPAx596 strengths also include 3.75MHz bandwidth, 12.8nV/√Hz noise spectral density, and low input bias current. These features make the OPAx596 an exceptional choice to gain or buffer the output of a digital-to-analog converter (DAC) in digitally programmable power supplies.

6.2 Functional Block Diagram

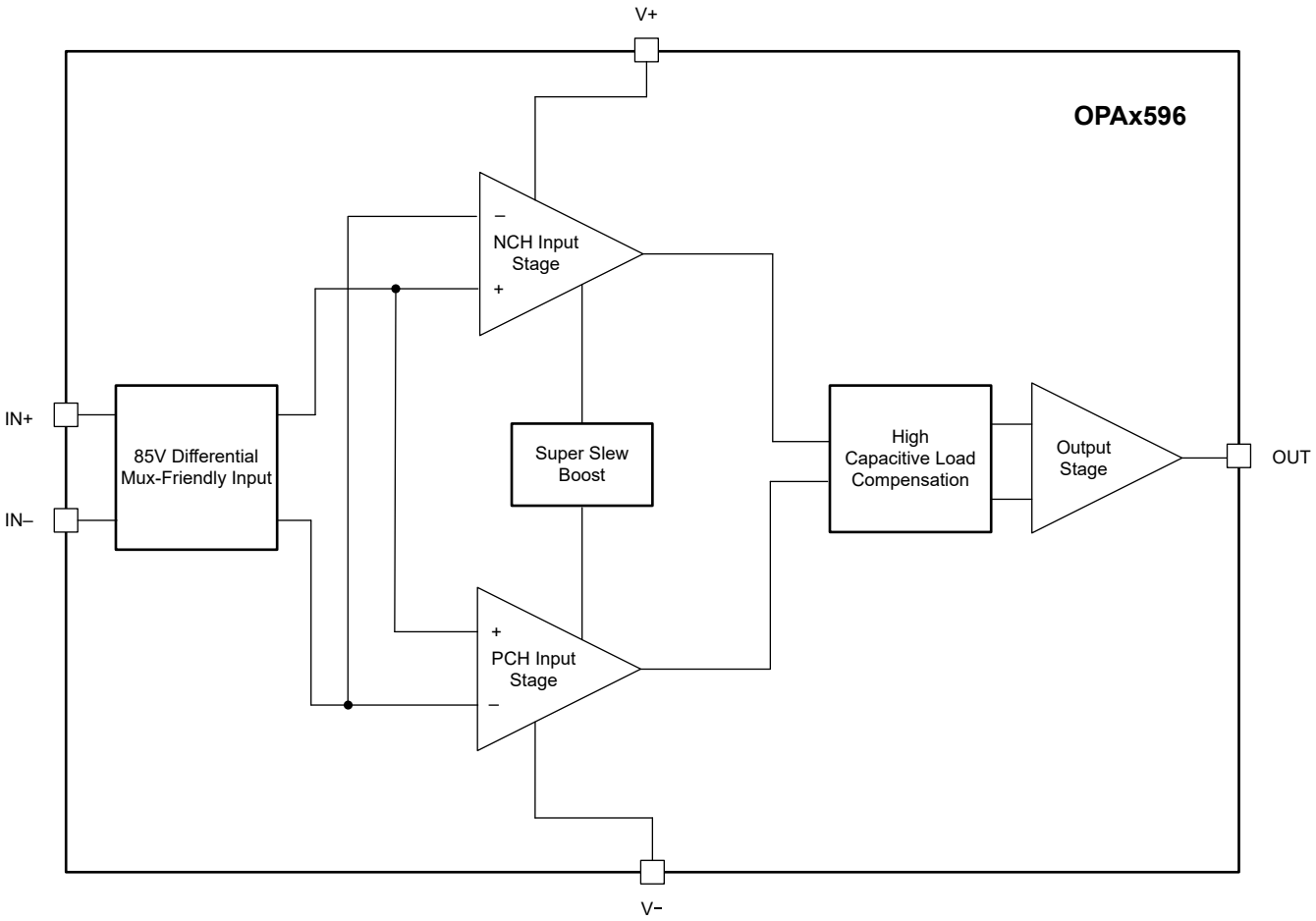

Figure 6-1. Functional Block Diagram

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6.3 Feature Description

6.3.1 Mux-Friendly Inputs

The OPAx596 use a unique input architecture to eliminate the need for input protection diodes but still provide robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 6-2 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 6-3. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current and result in extended settling time.

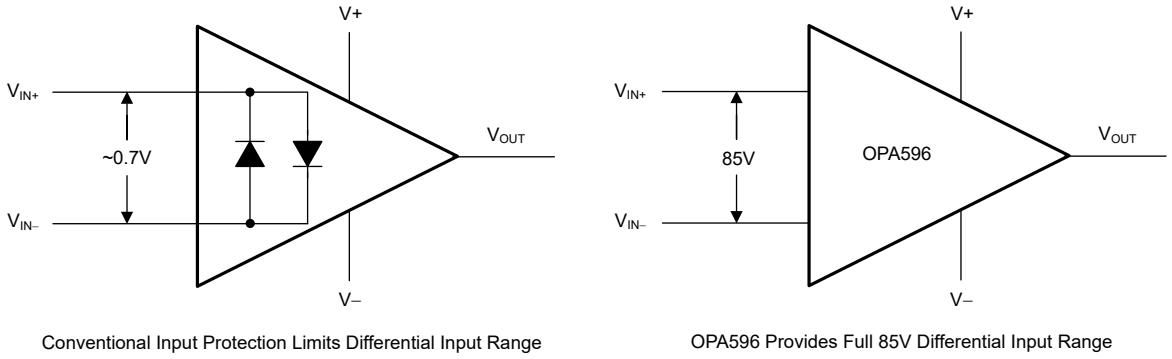

Figure 6-2. OPA596 Input Protection Does Not Limit Differential Input Capability

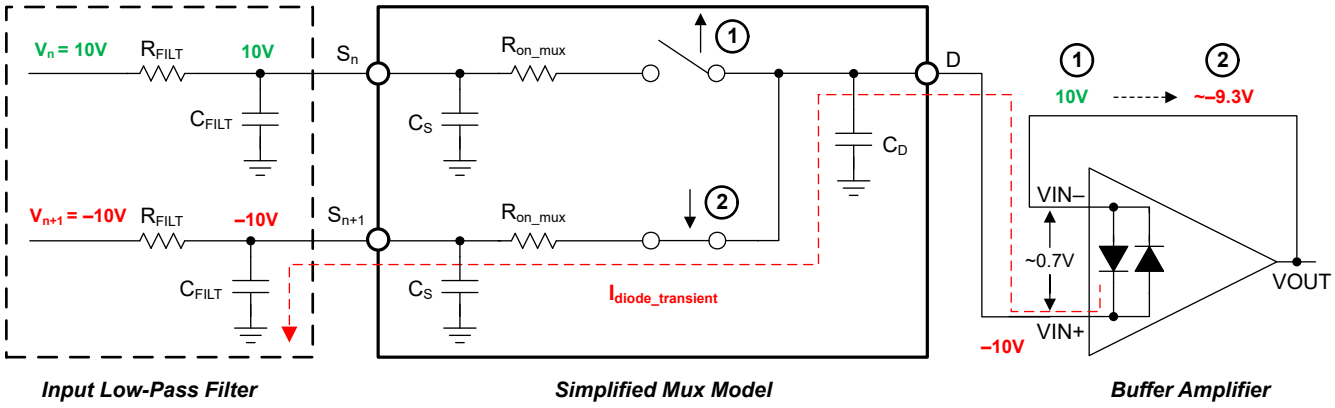

Figure 6-3. Back-to-Back Diodes Create Settling Issues

The OPAx596 feature a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making these devices an excellent choice for multichannel, high-switched, input applications. The OPAx596 tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 85V, making these devices a great choice for use as a comparator or in applications with fast-ramping or switched input signals.

6.3.2 Thermal Protection

The OPAx596 has a thermal protection feature that prevents damage from self heating. When the junction temperature (T_J) reaches approximately 180ºC, the op amp output stage disables. This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive. Thermal protection forces the output to a high-impedance state. The OPAx596 is designed with approximately 30°C of thermal hysteresis and returns to normal operation when the output stage temperature becomes less than approximately 150°C.

This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

6.3.3 Slew Boost

Slew rate is the maximum rate of change of output voltage change with respect to time and is typically specified in units of volts per microsecond, V/µs. The OPAx596 can enter a slew condition when a large, rapid moving signal is applied at the input. While slewing, the op amp enters an open loop condition and significant slew induced distortion can be seen on the output signal.

Equation 1 shows that the slew rate of an op amp is typically determined by the saturation current of the input stage, I_{SAT}, and the compensation capacitor, C_C.

$$SR = \frac{I_{SAT}}{C_C} \tag{1}$$

The slew rate scales with the quiescent current, I_Q, of the op amp. There are several ways that designers have overcome slew rate limitation. For example, decompensation improves slew rate at the expense of stability by lowering C_C. More commonly, modern op amps are equipped with slew boost technology that increases I_{SAT} to overcome the inherent slew rate limitations. Slew boost circuits can vary in implementation, but designers can typically expect about a 4 × improvement over comparable unboosted op amps.

The OPAx596 uses a proprietary design to achieve an unprecedented slew rate to I_Q ratio. The novel slew boost technology in OPAx596 provides a nearly 100 × slew rate improvement over comparable unboosted op amps.

6.3.4 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

6.4 Device Functional Modes

The OPAx596 has a single functional mode and is operational when the power-supply voltage is between 8V (±4V) and 85V (±42.5V).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx596 are low power (420µA), high-slew rate (100V/µs), 85V power operational amplifiers (op amps). These op amps use a proprietary design technique to achieve a very high slewing capability while consuming minimal power. The low power consumption helps reduce heat generation on the board while the output swings near the supply rail. The high slew reduces slew related distortion at the output when dealing with large peak, high frequency signals.

7.2 Typical Applications

7.2.1 Bridge-Connected Piezoelectric Driver

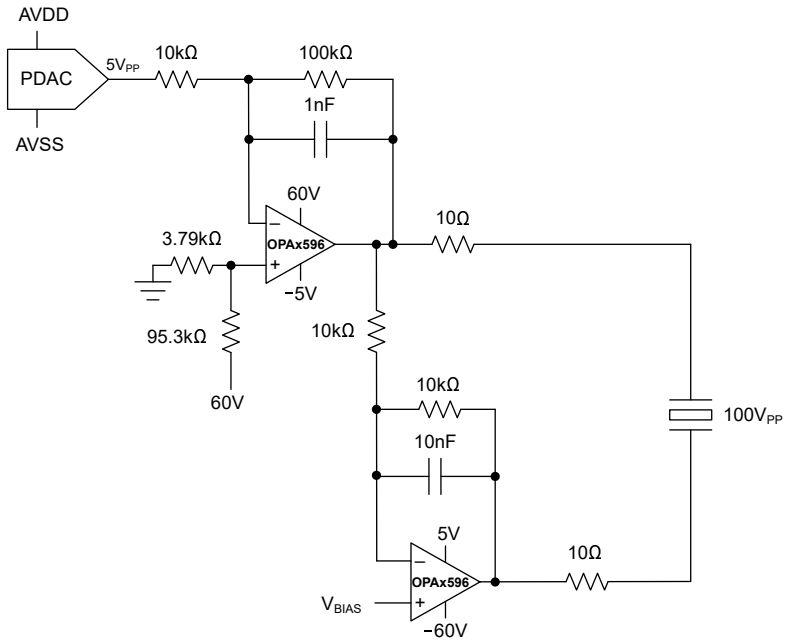


Figure 7-1. 100V_{PP} Piezoelectric Driver With Bridge Connected Load

7.2.1.1 Design Requirements

The OPAx596 is used to drive a piezoelectric actuator with a 100V operating range at a frequency of 100Hz. The large capacitance inherent to the piezoelectric actuator can cause undesired ringing of the driver amplifier. An inaccurate response of the actuator is possible due in part to amplifier instability. Adequate phase margin for a 500nF equivalent load is necessary for a robust driver circuit for the piezoelectric actuator presented here.

Table 7-1. Design Parameters

PARAMETER	VALUE
Positive supply voltage	60V
Negative supply voltage	–5V
Piezoelectric actuator capacitance (1kHz)	500nF
Piezoelectric operating voltage range	0V to 100V
Operating frequency	100Hz
DAC output voltage	$5V_{PP}$

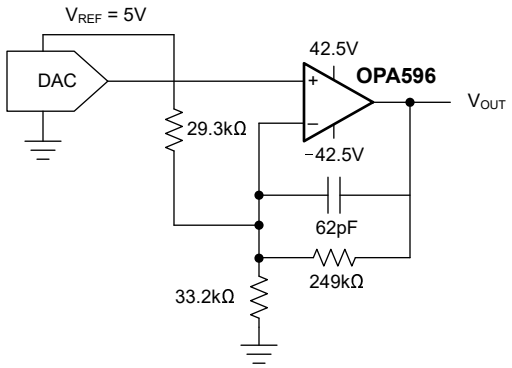
7.2.1.2 Detailed Design Procedure

Piezoelectric actuators offer many benefits over traditional solenoid counterparts. Piezoelectric actuators are more precise, power efficient, and smaller in general when compared to solenoid actuators. One challenge with piezoelectric actuators is that the piezoelectric actuators operate over a very wide voltage range. Driving voltages of more than 60V are not uncommon, and can easily reach hundreds of volts. The OPAx596 operate with a supply voltage of up to 85V.

In this design example, the OPAx596 are used to provide a $100V_{PP}$ signal to control a high-voltage piezoelectric actuator (see also Figure 7-1). The piezoelectric actuator can be modeled as a large capacitor when operated at less than the resonant frequency. The piezoelectric actuator is treated as a floating load driven by two op amps of the OPAx596. The outputs of the op amps are set to be 180° out-of-phase to essentially double the voltage seen by the actuator load.

The signal voltage of the digital-to-analog converter is applied a 10V/V gain by the OPAx596. A simple voltage divider provides a 2.5V reference to level shift the output to create a unipolar driving voltage. An isolation resistor improves phase margin and stability. Add a small 10Ω R_{ISO} at the output of the OPAx596.

7.2.2 DAC Output Gain and Buffer



7.2.2.1 Design Requirements

The OPAx596 is designed for use as an output driver stage with gain and provides a wide, bipolar supply voltage. Combined with the small size of the SOT23-5 package and the low power consumption, these features make this device a great choice for high-channel density systems, such as semiconductor test and manufacturing platforms where many channels are present. In this design example, the OPAx596 is configured for a gain of approximately 17V/V.

Table 7-2. Design Parameters

PARAMETER	VALUE
Supply voltage	−42.5V to +42.5V
Input voltage	0V to 5V
Output voltage	−42.5V to +42.5V
Gain	17V/V

7.2.2.2 Detailed Design Procedure

In this design example, the OPAx596 is configured as both a gain stage and output driver. The input signal to the amplifier is 0V to 5V, and the device is configured with a noninverting gain of 17V/V. The DAC reference voltage of 5V is used as a reference to enable a bipolar output swing. This configuration results in an output voltage of −42.5V to +42.5V. This design example is common in many systems that use a DAC to provide the input signal and require a wide output signal with low output current requirements. The OPAx596 can swing to either rail while remaining within the thermally specified limits. Such systems include test and measurement platforms and power supplies.

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7.2.3 Single-Supply Piezoelectric Driver

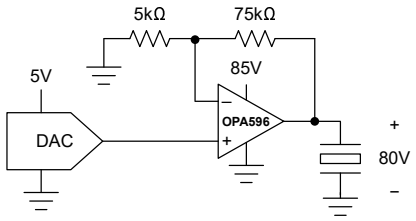

Figure 7-2. 80V Single-Supply Piezoelectric Driver

7.2.4 High-Side Current Sense

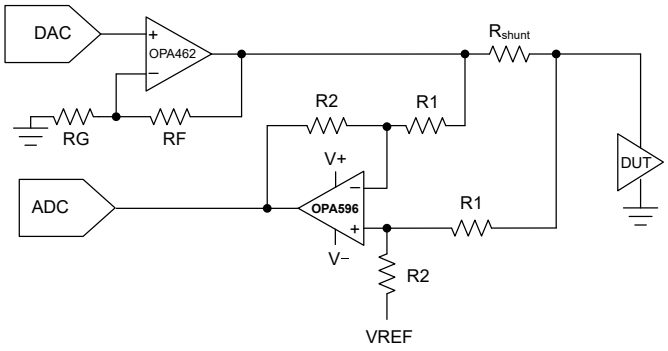

Figure 7-3. 100V High-Side Current Sense

7.2.5 High-Voltage Instrumentation Amplifier

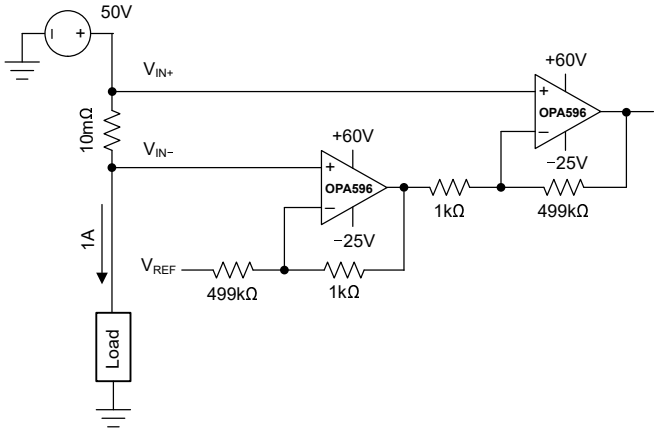

Figure 7-4. High-Voltage Instrumentation Amplifier

7.2.6 Composite Amplifier

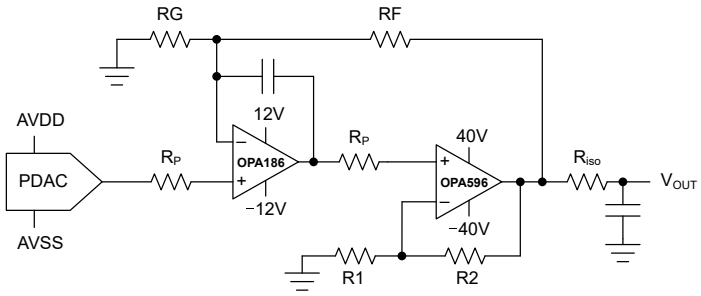

Figure 7-5. High-Precision, High-Voltage Output Composite Amplifier

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7.3 Power Supply Recommendations

The OPAx596 operates from power supplies up to ±42.5V (85V), and as little as ±4V (8V) with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. A power-supply bypass capacitor of at least 0.1µF is required for proper operation. Ensure that the capacitor voltage is rated for high voltage across the full operating temperature range. Some applications do not require an equal positive and negative output voltage swing. The OPAx596 can be powered with asymmetrical supplies.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the op amp and the circuit as a whole. Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground. Place the capacitors as close to the device as possible. A single bypass capacitor from V+ to ground is sufficient for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.1.1 Thermal Considerations

Through normal operation, the op amps can self-heat. Self-heating is a natural increase in the die junction temperature that occurs in every amplifier. This self-heating is a result of several factors, including quiescent power consumption, package thermal resistance, PCB layout, and device operating conditions.

Operate the OPAx596 within the rated junction temperature, T_J, range to avoid thermal shutdown. Use the Equation 2 to determine the estimated T_J

$$T_J = P_D \times \theta J_A + T_A \quad (2)$$

In a quiescent state, P_D is given by the product of the power supply and the quiescent current of the op amp. Equation 3 shows the calculation of T_J for the OPAx596 assuming an 85V power supply is used and an operating temperature of 25°C.

$$T_J = (85V \times 490\mu A) \times 165.4° \frac{C}{W} + 25°C \quad (3)$$

$$T_J = 31.89°C \quad (4)$$

The low power consumption of the OPAx596 causes minimal self-heating even in a small SOT23-5 package as given by Equation 4. In a loaded condition, P_D is equal to addition of the quiescent power, P_{DQ} and the power dissipated by the output stage, P_{DL}. The worst-case condition is given when the output voltage is equal to ½ of either supply rail (assuming symmetrical supplies, V+ and V-). In a worst-case condition, P_{DL} is given by Equation 5.

$$P_{DL} = \frac{(V+)^2}{4 \times R_L} \quad (5)$$

For example, assume the OPAx596 is powered with bipolar ±42.5V power supplies and drives a 5kΩ load, R_L, to ground. The maximum increase in T_J is expected to be about 22°C as given by Equation 6. In this example, to keep the op amp within the *Absolute Maximum Ratings*, operate in T_A well under 128°C to account for different factors.

$$\Delta T_J = (41.7mW + 90.3mW) \times 165.4 \frac{°C}{W} \quad (6)$$

ADVANCE INFORMATION

7.4.2 Layout Example

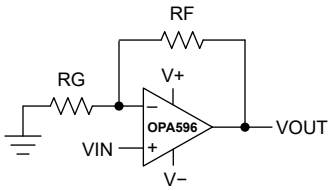

Figure 7-6. Schematic Representation of Noninverting Configuration

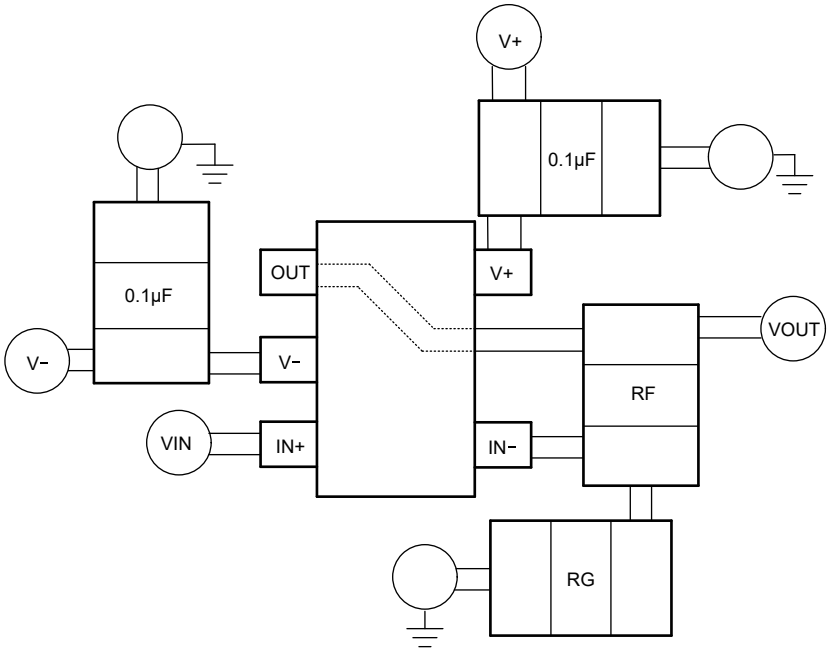

Figure 7-7. Board Layout for Noninverting Configuration of the SOT23-5 Package

ADVANCE INFORMATION

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2024	*	Initial Release

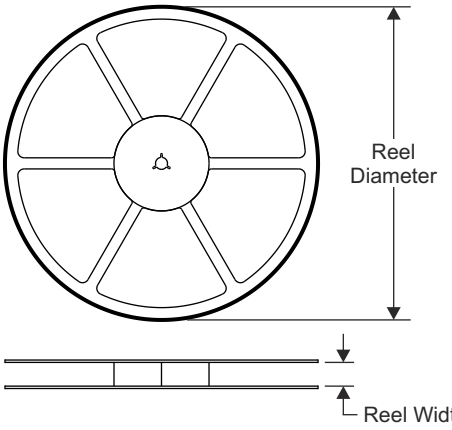
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

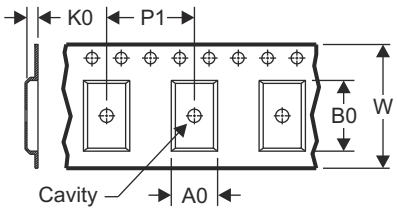
ADVANCE INFORMATION

10.1 Tape and Reel Information

REEL DIMENSIONS

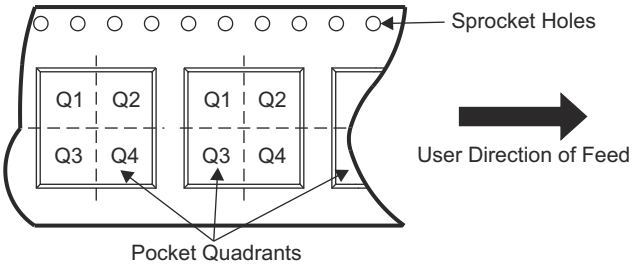


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

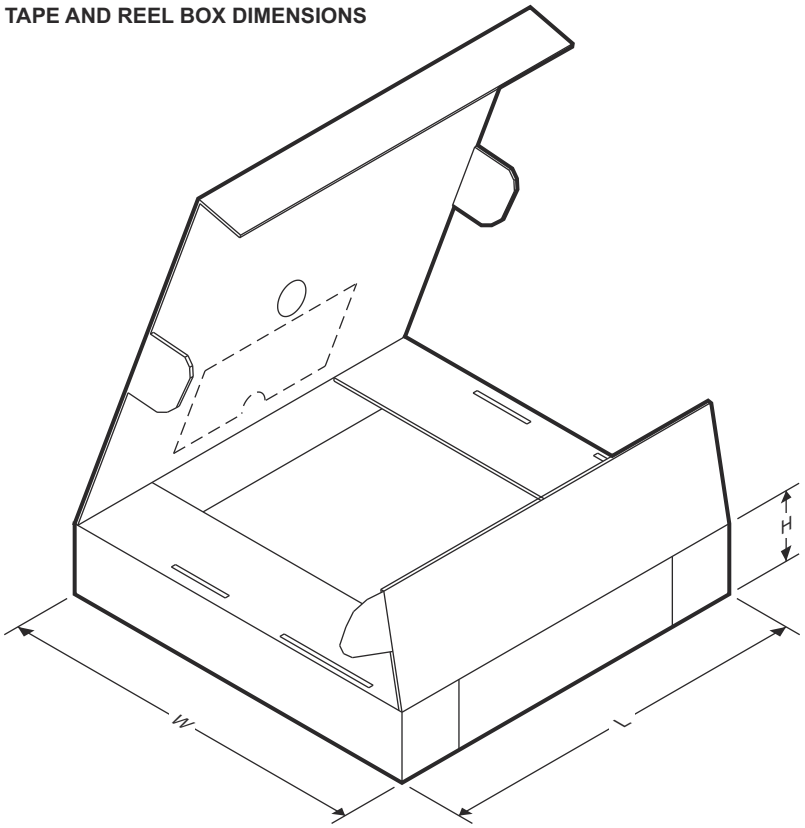
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA596DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA596DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA596DBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA596DBVT	SOT-23	DBV	5	250	223.0	270.0	35.0

ADVANCE INFORMATION

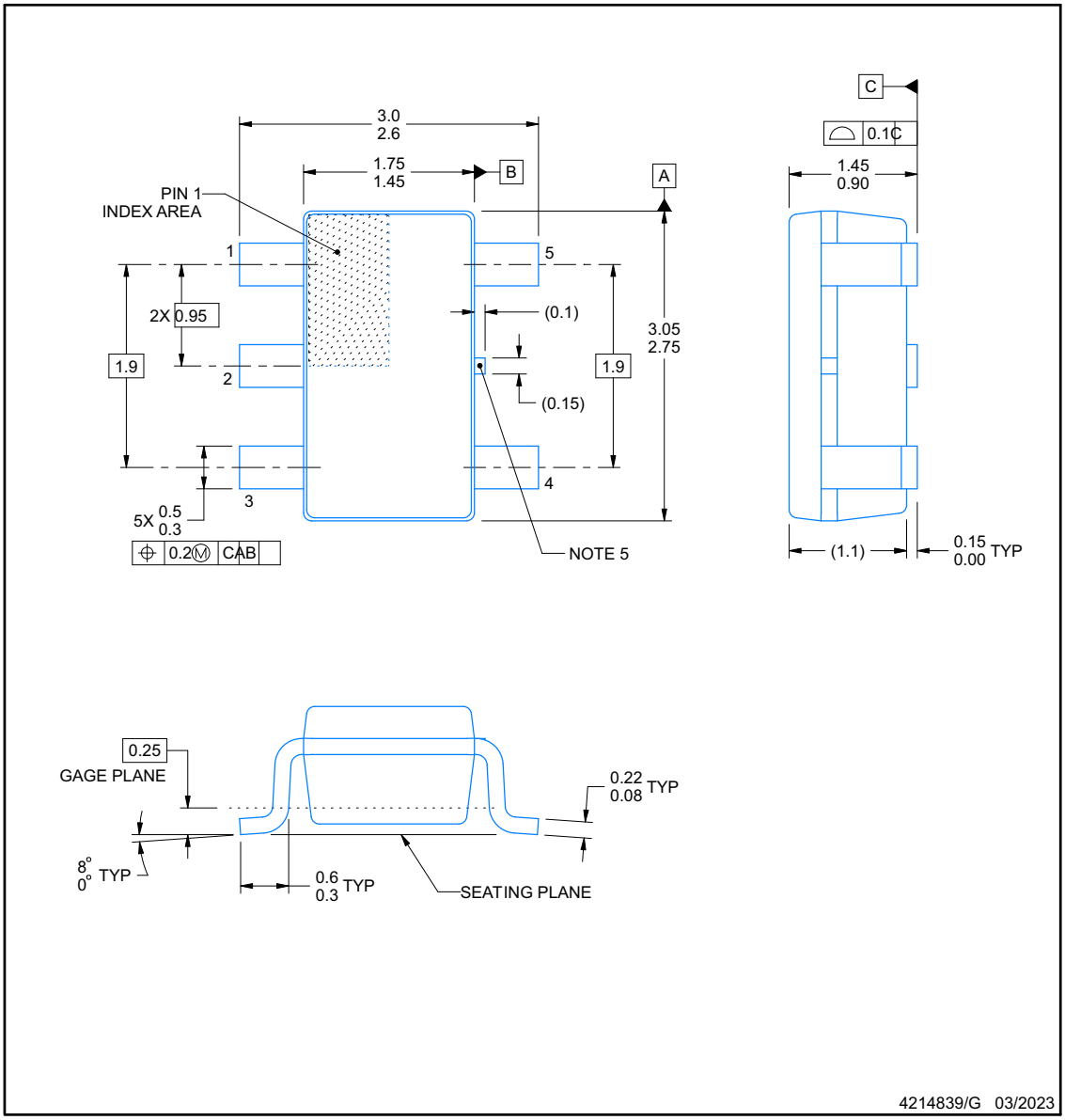
ADVANCE INFORMATION

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

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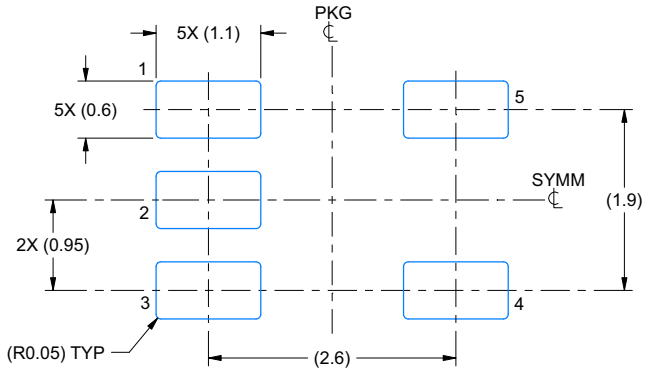
EXAMPLE BOARD LAYOUT

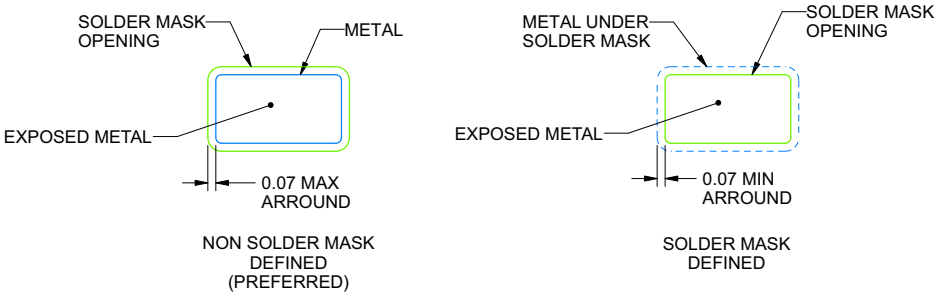
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

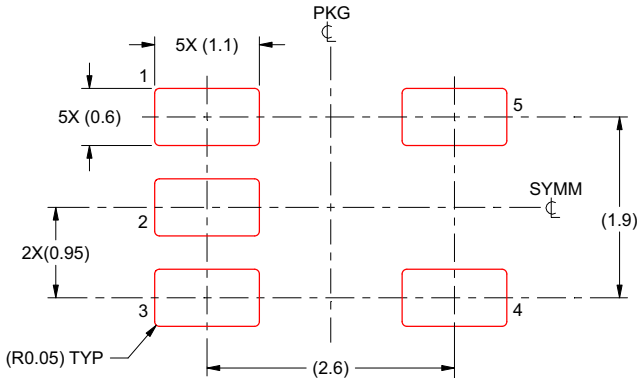
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DBV0005A — SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

NOTES: (continued)

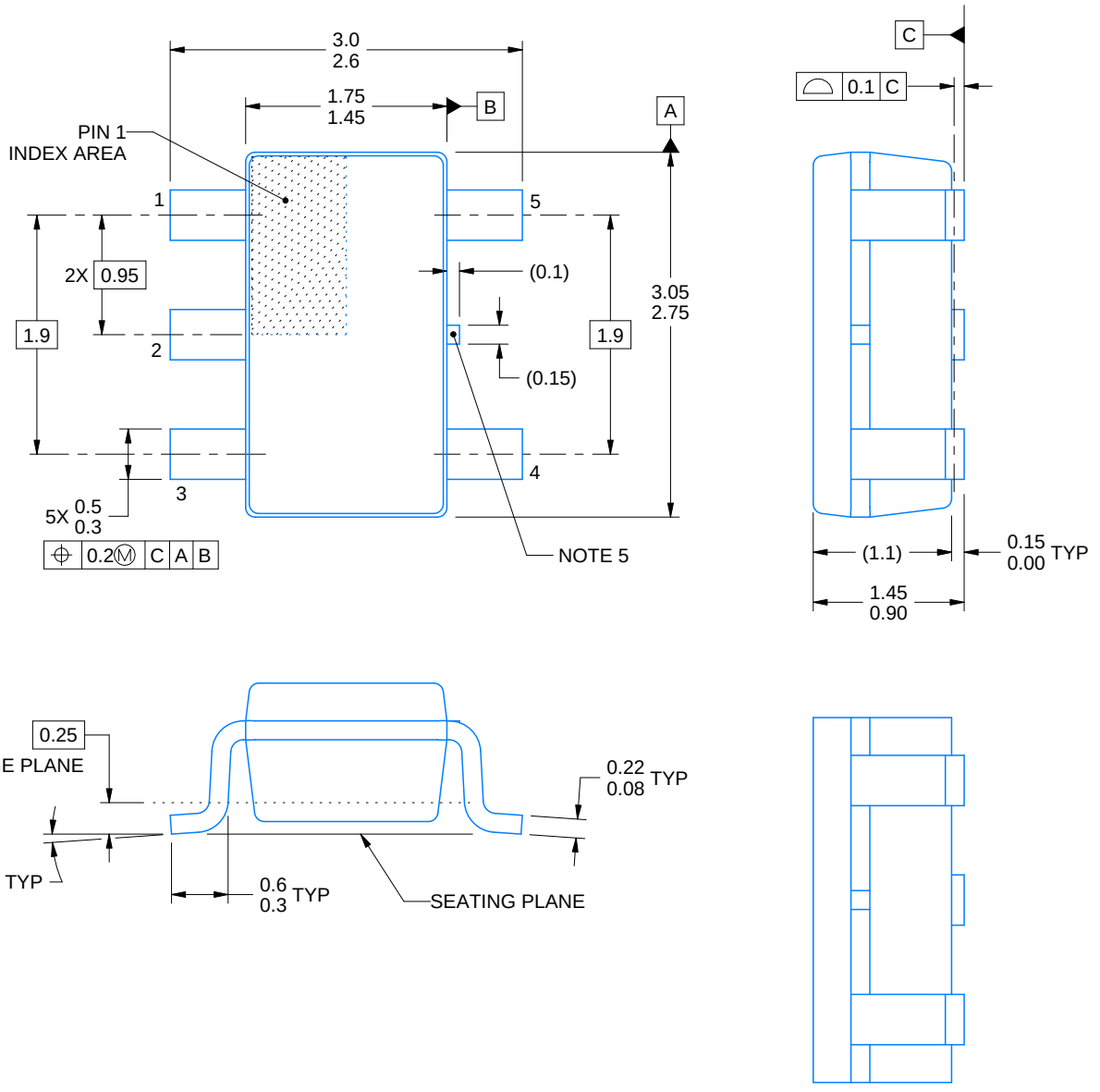
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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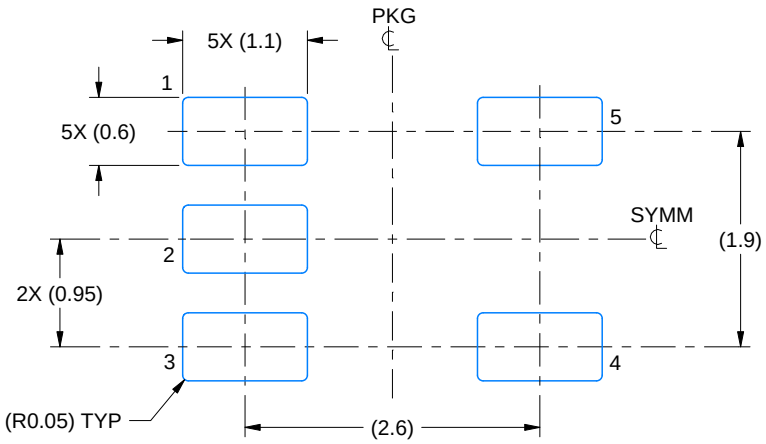
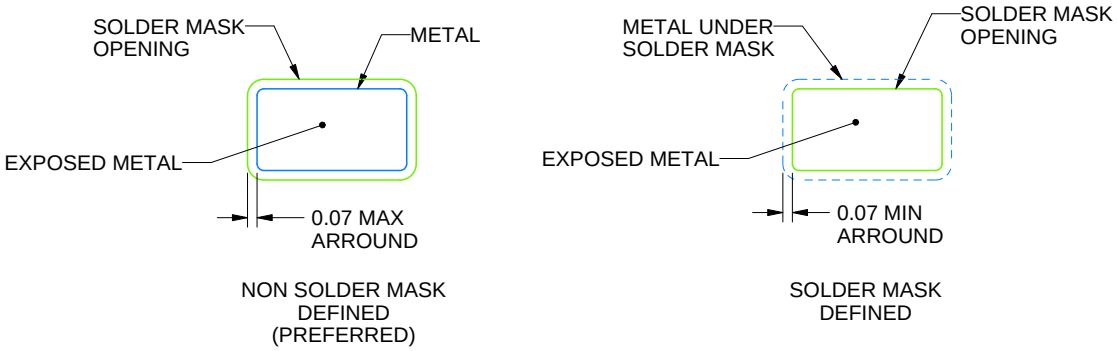


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

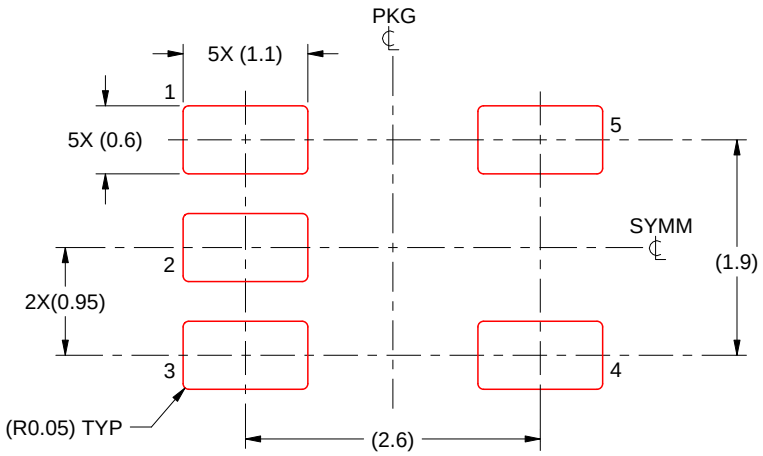


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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