







Texas Instruments

PGA302 SBASB65 – AUGUST 2024

PGA302 Sensor Signal Conditioner With 0V to 5V Ratiometric Output

1 Features

- Analog features:
 - Dual channel analog front-end
 - On-chip temperature sensor
 - Programmable gain up to 200V/V
 - 16-bit sigma-delta analog-to-digital converter
- Digital features:
 - 3rd-order linearity compensation algorithm
 - EEPROM memory for device configuration,
 - calibration data, and user data
 - I²C interface
 - One-wire interface through power line
- General features:
 - AFE sensor input, power supply, and output buffer diagnostics
 - Memory built-in self-test (MBIST)
 - Watchdog
 - Power management control

2 Applications

- Powertrain pressure sensors
- Powertrain exhaust sensors
- HVAC sensors
- Seat occupancy sensors
- Brake systems
- Battery management systems (BMS)

3 Description

The PGA302 is a low-drift, low-noise, programmable signal-conditioner device designed for a variety of resistive bridge-sensing applications like pressure-, temperature-, and level-sensing applications. The PGA302 can also support flow metering applications, weight scale and force-sensing applications that use strain gauge load cells, and other general resistive bridge signal-conditioning applications.

The PGA302 provides a bridge excitation voltage of 2.5V and a current output source with programmable current output up to 1mA. At the input, the device contains two identical analog front-end (AFE) channels followed by a 16-bit Sigma-Delta ADC. Each AFE channel has a dedicated programmable gain amplifier with gain up to 200V/V.

In addition, one of the channels integrates a sensor offset compensation function while the other channel integrates an internal temperature sensor.

At the output of the device, a 1.25V, 14-bit DAC is followed by a ratiometric-voltage supply output buffer with gain of 4V/V allowing a 0V-5V ratiometric voltage system output. The PGA302 device implements a third-order temperature coefficient (TC) and nonlinearity (NL) digital compensation algorithm to calibrate the analog output signal. All required parameters for the linearization algorithm as well as other user data is stored in the integrated EEPROM memory.

Package Information

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PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾						
PGA302	PW (TSSOP, 16)	5mm × 6.4mm						

(1) For more information, see the *Mechanical*, *Packaging*, and Orderable Information.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



PGA302 Simplified Block Diagram

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For system connectivity the PGA302 device integrates an I²C Interface as well as a one-wire interface (OWI) that supports communication and configuration through the power-supply line during final system calibration process. Diagnostics are implemented at the excitation output sources, the input to the AFE and the power supplies in the device. System Diagnostics like sensor open / short are also supported.

The PGA302 accommodates various sensing element types, such as piezoresistive, ceramic film, strain gauge, and steel membrane. The device can also be used in accelerometer, humidity sensor signal-conditioning applications, as well as in some current-sensing, shunt-based applications.



4 Device and Documentation Support

4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.3 Trademarks

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4.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA302EPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	PGA302	Samples
PGA302EPWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	PGA302	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM



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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions a	are nominal
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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA302EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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PACKAGE MATERIALS INFORMATION

25-Sep-2024



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA302EPWR	TSSOP	PW	16	2000	350.0	350.0	43.0

PW0016A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



PW0016A

EXAMPLE BOARD LAYOUT

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PW0016A

EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

9. Board assembly site may have different recommendations for stencil design.



^{8.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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