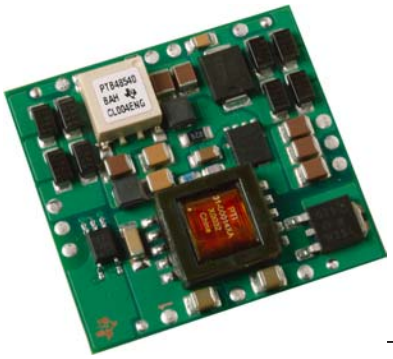
PTB48540 Series

10-W Power-Over-Ethernet Isolated Power Module Assembly

SLTS224B – APRIL 2004 – REVISED JULY 2004



Features

- Input Voltage Range: 36 V to 57 V
- 10 W Output
- IEEE Std. 802.3af Compliant *(for PoE-PD Interface)*
- 85 % Efficiency
- Low Profile (9 mm)
- Output Voltage Trim/Adjust
- Under-Voltage Lockout
- Input Transient Suppressor
- Internal EMI Filter
- Meets FCC Class B Radiated & Class A Conducted
- Output Inhibit Control
- Short Circuit Protection
- Over Temperature Shutdown
- 1500 VDC Isolation
- Safety Approvals (Pending): UL 60950, cUL 60950, EN60950

Description

The PTB48540 series of power modules is specifically designed to provide an isolated, low-voltage power source to a remote Powered Device (PD) in Power-Over-Ethernet (PoE) applications. These modules are rated 10 W and incorporate all the necessary interface requirements to comply with IEEE Std. 802.3af, for managing the input power to the PD from the PoE Power Sourcing Equipment (PSE). This includes PD detection and PD classification current signatures required for the PSE. The modules are compatible with PD classifications, class 0 through class 3.

In addition to a fully integrated DC/DC converter, each PTB48540 power module incorporates internal input diode bridges to support both Data Line and Spare Line pair standard Ethernet power connections, an integral transient suppressor for input over-voltage protection, and an EMI filter to ensure noise compatibility with Ethernet data signals.

Other features include an input under-voltage lockout (UVLO), over-current and short-circuit protection, an output voltage adjust/trim, and over-temperature protection. An "Output Inhibit" control allows the output voltage to be turned off to support an idle condition or power saving mode. The output voltage options are for 3.3-V, 5-V, or 12-V output. The target applications are small low-power remote IP appliances, such as security card readers and cameras, test dongles, and IP phone consoles.

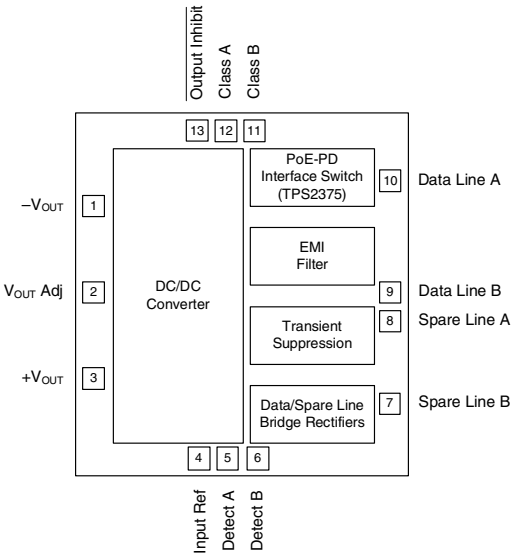
Pin Assignments

Pin	Function
1	–Vout
2	Vout Adj
3	+Vout
4	Input Ref
5	Detect A
6	Detect B
7	Spare Line B
8	Spare Line A
9	Data Line B
10	Data Line A
11	Class B
12	Class A
13	Output Inhibit *

Shaded functions indicate signals electrically common with the input.

** Denotes negative logic:*
Open = Normal operation
Low (Input Ref) = Output Off

Product Top View



Ordering Information

Output Voltage (PTB48540❒xx)

Code	Voltage
A	5 V
B	3.3 V
C	12 V

Package Options (PTB48540x❒❒)

Code	Description	Pkg Ref. (1)
AH	Horiz. T/H	(EUP)
AS	SMD, Standard (2)	(EUQ)

Notes: *(1) Reference the applicable package reference drawing for the dimensions and PC board layout*
(2) "Standard" option specifies 63/37, Sn/Pb pin solder material.

Pin Descriptions

$-V_{OUT}$: This is the negative output from the module, with respect to +Vout. Both the +Vout and –Vout terminals are isolated from the Ethernet input, and used to power the PD appliance. When this pin is connected to the PD appliance common, a positive supply voltage is produced at +Vout.

V_{OUT} Adj: By connecting a single resistor to this pin, the regulated output voltage may be adjusted/trimmed by up to ±10 % from the original set-point value. If no adjustment is desired, this pin should be left open circuit.

$+V_{OUT}$: This is the positive output from the module with respect to –Vout, and is used to power the PD appliance. By connecting this pin to the PD appliance common, a negative supply voltage will be produced at –Vout.

Input Ref: This pin provides access to the –Vin of the internal DC/DC converter, and is the 0-VDC reference for the '*Output Inhibit*' control.

Detect A: This is a control input that is normally left open circuit. The module incorporates an internal 24.9-kΩ resistor, between the '*Detect A*' and '*Detect B*' pins. This provides the PD with a correct "valid device" detection resistance for the PSE. By placing an external resistor between the '*Detect A*' and '*Detect B*' pins (in parallel with the internal 24.9-kΩ resistor) the module can be made to identify itself as a "non-valid device."

Detect B: This pin is used in conjunction with the '*Detect A*' input only when it is desired for the PD to communicate a "non-valid" device signature to the PSE (see '*Detect A*' description). '*Detect B*' is also the rectified DC output from the module's internal diode bridges, and represents the positive DC input to the module's DC/DC converter. Connecting an external capacitor between this pin and the '*Input Ref*' pin (0 V), adds more filter capacitance across the input of the DC/DC converter.

Data Line A/B: These are the main inputs from which the module obtains DC input power from the Ethernet connector. The connection of these inputs to the Ethernet connections must be via an IEEE 802.3af compliant signal tranformer, that is designed for use in a PoE application. This is necessary to preserve the integrity of the Ethernet data traffic. Consult the example application for further information.

Spare Line A/B: These are alternative inputs from which the module may obtain DC input power. In a PoE application, '*Spare Line A*' may be directly connected to pins 4 & 5, and '*Spare Line B*' to pins 7 & 8 of an Ethernet RJ-45 connector. These connections are not used for data transmission.

Class A/B: The control inputs '*Class A*' and '*Class B*' allow the PD Class to be programmed from the module. The module incorporates an internal 4.42-kΩ resistor between the '*Class A*' and '*Class B*' inputs. This corresponds to a default "Class 0" PD classification signature being sent to the PSE. By adding an external resistor across these pins, the module can be programmed to other PD classifications. For further information, consult the PD class reference table in the application notes.

Output Inhibit: This is an open-collector (or open-drain) negative logic input. Applying a low-level voltage to this input, with respect to the '*Input Ref*' pin, turns off the DC output voltage from the module. If the pin is left open-circuit, the module will operate as normal, producing an output voltage whenever it is connected to a valid PoE input source.

Specifications (Unless otherwise stated, T_a =25°C, V_{in} =48V (1), and I_o =$I_o$max)

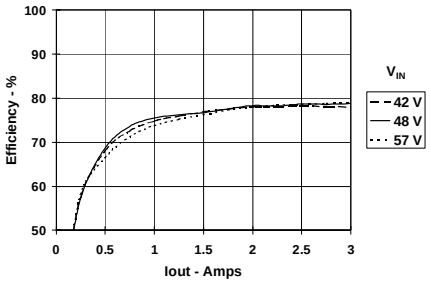
Characteristic	Symbol	Conditions		PTB48540 SERIES Min	Typ	Max	Units
Output Current	I_o	Over V_{in} range	PTB48540A (5 V) PTB48540B (3.3 V) PTB48540C (12 V)	0.1 (2) 0.1 (2) 0.1 (2)	— — —	2 3 0.85	A
Input Voltage Range	V_{in}	Over I_o Range		36	—	57 (1)	VDC
Set Point Voltage Tolerance	V_o tol			—	±1	±2	%V_o
Temperature Variation	Reg_{temp}	–40 ≤T_a ≤ +85 °C, I_o =$I_o$min		—	±0.2	—	%V_o
Line Regulation	Reg_{line}	Over V_{in} range		—	±1	—	mV
Load Regulation	Reg_{load}	Over I_o range		—	±5	—	mV
Total Output Voltage Variation	ΔV_otot	Includes set-point, line, load, –40 ≤T_a ≤ +85 °C		—	±1.5	±3	%V_o
Efficiency	η		PTB48540C (12 V) PTB48540A (5 V) PTB48540B (3.3 V)	— — —	85 82 79	— — —	%
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth		—	50	—	mV_{pp}
Transient Response	t_{tr}	1 A/µs load step, 50 % to 100 % $I_o$max		—	100	—	µs
	ΔV_{tr}	V_o over/undershoot	V_o ≤ 5 V V_o =12 V	— —	±150 ±200	— —	mV
Output Voltage Adjust	V_{adj}			—	±10	—	%V_o
Current Limit Threshold	I_{lim}	V_{in} = 42 V, ΔV_o = –1 %		—	150	—	%$I_o$max
Switching Frequency	f_s	Over V_{in} range		200	300	400	kHz
Under-Voltage Lockout	UVLO	V_{in} rising V_{in} falling		— 30	40 32	42 —	V
Output Inhibit (Pin 13) Input High Voltage Input Low Voltage Input Low Current	 V_{IH} V_{IL} I_{IL}	Referenced to Input Ref (pin 4)		 4.5 –0.2 —	 — — –2	 Open (3) +0.8 —	 V mA
Standby Input Current	I_{in} standby	pins 13 & 4 connected		—	1	—	mA
External Output Capacitance	C_{out}		V_o ≤ 5 V V_o = 12 V	0 (4) 0 (4)	— —	1000 330	µF
Internal Input Capacitance	C_{in}	V_{in} < UVLO threshold V_{in} > UVLO threshold		0.05 5	0.1 7	0.12 —	µF
Detection Resistance	R_{detect}	2.7 V ≤ V_{in} ≤ 10.1 V		23.75	24.9 (5)	26.25	kΩ
Classification Current	I_{class}	14.5 V ≤ V_{in} ≤ 20.5 V		2	2.5 (6)	3	mA
Operating Temperature Range	T_a	Over V_{in} range		–40	—	+85 (7)	°C
Over Temperature Protection	OTP	Measured at pin 7	Threshold Hysterisis	135 —	— 20	— —	°C
Isolation Voltage Capacitance Resistance		Input–output		1500 — 10	— 1,100 —	— — —	V pF MΩ
Solder Reflow Temperature	T_{reflow}	Surface temperature of module body or pins		—	—	235 (8)	°C
Storage Temperature	T_s	—		–40	—	+125	°C
Reliability	MTBF	Per Bellcore TR-332 50 % stress, T_a =40 °C, ground benign		4	—	—	10^6 Hrs
Mechanical Shock	—	Per Mil-Std-883D, method 2002.3, 1 mS, half-sine, mounted to a fixture		—	500	—	G's
Mechanical Vibration	—	Mil-Std-883D, Method 2007.2 20-2000 Hz, soldered to PC	Pkg EUP Pkg EUQ	— —	20 7.5	— —	G's
Weight	—	—		—	12	—	grams
Flammability	—	Materials meet UL 94V-0					

Notes: *(1) The input voltage Vin is applied and measured between 'Data Line A' (pin 10) and 'Data Line B' (pin 9), or between 'Spare Line A' (pin 8) and 'Spare Line B (pin 7). These inputs accept either polarity.*
(2) The DC/DC converter will operate at no load with reduced specifications.
(3) The Output Inhibit (pin 13) is referenced to 'Input Ref' (pin 4) and has an internal pull-up. If it is left open circuit the converter will operate when input power is applied. The open-circuit voltage is typically 5 V. Refer to the application notes for interface considerations.
(4) An output capacitor is not required for proper operation.
(5) This is the default for a "Valid Device" PD detection signature.
(6) This is the default for a "Class 0" PD classification signature.
(7) See Safe Operating Area curves or contact the factory for the appropriate derating.
(8) During the reflow of the SMD package version do not elevate the peak temperature of the module, pins, or internal components above the stated maximum.

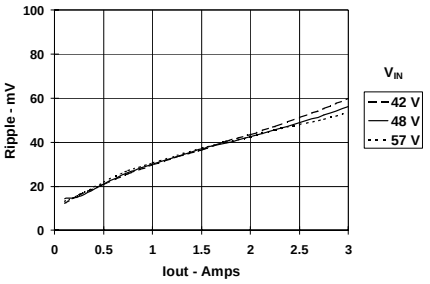
Typical Characteristics

PTB48540B; V_o =3.3 V *(See Note A)*

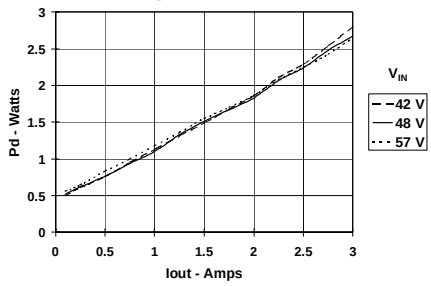
Efficiency vs Load Current



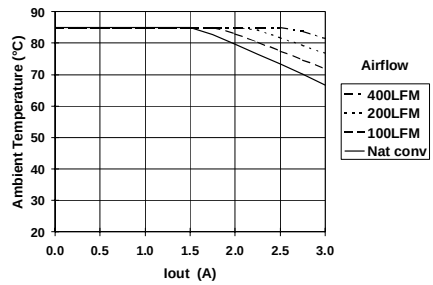
Output Ripple vs Load Current



Power Dissipation vs Load Current

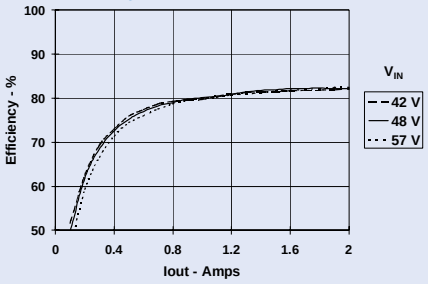


Safe Operating Area (See Note B)

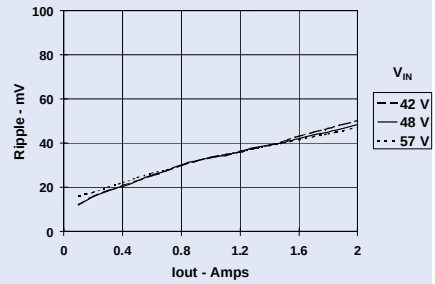


PTB48540A; V_o =5 V *(See Note A)*

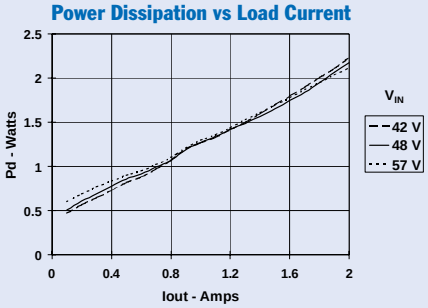
Efficiency vs Load Current



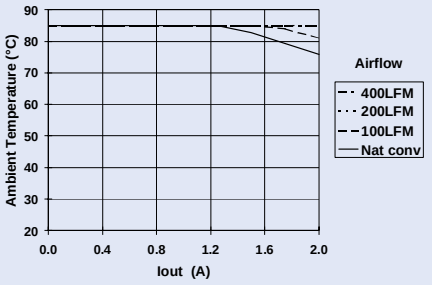
Output Ripple vs Load Current



Power Dissipation vs Load Current

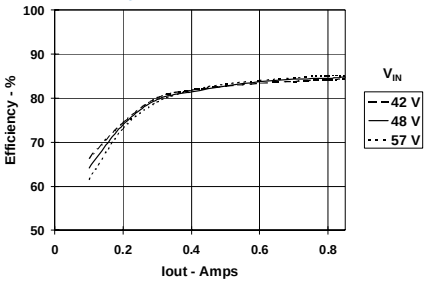


Safe Operating Area (See Note B)

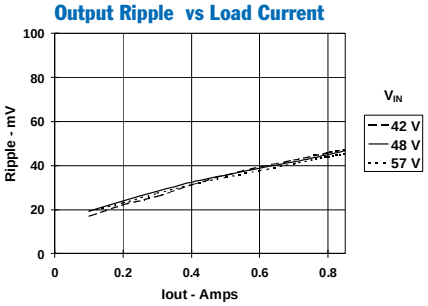


PTB48540C; V_o =12 V *(See Note A)*

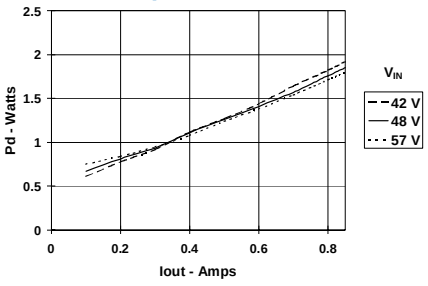
Efficiency vs Load Current



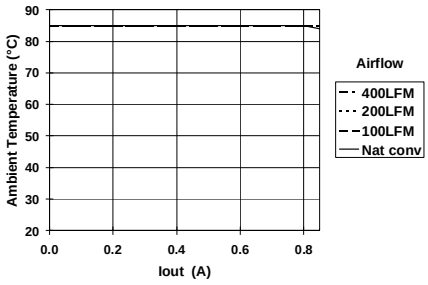
Output Ripple vs Load Current



Power Dissipation vs Load Current



Safe Operating Area (See Note B)



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.*

Operating Features of the PTB48540 Series Power-Over-Ethernet Modules

Overview

Figure 1-1 shows the block diagram of the PTB48540 series of Power-over-Ethernet (PoE) modules. Input power to the module can be supplied through either the Data Line A/B or Spare Line A/B associated Ethernet connections. A diode bridge associated with each of these input pairs allows the input source to be supplied in either polarity. A transient suppressor, located across the common output of the diode bridges, protects the module against power surges.

The input power to the internal DC/DC converter is controlled by the TPS2375 IC. This IC is a power interface switch, specifically designed for use with PoE powered devices. The IC provides the device detection, classification, and current limiting control that is necessary for a powered device (PD) to comply with the IEEE 802.af Standard. The DC/DC converter input circuit includes an EMI filter, which maintains the module in compliance with CISPR 22 (EN5022); class 'B' for radiated, and class 'A' for conducted emissions.

PD Detection

Prior to power up, the PoE power sourcing equipment (PSE) must detect a 24.9-kΩ "discovery" load resistance from the PD. This default value of resistance is necessary for the PD to be recognized as a "valid device" by the PSE. A 24.9-kΩ resistor is provided internally to the PTB48540 modules. It is located across the 'Detect A' (pin 5) and 'Detect B' (pin 6) terminals. By placing an external resistor across these pins (in parallel with the internal 24.9-kΩ resistor), the module can be made to communicate a "non-valid device" signature to the PSE. A non-valid device is recognized by a resistance of less than 12 kΩ. Connecting a 16.9-kΩ external resistor between the 'Detect A' and 'Detect B' pins creates an equivalent resistance of 10 kΩ. This is sufficient to communicate a non-valid device signature. The external resistor should not be less than 16.9 kΩ as this increases power dissipation in the power interface IC.

PD Classification Signature

The PSE uses a classification current to determine the maximum supply current that the PD is allowed to draw. The classification current is sensed by the PSE when the supply voltage to the PD is between 15 V and 20 V. The classification current is set on the PTB48540 by a programming resistance. Table 1-1 gives the resistance values

Figure 1 1; Block Diagram of the PTB48540 Series Modules

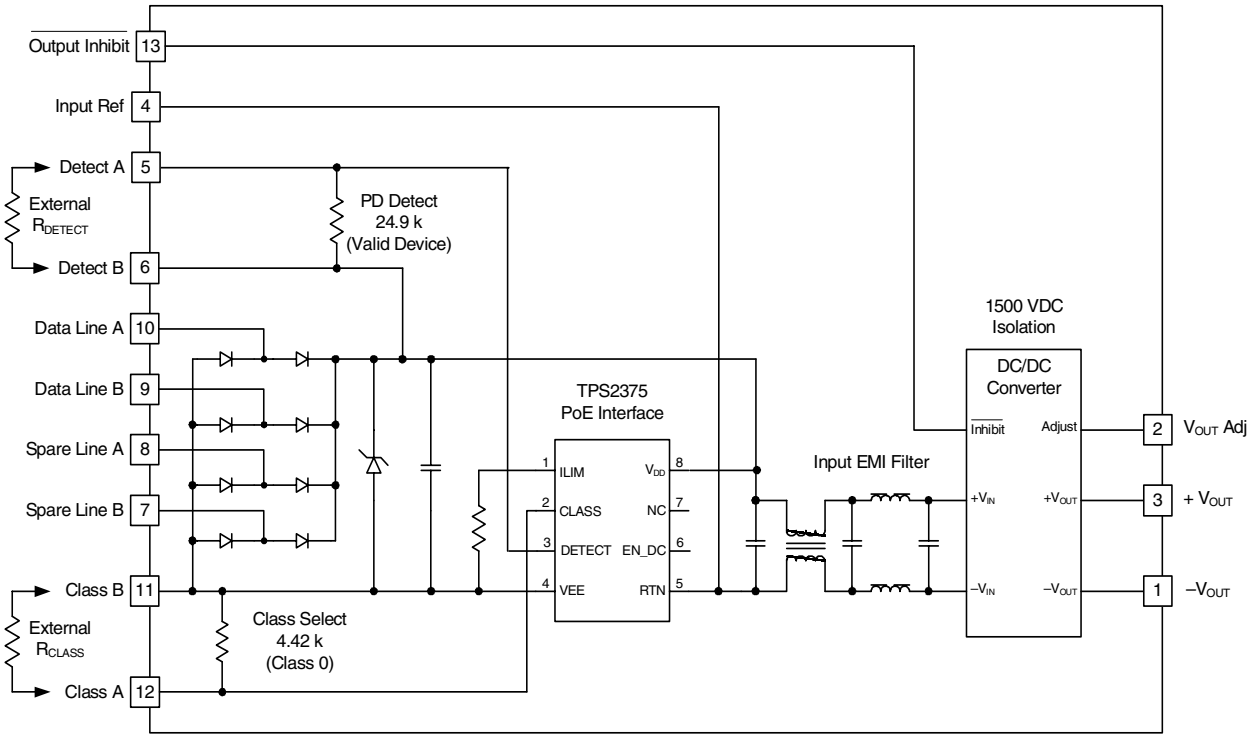


Table 1-1; PD Class Programming Resistance

PD Class	Usage	PD Demand (watts)		Class Program Resistance	External Resistor
		Min	Max		
0	Default	0.44	12.95	4.42 kΩ	None
1	Optional	0.44	3.84	950 Ω	1.21 kΩ
2	Optional	3.84	6.49	543 Ω	619 Ω
3	Optional	6.49	12.95	360 Ω	392 Ω
4	Not Allowed	— Future Use —		252 Ω	267 Ω

for the different types of PD class defined in the IEEE 802.3af Standard. The power modules support the PD classification protocol with a default 'Class 0' signature. 'Class 0' corresponds to a 4.42-kΩ programming resistance, which is set by an internal resistor located between the 'Class A' (pin 12) and 'Class B' (pin 11) terminals. By placing an external resistor across the Class A/B pins (in parallel with the internal 4.42-kΩ resistor) the power module can be made to communicate one of the alternate classifications to the PSE. Consult Table 1-1 for the external resistance values.

Under-Voltage Lockout

The UVLO prevents the internal DC/DC converter from seeing an input voltage until the voltage applied to either the 'Data Line A/B' or 'Spare Line A/B' pair of Ethernet connections approaches 42 V. The UVLO threshold correlates to a voltage between the 'Detect B' (pin 6) and 'Class B' (pin 11) terminals of approximately 39.3 V. Only after the voltage applied from the Ethernet is above the UVLO threshold is the module's internal bus voltage allowed to rise. The internal bus powers the DC/DC converter and can be measured between the 'Detect B' (pin 6) and 'Input Ref' (pin 4) terminals.

Input Capacitance

In accordance with the IEEE 802.3af Standard, the PTB48540 power modules provide an input capacitance of 0.1 µF to the PSE when communicating the required detection and classification signatures. Once fully powered (V_{in} ≥42 V), the PSE will see the combined input capacitance of the EMI filter and DC/DC converter; approximately 7 µF. This capacitance is sufficient to operate the module's internal DC/DC converter, and satisfies the 5 µF minimum capacitance required by the IEEE 802.3af Standard. For improved hold-up capability, this input capacitance can be increased with an external capacitor. Connect the anode of the external capacitor to 'Detect B' (pin 6), and the cathode to the 'Input Ref' (pin 4). During power up the power interface IC limits the inrush current for charging the input capacitance. Additional capacitance increases the power dissipation in the IC. For this reason the maximum recommended value of external capacitance is 220 µF (100-V electrolytic).

Startup

Startup of the module in a PoE application consists of a complex process of handshaking states between the module and PSE. During the PD detection state the PSE uses a low voltage (<10 V) to detect the module's "valid device" resistance signature. This is followed by the classification detection state where the PSE applies a voltage of 15 V to 20 V to detect the module's PD class. The PSE continues to raise the input voltage, but the input voltage to the internal DC/DC converter is held at zero until the voltage from the PSE approaches 42 V. At an input voltage of 42 V or higher, the module's power interface IC allows the internal bus voltage to rise using a limited amount of inrush current. Approximately 50 ms after the DC/DC converter input filter capacitors are fully charged, the module is able to produce a regulated output voltage.

Converter Over-Current Protection

The internal DC/DC converter has inherent protection against an output load fault. Whenever its load current exceeds the over-current protection threshold (see specification table) the converter momentarily turns its output off. After a short period (<100 ms), the regulator will attempt to power up again by executing a soft-start power up. The converter will continue in a successive cycle of shutdown, followed by soft-start power up until the load fault is removed.

When the DC/DC converter is powered from just the Ethernet source, a load current above its rated output (but below its over-current threshold) will likely activate the over-current protection offered by the power interface IC. This is especially at input voltages lower than 48 V.

Ethernet Over-Current Protection

Protection is also provided for the Ethernet power source equipment (PSE). In event of a fault across the module's internal bus, the onboard power interface IC limits the maximum current that may be drawn from the PSE to no less than 405 mA. This prevents the DC/DC converter from drawing excessive input current and also safeguards against external faults that may occur across the 'Detect B' (pin 6) and 'Input Ref' (pin 4) terminals. *Note: These terminals can be used to add capacitance to the module's internal bus.*

Load faults applied to the DC/DC converter's output will most often trigger the power interface IC's protection mechanism prior to activating the converter's own current limit threshold. In these instances the power interface IC will completely shut down the module's internal bus. This is a latched condition. It is reset by the PoE source when it attempts another power-up cycle after it senses loss of the PD's Maintain Power Signature (10 mA).

Adjusting the Output Voltage of the PTB48540 Series of Power Over Ethernet Modules

The set-point output voltage of the PTB48540 series of PoE modules may be adjusted (trimmed) by up to ±10 %. This is accomplished with the addition of a single external resistor. For the input voltage range specified in the data sheet, Table 2-1 gives the allowable adjustment range for each model as V_o (min) and V_o (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor, R_2 between pin 2 (V_{out} Adj), and pin 1 ($-V_{out}$).

Adjust Down: Add a resistor (R_1), between pin 2 (V_{out} Adj) and pin 3 ($+V_{out}$).

Refer to Figure 2-1 and Table 2-2 for both the placement and value of the required resistor, (R_1) or R_2.

The values of (R_1) [adjust down], and R_2 [adjust up], can also be calculated using the following formulas.

$$(R_1) = \frac{56.2\,(V_a - 1.225)}{V_o - V_a} - R_s \quad k\Omega$$

$$R_2 = \frac{68.845}{V_a - V_o} - R_s \quad k\Omega$$

Where, V_o = Original output voltage
V_a = Adjusted output voltage
R_s = Internal resistance (Table 2-1)

Notes:

1. Use only a single 1 % resistor in either the (R_1) or R_2 location. Place the resistor as close to the module as possible.
2. Never connect capacitors to V_o adjust. Any capacitance added to the V_o adjust control pin will affect the stability of the module.
3. The output power is limited to 10 W. If the output voltage is increased, the maximum load current must be derated according to the following equation.

$$I_o(max) = \frac{10}{V_a}$$

In any instance, the load current must not exceed the converter's rated current (See Table 2-1).

Table 2-1

DC/DC CONVERTER ADJUSTMENT PARAMETERS

Series Pt #	PTB48540B	PTB48540A	PTB48540C
Rated Current [3]	3 A	2 A	0.85 A
V_o(nom)	3.3 V	5 V	12 V
Vo(min)	2.95 V	4.5 V	10.8 V
Vo(max)	3.65 V	5.5 V	13.2 V
R_s (kΩ)	187	110	49.9

Figure 2-1; Adjust Resistor Placement

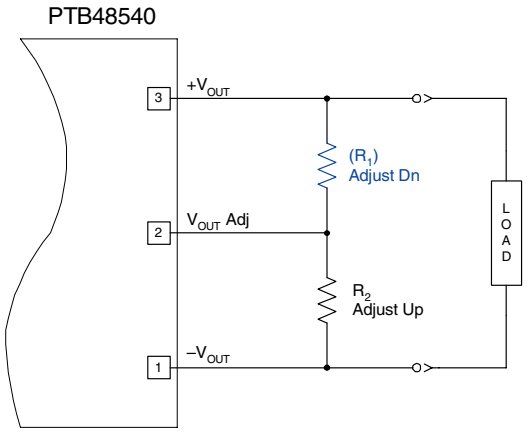


Table 2-2

DC/DC CONVERTER ADJUSTMENT RESISTOR VALUES

Series Pt #	PTB48540B	PTB48540A	PTB48540C
V_o(nom)	3.3 V	5 V	12 V
V_a(req'd)			
2.95	(90.0)kΩ		
3.0	(146.0)kΩ		
3.05	(223.0)kΩ		
3.1	(340.0)kΩ		
3.15	(534.0)kΩ		
3.2	(923.0)kΩ		
3.25	(2090.0)kΩ		
3.3			
3.35	1190.0kΩ		
3.4	501.0kΩ		
3.45	272.0kΩ		
3.5	157.0kΩ		
3.55	88.4kΩ		
3.6	42.5kΩ		
3.65	9.7kΩ		
•			
4.5		(258.0)kΩ	
4.6		(364.0)kΩ	
4.7		(541.0)kΩ	
4.8		(895.0)kΩ	
4.9		(1960.0)kΩ	
5.0			
5.1		578.0kΩ	
5.2		234.0kΩ	
5.3		119.0kΩ	
5.4		62.1kΩ	
5.5		27.7kΩ	
•			
10.8			(399.0)kΩ
11.0			(499.0)kΩ
11.5			(1110.0)kΩ
12.0			
12.5			87.8kΩ
13.0			18.9kΩ
13.2			7.5kΩ

R_1 = (Blue) R_2 = Black

Using the Output Inhibit Control with the PTB48540 Power-over-Ethernet Modules

The PTB48540 Power-over-Ethernet (PoE) modules incorporate all the necessary interface requirements to provide 10 W of regulated DC voltage from a recognized Power-over-Ethernet source.

One of the operating features of these modules allows the output voltage to be turned off, thereby placing the module in an idle state. This may be useful for applications that have an alternative voltage source available, such as a wall adapter.

The "Output Inihibit" control is provided by pin 13. The module functions normally with this pin open-circuit, providing a regulated output voltage whenever a valid source voltage is supplied from the Ethernet connection. When a low voltage is applied to pin 13, with respect to the "Input Ref" terminal (pin 4), the output is turned off. Even though the Ethernet source is still present.

Figure 3-1 is an application schematic, which shows how the "Output Inhibit" control may be used. Either a discrete transistor (Q_1), or a contact switch may be used. The "Output Inhibit" control pin has its own internal pull-up (See notes 2 & 3). Table 3-1 gives the threshold requirements.

When placed in the "Off" state, the standby current drawn from the input source is typically reduced to 1 mA [3].

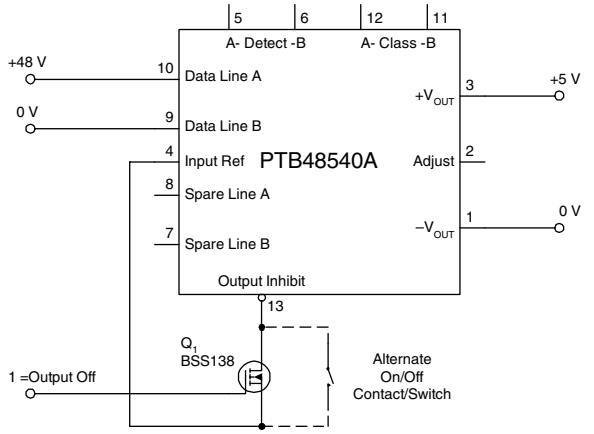
Table 3-1; Pin 13 Output Inhibit Control Parameters [1]

Parameter	Min	Typ	Max
Enable (V_{IH})	4.5 V	—	—
Disable (V_{IL})	—	—	0.8 V
$V_{O/C}$ [Open-Circuit]		5 V	
I_{in} [pins 13 & 4 connnected]	—	–1 mA	—

Notes:

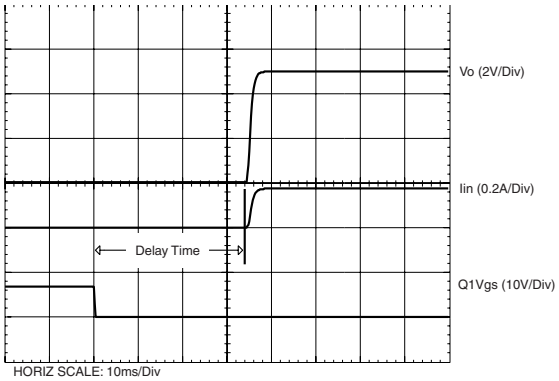
1. The *Output Inhibit* control uses *Input Ref* (pin 4) as its 0-V reference. All voltages specified are with respect to the *Input Ref* pin.
2. Use an open-collector device (preferably a discrete transistor or switch) for the *Output Inhibit* input. A pull-up resistor is not necessary. To turn the output off, the control pin should be pulled low to less than 0.8 VDC.
3. The module's idle current is typically less than 1 mA. This is below the minimum power signature (MPS) current, required for the PoE source to continue providing the PD with a source voltage. This will inevitably result in the removal of the module's input source. However, the PSE will endevour to periodically re-apply input power after detecting that the PD is still a valid device. This cycle may be prevented by also modifying the module's 'Detect' signature resistance so that it reflects an invalid device to the PSE.

Figure 3-1



Turn-On Time: In the circuit of Figure 3-1, turning Q_1 on applies a low-voltage to pin 13 and disables the module output. Correspondingly, turning Q_1 off allows pin 13 to be pulled high by an internal pull-up resistor. The module produces a regulated output voltage within 60 ms. Figure 3-2 shows shows the output response of a PTB48540A (5 V) following the turn-off of Q_1. The turn off of Q_1 corresponds to the drop in Q_1 Vgs. Although the rise-time of the output voltage is short (<5 ms), the indicated delay time will vary depending upon the input voltage and the module's internal timing. The waveform was measured with a 48 Vdc input voltage, and a 1.4 A resistive load.

Figure 3-2



Using the PTB48540 Series Module in a Power-Over-Ethernet (PoE) Application

The schematic of Figure 4-1 shows an example of how a PTB48540 module may be connected to a PoE compliant system. The connector J1 is the input from the PoE source.

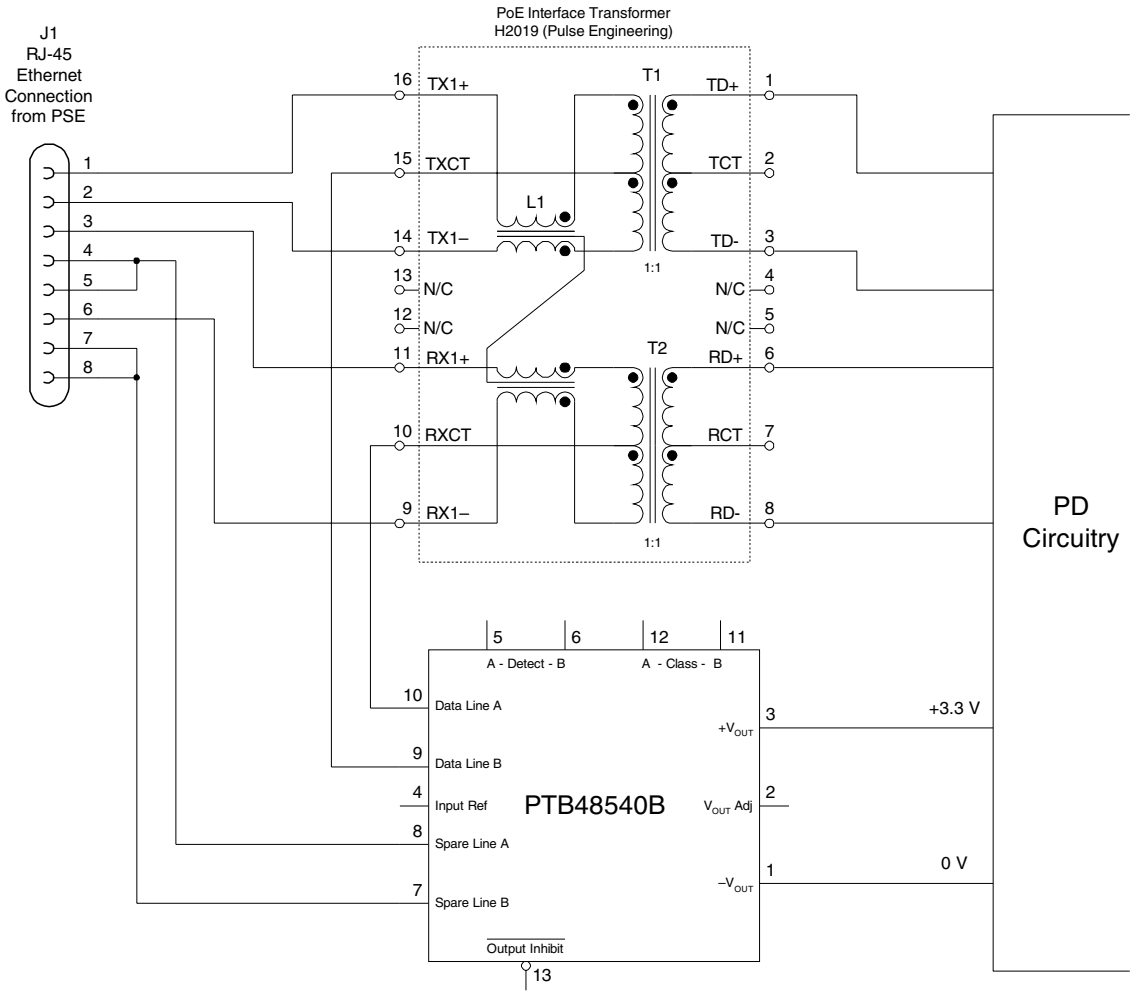
In a Power-over-Ethernet (PoE) application, the power and high-frequency data signals share the same conductors in the Ethernet cable. The data and power signals must be separated using an IEEE 802.3af compliant PoE magnetic module.

The magnetic module incorporates the customary isolation transformers, T1 and T2. The transformers each include a center tap, across which the dc current from the Ethernet power source equipment (PSE) is conveniently extracted. The transmit and receive hf Ethernet data appear as differential signals to each transformer. These signals are isolated by the transformers, allowing the Ethernet communication content to flow freely between the connector and the powered device (PD) circuitry.

The common-mode inductor, L1, is a popular addition to off-the-shelf PoE magnetic modules. The inductor provides additional rejection to common mode noise currents, which may otherwise be present on either the data or power signals.

The PTB48540 module complies with the PoE protocols, provides the required isolation, and converts the raw power from the PSE to a precision regulated 3.3-VDC power source for the remote PD circuitry.

Figure 4-1; Power-Over-Ethernet Application Schematic



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTB48540AAH	NRND	Through-Hole Module	EUP	13	12	RoHS (In Work) & non-Green	SN	N / A for Pkg Type	-40 to 85		
PTB48540BAH	NRND	Through-Hole Module	EUP	13	12	RoHS (In Work) & non-Green	SN	N / A for Pkg Type	-40 to 85		
PTB48540CAH	NRND	Through-Hole Module	EUP	13	12	RoHS Exempt & non-Green	SN	N / A for Pkg Type	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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