REF54 0.8ppm/°C Maximum Drift, 0.11ppm$_{p-p}$ 1/f Noise, 380µA Current, Precision Voltage Reference

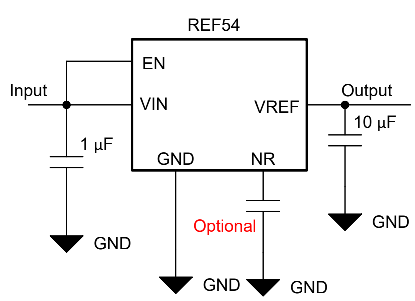
1 Features

- Low temperature drift coefficient:
  - 0.8ppm/°C maximum (C grade, 0°C to 70°C)
  - 1.5ppm/°C maximum (Q grade, –40°C to 125°C)
- Low noise (0.1Hz to 10Hz):
  - 0.11ppm$_{p-p}$ with C_{NR} = 100µF
  - 0.45ppm$_{p-p}$ with C_{NR} = Open
- High accuracy: ±0.02% maximum
- Low quiescent current: 380µA maximum
- Low long-term stability (1k hr): 25ppm
- Designed for a wide range of applications:
  - Wide input voltage up to 18V
  - Output current: ±10mA
  - Voltage options: 2.5V, 3V, 4.096V, 4.5V, 5V
- Fit for all design requirement:
  - Stable with 1µF to 100µF output low-ESR capacitor
  - High PSRR: 100dB at 1kHz
  - Operating temperature range: −40°C to +125°C
  - Pin-to-pin to REF50xx family when TEMP pin is not used

2 Applications

- Semiconductor test equipment
- Precision data acquisition systems
- Precision weight scales
- Ultrasound scanner
- X-ray systems
- Industrial instrumentation
- PLC analog I/O modules
- Field transmitters
- Power monitoring
- Battery management system

Basic Connection Diagram



Basic Connection Diagram

3 Description

The REF54 is a family of high precision, low-drift, low current consumption series voltage reference devices. The REF54 family offers low temperature drift coefficient (0.8ppm/°C), low noise (0.11ppm$_{p-p}$) and high accuracy (±0.02%) while consuming 260µA current. The REF54 with low long-term drift (25ppm), excellent load and line regulation helps meet strict performance requirements of high precision applications. The device family is designed as a companion device for high-resolution data converters such as ADS8900B, ADS127L11, ADS1285 and DAC11001B.

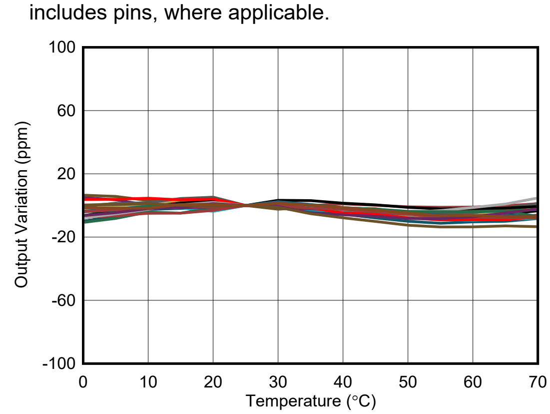
The REF54 family supports wide supply voltage rating of 18 V. This also protects the device in case of power supply IC failure. The REF54 device supports up to 10mA load current. The wide load current support allows for direct connection of REF54 as power supply to precision sensors.

The REF54 is specified for the two temperature ranges, C grade is specified for 0°C to 70°C and Q grade is specified for –40°C to +125°C . The wide temperature range enables operation across various industrial applications.

Package Information

PART NAME	PACKAGE (1)	PACKAGE SIZE(3)
REF54	SOIC (8)	4.9mm × 6mm
REF54	VSSOP (8) (2)	3mm × 4.9mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview package.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Output Voltage vs Free-Air-Temperature

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4 Device Comparison Table

PRODUCT		V_{REF}	SPECIFIED TEMPERATURE RANGE
SOIC (8)	VSSOP (8) [(2)]		
REF54250QDR [(2)]	REF54250QDGKR	2.5 V	-40ºC to 125ºC
REF54250CDR [(1)]	REF54250CDGKR	2.5 V	0ºC to 70ºC
REF54300CDR [(2)]	REF54300CDGKR	3.0 V	-40ºC to 125ºC
REF54300CDR [(2)]	REF54300CDGKR	3.0 V	0ºC to 70ºC
REF54410QDR [(2)]	REF54410QDGKR	4.096 V	-40ºC to 125ºC
REF54410CDR [(1)]	REF54410CDGKR	4.096 V	0ºC to 70ºC
REF54450QDR [(2)]	REF54450QDGKR	4.5 V	-40ºC to 125ºC
REF54450CDR [(2)]	REF54450CDGKR	4.5 V	0ºC to 70ºC
REF54500QDR [(2)]	REF54500QDGKR	5.0 V	-40ºC to 125ºC
REF54500CDR [(2)]	REF54500CDGKR	5.0 V	0ºC to 70ºC

(1) This orderable is released to market.
(2) Product preview. Contact local TI support for samples.

5 Pin Configuration and Functions

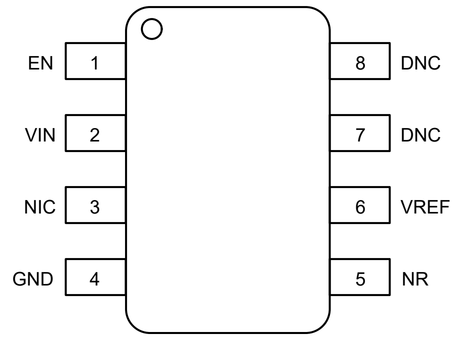

**Figure 5-1. D Package
8-Pin SOIC
Top View**

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	D		
EN	1	Input	Device enable control. Low level input disables the reference output and device enters shutdown mode. Device can be enabled by driving voltage > 1.6V or leaving the EN pin floating. See section Section 8.3.1 for additional details.
VIN	2	Power	Input supply voltage connection. Connect a minimum 0.1-μF decoupling capacitor to ground for the best performance. See section Section 9.3 for additional details.
NIC	3	No Connect	Not internally connected. Pin can be left floating or to a known potential.
GND	4	Ground	Ground connection.
NR	5	Output	Noise reduction pin. Connect a decoupling capacitor to ground for improved noise performance. The pin can be left floating. See section Section 8.3.2 for additional details.
VREF	6	Output	Reference voltage output. Connect a capacitor between 1 μF to 100 μF to ground for best performance.
DNC	7, 8	Do not Connect	Leave the pin floating or connect to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	VIN	-0.3	20	V
Enable voltage	EN	-0.3	VIN	V
Output voltage	V_{OUT}	-0.3	VIN	V
Output short circuit current	I_{SC}		25	mA
Operating temperature range	T_A	-55	150	°C
Storage temperature range	T_{stg}	-65	170	°C

(1) Stresses above these ratings can cause permanent damage. Exposure to absolute maximum conditions for extended periods can degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	± 1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	$V_{OUT} + V_{DO}$ [1]		18	V
EN	Enable voltage	0		V_{IN}	V
NR	Noise reduction	0		6	V
I_L	Output current	–10		10	mA
T_A	Operating ambient temperature	–40	25	125	°C

(1) V_{DO} = Dropout voltage.

6.4 Thermal Information

THERMAL METRIC[1]		REF54 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics REF54250

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25°C		–0.02		0.02	%
	Output voltage temperature coefficient	Q grade; –40°C ≤ T_A ≤ 125°C (1)				1.5	ppm/°C
		C grade; 0°C ≤ T_A ≤ 70°C				0.8	
LINE AND LOAD REGULATION							
ΔV_O / ΔV_{IN}	Line regulation	V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, 0°C ≤ T_A ≤ 70°C			1	3	ppm/V
		V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C (1)			1	3	
ΔV_O / ΔI_L	Load regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C			5	20	ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C (1)			5	30	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C			5	15	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C (1)			5	25	
NOISE							
e_{np-p}	Low frequency noise	*f* = 0.1 Hz to 10 Hz			0.45		ppm_{p-p}
		f = 0.1 Hz to 10 Hz, C_{NR} = 10µF			0.24		
		f = 0.1 Hz to 10 Hz, C_{NR} = 100µF			0.11		
e_n	Output voltage noise	*f* = 10 Hz to 1 kHz			0.7		ppm_{rms}
e_n	Output voltage noise	*f* = 10 Hz to 1 kHz , C_{NR} = 1µF			0.16		ppm_{rms}
R_{NR}	NR pin internal resistance				14		kΩ
HYSTERESIS AND LONG-TERM STABILITY							
ΔV_{OUT_LTD}	Long-term stability	250h T_A = 35°C			14		ppm
		1000h T_A = 35°C			25		
		2000h T_A = 35°C			32		
ΔV_{OUT_HYS}	Output voltage hysteresis	25°C, 0°C, 70°C, 25°C (cycle 1)			15		ppm
		25°C, 0°C, 70°C, 25°C (cycle 2)			0.8		
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF			0.4		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	–40°C ≤ T_A ≤ 125°C		0.1			µF
C_{OUT}	Stable output capacitor range (2)	–40°C ≤ T_A ≤ 125°C		1		100	µF
POWER SUPPLY							
V_{IN}	Input voltage			V_{OUT} + V_{DO}		18	V
I_Q	Quiescent current	T_A = 25°C	Active mode		260		µA
I_Q	Quiescent current	–40°C ≤ T_A ≤ 125°C				380	µA
		T_A = 25°C	Shutdown mode		0.5	1	uA
		–40°C ≤ T_A ≤ 125°C				2	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V

6.5 Electrical Characteristics REF54250 (continued)

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18 V		0.5		uA
		V_{IN} = V_{EN} = 18 V, –40°C ≤ T_A ≤ 125°C			1.5	uA
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C			250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C			400	mV
I_{SC}	Short circuit current	V_{OUT} = 0V		21		mA

(1) Specification subject to change with Q grade production release.
(2) ESR for the capacitor can range from 10 mΩ to 1 Ω.

6.6 Electrical Characteristics REF54300

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted (1)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25°C		–0.02		0.02	%
	Output voltage temperature coefficient	Q grade; –40°C ≤ T_A ≤ 125°C				1.5	ppm/°C
		C grade; 0°C ≤ T_A ≤ 70°C				0.8	ppm/°C
LINE AND LOAD REGULATION							
$\Delta V_O / \Delta V_{IN}$	Line regulation	V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, 0°C ≤ T_A ≤ 70°C			1	2	ppm/V
		V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C			1	3	ppm/V
$\Delta V_O / \Delta I_L$	Load regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C			5	30	ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C			5	20	ppm/mA
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C			5	25	ppm/mA
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C			5	15	ppm/mA
NOISE							
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz			0.45		ppm_{p-p}
		f = 0.1 Hz to 10 Hz, , C_{NR} = 100µF			0.1		ppm_{p-p}
e_n	Output voltage noise	f = 10 Hz to 1 kHz			0.7		ppm_{rms}
HYSTERESIS AND LONG-TERM STABILITY							
ΔV_{OUT_LTD}	Long-term stability	250h T_A = 35°C			14		ppm
		1000h T_A = 35°C			35		ppm
ΔV_{OUT_HYS}	Output voltage hysteresis	25°C, 0°C, 70°C, 25°C (cycle 1)			15		ppm
ΔV_{OUT_HYS}	Output voltage hysteresis	25°C, 0°C, 70°C, 25°C (cycle 2)			0.8		ppm
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF			0.44		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	–40°C ≤ T_A ≤ 125°C		0.1			µF
C_{OUT}	Stable output capacitor range (2)	–40°C ≤ T_A ≤ 125°C		1		100	µF
POWER SUPPLY							
V_{IN}	Input voltage			V_{OUT} + V_{DO}		18	V
I_Q	Quiescent current	T_A = 25°C	Active mode		260		µA
		–40°C ≤ T_A ≤ 125°C	Active mode			380	µA
		T_A = 25°C	Shutdown mode		0.5		uA
		–40°C ≤ T_A ≤ 125°C	Shutdown mode			1.5	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18V			0.25	0.7	uA
		V_{IN} = V_{EN} = 18V, –40°C ≤ T_A ≤ 125°C				1.2	uA
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C				250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C				400	mV

6.6 Electrical Characteristics REF54300 (continued)

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted [(1)]

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{SC}	Short circuit current	V_{OUT} = 0V		21		mA

(1) REF54300 device is in preview state. All specifications are preliminary and subject to change before production release .
(2) ESR for the capacitor can range from 10 mΩ to 1 Ω.

6.7 Electrical Characteristics REF54410

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage accuracy	T_A = 25°C	–0.02		0.02	%
	Output voltage temperature coefficient	Q grade; –40°C ≤ T_A ≤ 125°C[1]			1.5	ppm/°C
		C grade; 0°C ≤ T_A ≤ 70°C			1	
LINE AND LOAD REGULATION						
ΔV_O / ΔV_{IN}	Line regulation	V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, 0°C ≤ T_A ≤ 70°C		1	2	ppm/V
		V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C[1]		1	3	
ΔV_O / ΔI_L	Load regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C		5	20	ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C		5	30	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C		5	15	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C[1]		5	25	
NOISE						
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz		0.45		ppm_{p-p}
		f = 0.1 Hz to 10 Hz, C_{NR} = 10µF		0.2		
		f = 0.1 Hz to 10 Hz, C_{NR} = 100µF		0.09		
e_n	Output voltage noise	f = 10 Hz to 1 kHz		0.7		ppm_{rms}
		f = 10 Hz to 1 kHz, C_{NR} = 1µF		0.15		
R_{NR}	NR pin internal resistance			14		kΩ
HYSTERESIS AND LONG-TERM STABILITY						
ΔV_{OUT_LTD}	Long-term stability	250h T_A = 35°C		14		ppm
		1000h T_A = 35°C		25		
		2000h T_A = 35°C		32		
ΔV_{OUT_HYS}	Output voltage hysteresis	25°C, 0°C, 70°C, 25°C (cycle 1)		35		ppm
		25°C, 0°C, 70°C, 25°C (cycle 2)		3		
TURN ON TIME						
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF		0.6		ms
CAPACITIVE LOAD						
C_{IN}	Stable input capacitor range	–40°C ≤ T_A ≤ 125°C	0.1			µF
C_{OUT}	Stable output capacitor range [2]	–40°C ≤ T_A ≤ 125°C	1		100	µF
POWER SUPPLY						
V_{IN}	Input voltage		V_{OUT} + V_{DO}		18	V
I_Q	Quiescent current	T_A = 25°C, Active mode		300		µA
		–40°C ≤ T_A ≤ 125°C, Active mode			450	µA
		T_A = 25°C, Shutdown mode		0.5		uA
		–40°C ≤ T_A ≤ 125°C, Shutdown mode			1	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)	1.6			V
		Shutdown mode (EN=0)			0.5	V

6.7 Electrical Characteristics REF54410 (continued)

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18 V		0.25	0.7	uA
		V_{IN} = V_{EN} = 18 V, –40°C ≤ T_A ≤ 125°C			1.2	uA
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C			250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C			400	mV
I_{SC}	Short circuit current	V_{OUT} = 0V		21		mA

(1) Specification subject to change with Q grade production release.
(2) ESR for the capacitor can range from 10 mΩ to 1 Ω.

6.8 Electrical Characteristics REF54450

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted (1)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25°C		–0.02		0.02	%
	Output voltage temperature coefficient	Q grade; –40°C ≤ T_A ≤ 125°C				1.5	ppm/°C
		C grade; 0°C ≤ T_A ≤ 70°C				0.8	
LINE AND LOAD REGULATION							
$\Delta V_O / \Delta V_{IN}$	Line regulation	V_{OUT} + V_{DO} ≤ V_{IN} ≤ 10 V			4	30	ppm/V
		V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, 0°C ≤ T_A ≤ 70°C			1	5	
		V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C			1	10	
$\Delta V_O / \Delta I_L$	Load regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C			5	30	ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C			5	20	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C			5	40	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C			5	25	
NOISE							
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz			0.45		ppm_{p-p}
		f = 0.1 Hz to 10 Hz, , C_{NR} = 100µF			0.08		
e_n	Output voltage noise	f = 10 Hz to 1 kHz			0.7		ppm_{rms}
HYSTERESIS AND LONG-TERM STABILITY							
ΔV_{OUT_LTD}	Long-term stability	250h T_A = 35°C			14		ppm
		1000h T_A = 35°C			25		
ΔV_{OUT_HYS}	Output voltage hysteresis	25°C, 0°C, 70°C, 25°C (cycle 1)			15		ppm
		25°C, 0°C, 70°C, 25°C (cycle 2)			0.8		
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF			0.63		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	–40°C ≤ T_A ≤ 125°C		0.1			µF
C_{OUT}	Stable output capacitor range (2)	–40°C ≤ T_A ≤ 125°C		1		100	µF
POWER SUPPLY							
V_{IN}	Input voltage			V_{OUT} + V_{DO}		18	V
I_Q	Quiescent current	T_A = 25°C	Active mode		260	310	µA
		–40°C ≤ T_A ≤ 125°C				420	µA
		T_A = 25°C	Shutdown mode		0.25	0.7	uA
		–40°C ≤ T_A ≤ 125°C				1	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18 V			0.25	0.7	uA
		V_{IN} = V_{EN} = 18 V, –40°C ≤ T_A ≤ 125°C				1.2	uA
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C				250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C				400	mV

6.8 Electrical Characteristics REF54450 (continued)

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted [(1)]

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{SC}	Short circuit current	V_{OUT} = 0V		21		mA

(1) REF54450 device is in preview state. All specifications are preliminary and subject to change before production release.
(2) ESR for the capacitor can range from 10 mΩ to 1 Ω.

6.9 Electrical Characteristics REF54500

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted [1]

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage accuracy	T_A = 25°C	–0.02		0.02	%
	Output voltage temperature coefficient	Q grade; –40°C ≤ T_A ≤ 125°C			1.5	ppm/°C
		C grade; 0°C ≤ T_A ≤ 70°C			0.8	
LINE AND LOAD REGULATION						
$\Delta V_O / \Delta V_{IN}$	Line regulation	V_{OUT} + V_{DO} ≤ V_{IN} ≤ 10 V		4	30	ppm/V
$\Delta V_O / \Delta V_{IN}$	Line regulation	V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, 0°C ≤ T_A ≤ 70°C		1	5	ppm/V
		V_{OUT} + V_{DO} ≤ V_{IN} ≤ 18 V, –40°C ≤ T_A ≤ 125°C		1	10	
$\Delta V_O / \Delta I_L$	Load regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C		5	30	ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C		5	20	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, –40°C ≤ T_A ≤ 125°C		5	40	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT} + V_{DO}, 0°C ≤ T_A ≤ 70°C		5	25	
NOISE						
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz		0.45		ppm_{p-p}
		f = 0.1 Hz to 10 Hz, , C_{NR} = 100µF		0.08		
e_n	Output voltage noise	f = 10 Hz to 1 kHz		0.7		ppm_{rms}
HYSTERESIS AND LONG-TERM STABILITY						
ΔV_{OUT_LTD}	Long-term stability	250h T_A = 35°C		14		ppm
		1000h T_A = 35°C		25		
ΔV_{OUT_HYS}	Output voltage hysteresis	25°C, 0°C, 70°C, 25°C (cycle 1)		18		ppm
		25°C, 0°C, 70°C, 25°C (cycle 2)		0.8		
TURN ON TIME						
t_{ON}	Turn-on time	0.1% settling, C_{OUT} = 1µF		0.7		ms
CAPACITIVE LOAD						
C_{IN}	Stable input capacitor range	–40°C ≤ T_A ≤ 125°C	0.1			µF
C_{OUT}	Stable output capacitor range [2]	–40°C ≤ T_A ≤ 125°C	1		100	µF
POWER SUPPLY						
V_{IN}	Input voltage		V_{OUT} + V_{DO}		18	V
I_Q	Quiescent current	T_A = 25°C; Active mode		300	380	µA
		–40°C ≤ T_A ≤ 125°C; Active mode			430	µA
		T_A = 25°C; Shutdown mode		0.25	0.7	uA
		–40°C ≤ T_A ≤ 125°C; Shutdown mode			1	uA
V_{EN}	Enable pin voltage	Active mode (EN=1)	1.6			V
		Shutdown mode (EN=0)			0.5	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 18 V		0.25	0.7	uA
		V_{IN} = V_{EN} = 18 V, –40°C ≤ T_A ≤ 125°C			1.2	uA
V_{DO}	Dropout voltage	I_L = 5mA, –40°C ≤ T_A ≤ 125°C			250	mV
		I_L = 10mA, –40°C ≤ T_A ≤ 125°C			400	mV

6.9 Electrical Characteristics REF54500 (continued)

Typical specifications at T_A = 25°C, min-max specifications verified across temperature range, I_L = 0 mA, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, C_{NR} = Open, V_{IN} = V_{OUT} + V_{DO}, unless otherwise noted [(1)]

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{SC}	Short circuit current	V_{OUT} = 0V		21		mA

(1) REF54500 device is in preview state. All specifications are preliminary and subject to change before production release.
(2) ESR for the capacitor can range from 10 mΩ to 1 Ω.

6.10 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5 V, I_L = 0 mA, C_{Out} = 10 µF, C_{NR} = Open, C_{IN} = 0.1 µF, V_{REF} = 2.5 V (unless otherwise noted)

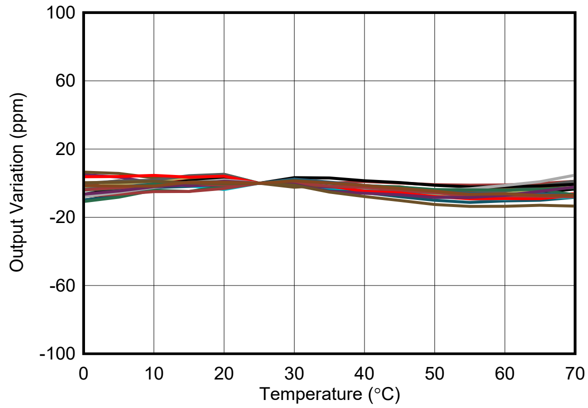

Figure 6-1. Output Voltage Vs Free-Air Temperature for C grade

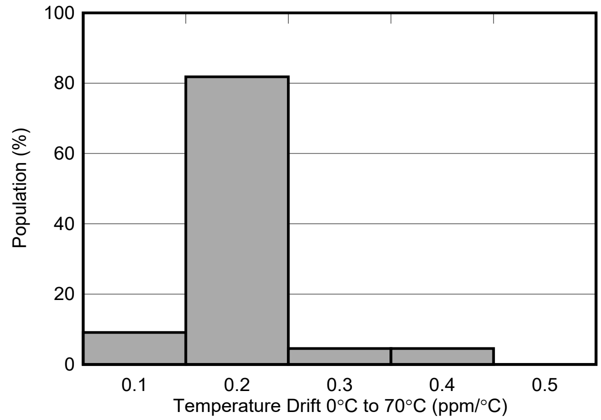

Figure 6-2. Temperature Drift Distribution

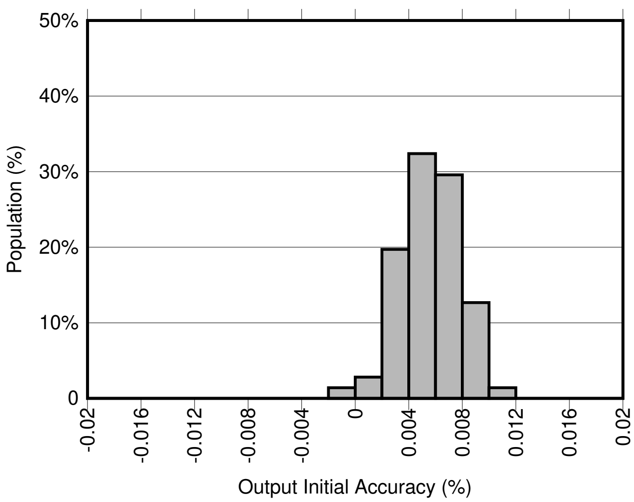

Figure 6-3. Accuracy Distribution

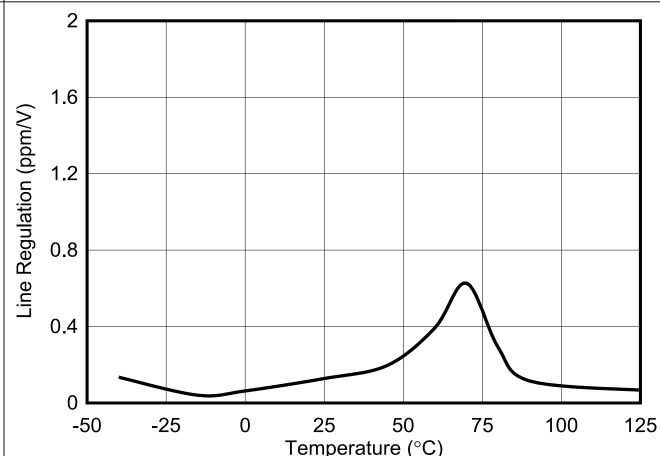

Figure 6-4. Line Regulation vs Temperature

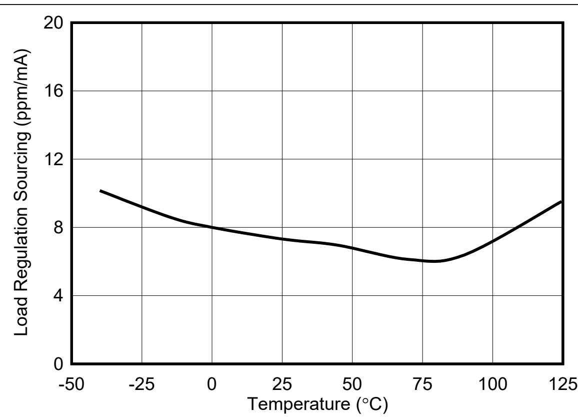

Figure 6-5. Load Regulation (Sourcing) vs Temperature

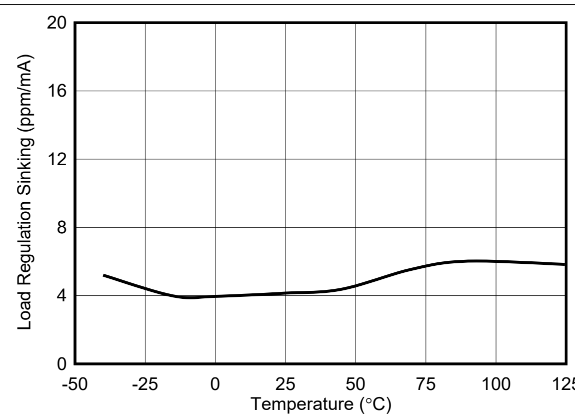

Figure 6-6. Load Regulation (Sinking) vs Temperature

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5 V, I_L = 0 mA, C_{Out} = 10 µF, C_{NR} = Open, C_{IN} = 0.1 µF, V_{REF} = 2.5 V (unless otherwise noted)

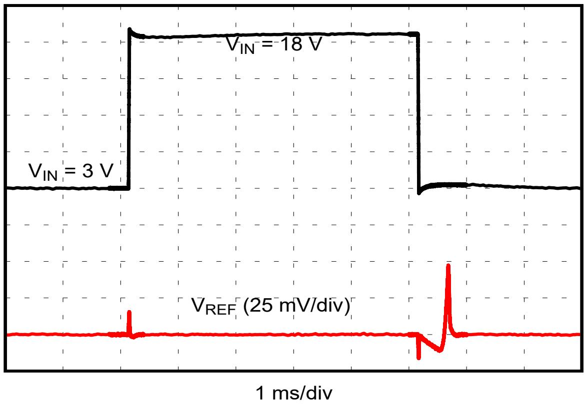

Figure 6-7. Line Transient Response

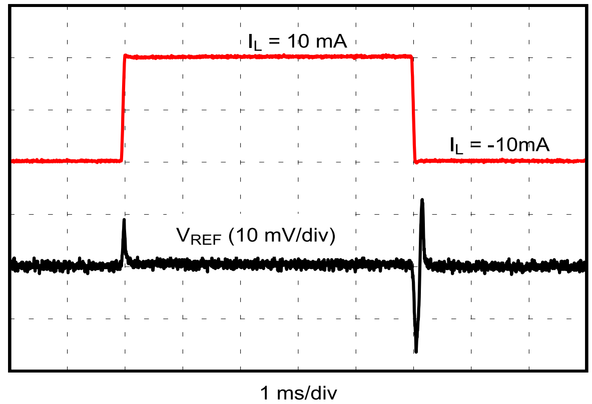

Figure 6-8. Load Transient Response (C_{OUT} = 10 µF)

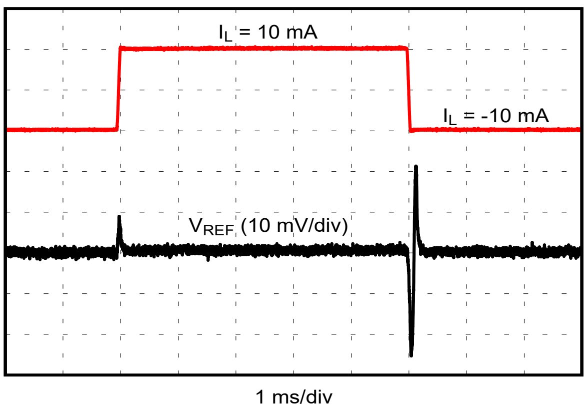

Figure 6-9. Load Transient Response (C_{OUT} = 1 µF)

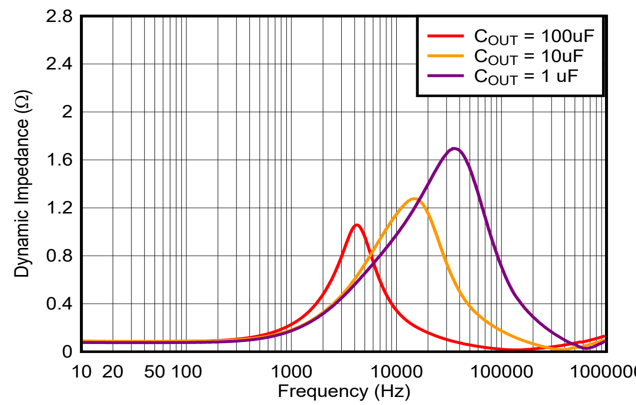

Figure 6-10. Output Impedance

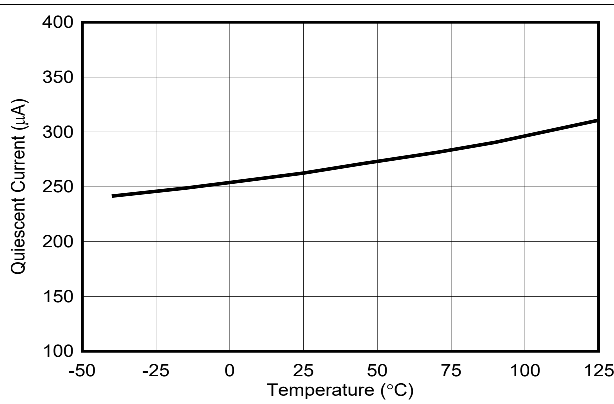

Figure 6-11. Quiescent Current vs Temperature

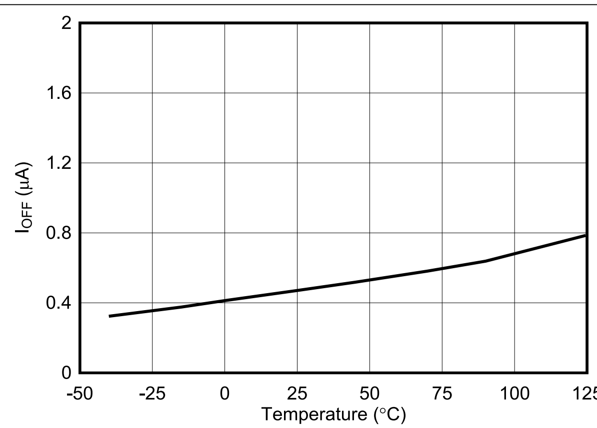

Figure 6-12. Shutdown Current vs Temperature

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.5 V, I_L = 0 mA, C_{Out} = 10 µF, C_{NR} = Open, C_{IN} = 0.1 µF, V_{REF} = 2.5 V (unless otherwise noted)

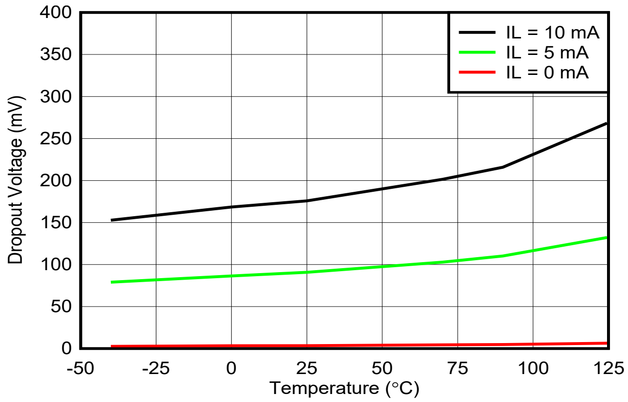

Figure 6-13. Dropout Voltage vs Temperature

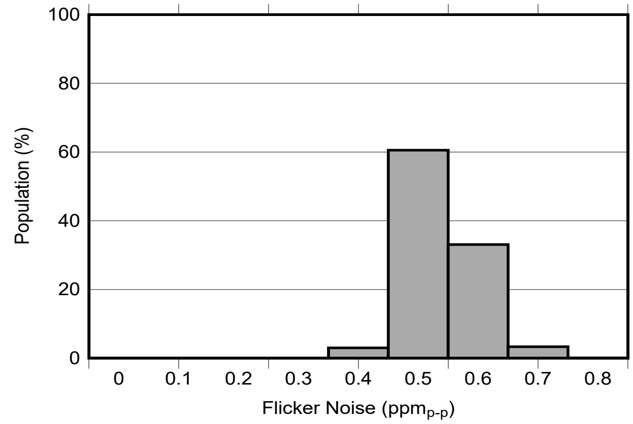

Figure 6-14. 0.1-Hz to 10-Hz Voltage Noise Distribution (C_{NR} = Open)

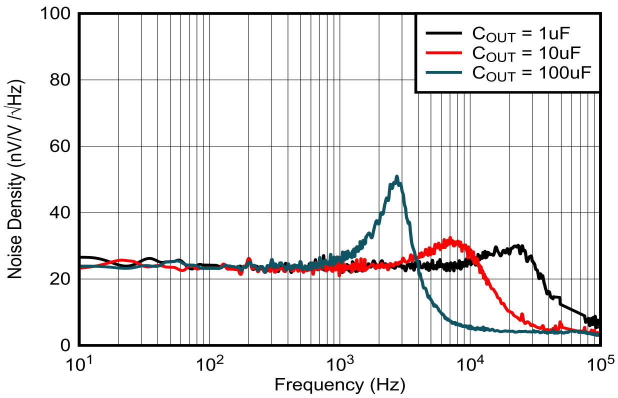

Figure 6-15. Noise Performance 10 Hz to 100 kHz (C_{NR} = Open)

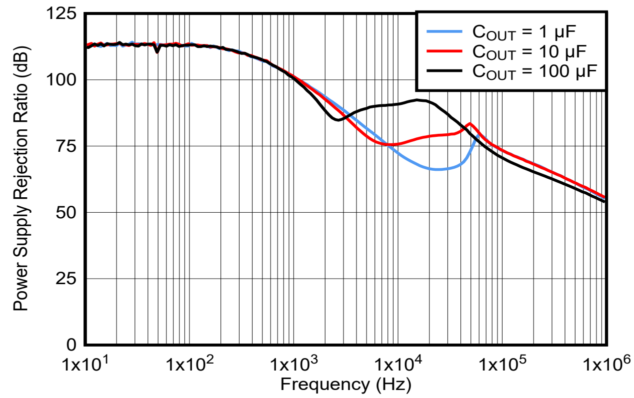

Figure 6-16. Power-Supply Rejection Ratio vs Frequency

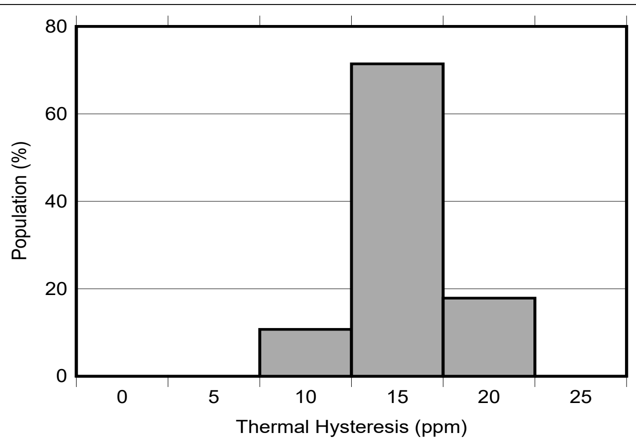

Figure 6-17. REF54250 Thermal Hysteresis Distribution (0°C to 70°C)

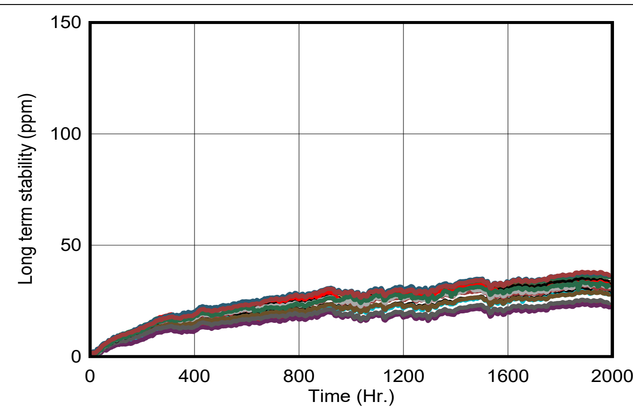

Figure 6-18. Long-Term Stability (First 2000 Hours)

7 Parameter Measurement Information

7.1 Temperature Drift

The REF54 is designed and tested for a minimal output voltage temperature drift, which is defined as the change in output voltage over temperature. Every unit shipped is tested at multiple temperatures to make sure that the product meets data sheet specifications. The temperature coefficient is calculated using the box method in which a box is formed by the min/max limits for the nominal output voltage over the operating temperature range. REF54 device C variant has maximum temperature coefficient of 0.8 ppm/°C from 0°C to 70°C and REF54 device Q variant has maximum temperature coefficient of 1.5 ppm/°C from -40°C to 125°C. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Due to temperature curvature correction to achieve low-temperature drift, the temperature drift is expected to be non-linear. See *SLYT183* for more information on the box method. The box method equation is shown in Equation 1:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(25°C)} \times \text{Temperature Range}} \right) \times 10^6 \quad (1)$$

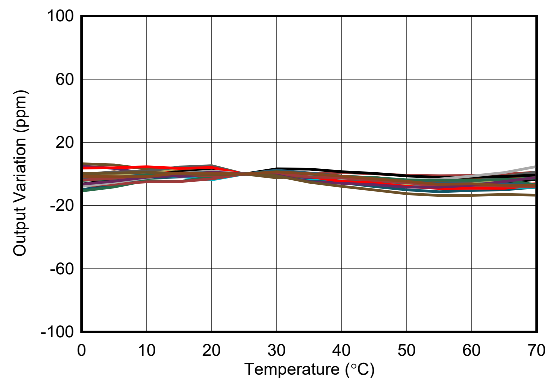

Figure 7-1. Output Voltage Vs Free-Air Temperature

7.2 Long-Term Stability

Long-term stability is a key performance parameter for series voltage references in all precision applications. This is defined as variation of reference voltage over time. The long-term stability value is tested in a typical setup that reflects standard PCB board manufacturing practices. The boards are made of standard FR4 material, the board does not have special cuts or grooves around the devices or go through burn-in process to relieve the mechanical stress of the PCB. These conditions reflect real world use case scenario and common manufacturing techniques.

During the long-term stability testing, precautions are taken to make sure that only the long-term stability drift is being measured. The boards are maintained at 35°C ± 0.02°C in an oil bath. The oil bath makes sure that the temperature is constant across the device over time. The measurements are captured every 30 minutes with a calibrated 8.5 digit multimeter.

Typical long-term stability characteristic are expressed as a deviation over time. Figure 7-2 shows the typical drift value for the REF54 V_{OUT} is 25 ppm from 0 to 1000 hours. The REF54 experiences the highest drift in the initial 1000 hr, subsequent deviation is typically lower than previous 1000 hours.

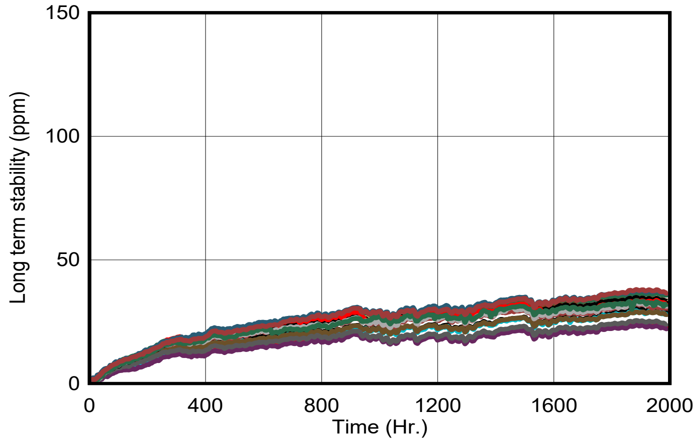

Figure 7-2. Long-Term Stability SOIC -2000 Hours (V_{OUT})

7.3 Noise Performance

7.3.1 1/f Noise

1/f noise, also known as flicker noise, is dominant mostly in the lower frequency bands. REF54 data sheet specifies flicker noise for 0.1 Hz to 10 Hz frequency band where 1/f noise has maximum power. Since the 1/f noise is an extremely low value, the frequency of interest is amplified and filtered through a precise band filter with very low noise floor as shown in Figure 7-3.

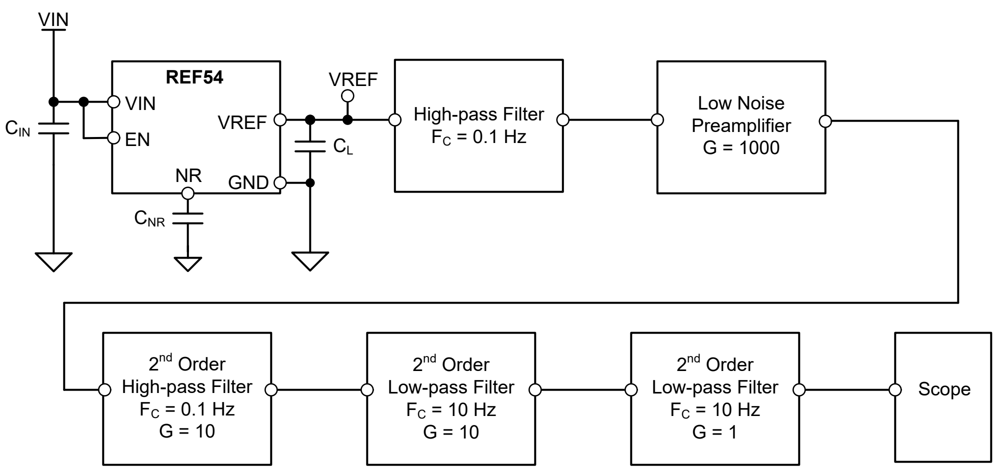

Figure 7-3. 1/f Noise Test Setup

Figure 7-4 shows typical distribution of flicker noise for multiple devices where more than 1000 samples have been captured for each device.

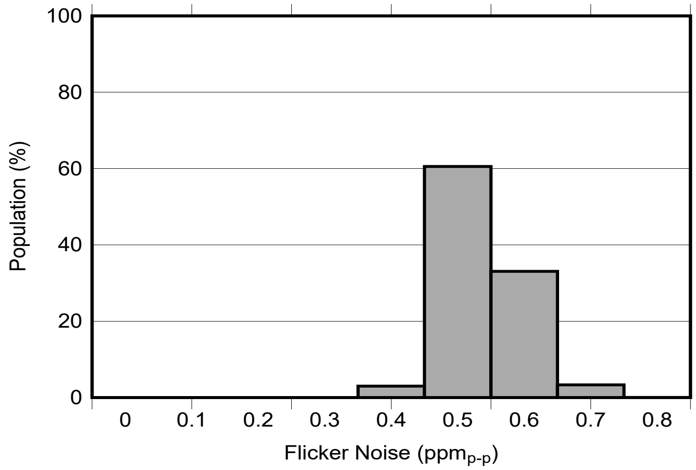

Figure 7-4. 0.1-Hz to 10-Hz Voltage Noise Distribution (C_{NR} = Open)

Noise sensitive designs prefer the lowest 1/f noise for the highest precision measurements. REF54 offers NR pin which creates a low pass filters on the band gap with typical resistance of 13 kΩ. 100 µF capacitor on NR pin removes the whole band of flicker noise (0.1 Hz) from the band gap reference as shown in Figure 7-5. A 10 µF capacitor on the NR pin creates a 1 Hz low-pass filter for the bandgap.

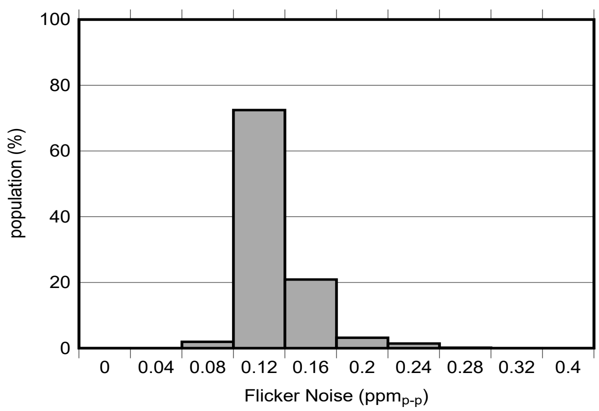

Figure 7-5. 0.1-Hz to 10-Hz Voltage Noise (C_{NR} = 100 µF)

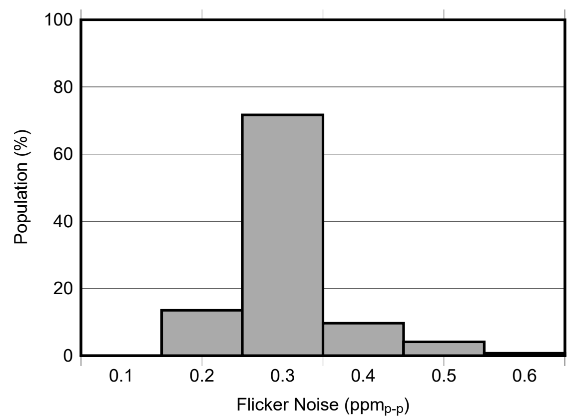

Figure 7-6. 0.1-Hz to 10-Hz Voltage Noise (C_{NR} = 10 µF)

7.3.2 Broadband Noise

Broadband noise or white noise is flat over the whole spectrum which is restricted by the bandwidth of internal bandgap reference. The broadband noise is measured by high-pass filtering the output of the REF54 and measuring the result on a precision spectrum analyzer as shown in Figure 7-7. The DC component of the REF54 is removed by using a high-pass filter and then amplified. Two stages of small gain has been used to maximize the noise bandwidth analysis.

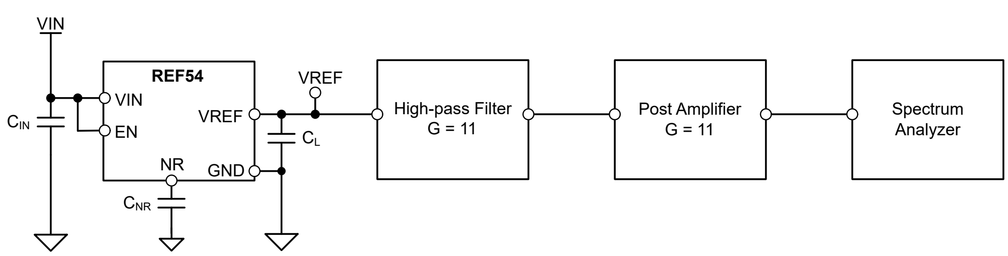

Figure 7-7. Broadband Noise Test Setup

Figure 7-8 shows the typical white noise floor for REF54. Designer can use NR pin to restrict the noise bandwidth to achieve required resolution for the signal chain. Connecting 1 µF at NR pin creates a typical low pass filter of 12 Hz for the band gap noise which reduces the white noise floor of REF54. Capacitor >1 µF eliminates all the noise in > 10 Hz band.

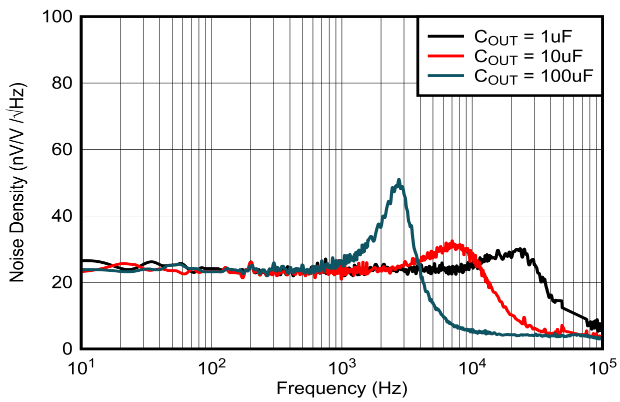

Figure 7-8. Noise Performance 10 Hz to 100 kHz (C_{NR} = Open)

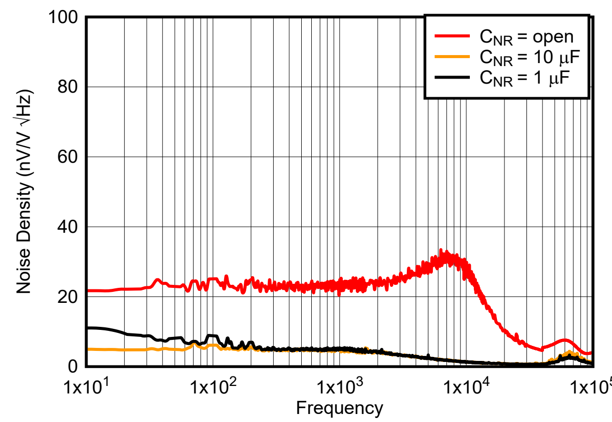

Figure 7-9. Noise Performance 10 Hz to 100 kHz (C_{OUT}) = 10 µF

7.4 Thermal Hysteresis

Thermal hysteresis is measured with the REF54 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. The fist thermal cycle for C variant is shown in Figure 7-10 and second cycle is shown in Figure 7-11. Thermal hysteresis for REF54250CDR settles after first cycle. Hysteresis can be expressed by Equation 2

$$V_{HYST} = \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (2)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range (for example, 0°C to 70°C) and returns to 25°C.

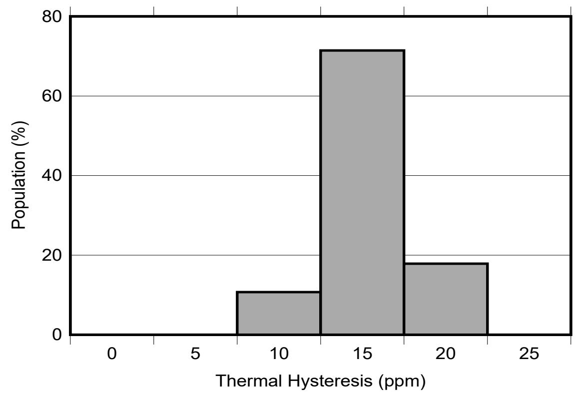

Figure 7-10. Thermal Hysteresis Distribution (0°C to 70°C) - Cycle 1 (REF54250CDR)

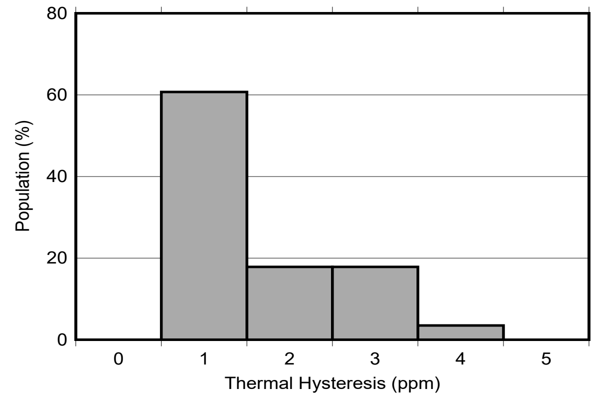

Figure 7-11. Thermal Hysteresis Distribution (0°C to 70°C) - Cycle 2 (REF54250CDR)

7.5 Solder Heat Shift

The packaging materials of the REF54 have different coefficients of thermal expansion than the PCB material, resulting in stress change on the device die when the part is heated during soldering process and cooled down afterwards. Thermal shock due to reflow and stress change on the device die causes the output voltages to shift, degrading the initial accuracy performance of the product. Reflow soldering is a common cause of this error. To quantify the impact, 32 devices were soldered on printed circuit boards using lead-free solder paste and the paste manufacturer suggested reflow profile to illustrate this effect. The reflow profile is as shown in Figure 7-12. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 137 mm × 168 mm.

For recommended reflow profiles using 'Sn-Pb Eutectic Assembly' or 'Pb-Free Assembly' please refer JEDEC J-STD-020 standard.

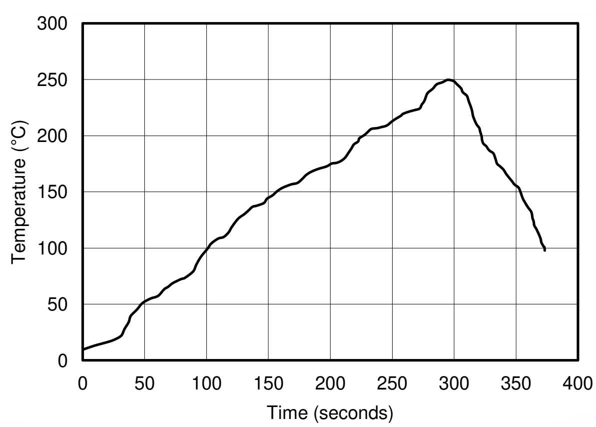

Figure 7-12. Reflow Profile

The reference output voltage is measured before and after the reflow process. Solder shift depends on the size, thickness, and material of the printed circuit board. An important note is that the Figure 7-13 displays the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize the exposure to thermal stress.

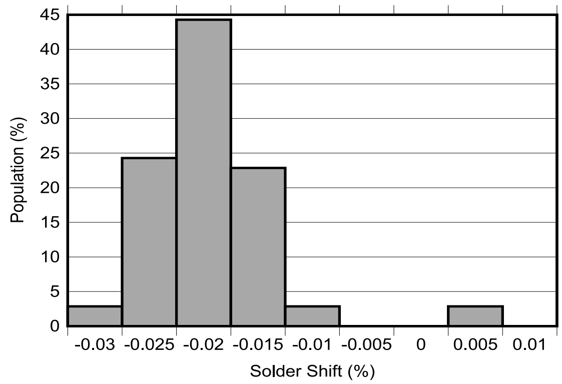

Figure 7-13. Solder Shift

7.6 Power Dissipation

The REF54 voltage references are capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to make sure that the device does not exceed the maximum power dissipation rating. The maximum power dissipation of the device can be calculated with Equation 3:

$$T_J = T_A + P_D \times R_{\theta JA} \tag{3}$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

Because of this relationship, acceptable load current in high temperature conditions can be less than the maximum current-sourcing capability of the device. Do not operate the device outside of the maximum power rating because doing so can result in premature failure or permanent damage to the device.

8 Detailed Description

8.1 Overview

The REF54 is family of high precision series references that are designed for excellent initial voltage accuracy and drift over time and temperature, and offer excellent noise while consuming low power. The *Figure 8-1* is a simplified block diagram of the REF54 showing basic band-gap topology.

8.2 Functional Block Diagram

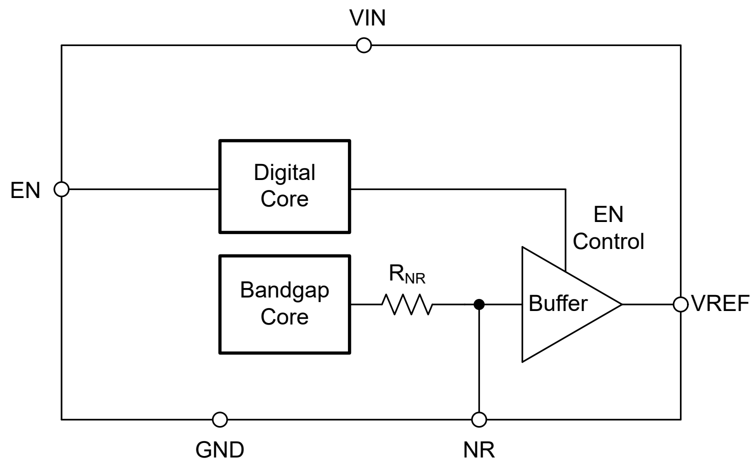

Figure 8-1. REF54 Functional Block Diagram

8.3 Feature Description

8.3.1 EN Pin

The output of REF54 comes in active state when EN pin voltage is more than 1.6V or EN pin is left floating. The enable feature of the REF54 is designed to achieve low quiescent current (I_Q) . No current is drawn from EN pin when EN pin is voltage is lower than VIN pin voltage. The device must be in active mode for normal operation. The REF54 can be placed in shutdown mode by pulling the EN pin low. When in shutdown mode, the output of the device is disabled and the quiescent current of the device reduces to 1.2 µA in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See the electrical table for logic high and logic low voltage levels.

8.3.2 NR Pin

Decoupling NR pin in REF54 creates a low pass filter in combination with the internal resistance of 13 kΩ to eliminate internal band gap noise. Unlike regular low pass filter at the output of the reference, connecting a capacitor on NR pin doesn't affect the output impedance hence extra buffer is not needed. Leakage of the capacitor directly impacts the accuracy and temperature drift. If NR functionality is used, choose a capacitor which has low leakage over temperature (film capacitors, COG, X7R (MLCC) are recommended). Note that using the capacitor on NR pin also increases start-up time.

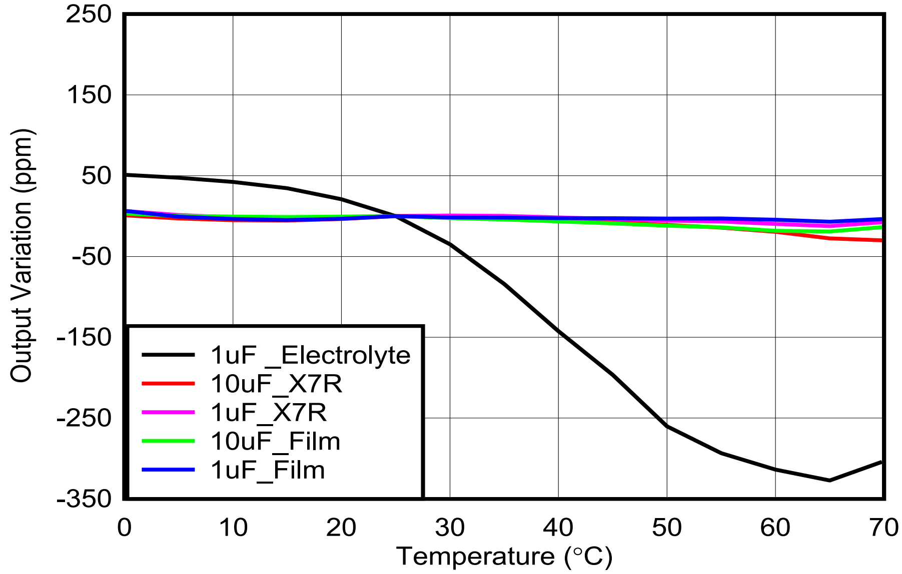

Figure 8-2. Temperature Drift Comparison with Film and X7R and Electrolyte Capacitor on NR

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The REF54 is designed for the applications where high precision is required at lower power. Low temperature drift and noise makes the REF54 excellent attach for high precision data converters to achieve best gain drift and resolution.

Table 9-1. List of companion Data Converters with REF54

APPLICATION	DATA CONVERTER
Precision Data Acquisition	ADS8900B, ADS1278, ADS1262, DAC80501, DAC8562
Passive Seismic Monitoring	ADS1285
Industrial Instrumentation	ADS127L11, ADS8699, ADS1256, ADS1251, DAC9881, DAC8811, DAC1220, DAC80508
Test & Measurement	ADS1262, ADS8598H, ADS131M08, ADS8686S, ADS8881, DAC11001B, DAC91001A, DAC7744
Power Monitoring, PLC Analog I/O	ADS131E04, ADS131A02
Field Transmitters	ADS1247, ADS1220

9.2 Typical Applications

9.2.1 Basic Voltage Reference Connection

Figure 9-1 shows the basic configuration for the REF54 references. Connect bypass capacitor C_{IN} and output capacitor C_{OUT} as per the guidelines in Section 9.2.1.2.

Basic Connection Diagram

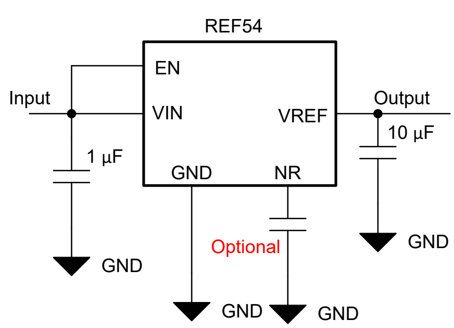

Figure 9-1. Basic Reference Connection

9.2.1.1 Design Requirements

A detailed design procedure is based on a design example. For this design example, use the parameters listed in Table 9-2 as the input parameters.

Table 9-2. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	3 V
Input capacitor	0.1-µF
Output capacitor	10-µF

9.2.1.2 Detailed Design Procedure

A bulk capacitor (0.1 µF to 10 µF) must be connected to the supply to improve transient response in the applications where the supply voltage can fluctuate. Connect an additional 0.1 µF capacitor at VIN pin closer to the device to bypass high frequency supply noise.

A low ESR (maximum 1 Ω) capacitor of 1 µF to 100 µF must be connected to the output to provide stable output. For very low noise applications, special care must be taken with X7R and other MLCC capacitors due to their piezoelectric effect. Piezoelectric property of multilayer ceramic capacitors (MLCC) can introduce a µV range noise due to mechanical vibrations, potentially dominating the noise of the REF54. More information on how the piezoelectric effect can be explored in systems can be found in Stress-induced outbursts: Microphonics in ceramic capacitors (Part 1) and Stress-induced outbursts: Microphonics in ceramic capacitors (Part 2). Designer must use film capacitors for noise sensitive applications. TI recommends placing the REF54 reference as close to the load as possible to minimize IR drop due to trace resistance.

The transient startup response of the REF54 is shown in Figure 9-2. The startup response of the REF54 family is dependent on the output and NR pin capacitor. Increasing the output capacitor improves the load transient performance of the device, however this also increases the startup time. Figure 9-3 shows the startup time with C_{NR} = 10 µF, increases to 3 seconds.

9.2.1.3 Application Curves

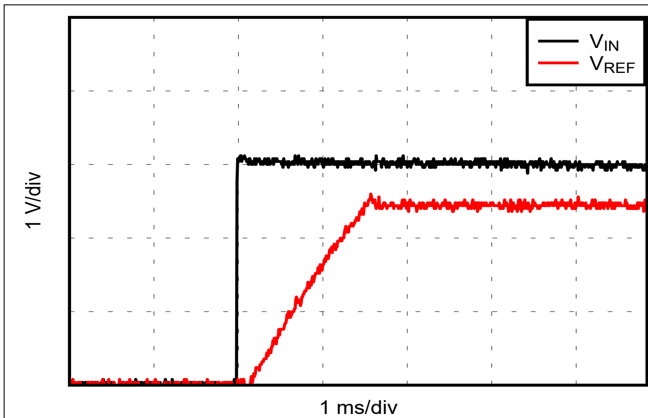

Figure 9-2. REF54250CDR Startup Response (C_{Out}= 10 uF, C_{NR}= Open)

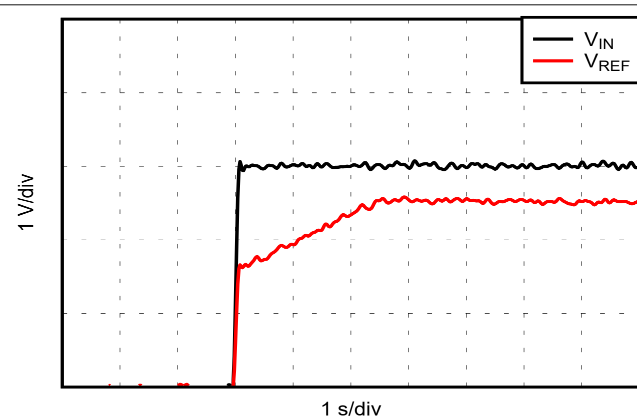

Figure 9-3. REF54250CDR Startup Response (C_{Out}= 10 uF, C_{NR}= 10uF)

9.2.2 Reference Attach With High Precision ADC

High precision ADCs require external precision voltage references to achieve the best SNR and gain drift with temperature and time. REF54 has flat dynamic impedance at lower frequency. However it's dynamic impedance increases for higher sampling rate. A low noise - low offset buffer with good bandwidth helps to improve THD and droop performance to achieve > 18 bit ENOB at higher sampling rate. Figure 9-4 shows evaluation circuit for ADS1285. Figure 9-5 and Figure 9-6 show the peak to peak code variation for constant DC input of 0 V and 2.08 V respectively. The performance meets data sheet specifications of ADS1285 with REF54.

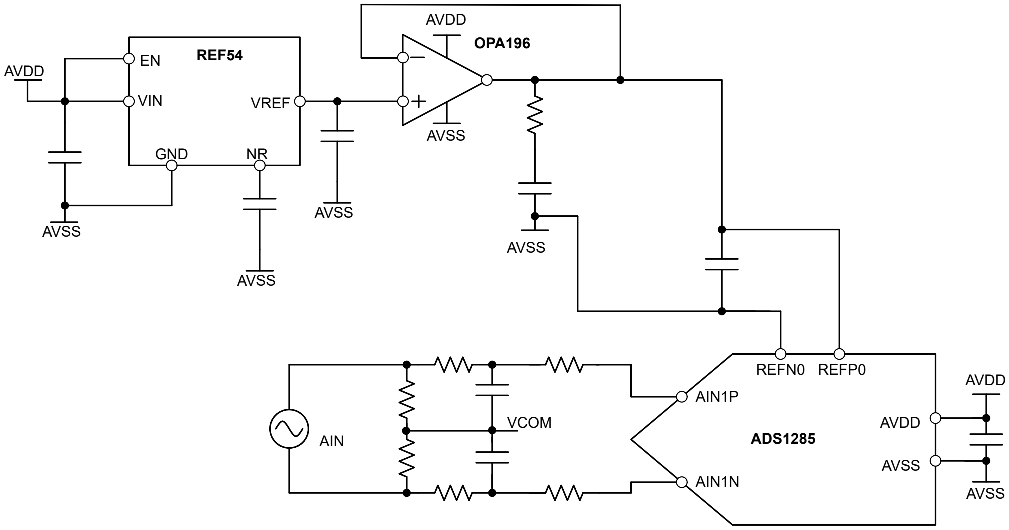

Figure 9-4. REF54 Attach With ADS1285

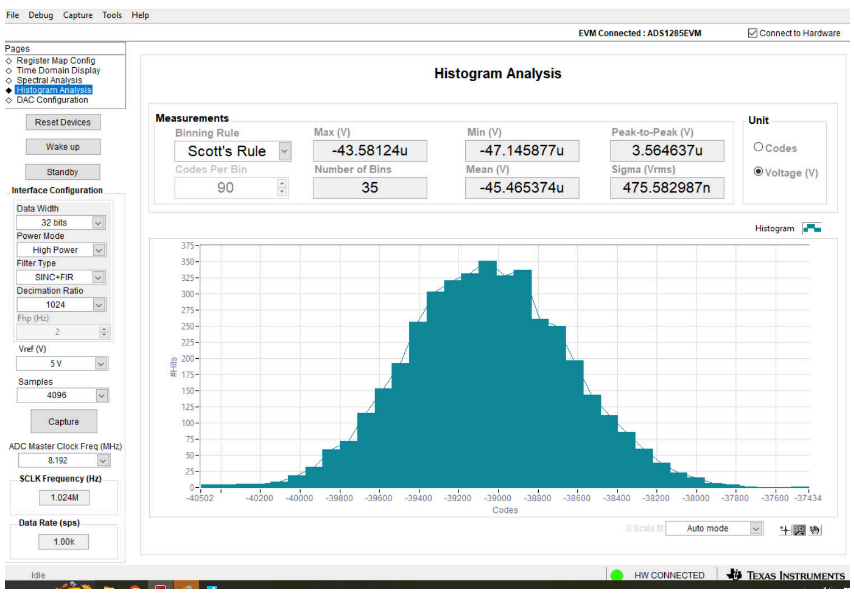

Figure 9-5. DC Measurement With ADS1285 (VIN = 0 V)

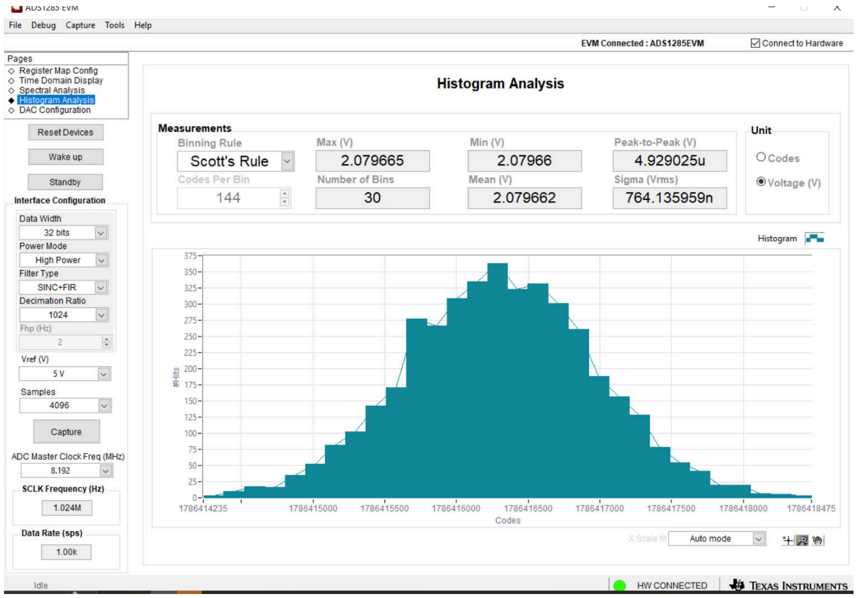

Figure 9-6. DC Measurement With ADS1285 (VIN = 2.0796 V (Close to FSR))

9.3 Power Supply Recommendation

The REF54 family of references features a low-dropout voltage. These references can be operated with a supply of only 250 mV above the output voltage for 5 mA output current conditions. TI recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF. REF54 family have excellent PSRR (100 dB at 1Khz) which relaxes the requirement of clean power supply for the designer.

During start-up the REF54 can experience moments of high input current due to the output capacitors. The input current can momentarily rise to short circuit current I_{SC}.

9.4 Layout

9.4.1 Layout Guidelines

- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is from 0.1 µF to 10 µF. If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. The smallest capacitor must be placed closest to the device.
- The output must be decoupled with a 1 µF to 100 µF low ESR (maximum 1 Ω) capacitor.
- Place a 1 µF to 100 µF low leakage noise filtering capacitor between the NR pin and ground.

9.4.2 Layout Example

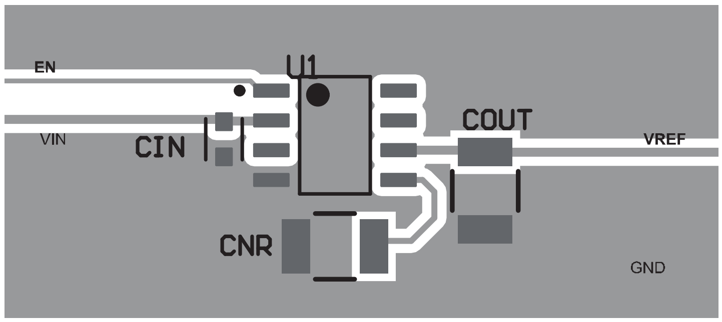

Figure 9-7. Layout Example for SOIC package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Voltage Reference Design Tips For Data Converters*
- Texas Instruments, *Voltage Reference Selection Basics*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2023) to Revision B (June 2024)	Page
• Changed the REF54410CDR device variant status from preview to production data	3
• Added 2000 hours long term stability spec	6
• Added the 2000 hours data to the long-term stability graphs Figure 6-16 and Figure 6-18	16
• Added the 2000 hours long term stability data to Figure 7-2	19
• Added variant names to the thermal hysteresis graphs Figure 7-10 and Figure 7-11	22

Changes from Revision * (November 2023) to Revision A (December 2023)	Page
• Production Data Release	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF54250CDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	R5425C	Samples
REF54410CDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R5441C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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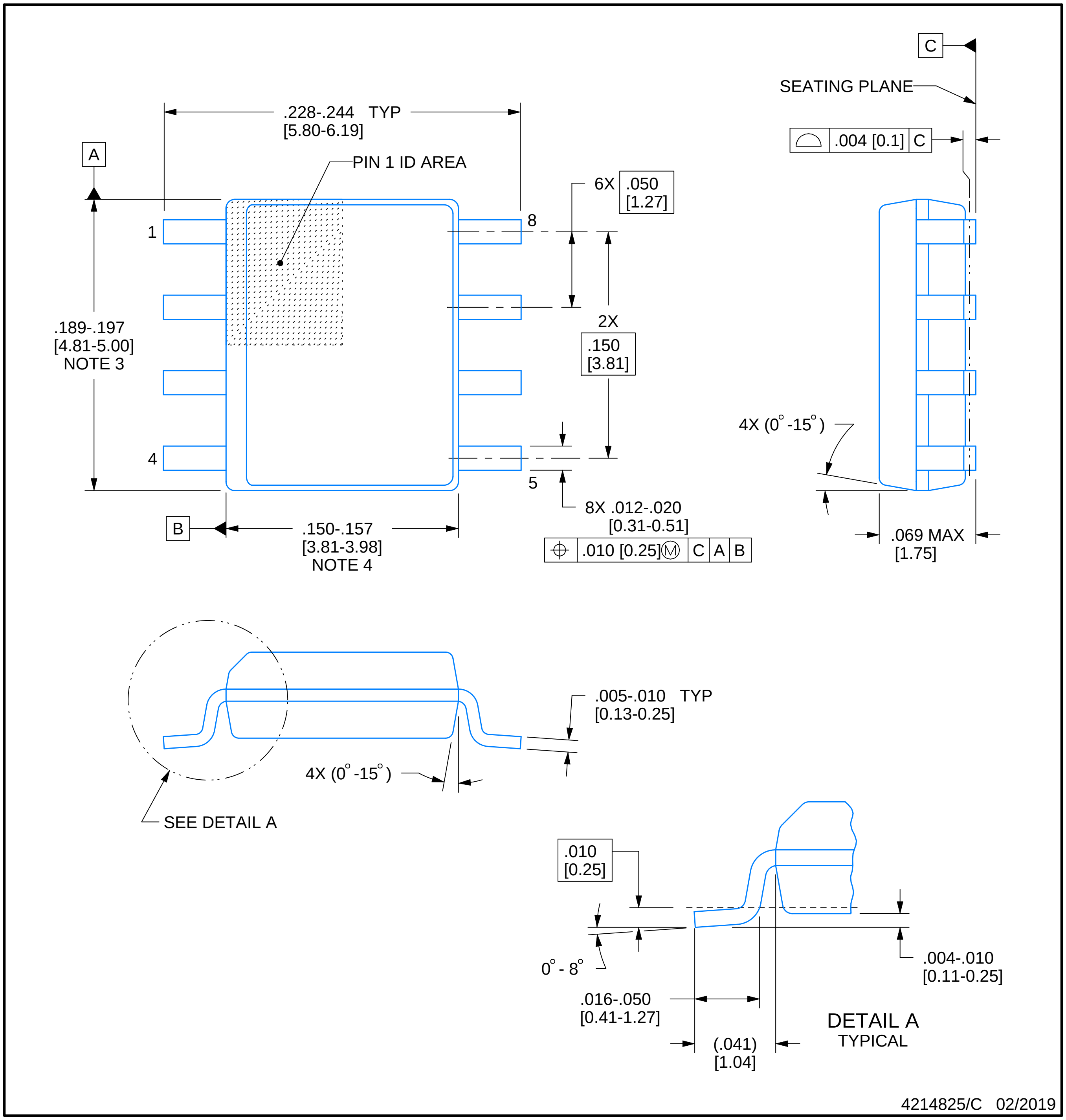
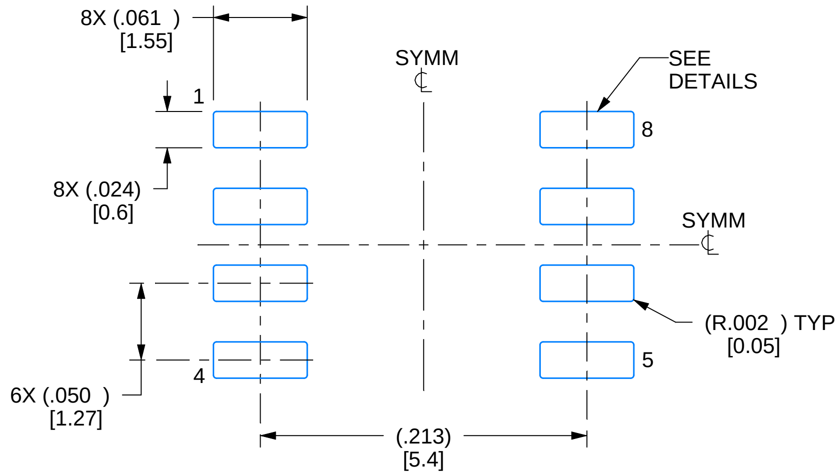
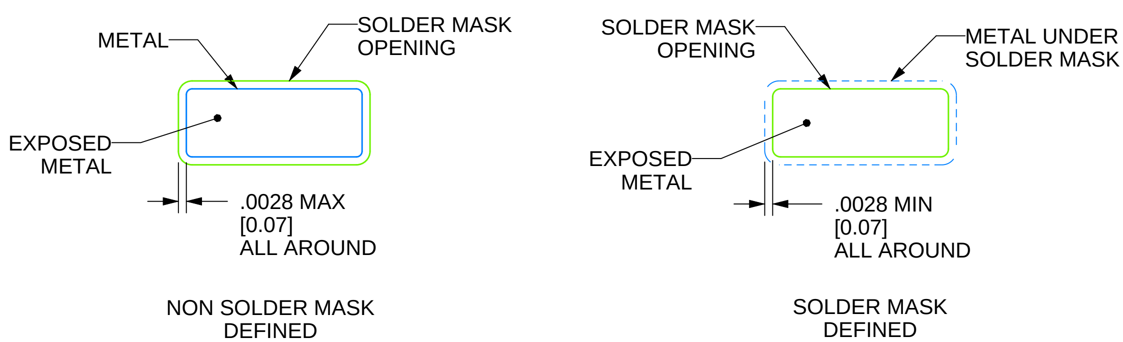


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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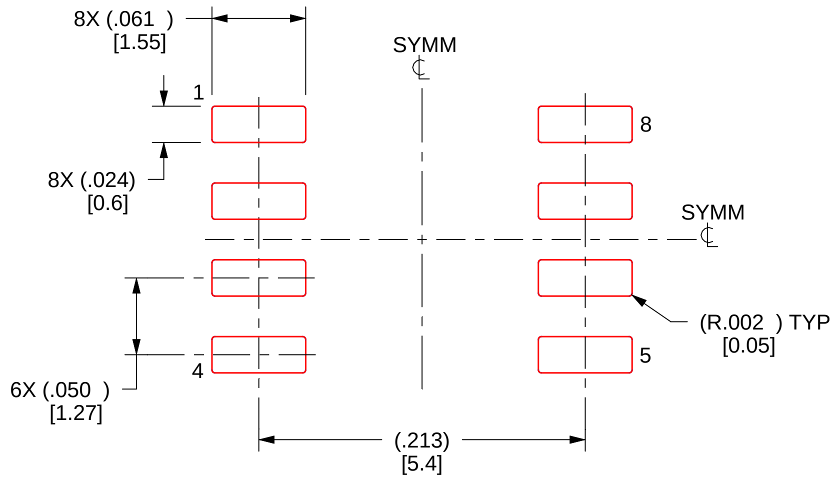
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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