REF80 Temperature-Controlled Buried Zener Reference with 0.05ppm/°C Drift and < 1ppm Stability

1 Features

- 7.6V ultra-precision reference with minimal number of external components
- Ultra-low temperature drift: 0.05ppm/°C
- Excellent long term stability: < 1ppm
- Integrated heater with temperature stable indicator
- 1/f noise (0.1Hz to 10Hz) : 0.16ppm$_{pk-pk}$
- Input Voltage range: 10V to 16.5V
- Heater supply range: 10V to 42V
- Hermetically sealed ceramic package (20 pin LCCC)

2 Applications

- Parametric measurement unit
- Lab and field instrumentation
- Precision weight scales
- Battery test equipment
- Digital multimeter
- Source measurement unit
- Data acquisition

3 Description

The REF80 is a highly integrated ultra-low drift buried zener precision voltage reference. The REF80 combines a precision 7.6V reference with an internal heater to achieve extremely low temperature drift of 0.05ppm/°C. The integrated heater maintains the internal temperature of the die at a constant set point. This helps the reference voltage stay constant irrespective of ambient temperature variations. The device internal temperature is pre-programmed to eliminate design complexities. This allows for fast design cycles, easy bring up and no dependence on high-cost external precision components.

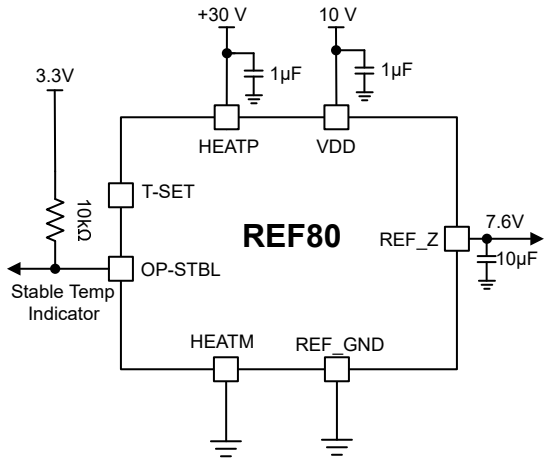
The REF80 family is available in a 20-pin LCCC package. The LCCC package is a hermetically sealed ceramic package that enables ultra-low long-term stability specification of 1ppm, critical for applications that demand a long time period without calibration. The package also offers excellent immunity against humidity variation.

Device Information

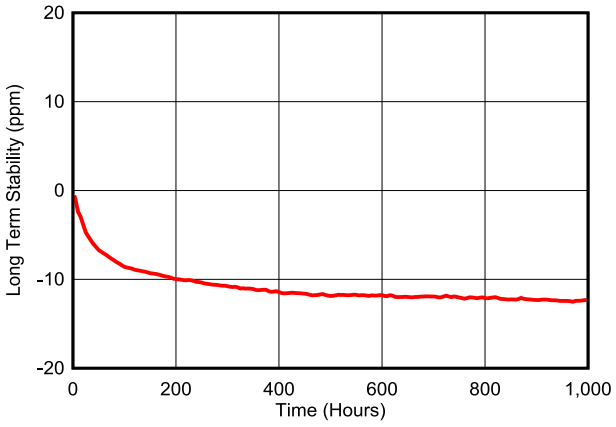
PART NAME	PACKAGE (1)	BODY SIZE (NOM) (2)
REF80	LCCC (20)	8.89mm × 8.89mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

ADVANCE INFORMATION



REF80 Circuit Diagram (With Supply and Passive Requirement)



Reference Voltage Drift Vs Time

ADVANCE INFORMATION

Table of Contents

4 Device Comparison Table

PRODUCT	V_{REF_Z}
REF80000B1NAJT	7.6V

ADVANCE INFORMATION

5 Pin Configuration and Functions

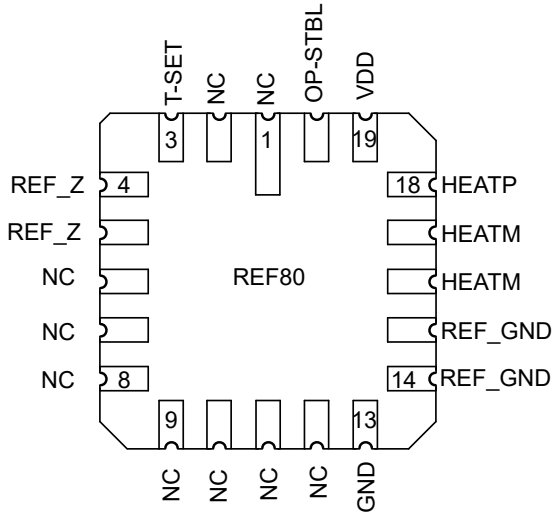


Figure 5-1. NAJ Package
20-Pin LCCC
Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	Number		
NC	1, 2, 6-12	No Connect	No connect pin. Leave this pin floating or connected to GND.
T-SET	3	Input	Connect resistor to adjust the heater temperature. Leave the pin floating to use factory programmed heater set point. Refer Section 7.3.1 for more details.
REF_Z	4,5	Output	Reference voltage output. Connect an output capacitor between 10µF to 100µF for the best performance.
GND	13	GND	This pin should be shorted to REF_GND pin.
REF_GND	14, 15	Ground	Reference ground pin. This pin carries the current through the buried zener reference.
HEATM	16, 17	Power	Heater power supply negative connection.
HEATP	18	Power	Heater power supply positive connection.
VDD	19	Power	Power supply for buried zener core and buffer.
OP_STBL	20	Output	Active high output. Indicates the internal heater is stabilized at factory programmed temperature.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, all the voltages ratings are specified with respect to REF_GND pin voltage (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	VDD, OP-STBL, NIC, NC	–0.3	18	V
Voltage	REF_Z	–0.3	10	V
Voltage	HEATP	–0.3	48	V
Voltage	HEATM	–42	0.3	V
Voltage	HEATP - HEATM	0	42	
Output short circuit current	I_{SC}		30	mA
Operating temperature range	T_A	–55	125	°C
Storage temperature range	T_{stg}	–65	170	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		REF80 NAJ (LCCC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range, all the voltages ratings are specified with respect to REF_GND pin voltage (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD (Input voltage)	10		16.5	V
	REF_Z	0		8	
	VHET Heater voltage, $V_{(HEATP - HEATM)}$	10		42	
	HEATP	0		42	
	HEATM	-42		0	
	OP-STBL (Output voltage stable indicator)	0		V_{IN}	

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6.4 Recommended Operating Conditions (continued)

over operating free-air temperature range, all the voltages ratings are specified with respect to REF_GND pin voltage (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Current	OP-STBL Current (Output Logic Low, Active HIGH output)	0		5	mA
T_A	Operating temperature	0		70	°C

6.5 Electrical Characteristics

At VDD = 10V, V_{HEATER} = 30V, C_{REF_Z} = 10µF, C_{VDD} = 1µF, I_L = 0 mA, minimum and maximum specifications across supported temperature range, typical specifications T_A = 25°C; unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage	T_A = 25°C		7.6		V
	Output voltage accuracy	T_A = 25°C	–50		50	mV
	Output voltage temperature coefficient			0.05	0.2	ppm/°C
HYSTERESIS AND LONG-TERM STABILITY						
	Long-term stability	0 to 336 Hours (14 days), T_A = 25°C, T_{SET} = 115°C		10		ppm
		336 Hours to 1000 Hours, T_A = 25°C, T_{SET} = 115°C		0.9		
e_{np-p}	Low frequency noise	f = 0.1Hz to 10Hz		0.16		ppm_{p-p}
NOISE						
e_n	Output voltage noise	f = 10Hz to 100Hz,		0.6		uV_{rms}
LINE AND LOAD REGULATION						
$\Delta V_{REF\_Z}/\Delta VDD$	Line regulation	VDD = 10V to 16.5V		4	10	ppm/V
POWER SUPPLY						
VDD	Input voltage		10		16.5	V
V_{HEATER}	Input voltage	(HEATP - HEATM)	10		42	V
I_{HEATER}	Start up current			335		mA
	Quiescent current	T_A = 25°C, T_{SET} = 115°C, V_{HEATER} = 10V		75		
		T_A = 25°C, T_{SET} = 115°C, V_{HEATER} = 42V		18		
I_{VDD}	Quiescent current			15		mA
TURNON TIME						
Start-up	V_{REF_Z}	REF_Z settled within ±3ppm		100		sec
	Heater Turn-on time	OP-STBL = 1		250		ms
STABLE CAPACITANCE RANGE						
	Input capacitor range		0.1			µF
	Output capacitor range (1)		10		100	µF

(1) ESR for the capacitor can range from 10 mΩ to 400 mΩ

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6.6 Typical Characteristics

at T_A = 25°C, V_{IN} = 10V, V_{HEATER} = 30V, C_{REFZ} = 10µF, C_{VDD} = 1µF, (unless otherwise noted)

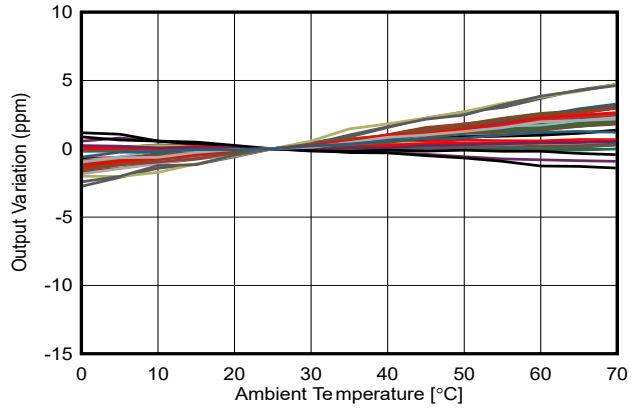

Figure 6-1. Output Voltage Vs Free-Air Temperature

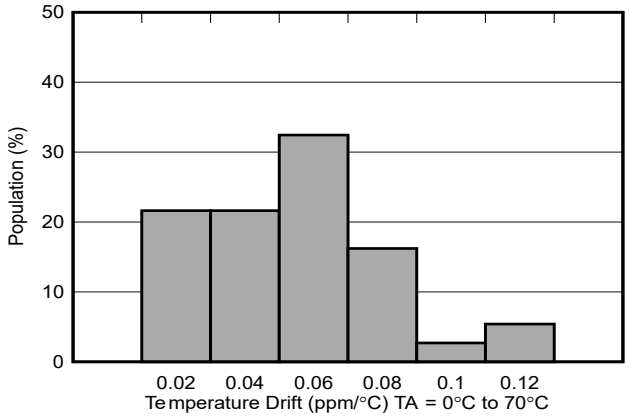

Figure 6-2. Temperature Drift Distribution

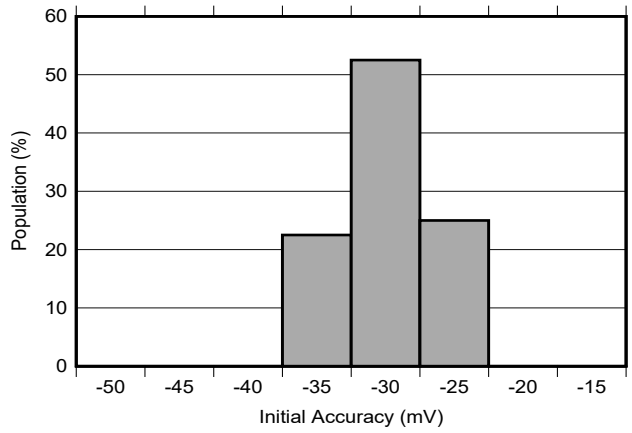

Figure 6-3. Accuracy Distribution

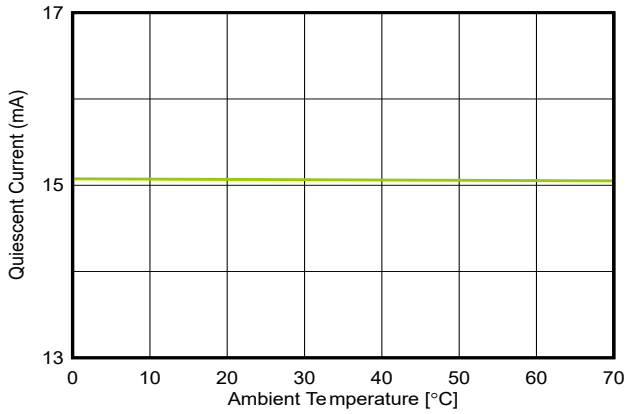

Figure 6-4. Supply Current (I_{VDD}) vs Temperature

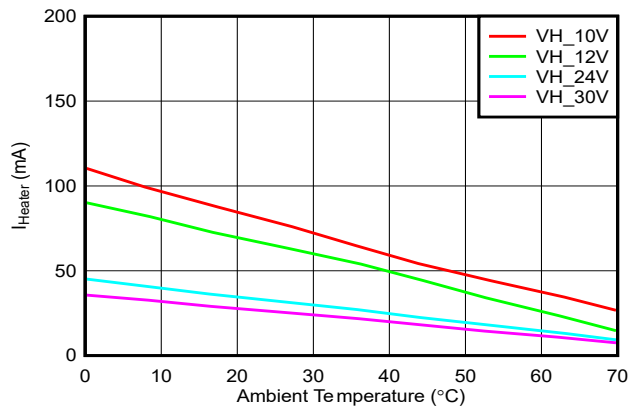

Figure 6-5. Heater Current (I_{Heater}) vs Temperature

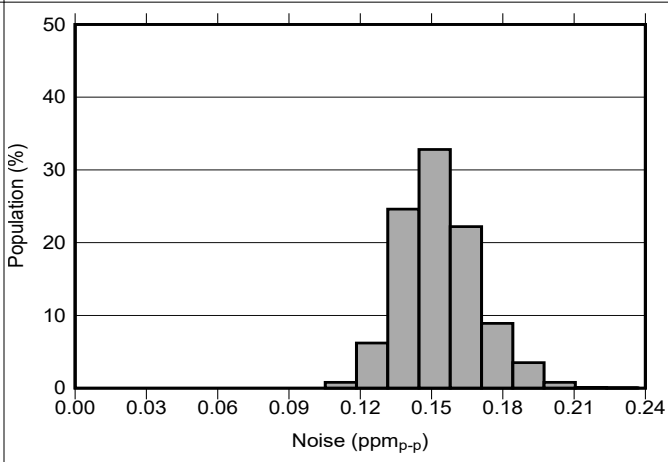

Figure 6-6. 0.1Hz to 10Hz Voltage Noise Distribution

ADVANCE INFORMATION

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 10V, V_{HEATER} = 30V, C_{REFZ} = 10µF, C_{VDD} = 1µF, (unless otherwise noted)

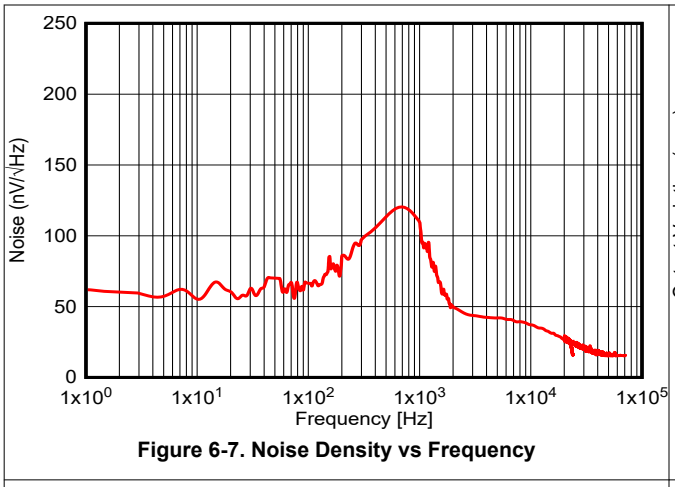

Figure 6-7. Noise Density vs Frequency

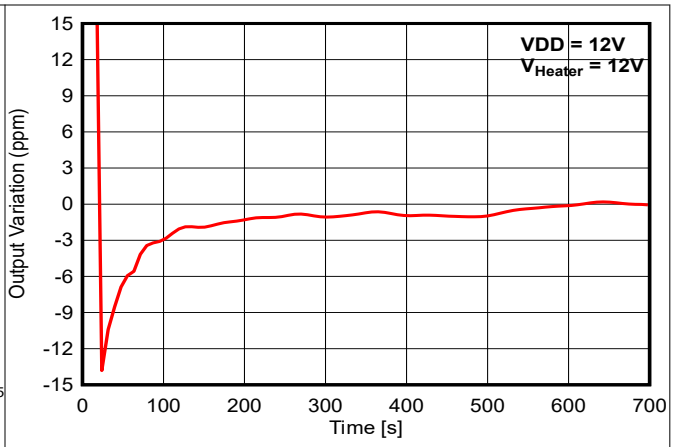

Figure 6-8. Startup Behavior

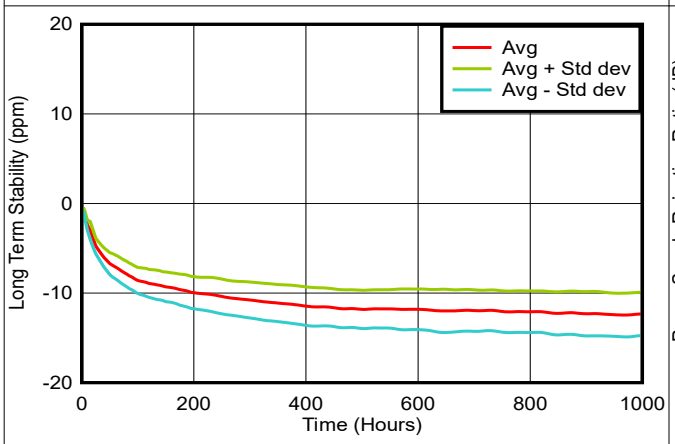

Figure 6-9. Long-Term Stability

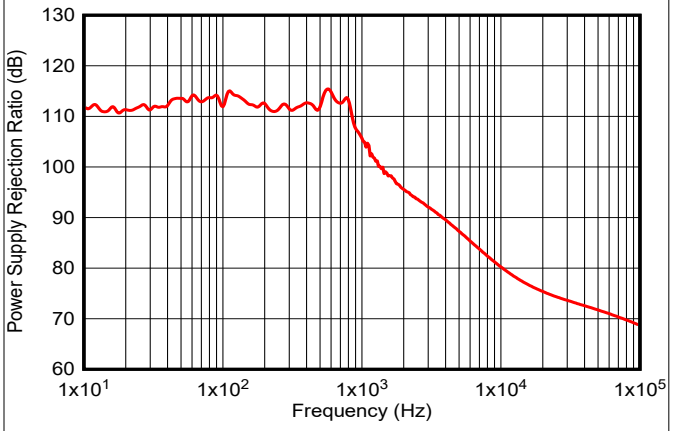

Figure 6-10. Power-Supply Rejection Ratio vs Frequency

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7 Detailed Description

7.1 Overview

The REF80 is temperature controlled, buried zener voltage references specifically designed for excellent voltage stability over time and temperature. The Figure 7-1 is the simplified block diagram of the REF80 showing the generation of voltage reference with buried zener and on chip heater control.

7.2 Functional Block Diagram

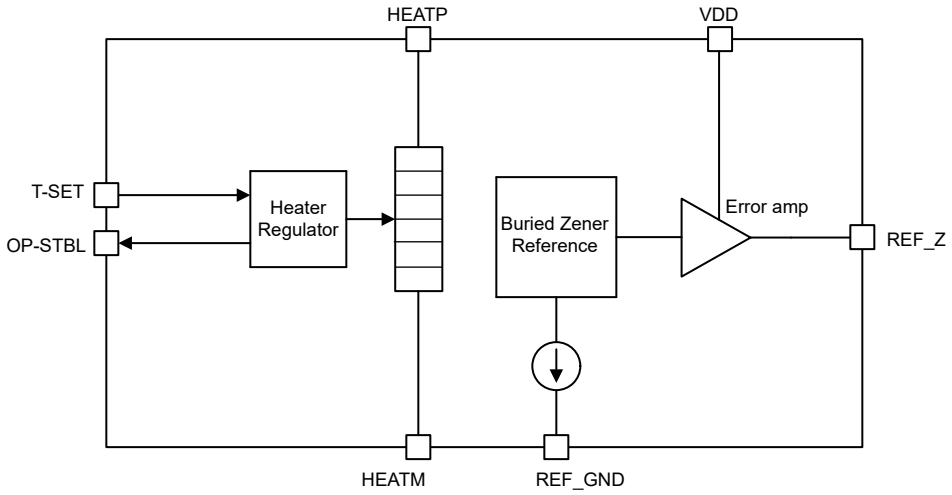

Figure 7-1. Functional Block Diagram for REF80

7.3 Feature Description

7.3.1 Heater

REF80 has on chip heater which is factory programmed to T_{SET} temperature as per T_{SET} of Heater to regulate the temperature of the die within ± 1ºC, for the entire operating ambient temperature range. This allows REF80 to achieve ultra low temperature drift of 0.05ppm/ ºC. Heater has dedicated supply pins HEATP and HEATM which run independent of VDD supply pin. The steady state power dissipation of the heater is directly proportional to the difference between ambient temperature T_A and T_{SET} as per Equation 1. Heater current depends on (HEATP - HEATM) voltage. Heater takes high transient current at the time of start-up to heat up the device from ambient. REF80 has heater indicator pin OP_STBL, which de-asserts when the heater reaches within ±0.1% of T_{SET}.

T_{SET} of Heater

Operating Temperature Range	T_{SET}
0ºC to 70ºC	115ºC

$$P_{HEATER} = \frac{T_{SET} - T_A}{R_{\theta JA}} - V_{DD} \times I_{VDD} \quad (1)$$

V_{DD} is supply voltage for the chip and I_{VDD} is the supply current.

$R_{\theta JA}$ depends on board thickness and layout. The data sheet value of $R_{\theta JA}$ is based on JEDEC standard board.

REF80 offers flexibility to decrease the heater temperature by putting a resistor on the T-SET pin as per T-SET Pin Resistor VS Change in T_{SET} to save power and reduce the thermal noise for restricted ambient temperature applications. T_{SET} must be programmed to 45ºC above the max ambient temperature to make sure that the heater is regulating the temperature properly. REF80 samples the value of the resistor at the time of startup and the value of T_{SET} is modified accordingly. Small drift in resistor value will not impact the T_{SET} temperature as T-SET pin samples discreet value.

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T-SET Pin Resistor VS Change in T_{SET}

Resistor on T-SET pin	Heater Temperature
0	T_{SET}
130kΩ	T_{SET} - 10ºC
360kΩ	T_{SET} - 20ºC
800kΩ	T_{SET} - 30ºC
OPEN	T_{SET}

7.3.2 Buried Zener Reference

The 7.6V reference output is generated with an ultra low noise buried zener diode which is biased at 15mA current. This buried zener exhibits extremely stable long term stability characteristics, which helps REF80 to achieve an accuracy of calibration grade instruments.

8 Parameter Measurement Information

8.1 Long-Term Stability

Buried zener references typically exhibit very stable long term stability and used as a ultra stable reference for internal calibration of the signal chain system. The long-term stability value is tested in a typical setup that reflects standard PCB board manufacturing practices for references with strain modulation structure around the device. The boards are made of standard FR4 material with 35µm of Copper.

Long term stability setup is designed with utmost care to minimize impact of thermocouple error, strain impact and mechanical vibration in long term stability measurement. The boards are maintained at 25°C in an air drift oven with heater temperature set to 115°C in powered on condition for long term stability measurement.

Typical long-term stability characteristic is expressed as a deviation over time. Figure 8-1 shows the typical drift value for the REF80 V_{REF_Z} is 9ppm from 0 to 300 hours. Drift of REF80 quickly settles around 300 hours. Subsequent deviation is typically lower than 1ppm for the next 1000hr.

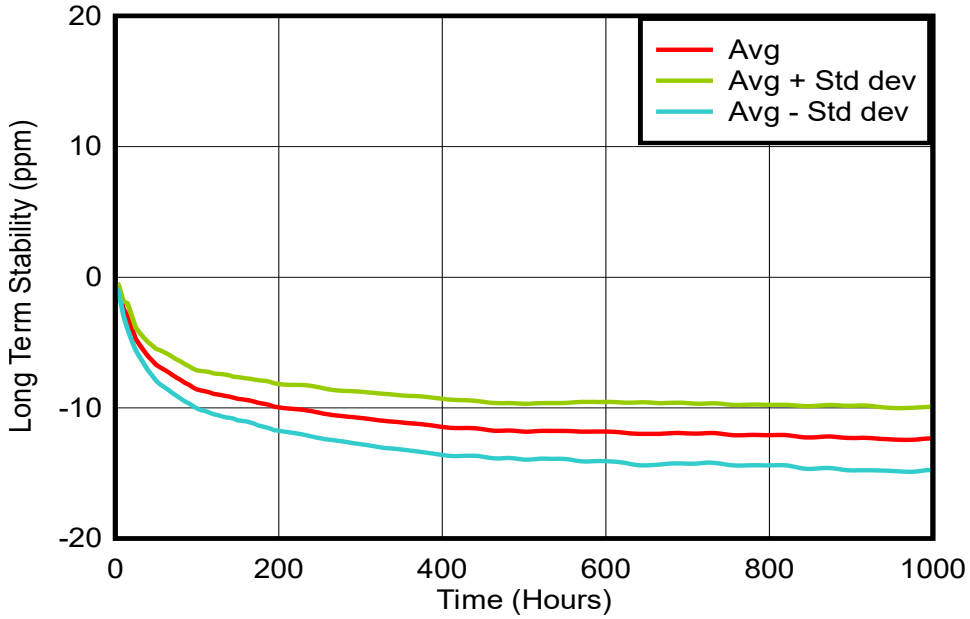

Figure 8-1. Long Term Stability (V_{REF_Z})

8.2 Temperature Drift

The REF80 has integrated on chip heater, which is factory programmed to T_{SET} = 105°C temperature. Heater regulates the T_{SET} temperature to ± 1°C for entire operating temperature range. This results in 0.05ppm/°C tempco for REF80.

The temperature coefficient is calculated using the box method in which a box is formed by the min/max variation for the nominal output voltage over the operating temperature range. REF80 has a maximum temperature coefficient of 0.2ppm/°C for 0°C to70°C temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. See *SLYT183* for more information on the box method. The box method equation is shown in Equation 2:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(25°C)} \times \text{Temperature Range}} \right) \times 10^6 \quad (2)$$

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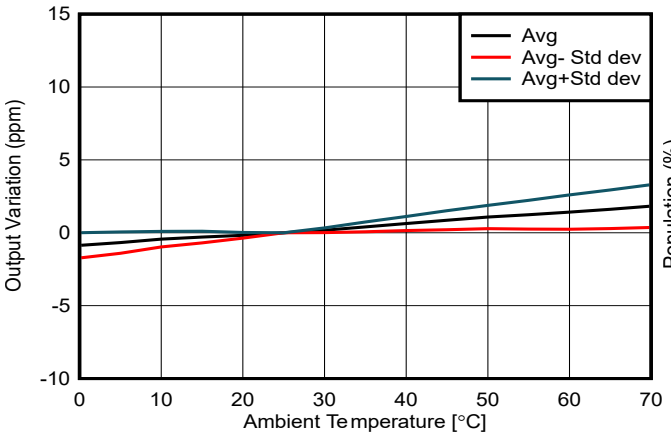

Figure 8-2. Output Voltage Vs Free-Air Temperature

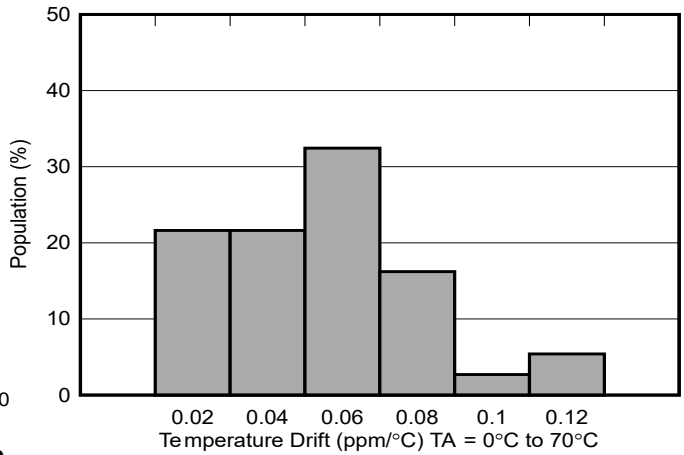

Figure 8-3. Temperature Drift Distribution

8.3 Noise Performance

8.3.1 1/f Noise

1/f noise, also known as flicker noise, is dominant mostly in the lower frequency bands. Flicker noise affects the device output voltage which can affect the ENOB of the signal chain. REF80 data sheet specifies flicker noise for 0.1Hz to 10Hz frequency band where 1/f noise has maximum power. Flicker noise is measured by filtering the output from 0.1Hz to 10Hz. Since the 1/f noise is an extremely low value, the frequency of interest needs to be amplified and band-pass filtered as shown in Figure 8-4. 1/f noise must be tested in a Faraday cage enclosure to block environmental noise. Refer to application note Techniques for Noise Measurements in Precision Series References for more detail on noise measurement for precision series references.

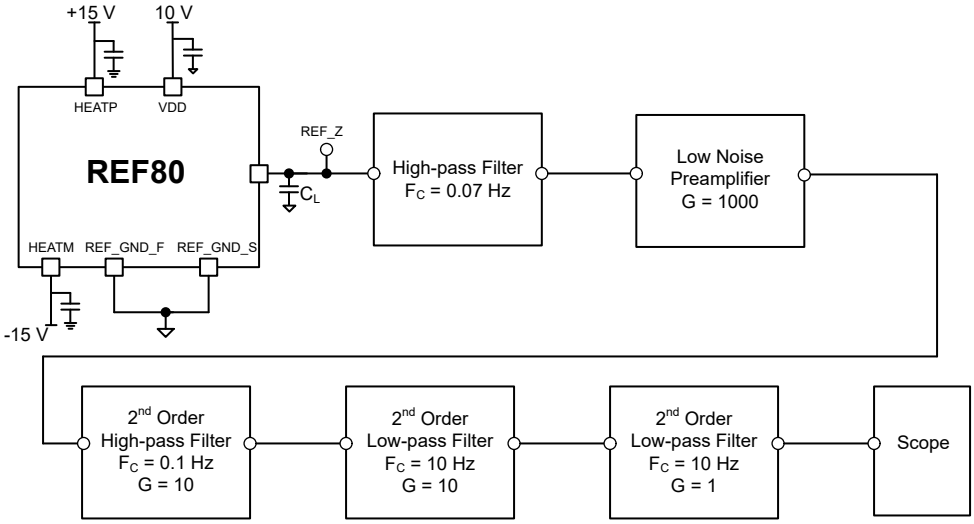

Figure 8-4. 1/f Noise Test Setup

Typical 1/f noise (0.1Hz to 10Hz) distribution can be seen in Figure 8-5.

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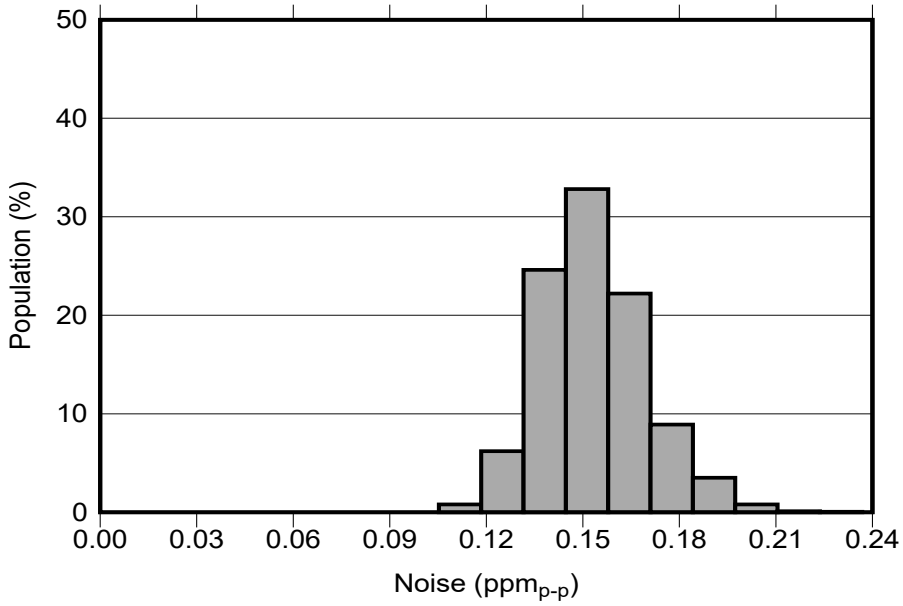

Figure 8-5. 0.1Hz to 10Hz Voltage Noise Distribution

The 1/f noise is in such a low frequency range that it is not practical to filter out which makes it a key parameter for ultra-low noise measurements. Noise sensitive designs must use the lowest 1/f noise for the highest precision measurements. Figure 8-6 shows the effect of 1/f noise over 10s.

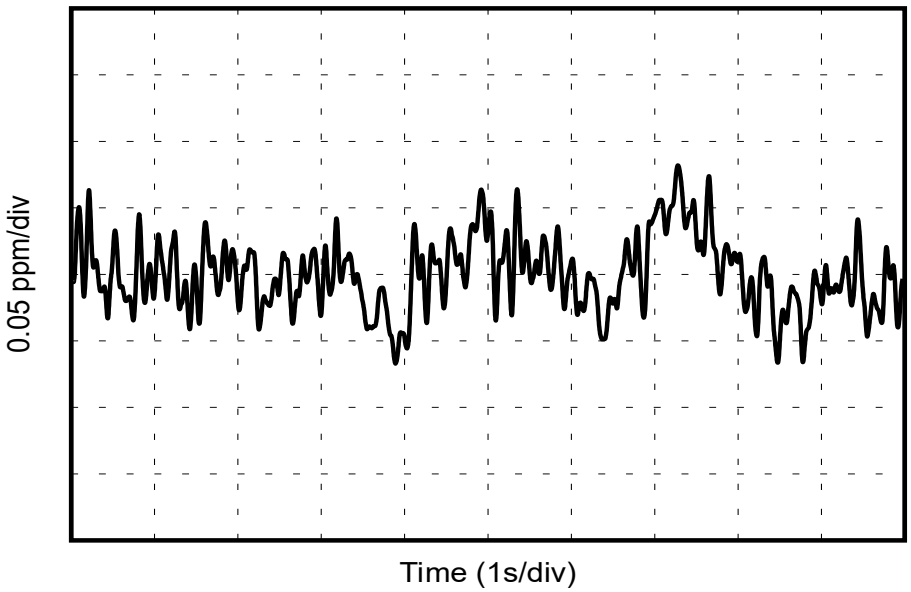

Figure 8-6. 0.1Hz to 10Hz Voltage Noise

8.3.2 Broadband Noise

Broadband noise is a noise that appears at higher frequency compared to 1/f noise. The broadband noise is dominated by white noise as shown in Figure 8-8 . The broadband noise is measured by high-pass filtering the output of the REF80 and measuring the result on a spectrum analyzer as shown in Figure 8-7. The DC component of the REF80 is removed by using a high-pass filter and then amplified. When measuring broadband noise, it is not necessary to have high gain to achieve maximum bandwidth.

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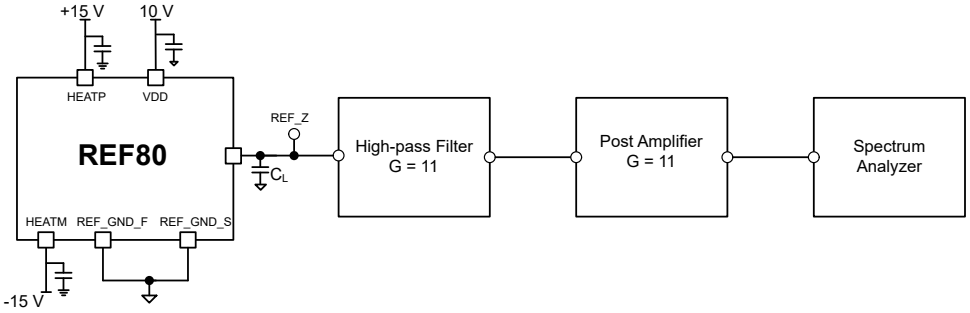

Figure 8-7. Broadband Noise Test Setup

For noise sensitive designs, a low-pass filter can be used to reduce broadband noise output noise levels by removing the high frequency components. When designing a low-pass filter special care must be taken to make sure the output impedance of the filter does not degrade ac performance. This can occur in RC low-pass filters where a large series resistance can impact the load transients due to output current fluctuations.

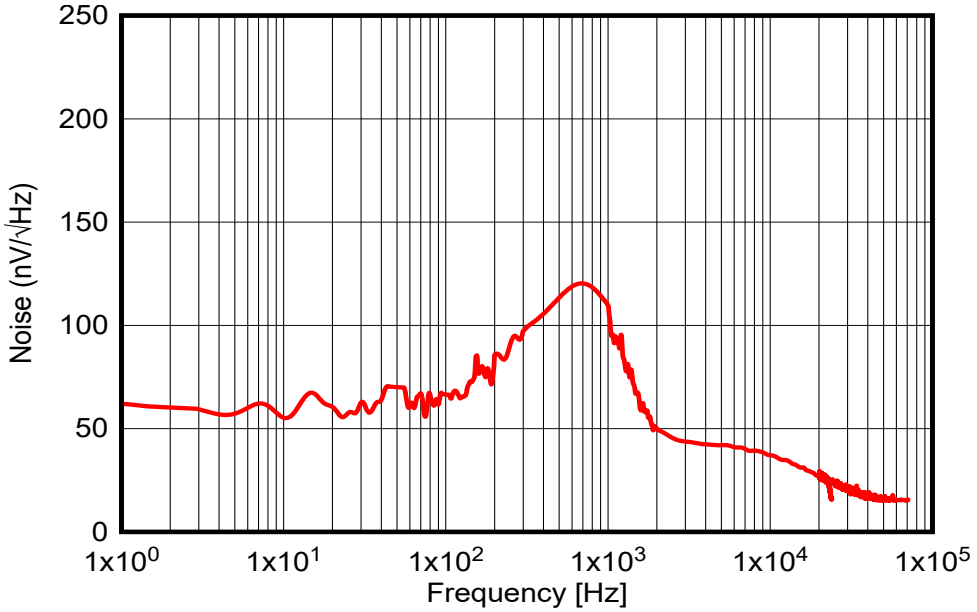

Figure 8-8. Noise Performance 10Hz to 10kHz

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Basic applications convert the REFZ output to calibration signal or connect it to <= 5V signal for precision data converter. The table below shows the typical applications of REF80 and its companion data converters.

APPLICATION	DATA CONVERTER
Test & Measurement	DAC11001B

9.2 Typical Applications

9.2.1 Typical Application: Basic Voltage Reference Connection

The circuit shown in Figure 9-1 shows the basic configuration for the REF80 references. Connect bypass capacitors according to the guidelines in Section 9.4.1.

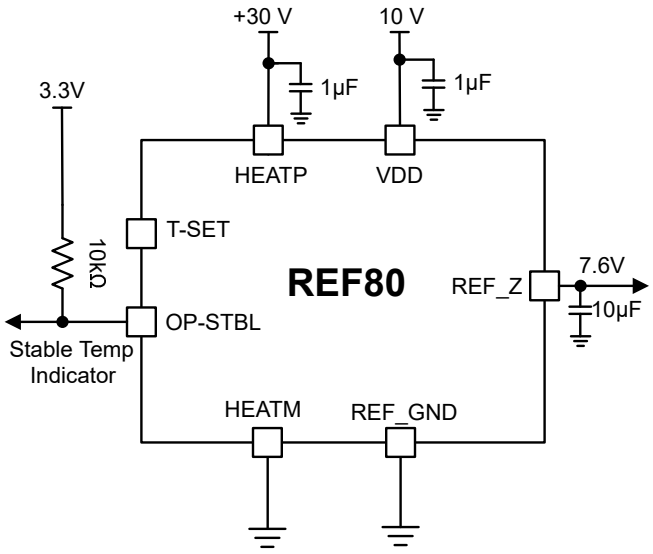

Figure 9-1. Basic Reference Connection

ADVANCE INFORMATION

9.2.1.1 Design Requirements

A detailed design procedure is based on a design example. For this design example, use the parameters listed in Table 9-1 as the input parameters.

Table 9-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{DD}	10V
Heater Voltage V_{HEATER} (HEATP - HEATM)	30V
Supply decoupling capacitor	1µF
Heater supply decoupling capacitor	1µF
OP-STBL pull-up resistor	10kΩ
OP-STBL pull-up supply	3V

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Application Curve

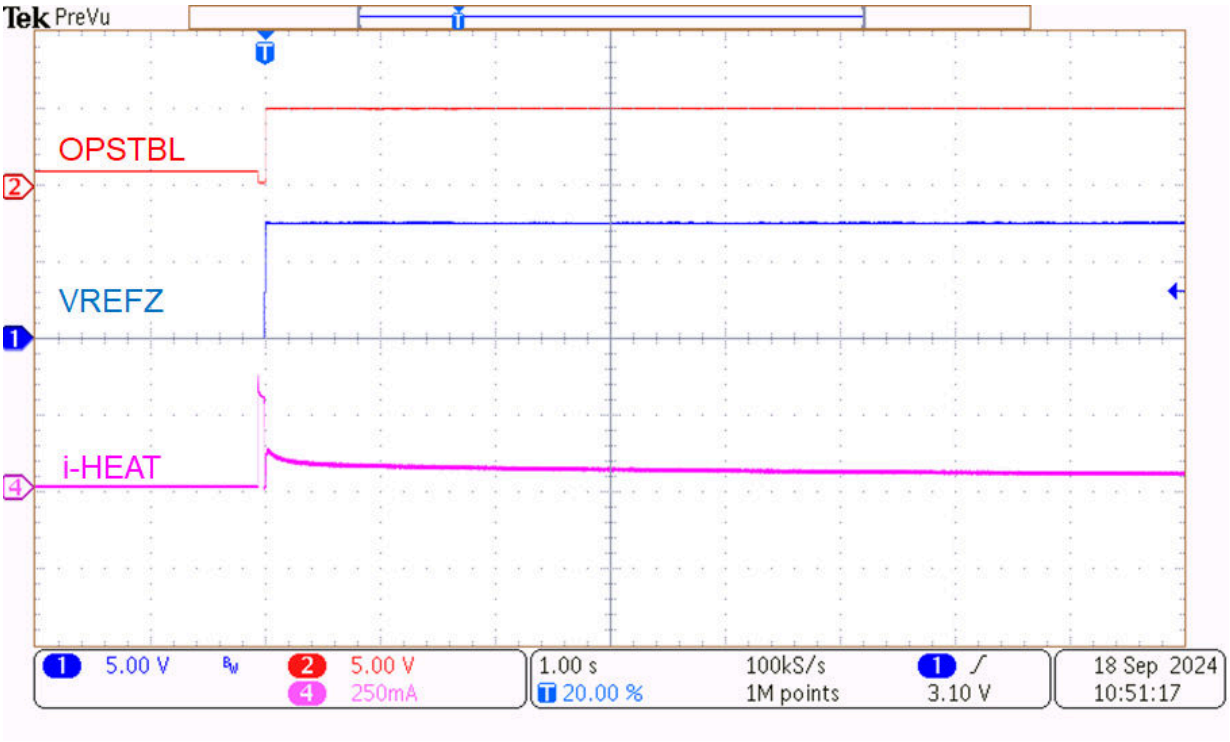

Figure 9-2. REF80 Startup Behaviuo

9.2.2 Typical Application Circuits

9.2.2.1 Precision Voltage Divider Connection

Precision data converters typically require voltage reference which is less than or equal to 5V. REF80 requires a precision resistor divider followed by low noise buffer to generate reference voltage for data converters as shown in Figure 9-3.

The selection of resistor depends on the current capability (< 1mA is preferred) and noise requirement. Minimum value of resistors are decided by the output current as per Equation 4.

$$R1 + R2 \geq 7.6k\Omega \tag{3}$$

Maximum value of the resistors are decided by the noise consideration. Thermal noise of the resistors (parallel equivalent) is added as per Equation 5

$$VREF_{Noise} = \sqrt{\left(\left(\frac{R2}{R1 + R2} \times REF\_Z_{Noise}\right)^2 + \left(R1||R2_{Thermal\ Noise}\right)^2\right.} \tag{4}$$

Where

- $VREF_{Noise}$ = Reference noise requirement in desired frequency band
- REF_Z_{Noise} = REF80 noise in desired frequency band
- $R1||R2_{Thermal\ noise}$ = Thermal noise of parallel equivalent of R1 and R2 resistor

R1 and R2 must be precision foil resistors with matched temperature drift for best performance.

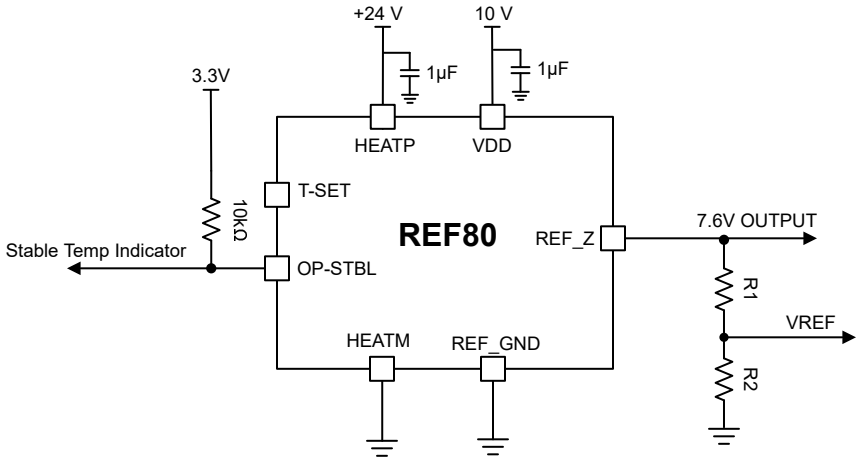

Figure 9-3. Precision Resistor Divider Connection

9.2.2.2 Calibration Signal

Ultra low long term stability and temperature drift makes REF80 an excellent choice for metrology grade calibration signal generation.

ADVANCE INFORMATION

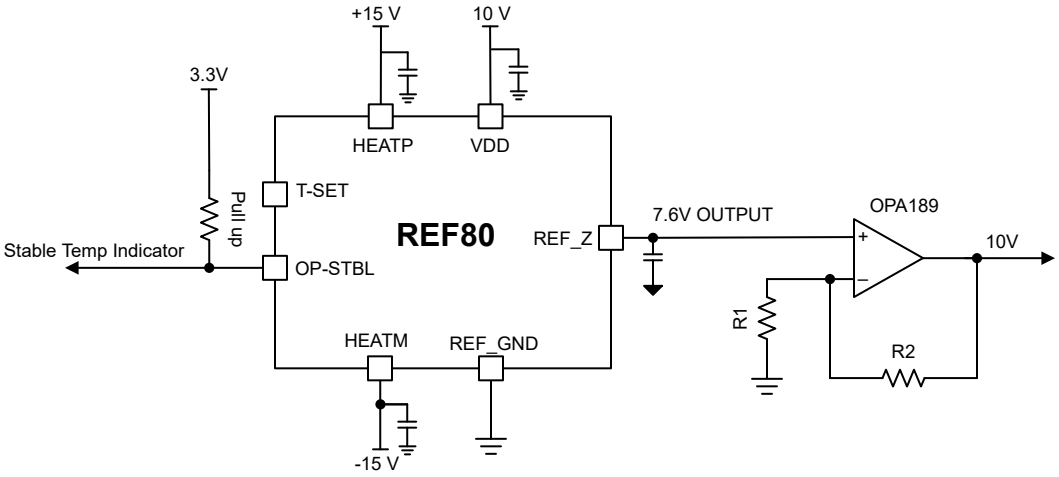

Figure 9-4. 10V Precision Signal With Amplifier And Precision Resistors

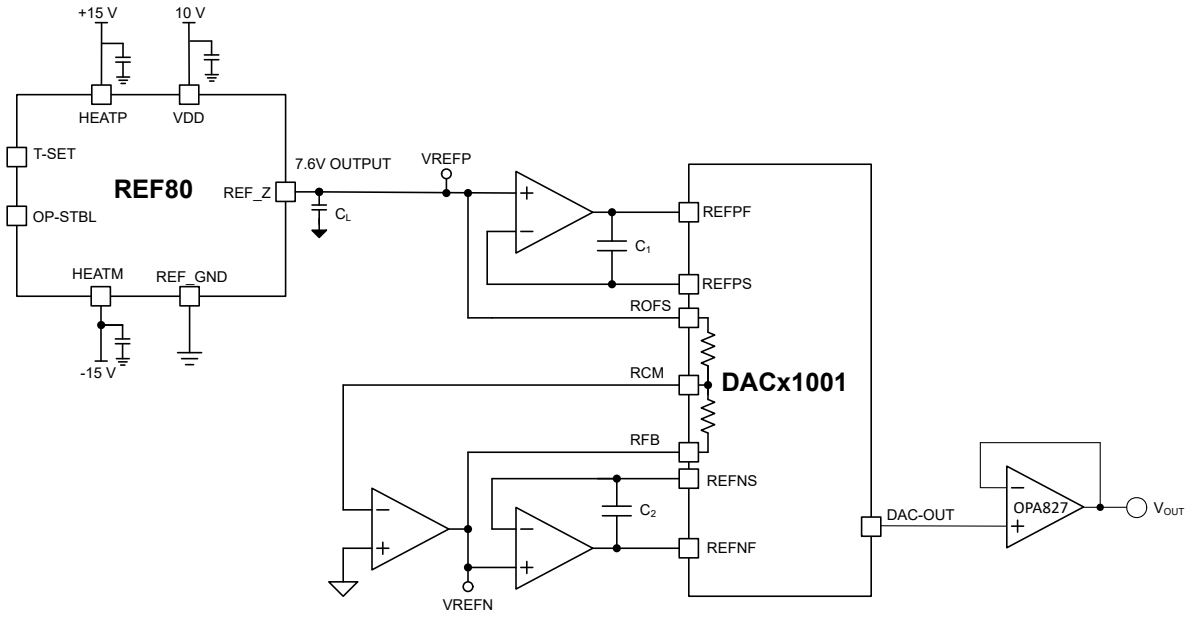

Figure 9-5. Precision Signal With DACx1001

ADVANCE INFORMATION

9.3 Power Supply Recommendation

The buried zener reference requires a stable power supply of 10V to 16.5V for stable operation of the REF_Z pin. Potential difference between HEATP and HEATM pin must be 10V to 42V. HEATP must always be connected to a positive supply or ground. HEAM must always be connected to a negative supply or ground. The heater supply must be able to provide high inrush current for fast start-up of the device. TI recommends a supply bypass capacitor ranging between 0.1µF to 10µF.

9.4 Layout

9.4.1 Layout Guidelines

Layout Example illustrates an example of a PCB layout for a data acquisition system using the REF80. Some key considerations are:

- **Noise performance**
  - Connect low-ESR, 0.1µF ceramic bypass capacitors at V_{DD}, HEATM and HEATP of the REF80.
  - Connect 10uF to 100uF class 1 capacitor at REFZ of the REF80.
  - Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.
- **Thermal performance**
  - The layout must minimize the heat dissipation to maintain good thermal resistance for REF80.
  - Use minimum copper to route V_{DD}, REF_Z, REF_GND signal.
  - Use copper as per current requirement for HEATP and HEATM pin.
  - Avoid direct copper pours underneath the package.
- **Seebeck effect**
  - Avoid multiple metal-metal junction to minimize Seebeck effect.
- **Long term stability performance**
  - Provide strain relief directly to pins as shown in the Layout Example.
  - Provide cuts near to the pin, perpendicular to the pins and corners.
  - Avoid single point strain accumulation.

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Voltage Reference Design Tips For Data Converters*
- Texas Instruments, *Voltage Reference Selection Basics*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PREF80000B1NAJT	ACTIVE	LCCC	NAJ	20	250	TBD	Call TI	Call TI	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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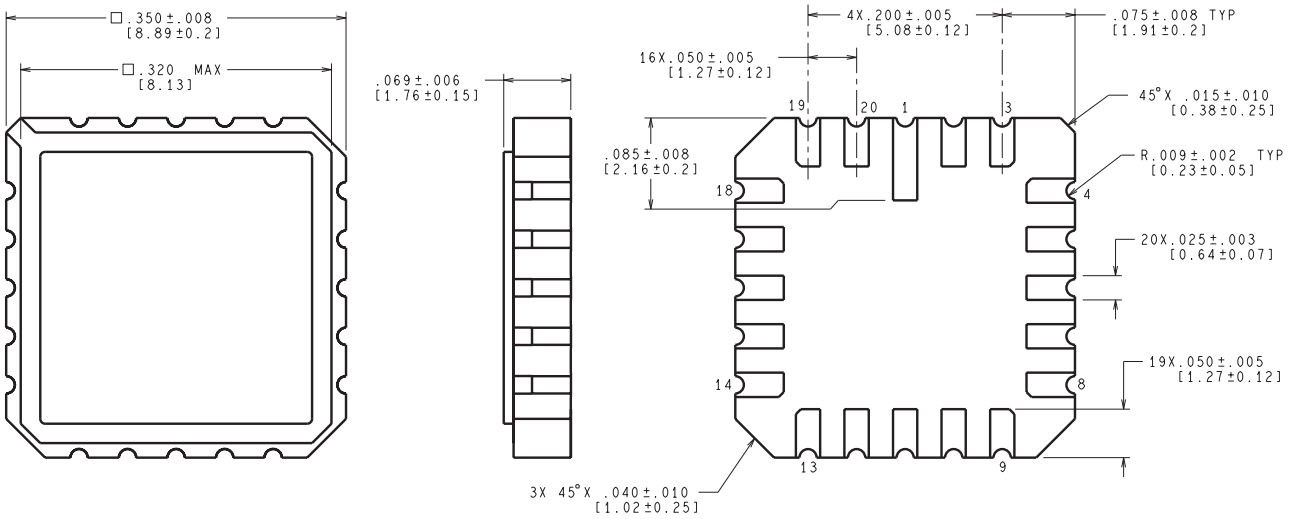

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E20A (Rev F)

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