# Micropower Voltage Regulator

Check for Samples: SM72238

## FEATURES

- Renewable Energy Grade
- High-Accuracy Output Voltage
- Ensured 100mA Output Current
- Extremely Low Quiescent Current
- Low Dropout Voltage
- Extremely Tight Load and Line Regulation
- Very Low Temperature Coefficient
- Use as Regulator or Reference
- Needs Minimum Capacitance for Stability
- Current and Thermal Limiting
- Stable With Low-ESR Output Capacitors (10mΩ to 6Ω)

## DESCRIPTION

The SM72238 is a micropower voltage regulator with very low quiescent current (75µA typ.) and very low dropout voltage (typ. 40mV at light loads and 380mV at 100mA). It is ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the SM72238 increases only slightly in dropout, prolonging battery life.

The SM72238 is available in the surface-mount D-Pak package.

Careful design of the SM72238 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

## Block Diagram and Typical Applications

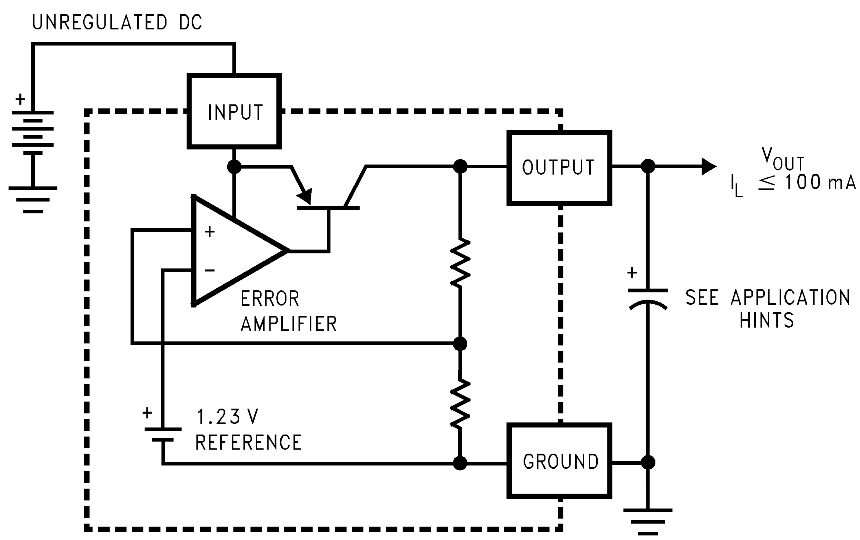



Figure 1. SM72238

## Connection Diagrams

**Front View**

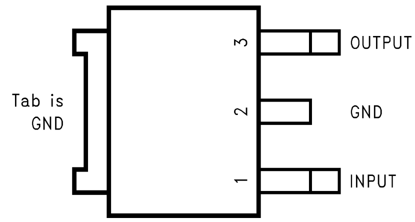



**Figure 2. PFM Package**
**See Package Number NDP0003B**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)

| | | |
|---|---|---|
| Input Supply Voltage | | −0.3 to +30V |
| Power Dissipation | | Internally Limited |
| Junction Temperature ($T_J$) | | +150°C |
| Ambient Storage Temperature | | −65° to +150°C |
| Soldering Dwell Time, Temperature | Wave | 4 seconds, 260°C |
| | Infrared | 10 seconds, 240°C |
| | Vapor Phase | 75 seconds, 219°C |
| ESD Rating | Human Body Model(3) | 2500V |

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model 1.5kΩ in series with 100pF.

## Operating Ratings(1)

| | |
|---|---|
| Maximum Input Supply Voltage | 30V |
| Junction Temperature Range, ($T_J$)(2) | −40° to +125°C |

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) Junction-to-case thermal resistance for the PFM package is 5.4°C/W.

## Electrical Characteristics[1]

| Parameter | Conditions[1] | Typ | Tested Limit[2] | Design Limit[3] | Units |
|---|---|---|---|---|---|
| **3V Versions** | | | | | |
| Output Voltage | $T_J$ = 25°C | 3.0 | 3.030 | | V max |
| | | | 2.970 | | V min |
| | −25°C ≤ $T_J$ ≤ 85°C | 3.0 | | 3.045 | V max |
| | | | | 2.955 | V min |
| | Full Operating Temperature Range | 3.0 | | **3.060** | V max |
| | | | | **2.940** | V min |
| Output Voltage | 100µA ≤ $I_L$ ≤ 100mA, $T_J$ ≤ $T_{JMAX}$ | 3.0 | | **3.072** | V max |
| | | | | **2.928** | V min |
| **3.3V Versions** | | | | | |
| Output Voltage | $T_J$ = 25°C | 3.3 | 3.333 | | V max |
| | | | 3.267 | | V min |
| | −25°C ≤ $T_J$ ≤ 85°C | 3.3 | | 3.350 | V max |
| | | | | 3.251 | V min |
| | Full Operating Temperature Range | 3.3 | | **3.366** | V max |
| | | | | **3.234** | V min |
| Output Voltage | 100µA ≤ $I_L$ ≤ 100mA $T_J$ ≤ $T_{JMAX}$ | 3.3 | | **3.379** | V max |
| | | | | **3.221** | V min |
| **5.0V Versions** | | | | | |
| Output Voltage | $T_J$ = 25°C | 5.0 | 5.05 | | V max |
| | | | 4.95 | | V min |
| | −25°C ≤ $T_J$ ≤ 85°C | 5.0 | | 5.075 | V max |
| | | | | 4.925 | V min |
| | Full Operating Temperature Range | 5.0 | | **5.1** | V max |
| | | | | **4.9** | V min |
| Output Voltage | 100µA ≤ $I_L$ ≤ 100mA $T_J$ ≤ $T_{JMAX}$ | 5.0 | | **5.12** | V max |
| | | | | **4.88** | V min |
| **All Voltage Options** | | | | | |
| Output Voltage Temperature Coefficient | See[4] | **50** | | **150** | ppm/°C |
| Line Regulation[5] | ($V_O$NOM + 1)V ≤ $V_{in}$ ≤ 30V[6] | 0.04 | 0.2 | | % max |
| | | | | **0.4** | % max |
| Load Regulation[5] | 100µA ≤ $I_L$ ≤ 100mA | 0.1 | 0.2 | | % max |
| | | | | **0.3** | % max |
| Dropout Voltage[7] | $I_L$ = 100µA | | 80 | | mV max |
| | | 50 | | **150** | mV max |
| | $I_L$ = 100mA | | 450 | | mV max |
| | | 380 | | **600** | mV max |

(1) Unless otherwise specified all limits ensured for $V_{IN}$ = ($V_{ONOM}$ + 1)V, $I_L$ = 100µA and $C_L$ = 1µF. Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for $T_A$ = $T_J$ = 25°C.
(2) Ensured and 100% production tested.
(3) Ensured but not 100% production tested. These limits are not used to calculate outgoing AQL levels.
(4) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
(5) Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
(6) For $I_L$ = 100µA and $T_J$ = 125°C, line regulation is ensured by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.
(7) Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.

## Electrical Characteristics[1] (continued)

| Parameter | Conditions[1] | Typ | Tested Limit[2] | Design Limit[3] | Units |
|---|---|---|---|---|---|
| Ground Current | $I_L$ = 100µA | 75 | 120 | | µA max |
| | | | | **140** | µA max |
| | $I_L$ = 100mA | 8 | 12 | | mA max |
| | | | | **14** | mA max |
| Dropout Ground Current | $V_{in}$ = ($V_O$NOM − 0.5)V, $I_L$ = 100µA | 110 | 170 | | µA max |
| | | | | **200** | µA max |
| Current Limit | $V_{out}$ = 0 | 160 | 200 | | mA max |
| | | | | **220** | mA max |
| Thermal Regulation | See[8] | 0.05 | 0.2 | | %/W max |
| Output Noise, 10 Hz to 100 kHz | $C_L$ = 1µF (5V Only) | 430 | | | µV rms |
| | $C_L$ = 200µF | 160 | | | µV rms |
| | $C_L$ = 3.3µF (Bypass = 0.01µF) | 100 | | | µV rms |

(8) Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50mA load pulse at $V_{IN}$ = 30V (1.25W pulse) for T = 10ms.

## Typical Performance Characteristics

**Quiescent Current**

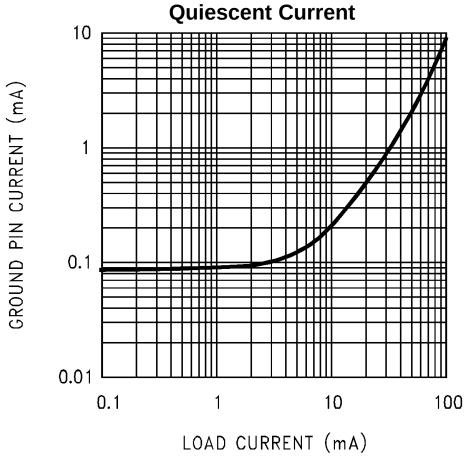



**Figure 3.**

**Dropout Characteristics**

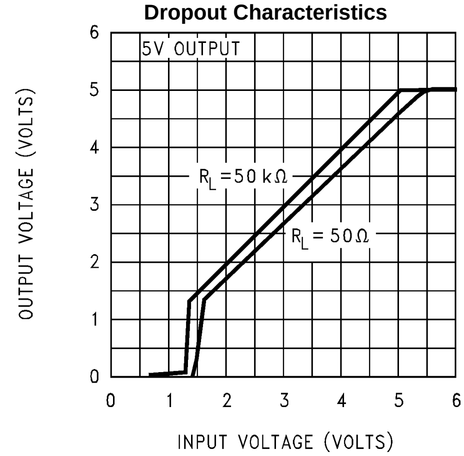



**Figure 4.**

**Input Current**

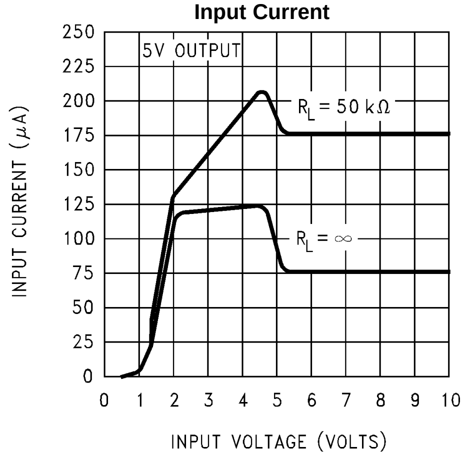



**Figure 5.**

**Input Current**

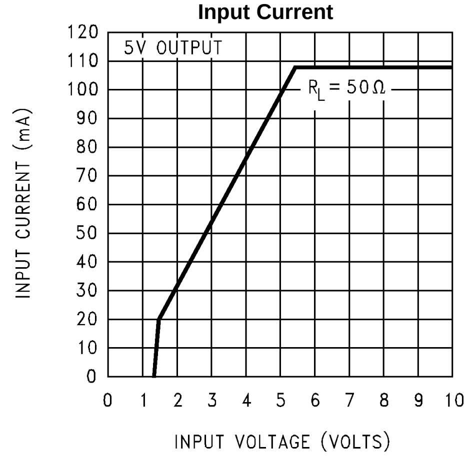



**Figure 6.**

**Output Voltage vs. Temperature of 3 Representative Units**

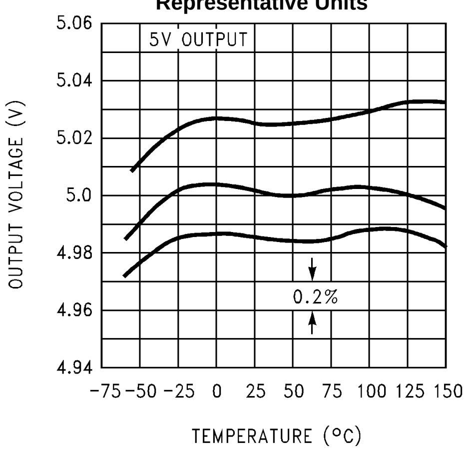



**Figure 7.**

**Quiescent Current**

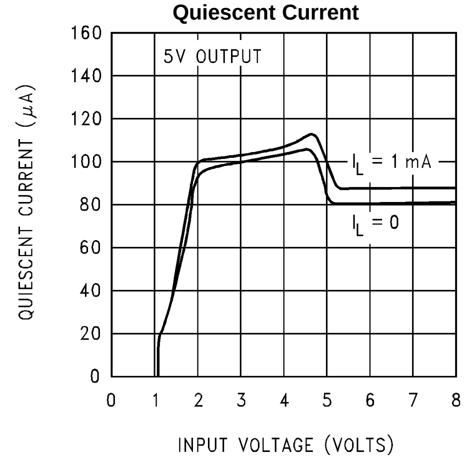



**Figure 8.**

## Typical Performance Characteristics (continued)

**Quiescent Current**

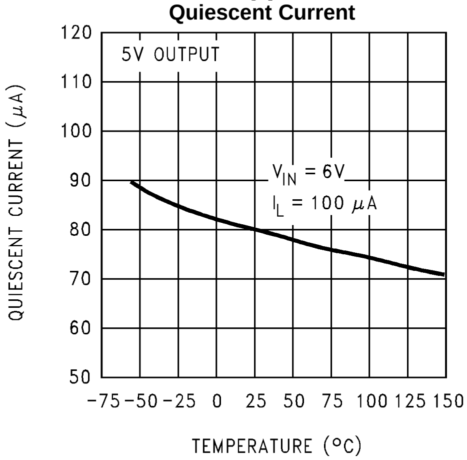



**Figure 9.**

**Quiescent Current**

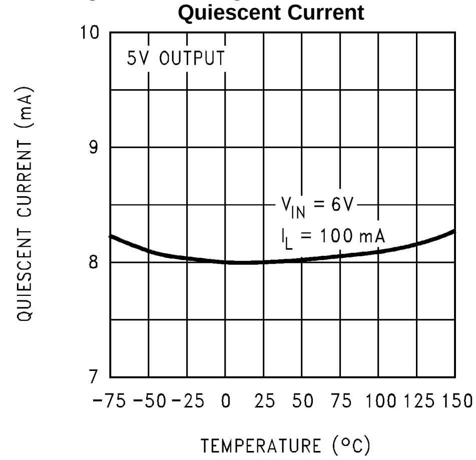



**Figure 10.**

**Quiescent Current**

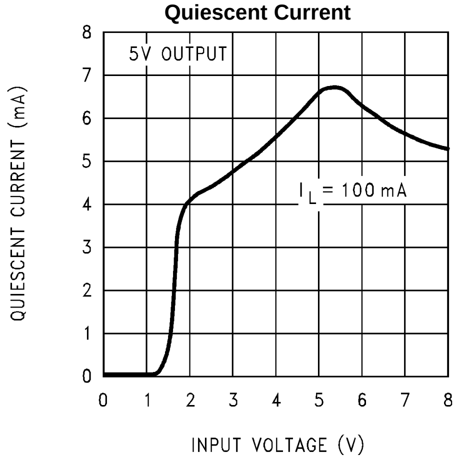



**Figure 11.**

**Short Circuit Current**

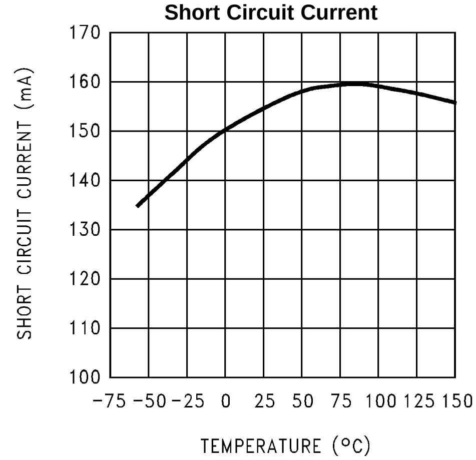



**Figure 12.**

**Dropout Voltage**

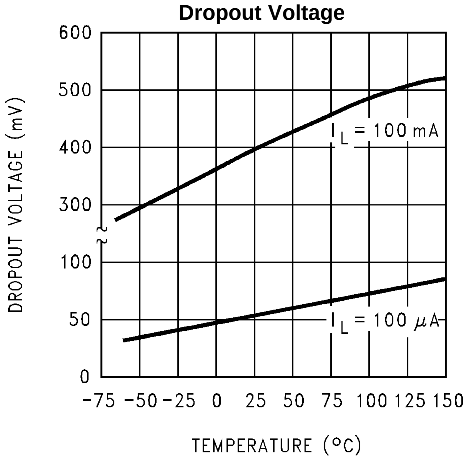



**Figure 13.**

**Line Transient Response**

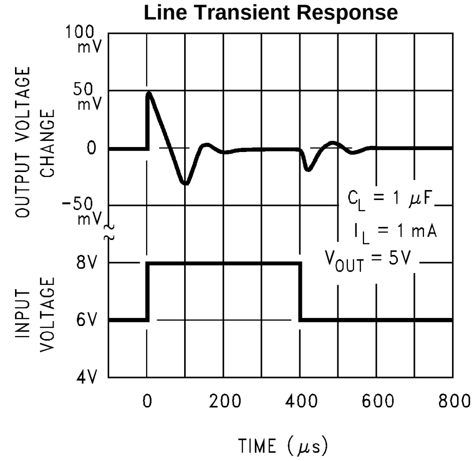



**Figure 14.**

## Typical Performance Characteristics (continued)

**Load Transient Response**

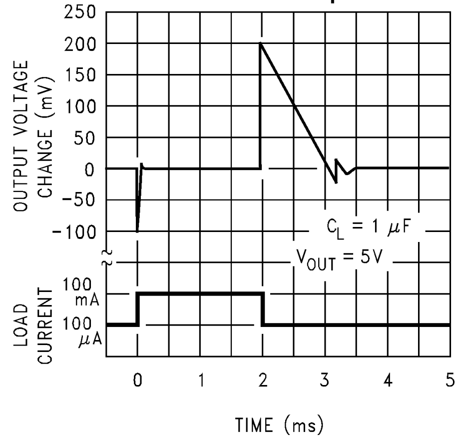



**Figure 15.**

**Load Transient Response**

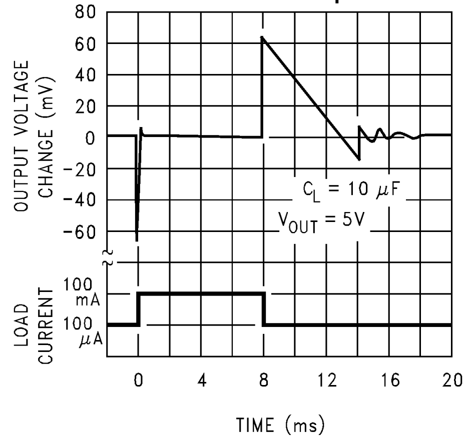



**Figure 16.**

**Output Impedance**

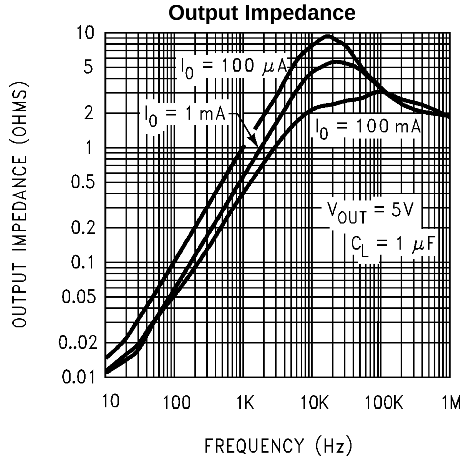



**Figure 17.**

**Ripple Rejection**

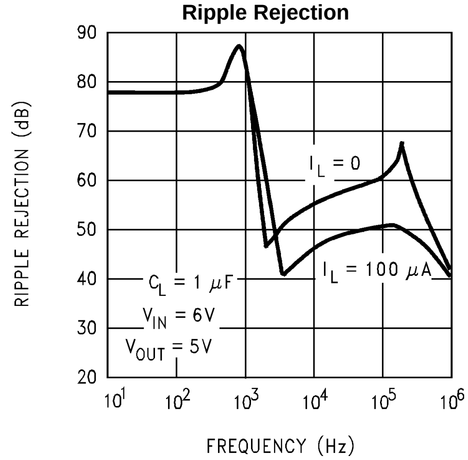



**Figure 18.**

**Ripple Rejection**

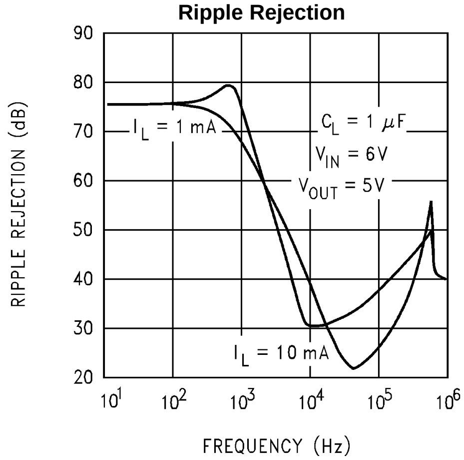



**Figure 19.**

**Ripple Rejection**

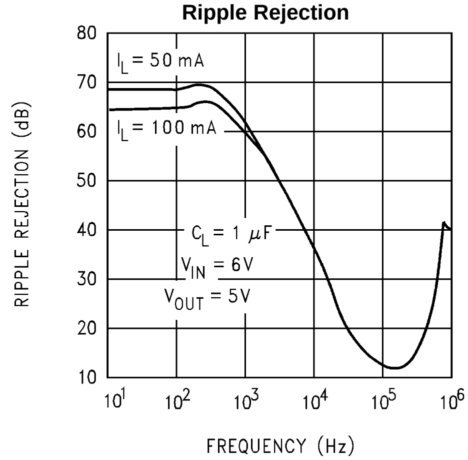



**Figure 20.**

## Typical Performance Characteristics (continued)

**Shutdown Threshold Voltage**

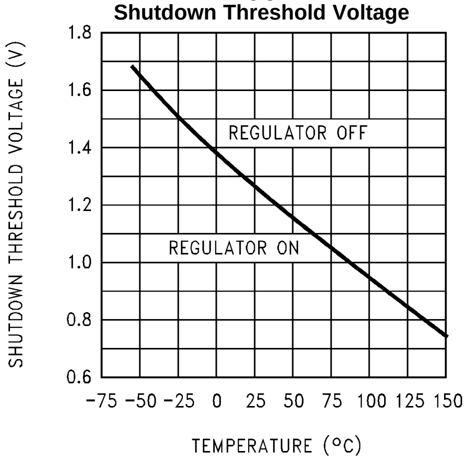



**Figure 21.**

**Line Regulation**

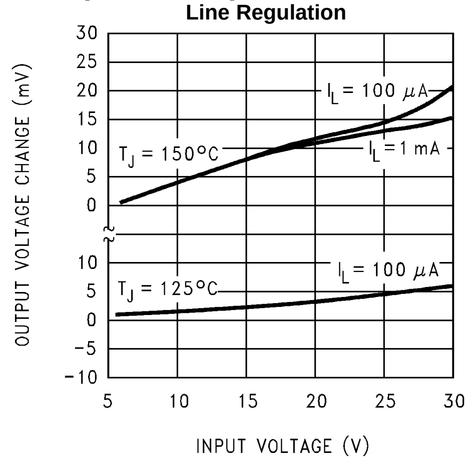



**Figure 22.**

**Maximum Rated Output Current**

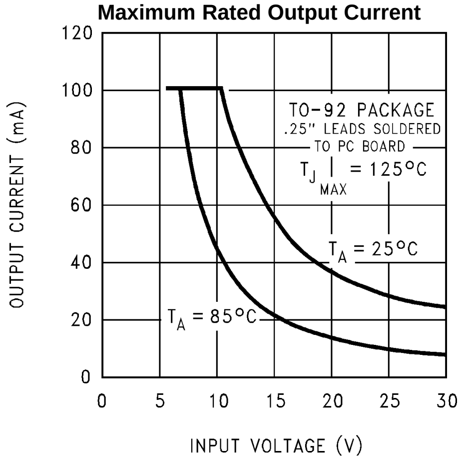



**Figure 23.**

**Thermal Response**

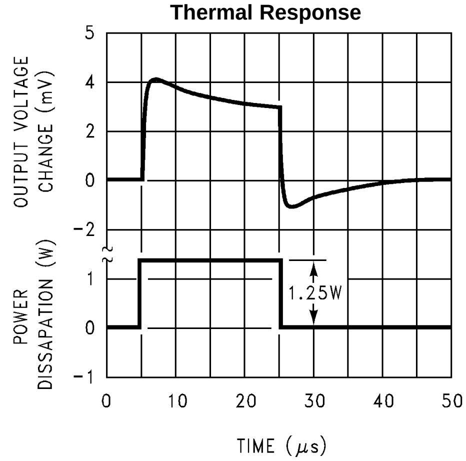



**Figure 24.**

**Output Capacitor ESR Range**

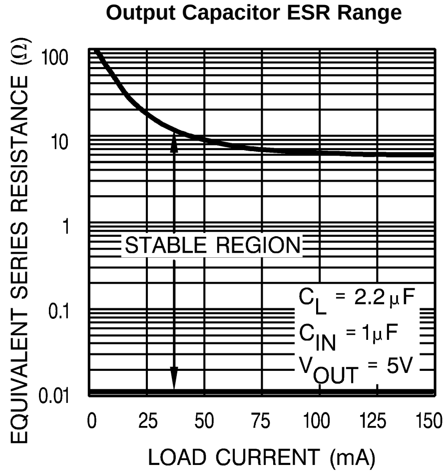



**Figure 25.**

# APPLICATION HINTS

## EXTERNAL CAPACITORS

A 1.0µF (or greater) capacitor is required between the output and ground for stability. Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

Ceramic capacitors whose value is greater than 1000pF should not be connected directly from the SM72238 output to ground. Ceramic capacitors typically have ESR values in the range of 5 to 10mΩ, a value below the lower limit for stable operation (see Figure 25).

The reason for the lower ESR limit is that the loop compensation of the part relies on the ESR of the output capacitor to provide the zero that gives added phase lead. The ESR of ceramic capacitors is so low that this phase lead does not occur, significantly reducing phase margin. A ceramic output capacitor can be used if a series resistance is added (recommended value of resistance about 0.1Ω to 2Ω).

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33µF for currents below 10mA or 0.1µF for currents below 1mA.

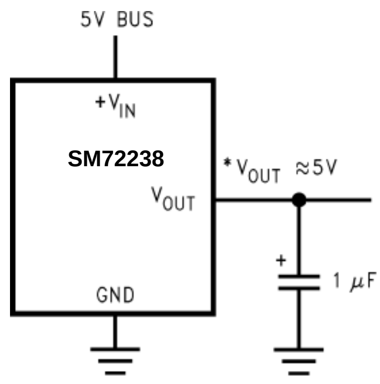
Unlike many other regulators, the SM72238 will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications.

A 1µF tantalum, ceramic or aluminum electrolytic capacitor should be placed from the SM72238 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

## REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced but is relatively inefficient, as increasing the capacitor from 1µF to 220µF only decreases the noise from 430µV to 160µV rms for a 100kHz bandwidth at 5V output.

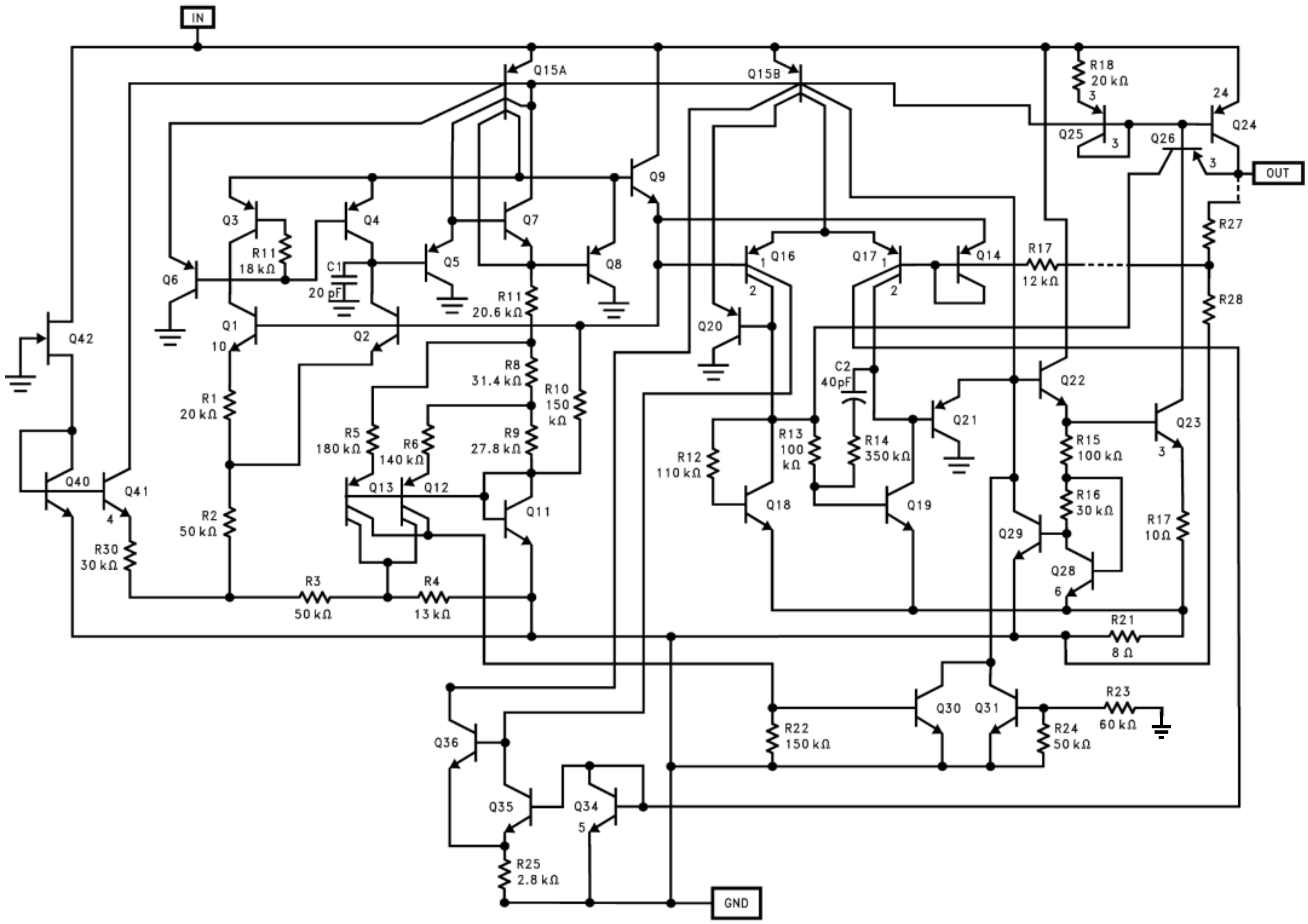
# Typical Applications




*Minimum input-output voltage ranges from 40mV to 400mV, depending on load current. Current limit is typically 160mA.

**Figure 26. 5 Volt Current Limiter**

## Schematic Diagram



## REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 10 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SM72238TD-3.3/NOPB | ACTIVE | TO-252 | NDP | 3 | 75 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | S72238<br>-3.3 | Samples |
| SM72238TD-5.0/NOPB | ACTIVE | TO-252 | NDP | 3 | 75 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | S72238 | Samples |
| SM72238TDE-3.3/NOPB | NRND | TO-252 | NDP | 3 | 250 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | S72238<br>-3.3 | |
| SM72238TDE-5.0/NOPB | NRND | TO-252 | NDP | 3 | 250 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | S72238 | |
| SM72238TDX-3.3/NOPB | NRND | TO-252 | NDP | 3 | 2500 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | S72238<br>-3.3 | |
| SM72238TDX-5.0/NOPB | NRND | TO-252 | NDP | 3 | 2500 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | S72238 | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

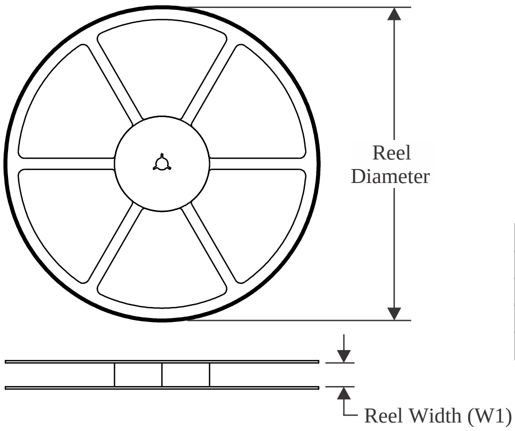
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

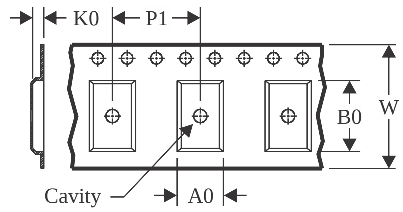
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

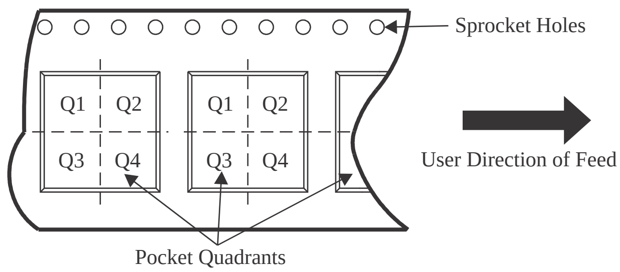



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

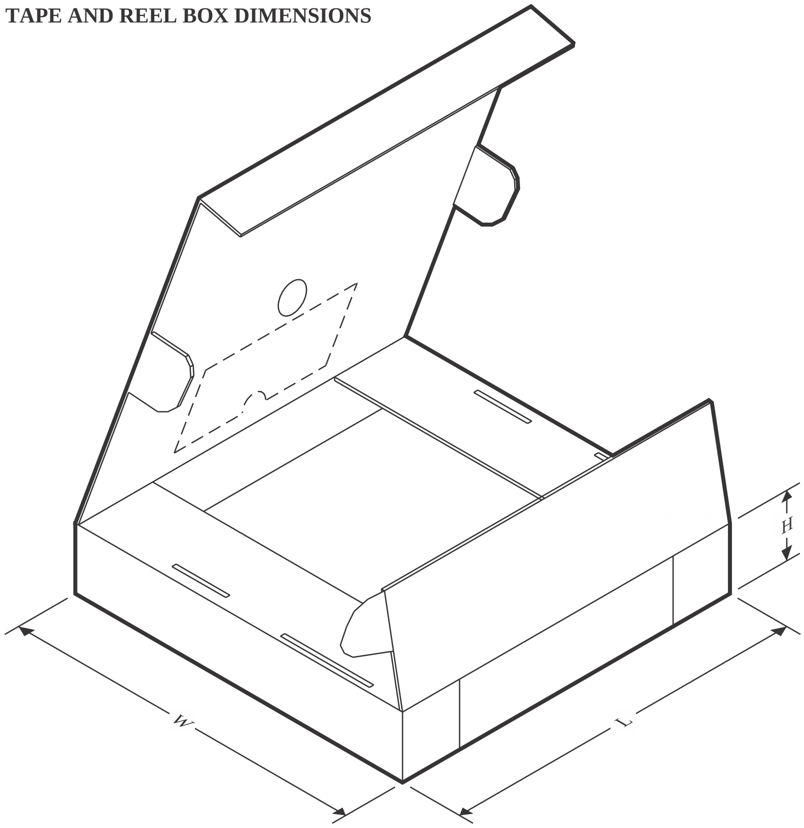
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SM72238TDE-3.3/NOPB | TO-252 | NDP | 3 | 250 | 178.0 | 16.4 | 6.9 | 10.5 | 2.7 | 8.0 | 16.0 | Q2 |
| SM72238TDE-5.0/NOPB | TO-252 | NDP | 3 | 250 | 178.0 | 16.4 | 6.9 | 10.5 | 2.7 | 8.0 | 16.0 | Q2 |
| SM72238TDX-3.3/NOPB | TO-252 | NDP | 3 | 2500 | 330.0 | 16.4 | 6.9 | 10.5 | 2.7 | 8.0 | 16.0 | Q2 |
| SM72238TDX-5.0/NOPB | TO-252 | NDP | 3 | 2500 | 330.0 | 16.4 | 6.9 | 10.5 | 2.7 | 8.0 | 16.0 | Q2 |

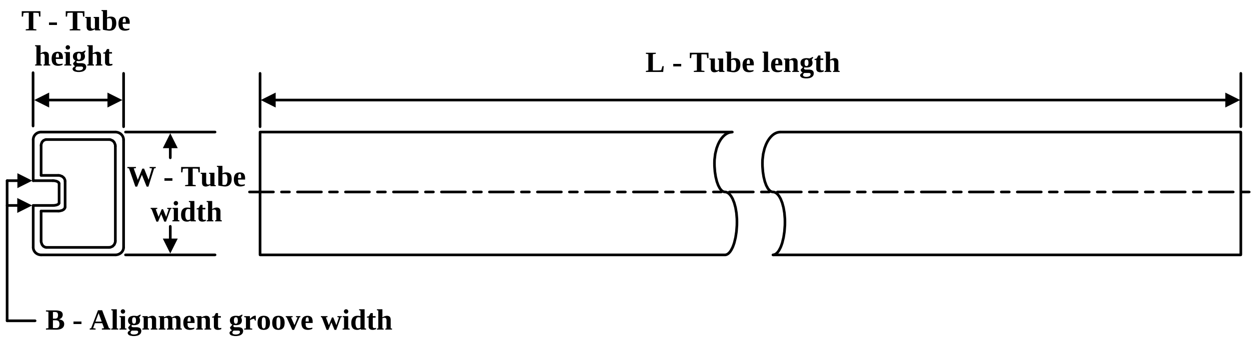
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SM72238TDE-3.3/NOPB | TO-252 | NDP | 3 | 250 | 208.0 | 191.0 | 35.0 |
| SM72238TDE-5.0/NOPB | TO-252 | NDP | 3 | 250 | 208.0 | 191.0 | 35.0 |
| SM72238TDX-3.3/NOPB | TO-252 | NDP | 3 | 2500 | 356.0 | 356.0 | 36.0 |
| SM72238TDX-5.0/NOPB | TO-252 | NDP | 3 | 2500 | 356.0 | 356.0 | 36.0 |

## TUBE



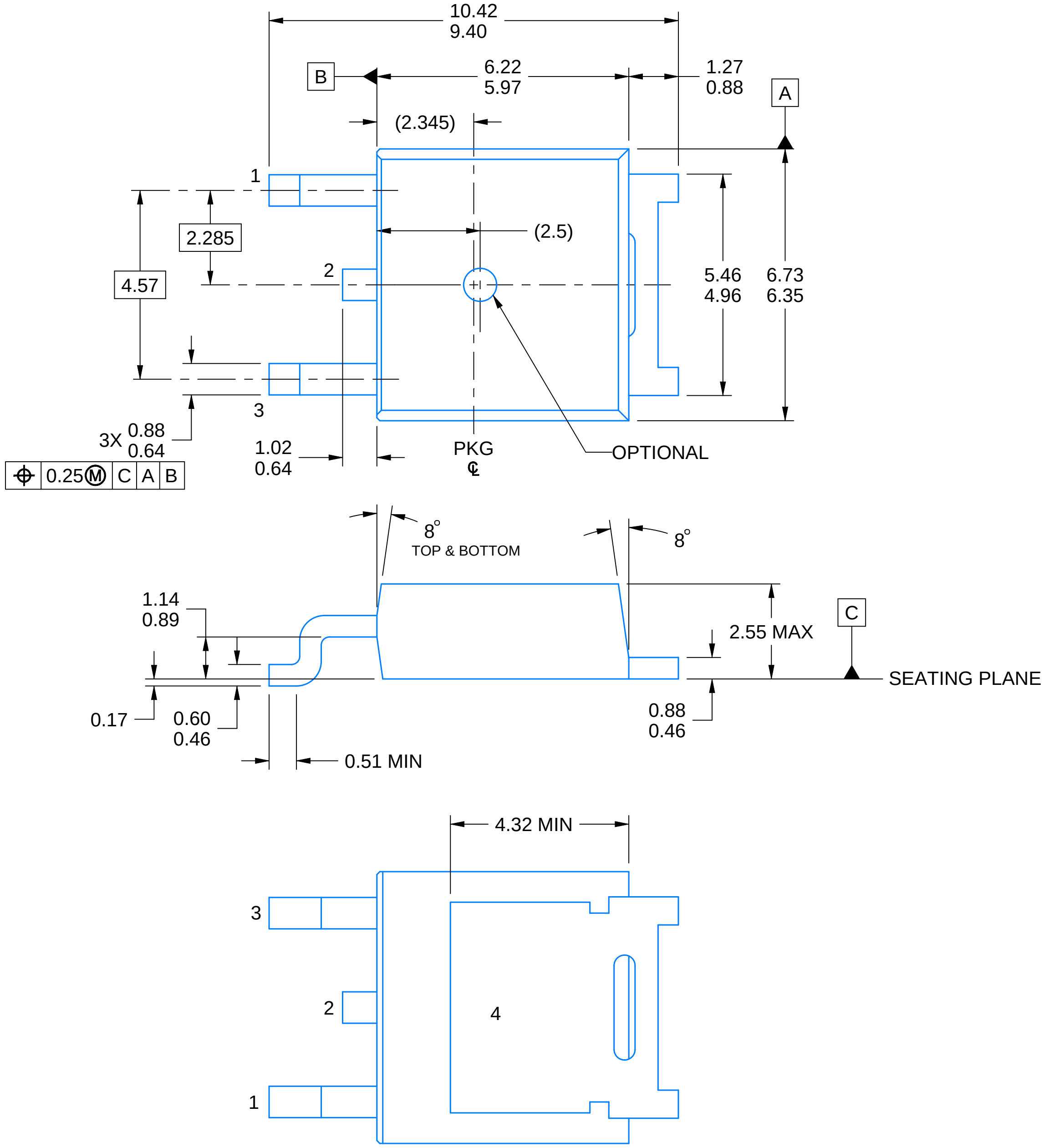

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SM72238TD-3.3/NOPB | NDP | TO-252 | 3 | 75 | 508 | 20 | 4165.6 | 3.1 |
| SM72238TD-5.0/NOPB | NDP | TO-252 | 3 | 75 | 508 | 20 | 4165.6 | 3.1 |

# PACKAGE OUTLINE

## TO-252 - 2.55 mm max height

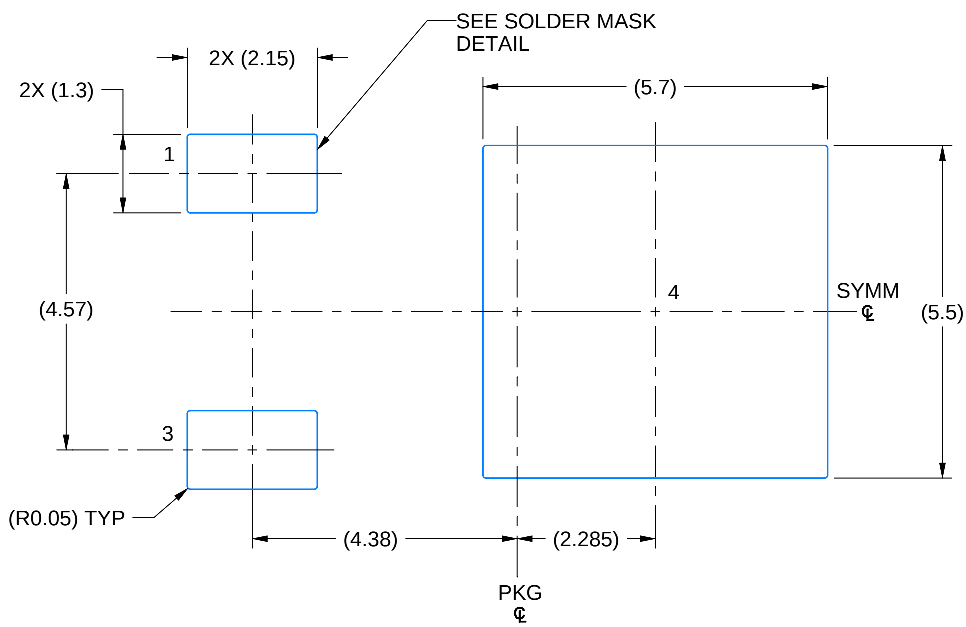
TRANSISTOR OUTLINE



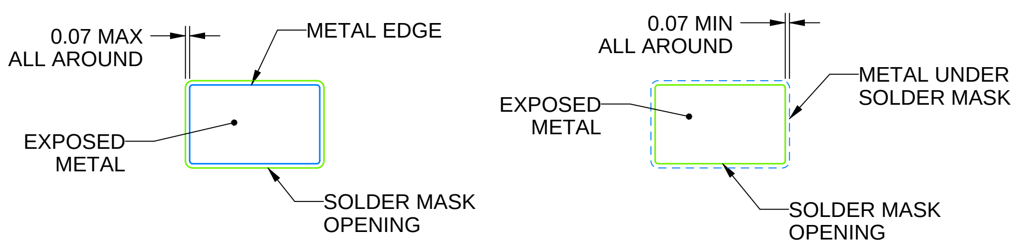

4219870/A 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-252.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X




NON SOLDER MASK
DEFINED
(PREFERRED)

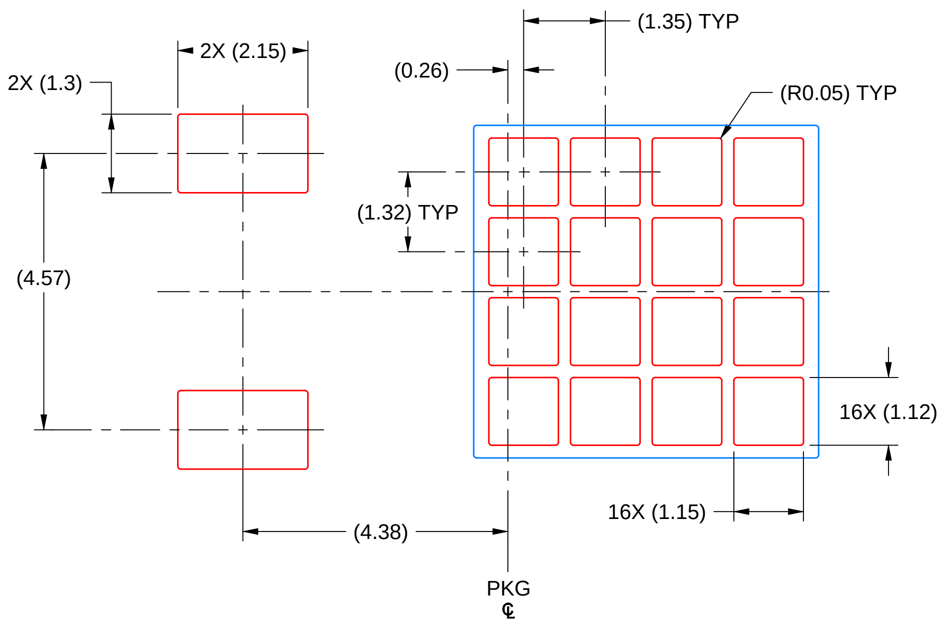
SOLDER MASK DEFINED

SOLDER MASK DETAIL

4219870/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

4219870/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.