

# SN54ABT2245, SN74ABT2245 OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

SCBS234D – SEPTEMBER 1992 – REVISED MAY 1997

- B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

## description

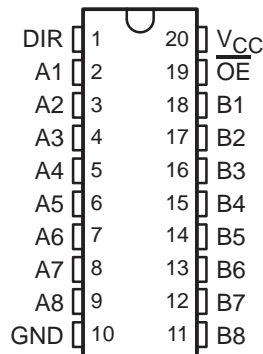
These octal transceivers and line drivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

The B-port outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

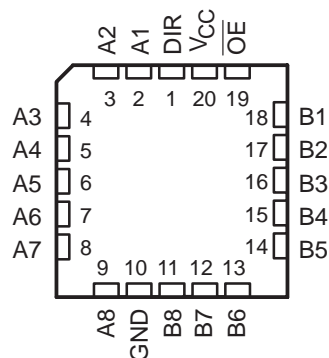
When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT2245 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT2245 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT2245 . . . J OR W PACKAGE  
SN74ABT2245 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ABT2245 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE

| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

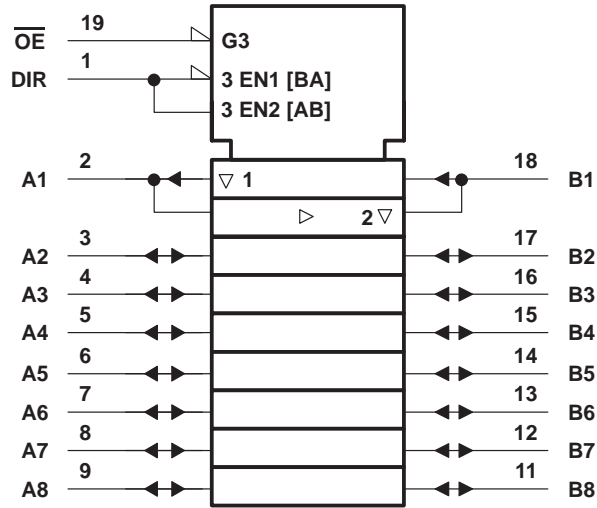
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# SN54ABT2245, SN74ABT2245 OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

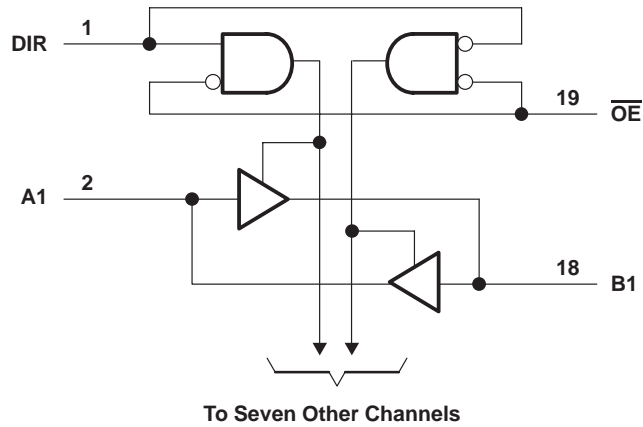
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

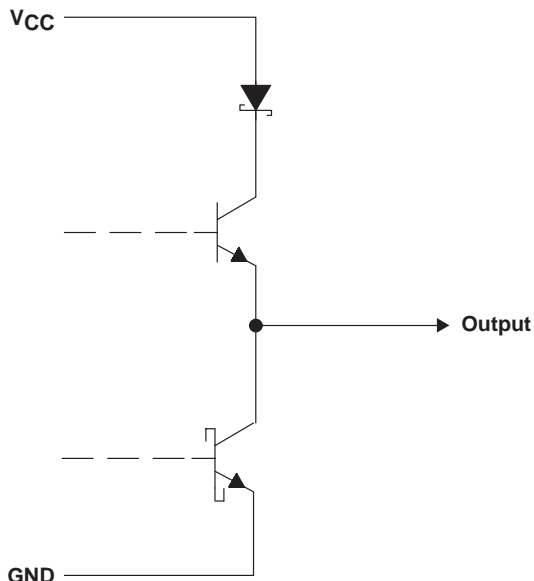
## logic diagram (positive logic)



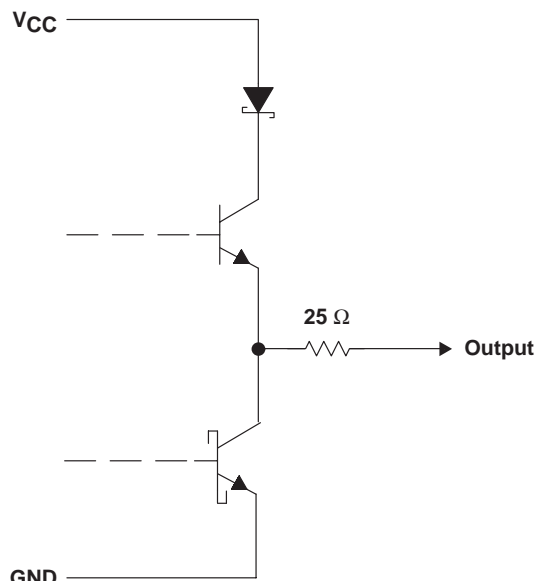
# SN54ABT2245, SN74ABT2245 OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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**schematic of A-port outputs**



**schematic of B-port outputs**



All resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

|   |                 |
|---|-----------------|
| Supply voltage range, $V_{CC}$ .....  | -0.5 V to 7 V   |
| Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....                    | -0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ .....     | -0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT2245 (except B port) ..... | 96 mA           |
| SN74ABT2245 (except B port) .....   | 128 mA          |
| B port .....  | 30 mA           |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....                                   | -18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....                                  | -50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....             | 115°C/W         |
| DW package .....  | 97°C/W          |
| N package .....   | 67°C/W          |
| PW package .....  | 128°C/W         |
| Storage temperature range, $T_{stg}$ .....  | -65°C to 150°C  |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

**SN54ABT2245, SN74ABT2245**  
**OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 3)**

|                     |                                    | SN54ABT2245     |                 | SN74ABT2245 |                 | UNIT |
|---------------------|------------------------------------|-----------------|-----------------|-------------|-----------------|------|
|                     |                                    | MIN             | MAX             | MIN         | MAX             |      |
| V <sub>CC</sub>     | Supply voltage                     | 4.5             | 5.5             | 4.5         | 5.5             | V    |
| V <sub>IH</sub>     | High-level input voltage           | 2               |                 | 2           |                 | V    |
| V <sub>IL</sub>     | Low-level input voltage            |                 | 0.8             |             | 0.8             | V    |
| V <sub>I</sub>      | Input voltage                      | 0               | V <sub>CC</sub> | 0           | V <sub>CC</sub> | V    |
| I <sub>OH</sub>     | High-level output current          | A port          |                 | -24         |                 | mA   |
|                     |                                    | B port          |                 | -12         |                 |      |
| I <sub>OL</sub>     | Low-level output current           | A port          |                 | 48          |                 | mA   |
|                     |                                    | B port          |                 | 12          |                 |      |
| Δt/Δv               | Input transition rise or fall rate | Outputs enabled |                 | 5           |                 | ns/V |
| Δt/ΔV <sub>CC</sub> | Power-up ramp rate                 | 200             |                 | 200         |                 | μs/V |
| T <sub>A</sub>      | Operating free-air temperature     | -55             | 125             | -40         | 85              | °C   |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.



# SN54ABT2245, SN74ABT2245 OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER               |                         | TEST CONDITIONS  |                          | T <sub>A</sub> = 25°C   |      |         | SN54ABT2245 |      | SN74ABT2245 |      | UNIT |     |      |
|-------------------------|-------------------------|--|--------------------------|---|------|---------|-------------|------|-------------|------|------|-----|------|
|                         |                         |  |                          | MIN   | TYP† | MAX     | MIN         | MAX  | MIN         | MAX  |      |     |      |
| V <sub>IK</sub>         |                         | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA                                     |                          | -1.2  |      |         | -1.2        |      | -1.2        |      | V    |     |      |
| V <sub>OH</sub>         | B port                  | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA                                     |                          | 3.35  |      |         | 3.3         |      | 3.35        |      | V    |     |      |
|                         |                         | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -1 mA                                       |                          | 3.85  |      |         | 3.8         |      | 3.85        |      |      |     |      |
|                         |                         | V <sub>CC</sub> = 4.5 V  |                          | I <sub>OH</sub> = -3 mA   |      | 2.6     |             |      | 3           |      |      | 3.1 |      |
|                         | V <sub>CC</sub> = 4.5 V |  | I <sub>OH</sub> = -12 mA |   | 2.6  |         |             | 2.6  |             | 2.6  |      |     |      |
|                         | A port                  | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA                                     |                          | 2.5   |      |         | 2.5         |      | 2.5         |      |      | 2.5 |      |
|                         |                         | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA                                       |                          | 3   |      |         | 3           |      | 3           |      |      | 3   |      |
| V <sub>CC</sub> = 4.5 V |                         | I <sub>OH</sub> = -24 mA   |                          | 2   |      |         | 2           |      | 2           |      |      |     |      |
| V <sub>CC</sub> = 4.5 V |                         | I <sub>OH</sub> = -32 mA   |                          | 2*  |      |         | 2           |      | 2           |      | 2    |     |      |
| V <sub>OL</sub>         | B port                  | V <sub>CC</sub> = 4.5 V  |                          | I <sub>OL</sub> = 8 mA  |      | 0.65    |             |      | 0.8         |      | 0.65 |     |      |
|                         |                         |  |                          | I <sub>OL</sub> = 12 mA   |      | 0.8     |             |      | 0.8         |      | 0.8  |     |      |
|                         | A port                  |  |                          | I <sub>OL</sub> = 48 mA   |      | 0.55    |             |      | 0.55        |      | 0.55 |     |      |
|                         |                         |  |                          | I <sub>OL</sub> = 64 mA   |      | 0.55*   |             |      | 0.55        |      | 0.55 |     |      |
| V <sub>hys</sub>        |                         |  |                          | 100   |      |         |             |      |             |      | mV   |     |      |
| I <sub>I</sub>          | Control inputs          | V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                |                          | ±1  |      |         | ±1          |      | ±1          |      | μA   |     |      |
|                         | A or B ports            | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND            |                          | ±20   |      |         | ±20         |      | ±20         |      |      |     |      |
| I <sub>OZH</sub> ‡      |                         | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V   |                          | 10  |      |         | 10          |      | 10          |      | μA   |     |      |
| I <sub>OZL</sub> ‡      |                         | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V   |                          | -10   |      |         | -10         |      | -10         |      | μA   |     |      |
| I <sub>OZPU</sub> §     |                         | V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                          | ±50   |      |         | ±50         |      | ±50         |      | μA   |     |      |
| I <sub>OZPD</sub> §     |                         | V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                          | ±50   |      |         | ±50         |      | ±50         |      | μA   |     |      |
| I <sub>off</sub>        |                         | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                        |                          | ±100  |      |         |             |      | ±100        |      | μA   |     |      |
| I <sub>CEX</sub>        | Outputs high            | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                                      |                          | 50  |      |         | 50          |      | 50          |      | μA   |     |      |
| I <sub>O</sub> ¶        | B port                  | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                      |                          | -25   |      | -100    |             | -25  |             | -100 |      | mA  |      |
|                         | A port                  |  |                          | -50   |      | -100    |             | -180 |             | -50  |      |     | -180 |
| I <sub>CC</sub>         | A or B ports            | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND |                          | Outputs high  |      | 1 250   |             | 250  |             | 250  |      | μA  |      |
|                         |                         |  |                          | Outputs low   |      | 24 32   |             | 32   |             | 32   |      | mA  |      |
|                         |                         |  |                          | Outputs disabled  |      | 0.5 250 |             | 250  |             | 250  |      | μA  |      |
| ΔI <sub>CC</sub> #      | Data inputs             | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  |                          | Outputs enabled   |      | 1.5     |             | 1.5  |             | 1.5  |      | mA  |      |
|                         |                         |  |                          | Outputs disabled  |      | 0.05    |             | 0.05 |             | 0.05 |      |     |      |
|                         | Control inputs          |  |                          | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND |      | 1.5     |             | 1.5  |             | 1.5  |      |     |      |
| C <sub>i</sub>          |                         | V <sub>I</sub> = 2.5 V or 0.5 V  |                          | 3   |      |         |             |      |             |      | pF   |     |      |
| C <sub>io</sub>         |                         | V <sub>O</sub> = 2.5 V or 0.5 V  |                          | 6   |      |         |             |      |             |      | pF   |     |      |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ This parameter is characterized but not production tested.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | $V_{CC} = 5$ V,<br>$T_A = 25^\circ$ C |     |     | SN54ABT2245 |     | SN74ABT2245 |     | UNIT |
|-----------|-----------------|-------------|---------------------------------------|-----|-----|-------------|-----|-------------|-----|------|
|           |                 |             | MIN                                   | TYP | MAX | MIN         | MAX | MIN         | MAX |      |
| $t_{PLH}$ | A               | B           | 1                                     | 2.5 | 3.4 | 1           | 4   | 1           | 3.8 | ns   |
| $t_{PHL}$ |                 |             | 1                                     | 3.2 | 4.2 | 1           | 4.6 | 1           | 4.5 |      |
| $t_{PLH}$ | B               | A           | 1                                     | 2.2 | 3.2 | 1           | 3.8 | 1           | 3.6 | ns   |
| $t_{PHL}$ |                 |             | 1                                     | 2.7 | 3.6 | 1           | 4.2 | 1           | 4   |      |
| $t_{PZH}$ | $\overline{OE}$ | A           | 1                                     | 3.3 | 4.6 | 1           | 5.6 | 1           | 5.5 | ns   |
| $t_{PZL}$ |                 |             | 1                                     | 3.2 | 4.7 | 1           | 6   | 1           | 5.7 |      |
| $t_{PHZ}$ | $\overline{OE}$ | A           | 2                                     | 4   | 5.1 | 2           | 5.7 | 2           | 5.6 | ns   |
| $t_{PLZ}$ |                 |             | 1                                     | 2.9 | 4   | 1           | 4.6 | 1           | 4.5 |      |
| $t_{PZH}$ | $\overline{OE}$ | B           | 1.5                                   | 3.6 | 4.9 | 1.5         | 6.3 | 1.5         | 6.1 | ns   |
| $t_{PZL}$ |                 |             | 1.5                                   | 3.9 | 5.3 | 1.5         | 6.6 | 1.5         | 6.3 |      |
| $t_{PHZ}$ | $\overline{OE}$ | B           | 1.5                                   | 3.6 | 4.7 | 1.5         | 5.5 | 1.5         | 5.3 | ns   |
| $t_{PLZ}$ |                 |             | 1.5                                   | 3.3 | 4.4 | 1.5         | 4.9 | 1.5         | 4.8 |      |



# SN54ABT2245, SN74ABT2245 OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

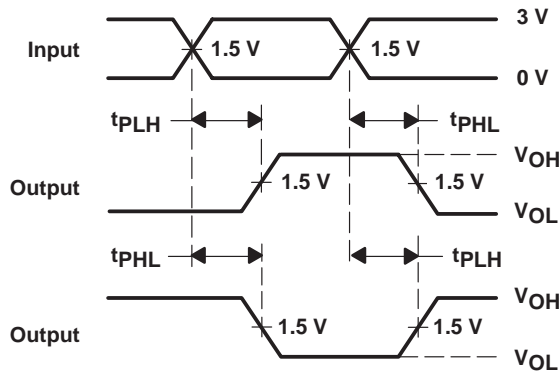
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



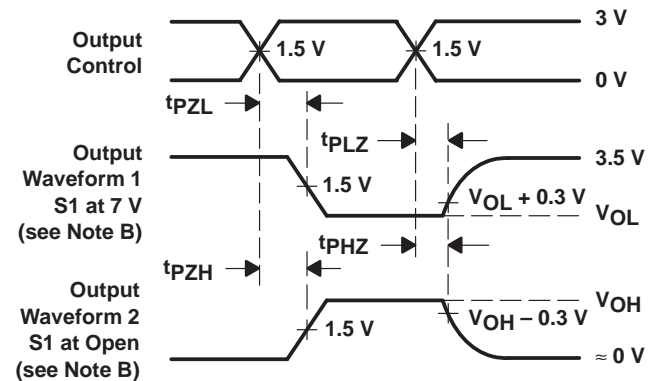
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)               | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|---------------------------------------|-------------------------|
| 5962-9560601Q2A  | ACTIVE        | LCCC         | FK              | 20   | 55          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9560601Q2A<br>SNJ54<br>ABT2245FK | <a href="#">Samples</a> |
| 5962-9560601QRA  | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9560601QR<br>A<br>SNJ54ABT2245J  | <a href="#">Samples</a> |
| 5962-9560601QSA  | ACTIVE        | CFP          | W               | 20   | 25          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9560601QS<br>A<br>SNJ54ABT2245W  | <a href="#">Samples</a> |
| SN74ABT2245DBR   | ACTIVE        | SSOP         | DB              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AA245                                 | <a href="#">Samples</a> |
| SN74ABT2245DBRG4 | ACTIVE        | SSOP         | DB              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AA245                                 | <a href="#">Samples</a> |
| SN74ABT2245DW    | ACTIVE        | SOIC         | DW              | 20   | 25          | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT2245                               | <a href="#">Samples</a> |
| SN74ABT2245DWR   | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT2245                               | <a href="#">Samples</a> |
| SN74ABT2245N     | ACTIVE        | PDIP         | N               | 20   | 20          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74ABT2245N                          | <a href="#">Samples</a> |
| SN74ABT2245PW    | ACTIVE        | TSSOP        | PW              | 20   | 70          | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AA245                                 | <a href="#">Samples</a> |
| SN74ABT2245PWR   | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AA245                                 | <a href="#">Samples</a> |
| SNJ54ABT2245FK   | ACTIVE        | LCCC         | FK              | 20   | 55          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9560601Q2A<br>SNJ54<br>ABT2245FK | <a href="#">Samples</a> |
| SNJ54ABT2245J    | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9560601QR<br>A<br>SNJ54ABT2245J  | <a href="#">Samples</a> |
| SNJ54ABT2245W    | ACTIVE        | CFP          | W               | 20   | 25          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9560601QS<br>A<br>SNJ54ABT2245W  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.



**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ABT2245, SN74ABT2245 :**

● Catalog : [SN74ABT2245](#)

● Military : [SN54ABT2245](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT2245DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ABT2245DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74ABT2245PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT2245DBR | SSOP         | DB              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74ABT2245DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74ABT2245PWR | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9560601Q2A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-9560601QSA | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74ABT2245DW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74ABT2245N    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74ABT2245PW   | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| SNJ54ABT2245FK  | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54ABT2245W   | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.



# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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