TEXAS INSTRUMENTS

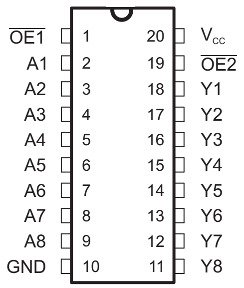
SN54ABT541, SN74ABT541B OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS093L – DECEMBER 1993 – REVISED DECEMBER 2006

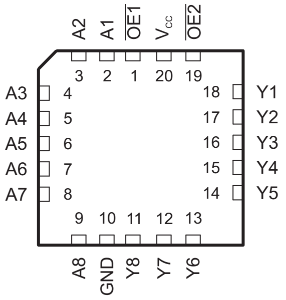
FEATURES

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (N) and Ceramic (J) DIPs**

SN54ABT541...J OR W PACKAGE
SN74ABT541B...DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT541...FK PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN54ABT541 and SN74ABT541B octal buffers and line drivers are ideal for driving bus lines or buffering memory address registers. The devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Reel of 1000	SN74ABT541BN	SN74ABT541BN
	SOIC – DW	Tube of 25	SN74ABT541BDW	ABT541B
		Reel of 2000	SN74ABT541BDWR	
	SSOP – DB	Reel of 2000	SN74ABT541BDBR	AB541B
			SN74ABT541BDBRG4	
	TSSOP – PW	Reel of 1050	SN74ABT541BPW	AB541B
		Reel of 2000	SN74ABT541BPWR	
–55°C to 125°C	CDIP – J	Reel of 1000	SNJ54ABT541J	SNJ54ABT541J
	CFP – W	Reel of 510	SNJ54ABT541W	SNJ54ABT541W
	LCCC – FK	Reel of 2200	SNJ54ABT541FK	SNJ54ABT541FK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

EPIC-IIB is a trademark of Texas Instruments.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{\text{OE1}}$ or $\overline{\text{OE2}}$) input is high, all eight outputs are in the high-impedance state.

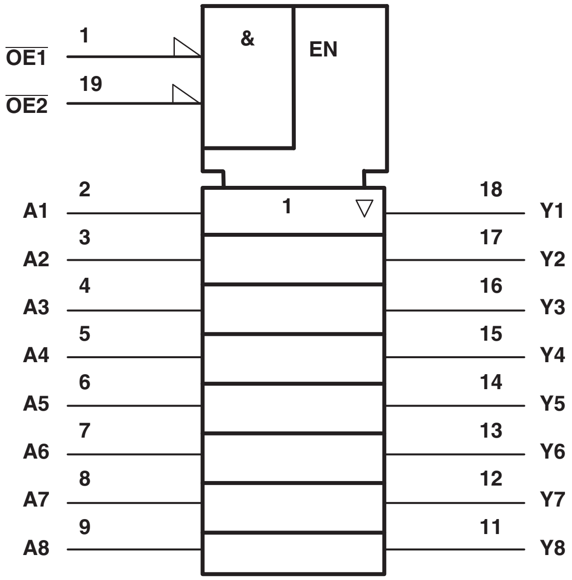
When VCC is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{\text{OE}}$ should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT541B is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

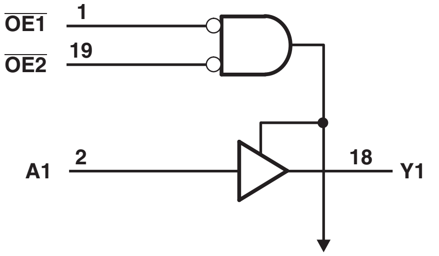
INPUTS			OUTPUTS Y
$\overline{\text{OE1}}$	$\overline{\text{OE2}}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

LOGIC SYMBOL(1)



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



To Seven Other Channels

Absolute Maximum Ratings[1]

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[2]		–0.5	7	V
V_O	Voltage range applied to any output in the high or power-off state		–0.5	5.5	V
I_O	Current into any output in the low state	SN54ABT541		96	mA
		SN74ABT541B		128	
I_{IK}	Input clamp current	$V_I < 0$		–18	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance[3]	DB package		115	°C/W
		DW package		97	
		N package		67	
		PW package		128	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

Recommended Operating Conditions[1]

over recommended operating free-air temperature range (unless otherwise noted)

		SN54ABT541		SN74ABT541B		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate			200		µs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT51		SN74ABT541B		UNIT
			MIN	TYP(1)	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA	3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = –24 mA	2			2				
		I_{OH} = –32 mA	2(2)					2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55		0.55			VV
		I_{OL} = 64 mA			0.55(2)				0.55	
V_{hys}				100						mV
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZPU}	V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50(3)		±50(3)		±50	µA
I_{OZPD}	V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50(3)		±50(3)		±50	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			–10		–10		–10	µA
I_{off}	V_{CC} = 0 V,	V_I or $V_O \le$ 4.5 V			±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V,	Outputs high			50				50	µA
I_O	V_{CC} = 5.5 V(4),	V_O = 2.5 V	–50	–140	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0 V, V_I = V_{CC} or GND	Outputs high		5	250		250		250	µA
		Outputs low		22	30		30		30	mA
		Outputs disabled		1	250		250		250	µA
ΔI_{CC}	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND(5)	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA
		Control Inputs			1.5		1.2		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			6						pF

(1) All typical values are at V_{CC} = 5 V.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.
(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(4) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
(5) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Switching Characteristics, SN54ABT541

over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 5 V, TA = 25°C					UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.6	4.1	1	4.6	ns
t_{PHL}			1	2.9	4.2	1	4.7	
t_{PZH}	$\overline{OE}$	Y	1.1	3.1	4.8	1.1	5.4	ns
t_{PZL}			2.1	4.4	5.9	2.1	7	
t_{PHZ}	$\overline{OE}$	Y	2.1	5.1	6.6	2.1	7.5	ns
t_{PLZ}			1.7	4.7	6.2	1.7	6.7	

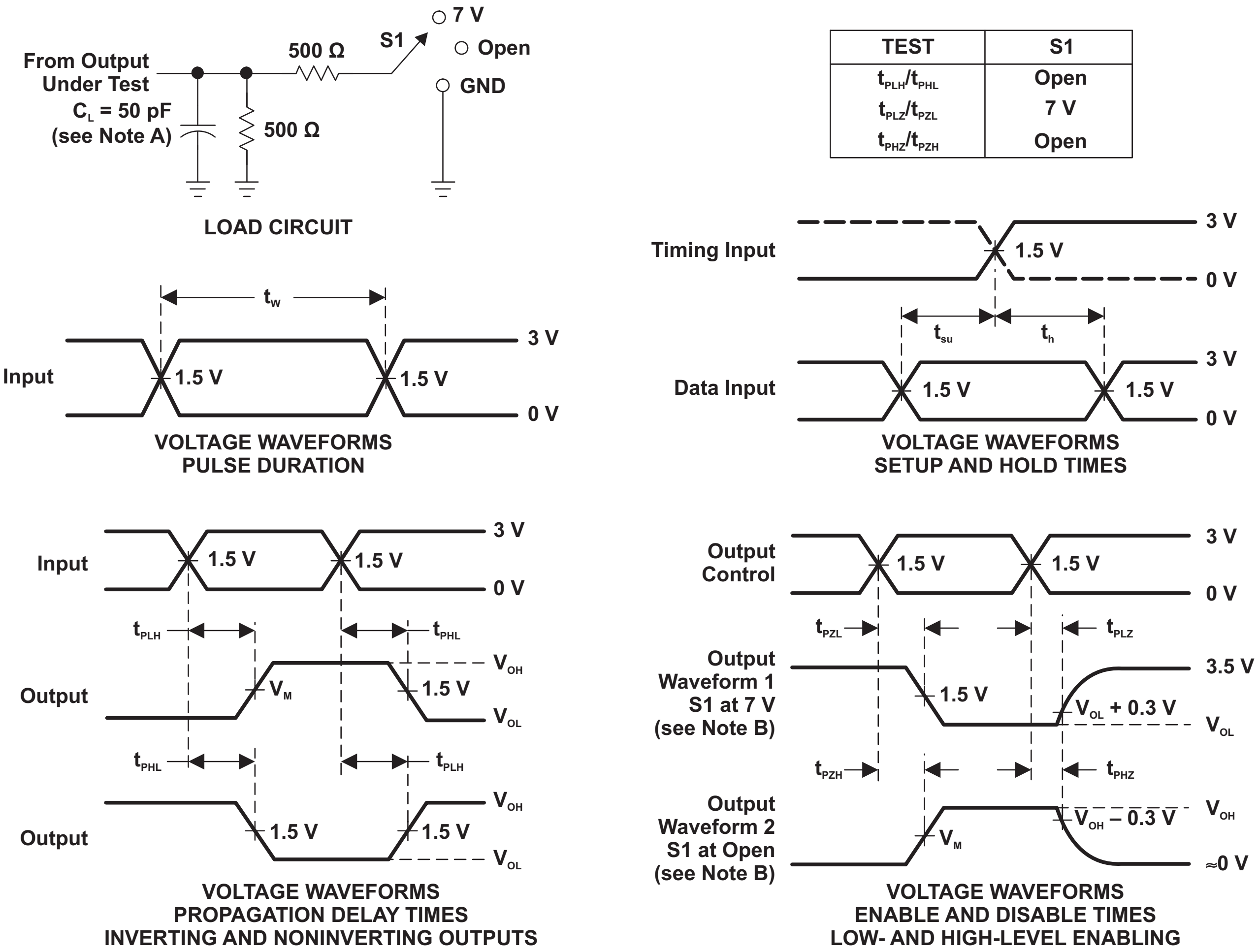
Switching Characteristics, SN74ABT541B

over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 5 V, TA = 25°C					UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2	3.2	1	3.9	ns
t_{PHL}			1	2.6	3.5	1	3.9	
t_{PZH}	$\overline{OE}$	Y	2	3.5	4.5	2	4	ns
t_{PZL}			1.9	4	5.1	1.9	5.9	
t_{PHZ}	$\overline{OE}$	Y	2.2	4.4	5.4	2.2	5.8	ns
t_{PLZ}			1.5	3	4	1.5	4.4	
$t_{sk(o)}$ (1)					0.5		0.5	ns

(1) Skew between any two outputs of the same package switching in the same direction.

PARAMETER MEASURMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9471801Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9471801Q2A SNJ54ABT541FK	Samples
5962-9471801QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9471801QRA SNJ54ABT541J	Samples
5962-9471801QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9471801QSA SNJ54ABT541W	Samples
SN74ABT541BDBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB541B	Samples
SN74ABT541BDBRE4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB541B	Samples
SN74ABT541BDBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB541B	Samples
SN74ABT541BDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT541B	Samples
SN74ABT541BDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT541B	Samples
SN74ABT541BDWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT541B	Samples
SN74ABT541BDWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT541B	Samples
SN74ABT541BN	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT541BN	Samples
SN74ABT541BNSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT541B	Samples
SN74ABT541BPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB541B	Samples
SN74ABT541BPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB541B	Samples
SN74ABT541BPWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB541B	Samples
SNJ54ABT541FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9471801Q2A SNJ54ABT541FK	Samples

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54ABT541J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9471801QR A SNJ54ABT541J	Samples
SNJ54ABT541W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9471801QS A SNJ54ABT541W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74ABT541B :

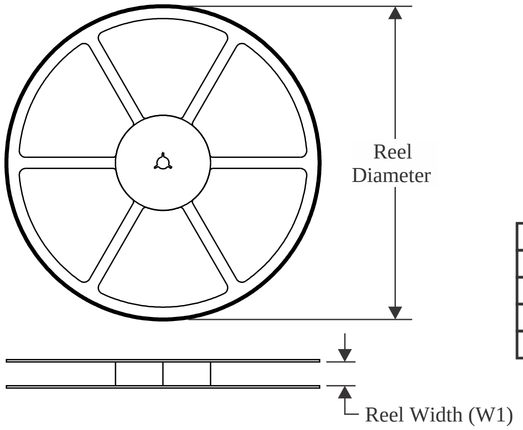
- Automotive : SN74ABT541B-Q1
- Enhanced Product : SN74ABT541B-EP

NOTE: Qualified Version Definitions:

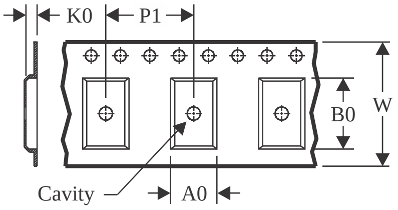
  - Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
  - Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

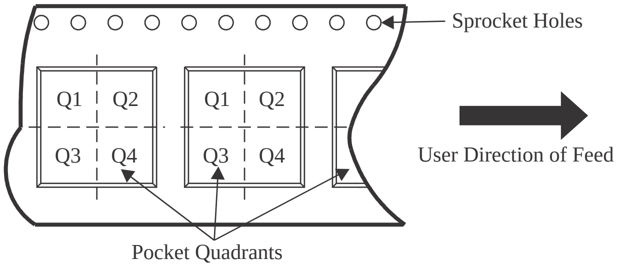


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

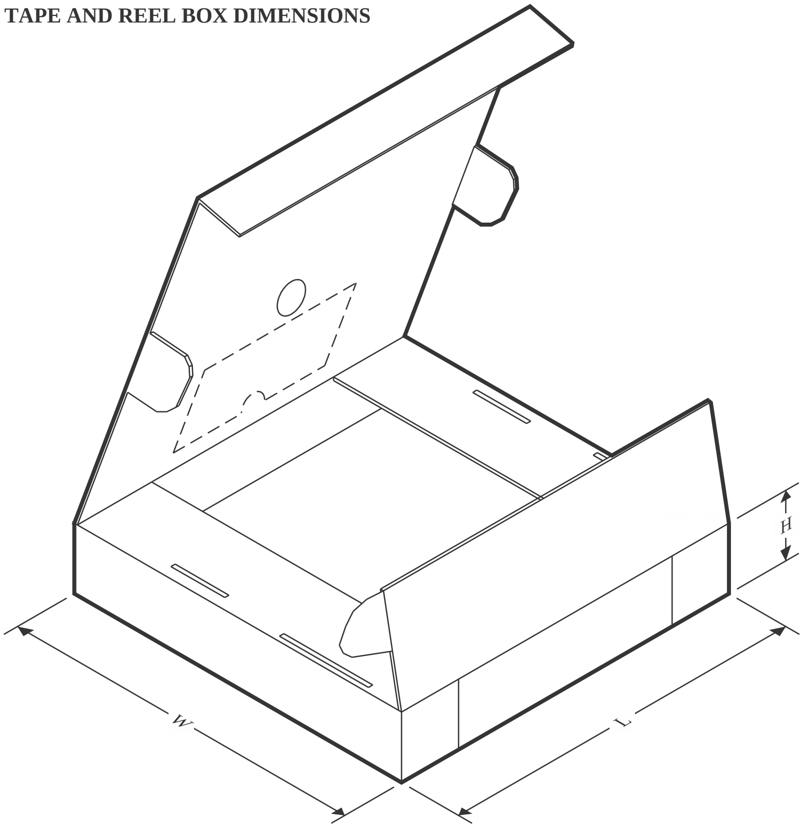
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT541BDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT541BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT541BNSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ABT541BPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

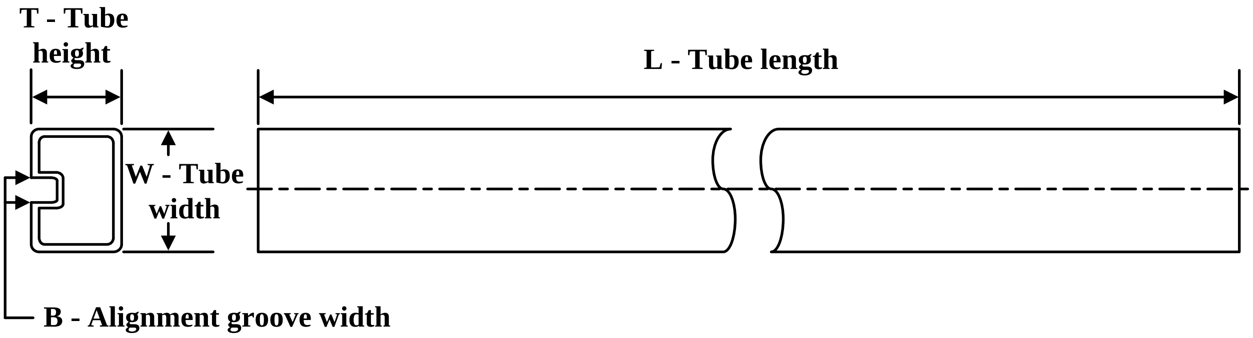
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT541BDBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74ABT541BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ABT541BNSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ABT541BPWR	TSSOP	PW	20	2000	356.0	356.0	35.0

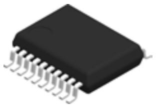
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9471801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9471801QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ABT541BDW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT541BN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT541BPW	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54ABT541FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ABT541W	W	CFP	20	25	506.98	26.16	6220	NA

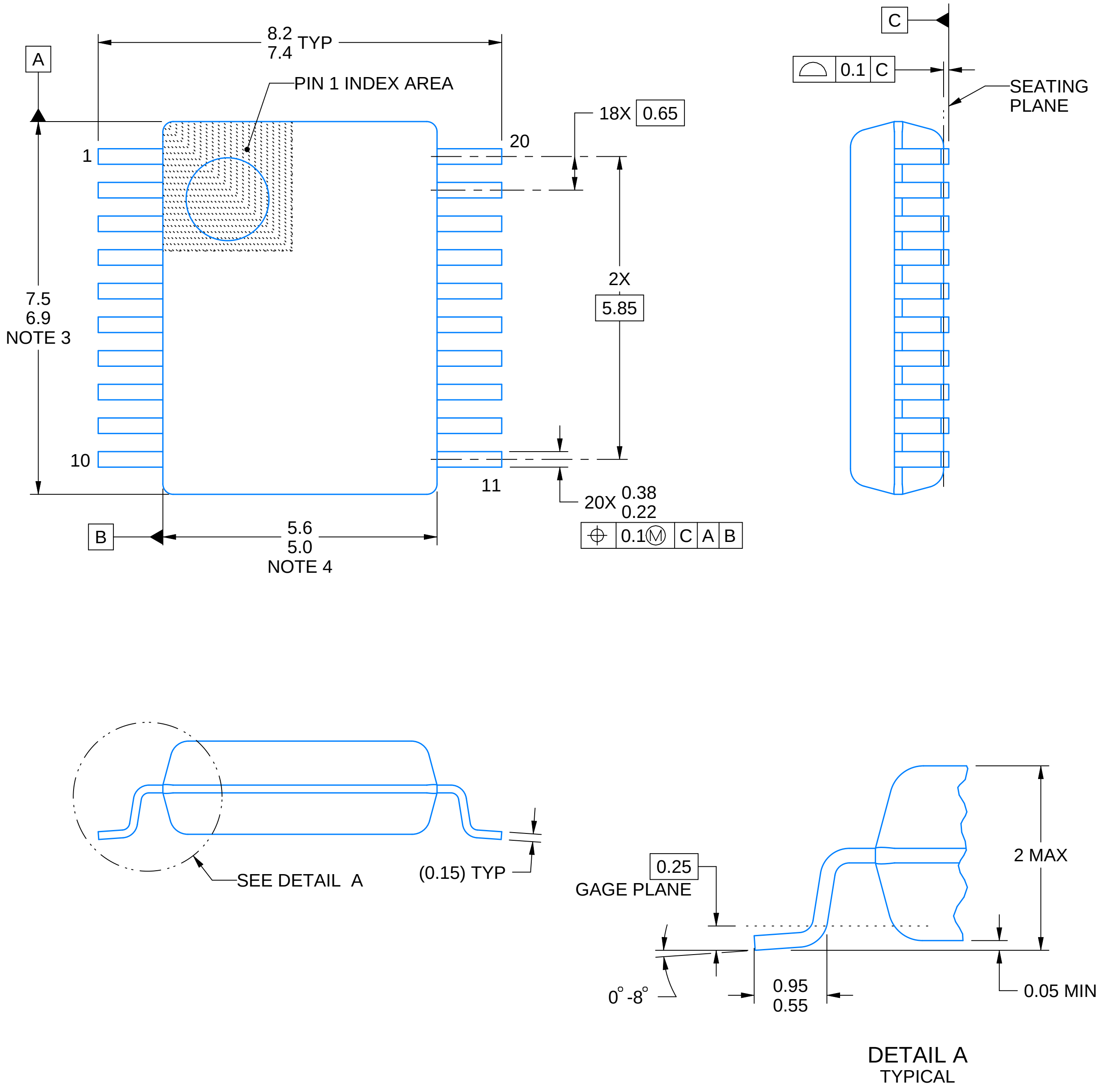
PACKAGE OUTLINE



DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

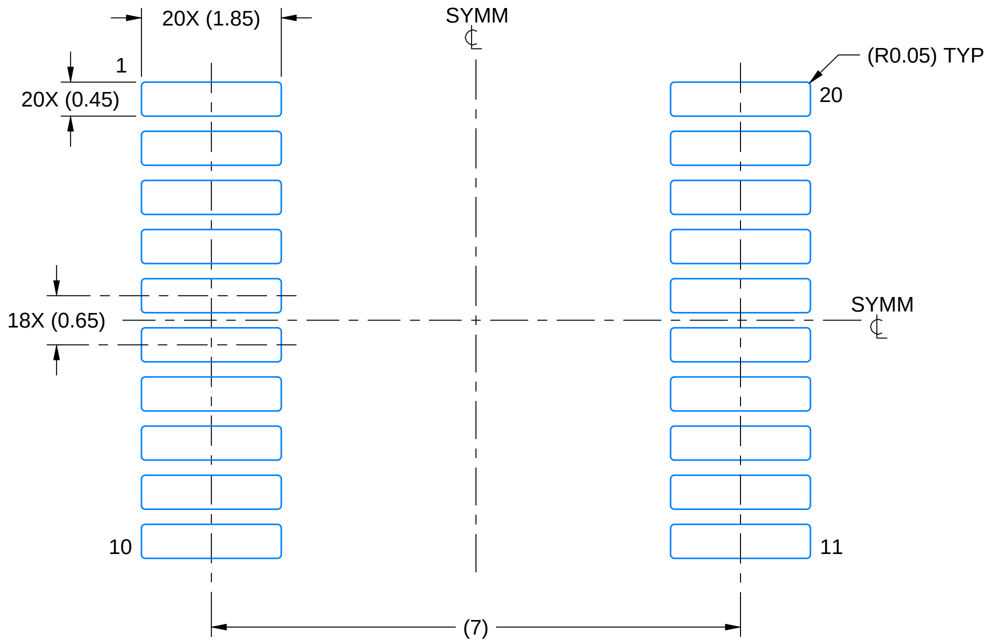
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

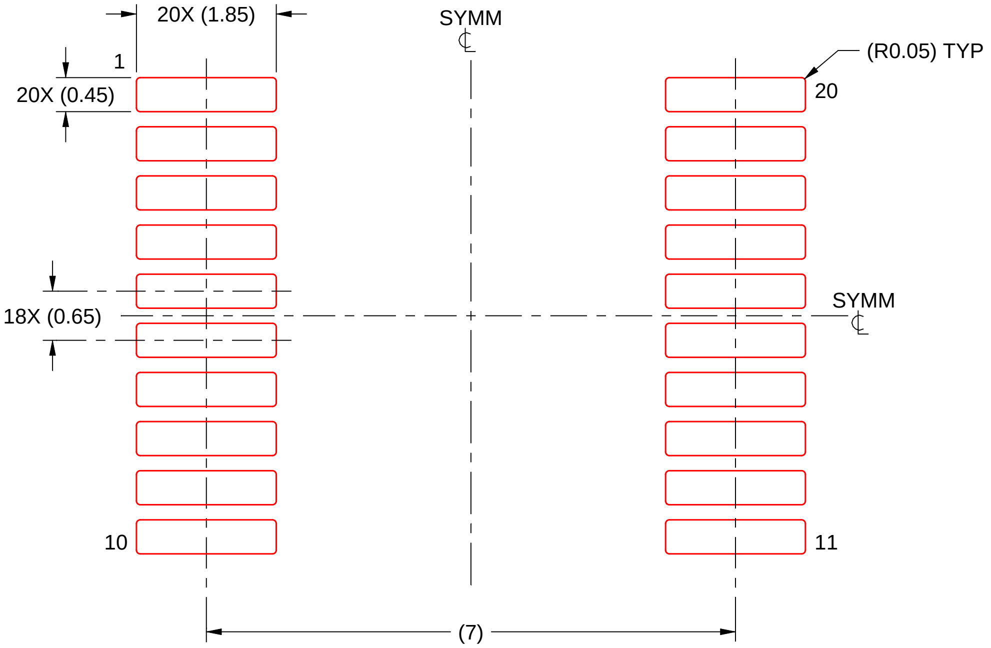
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

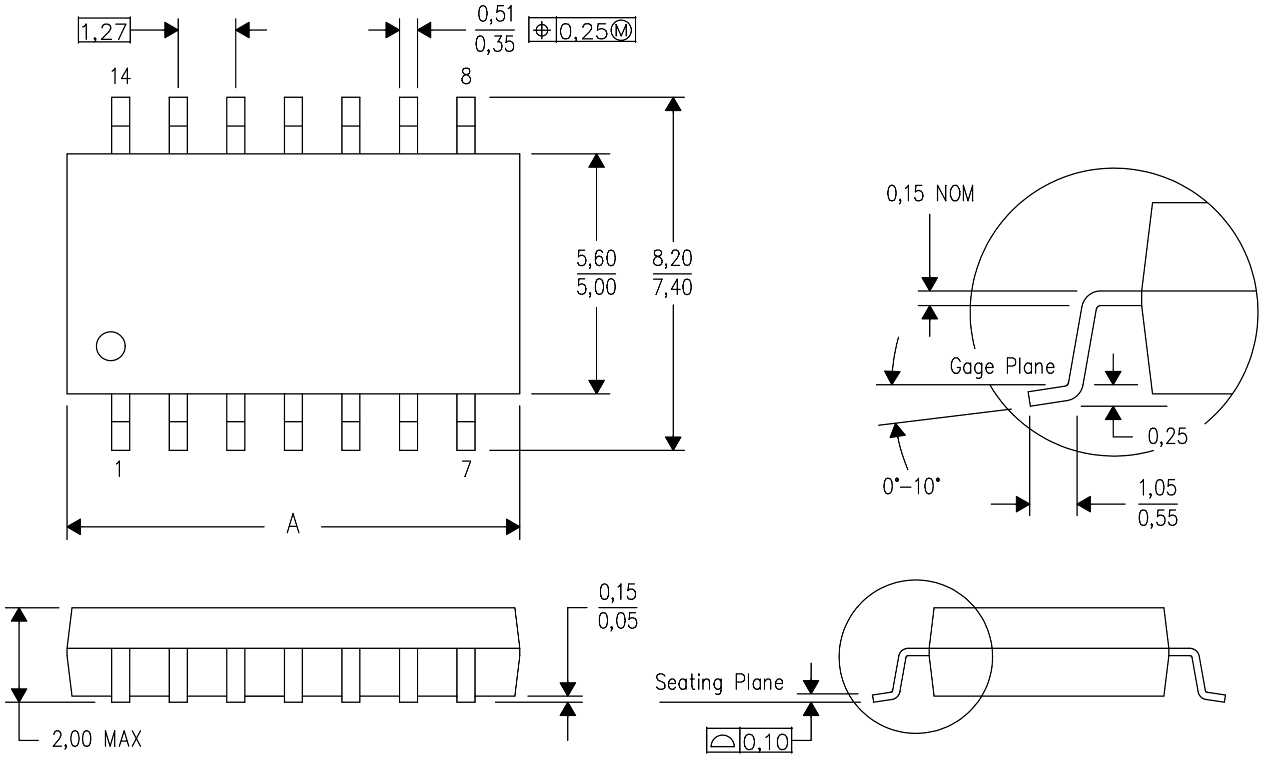
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



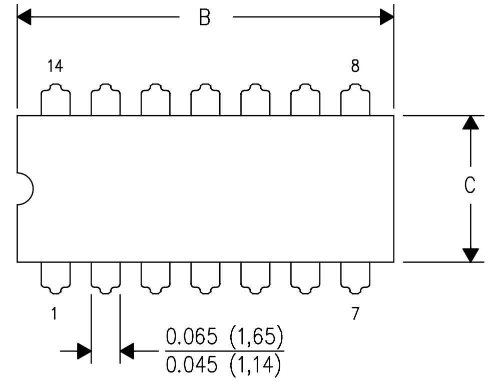
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

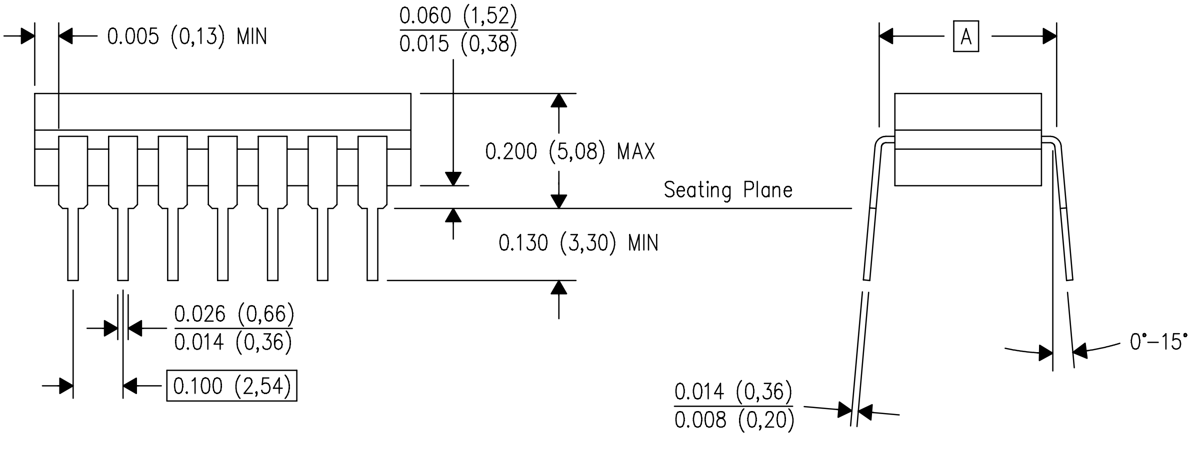
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R−GDIP−T**) CERAMIC DUAL IN−LINE PACKAGE

14 LEADS SHOWN



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

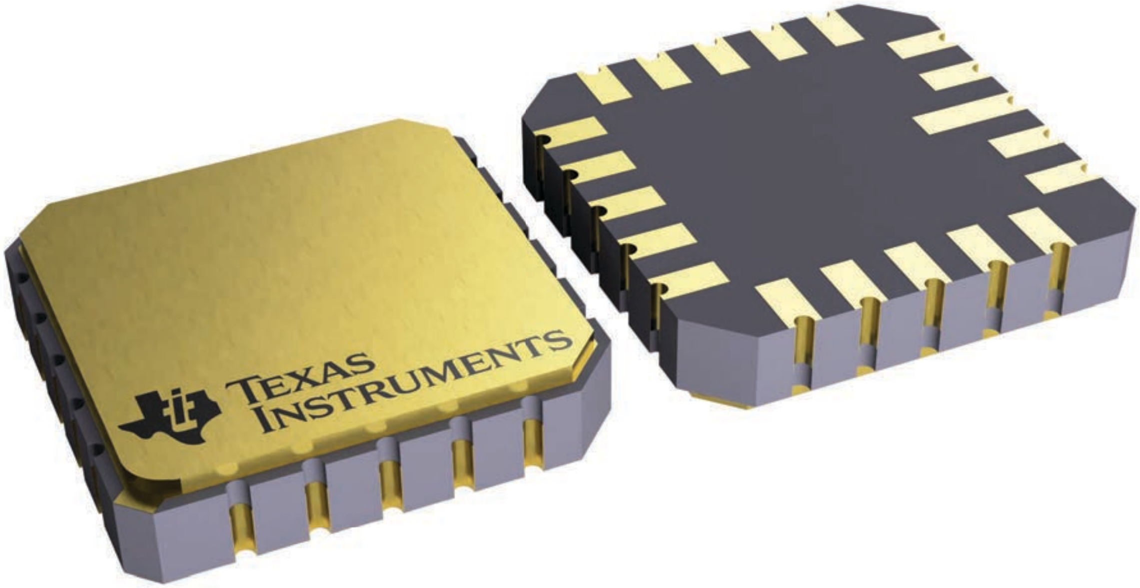
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

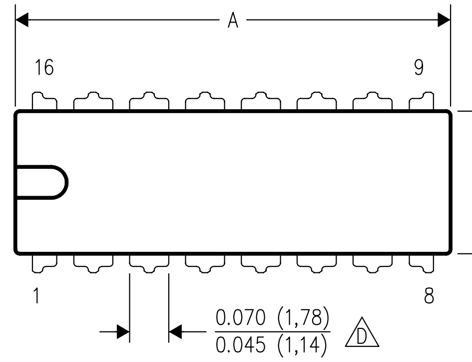
LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

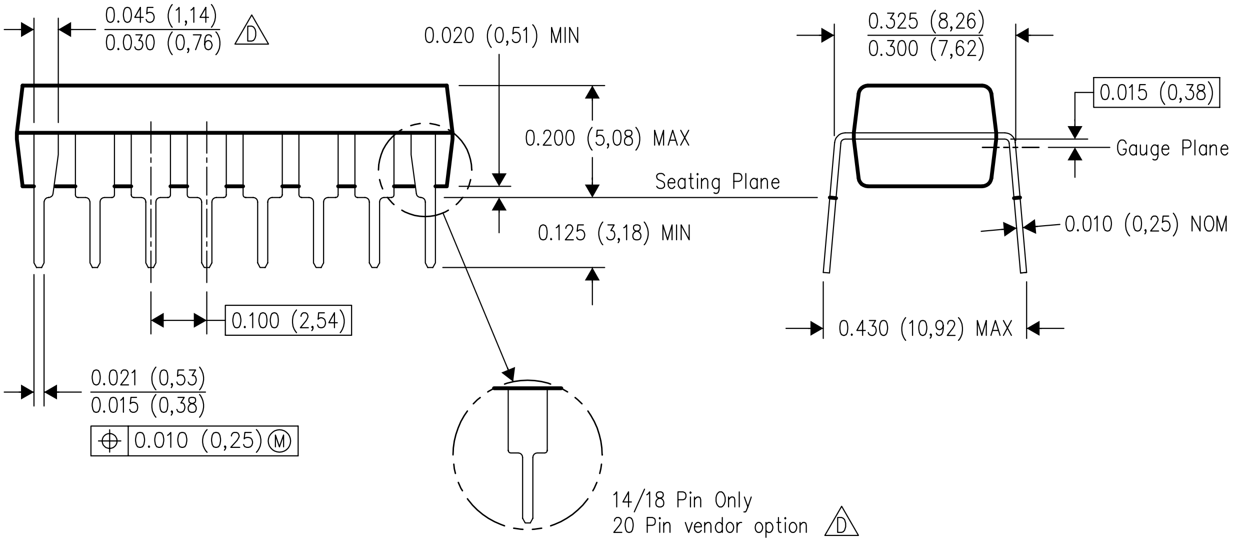


N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

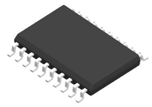


PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
△C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
△D The 20 pin end lead shoulder width is a vendor option, either half or full width.

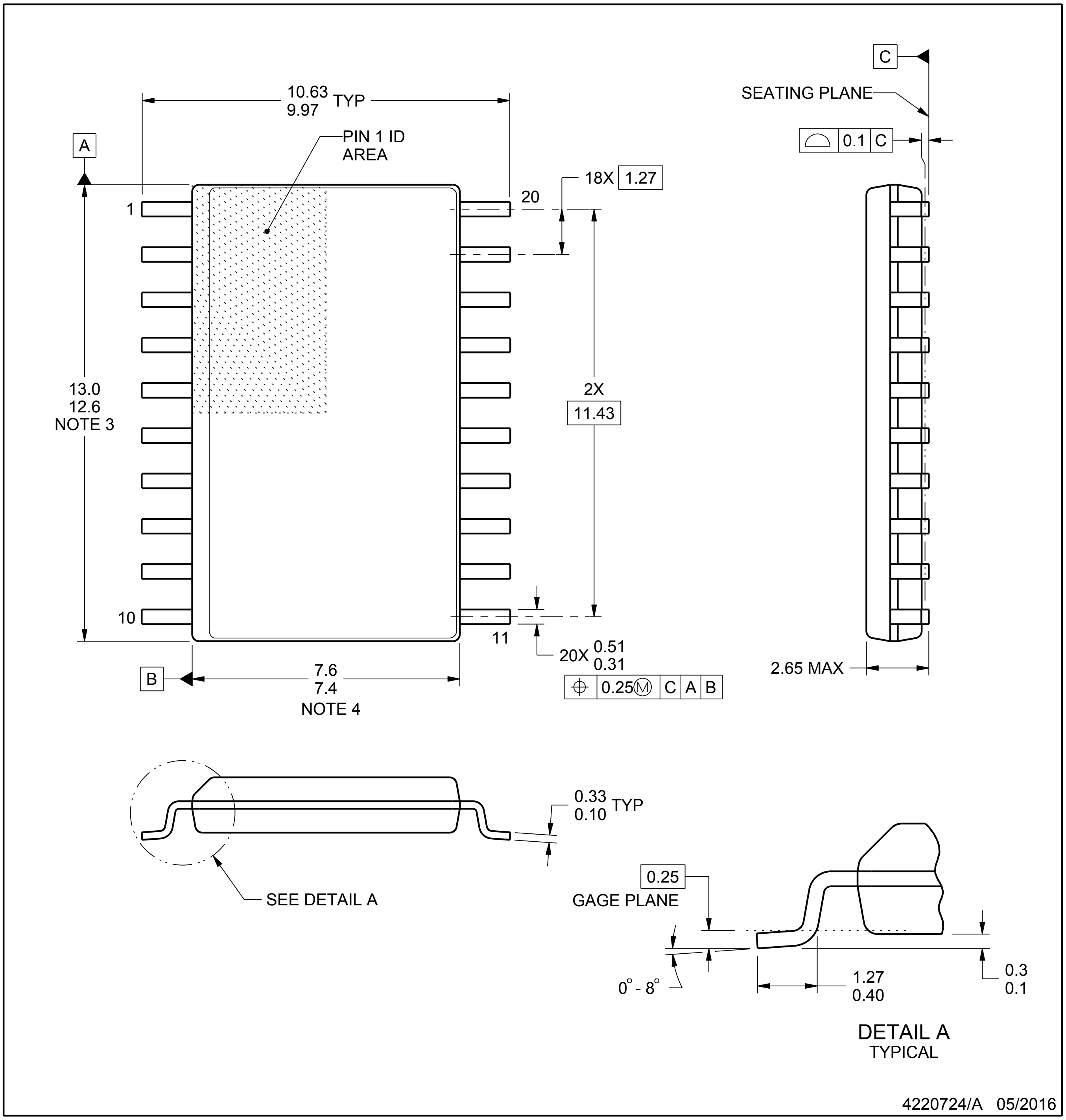


PACKAGE OUTLINE

DW0020A

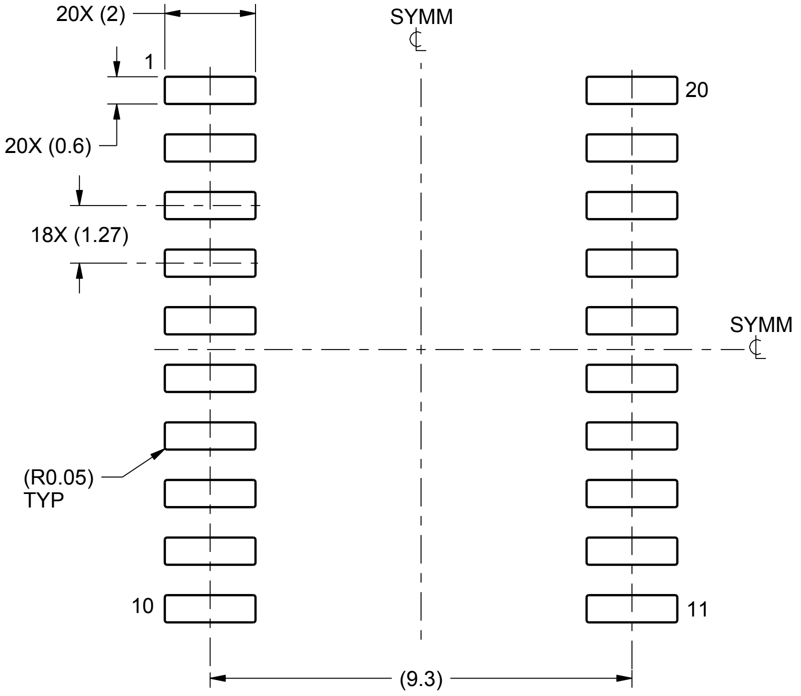
SOIC - 2.65 mm max height

SOIC

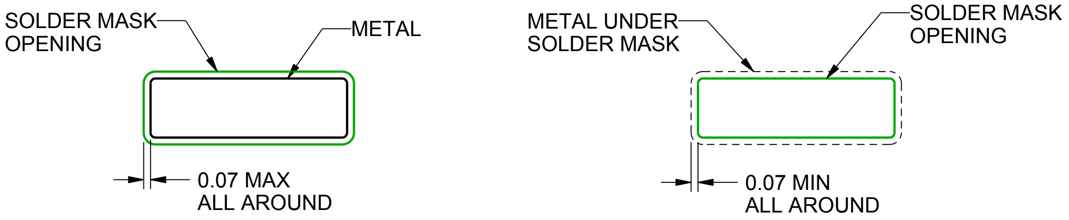


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



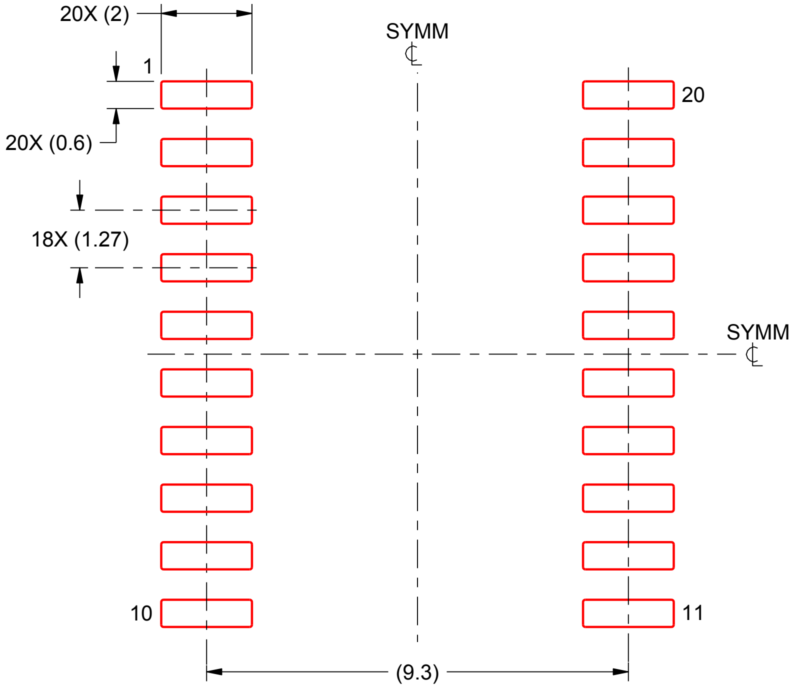
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



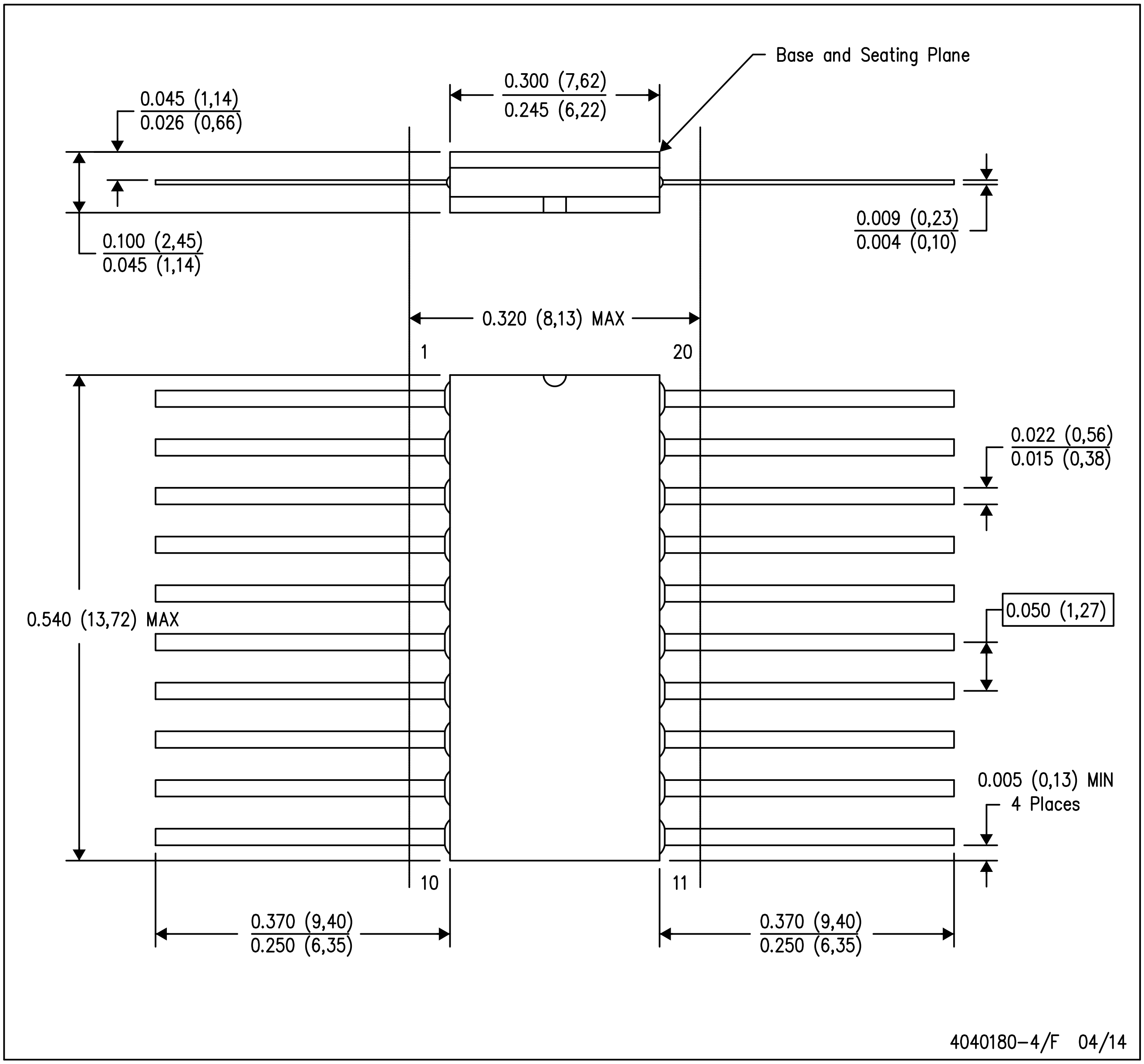
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

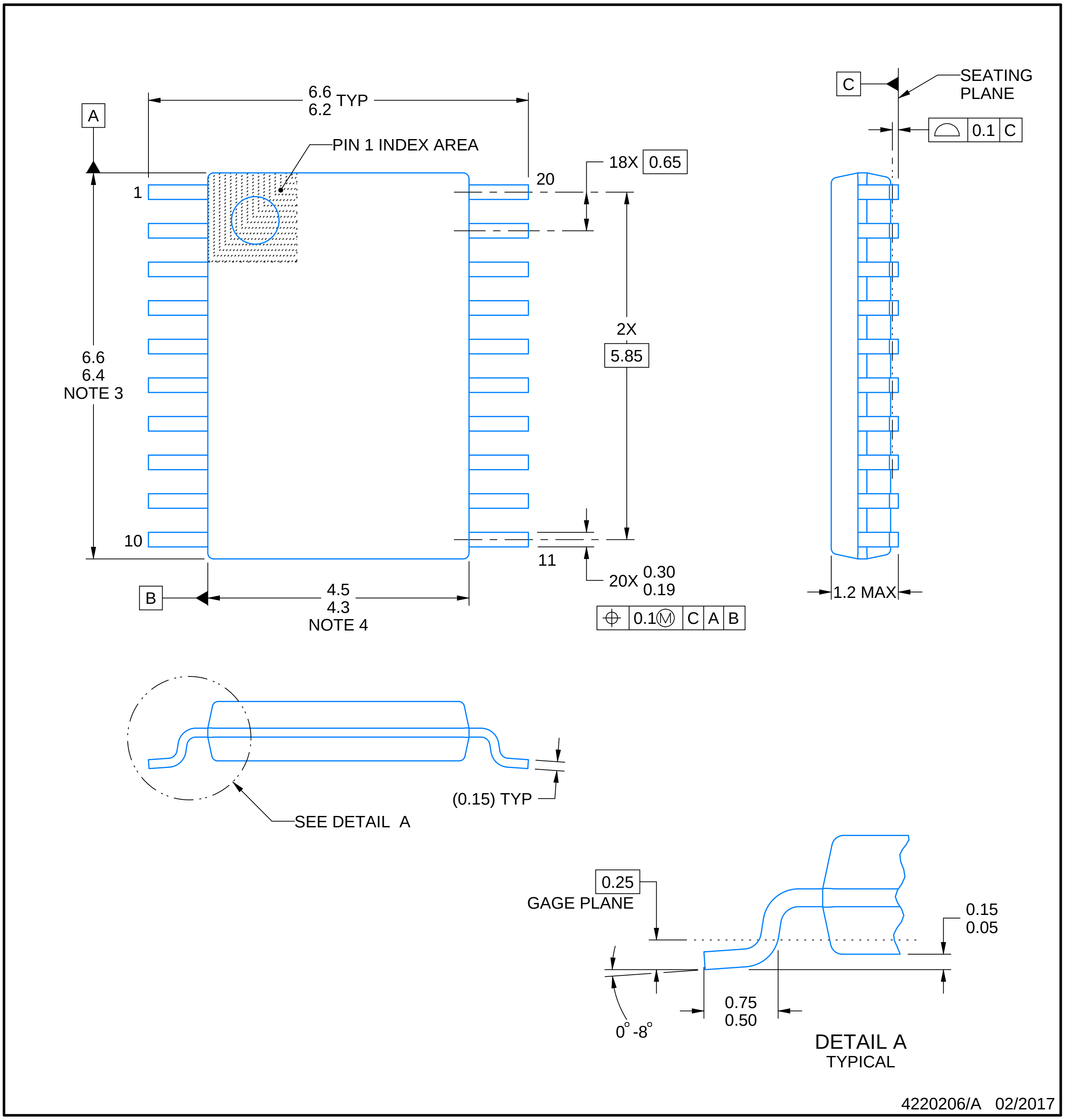
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK

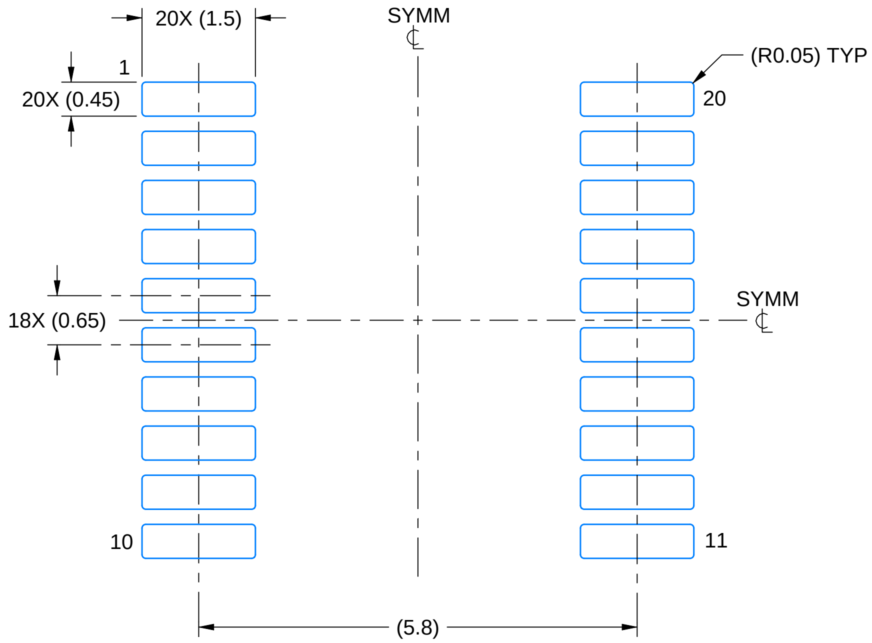


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil–Std 1835 GDFP2–F20



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

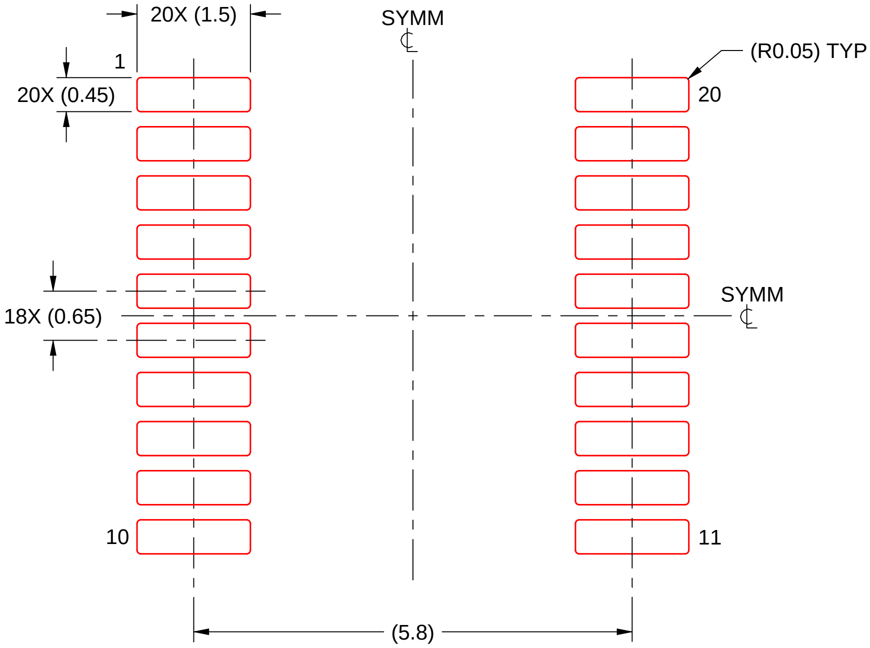
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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