SNx4AC244 Octal Buffers or Drivers with 3-State Outputs

1 Features

- Operation of 2V to 6V V_{CC}
- Inputs accept voltages to 6V
- Max t_{pd} of 7.5ns at 5V

2 Applications

- Servers and network switches
- LED displays
- Telecom infrastructure
- Motor-drive control boards

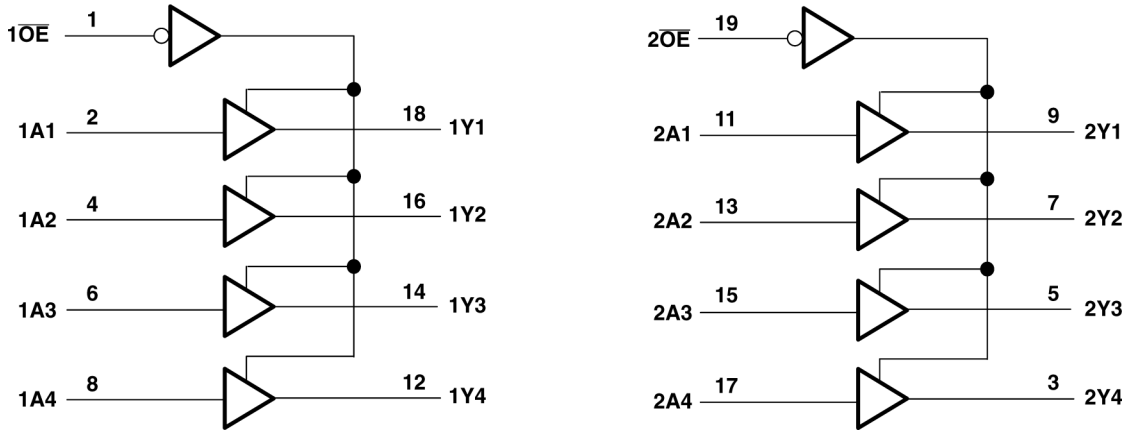
3 Description

These octal buffers and line drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AC244	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.3mm
	DGS (VSSOP, 20)	5.1mm × 4.9mm	5.1mm × 3mm
	DW (SOIC, 20)	12.8mm × 10.3mm	12.8mm × 7.5mm
	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm
	PW (TSSOP, 20)	6.5mm × 4.4mm	6.5mm × 4.4mm
	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm
SN54AC244	J (CDIP, 20)	24.2mm x 7.62mm	24.2mm × 6.92mm
	W (CFP, 20)	13.09mm x 8.13mm	13.09mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

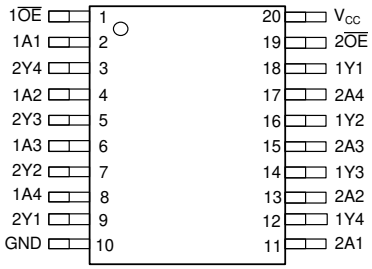


Figure 4-1. SN54AC244 J or W Package; SN74AC244 DB, DGS, DW, N, NS, or PW Package (Top View)

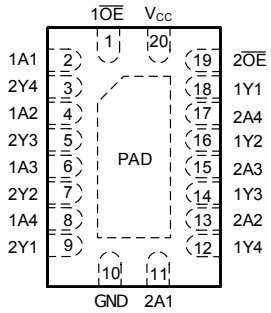


Figure 4-2. SN74AC244 RKS Package (Top View)

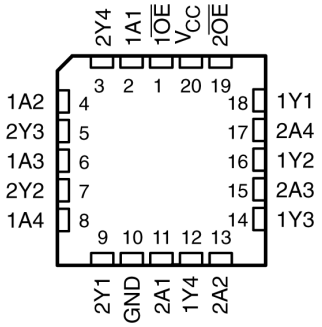


Figure 4-3. SN54AC244 FK Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1A1	2	I	Input
1A2	4	I	Input
1A3	6	I	Input
1A4	8	I	Input
1$\overline{OE}$	1	I	Output enable
1Y1	18	O	Output
1Y2	16	O	Output
1Y3	14	O	Output
1Y4	12	O	Output
2A1	11	I	Input
2A2	13	I	Input
2A3	15	I	Input
2A4	17	I	Input
2 $\overline{OE}$	19	I	Output enable
2Y1	9	O	Output
2Y2	7	O	Output
2Y3	5	O	Output
2Y4	3	O	Output
GND	10	—	Ground
V_{CC}	20	—	Power pin
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output
(2) RKS package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I [1]	Input voltage range		-0.5	V_{CC}+0.5	V
V_O [1]	Output voltage range		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK}	Output clamp current,	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 or V_{CC})		±50	mA
	Continuous current through V_{CC} or GND			±200	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)[1]

			SN54AC244		SN74AC244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		2.1		V
		V_{CC} = 4.5 V	3.15		3.15		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9		0.9	V
		V_{CC} = 4.5 V		1.35		1.35	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		-12		-12	mA
		V_{CC} = 4.5 V		-24		-24	
		V_{CC} = 5.5 V		-24		-24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12		12	mA
		V_{CC} = 4.5 V		24		24	
		V_{CC} = 5.5 V		24		24	
Δt/Δv	Input transition rise or fall rate			8		8	ns/V
T_a	Operating free-air temperature		-55	125	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC[1]		SNx4AC244							UNIT
		DB (SSOP)	DGS (VSSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	RKS (VQFN)	
		20 PINS							
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	123.5	101.2	69	106.2	126.2	67.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54AC244		SN74AC244		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = -50 µA		3 V	2.9			2.9		2.9		V
				4.5 V	4.4			4.4		4.4		
				5.5 V	5.4			5.4		5.4		
		I_{OH} = -12 mA		3 V	2.56			2.4		2.46		
		I_{OH} = -24 mA		4.5 V	3.86			3.7		3.76		
				5.5 V	4.86			4.7		4.76		
		I_{OH} = -50 mA[1]		5.5 V				3.85				
		I_{OH} = -75 mA[1]		5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA		3 V			0.1		0.1		0.1	V
				4.5 V			0.1		0.1		0.1	
				5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA		3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA		4.5 V			0.36		0.5		0.44	
				5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA[1]		5.5 V					1.65			
		I_{OL} = 75 mA[1]		5.5 V							1.65	
I_I	Data inputs	V_I = V_{CC} or GND		5.5 V			±0.1		±1		±1	µA
	Control inputs	V_I = V_{CC} or GND					±0.1		±1		±1	
I_{OZ}		V_O = V_{CC} or GND, V_I(OE) = V_{IL} or V_{IH}		5.5 V			±0.25		±5		±2.5	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	5.5 V			4		80		40	µA
C_i		V_I = V_{CC} or GND		5 V		2.5						pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

5.5 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC244		SN74AC244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	6.5	9	1	12.5	1.5	10	ns
t_{PHL}			2	6.5	9	1	12	2	10	
t_{PZH}	$\overline{OE}$	Y	2	6	10.5	1	11.5	1.5	11	ns
t_{PZL}			2.5	7.5	10	1	13	2	11	
t_{PHZ}	$\overline{OE}$	Y	3	7	10	1	12.5	1.5	10.5	ns
t_{PLZ}			2.5	7.5	10.5	1	13	2.5	11.5	

5.6 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 6-1)

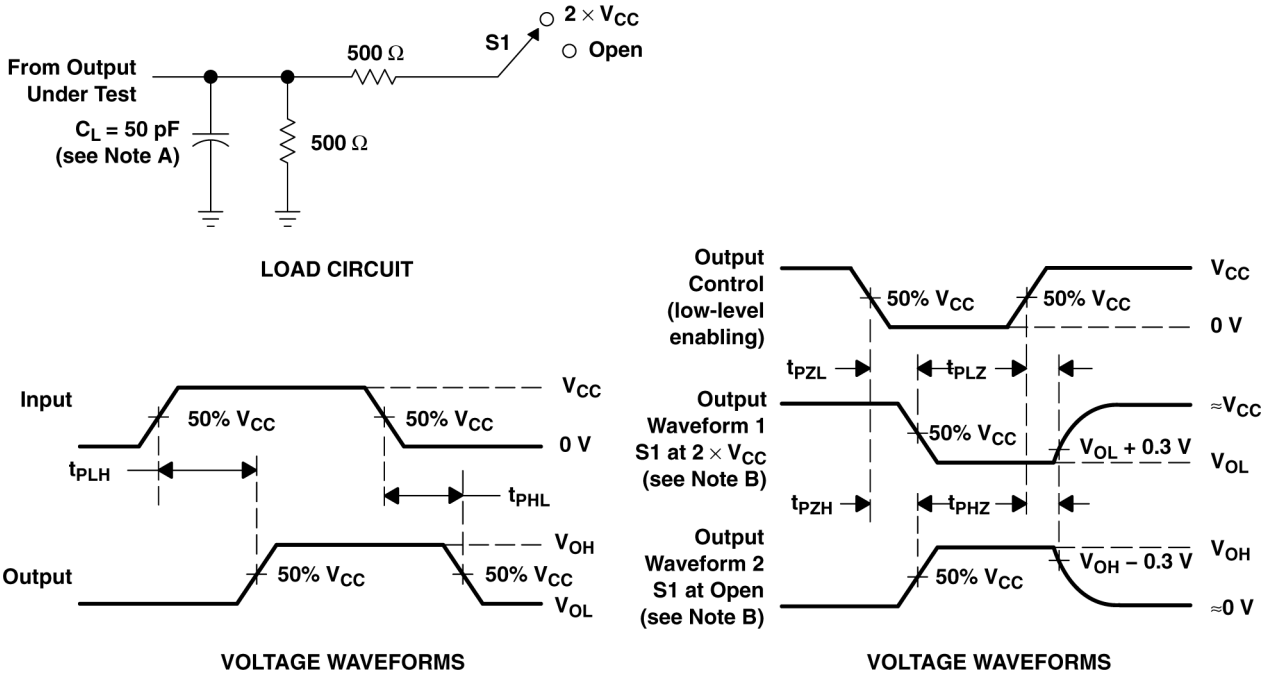
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC244		SN74AC244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	5	7	7	9.5	1	7.5	ns
t_{PHL}			1.5	5	7	7	9	1	7.5	
t_{PZH}	$\overline{OE}$	Y	1.5	5	7	7	9	1.5	8	ns
t_{PZL}			1.5	5.5	8	8	10.5	1.5	8.5	
t_{PHZ}	$\overline{OE}$	Y	2.5	6.5	9	9	10.5	1	9.5	ns
t_{PLZ}			2	6.5	9	9	11	2	9.5	

5.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	C_l = 50 pF, f = 1 MHz	45	pF

6 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open

7 Detailed Description

7.1 Overview

The 'AC244 devices are organized as two 4-bit buffers or drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes non-inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

For the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

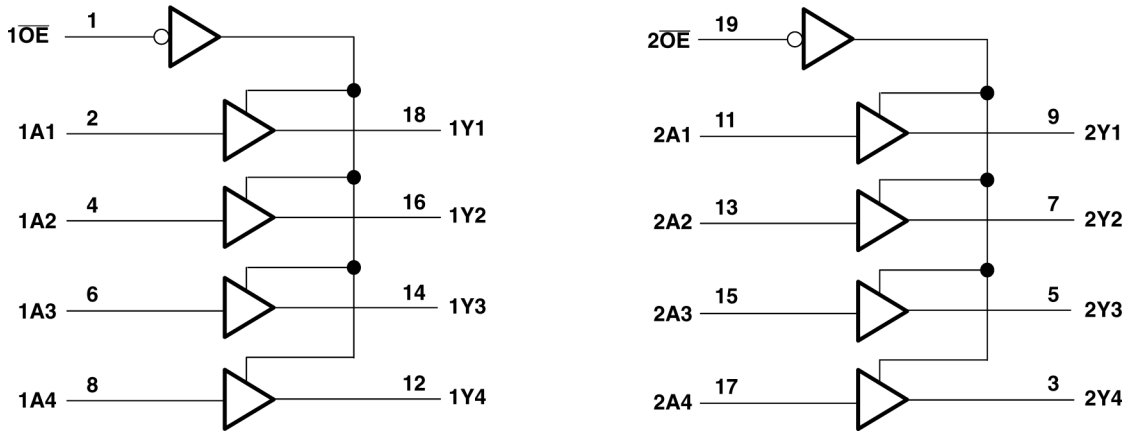


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

Table 7-1. Function Table (Each Buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

8.2 Layout

8.2.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace, which results in the reflection. Not all PCB traces can be straight; therefore, some traces must turn corners. Layout example for SNx4AC244 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.2.1.1 Layout Example

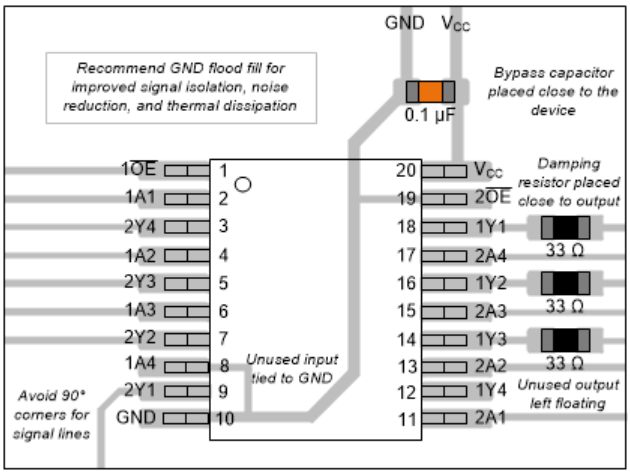


Figure 8-1. Layout Example for the SNx4AC244 in the PW Package

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (August 2023) to Revision H (March 2024)	Page
• Added DGS package to *Device Information* table, *Pin Configuration and Functions* section and *Thermal Information* table; Updated J and W package sizes in *Device Information* table	1
• Updated RθJA values: DW = 58 to 101.2, NS = 60 to 106.2, PW = 83 to 126.2, all values in °C/W	5
• Added *Application and Implementation* section	9

Changes from Revision F (May 2023) to Revision G (August 2023)	Page
• Updated the *Device Information* table to include package lead size	1
• Added *RKS* package information	1
• Updated high-level input voltage values in *Recommended Operating Conditions* table	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87552012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87552012A SNJ54AC 244FK	Samples
5962-8755201RA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201RA SNJ54AC244J	Samples
5962-8755201SA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201SA SNJ54AC244W	Samples
5962-8755201VRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201VRA SNV54AC244J	Samples
5962-8755201VSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201VSA SNV54AC244W	Samples
SN74AC244DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC244	Samples
SN74AC244DGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		AC244	Samples
SN74AC244DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	AC244	
SN74AC244DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC244	Samples
SN74AC244N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC244N	Samples
SN74AC244NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC244N	Samples
SN74AC244NSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC244	Samples
SN74AC244PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	AC244	
SN74AC244PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC244	Samples
SN74AC244RKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC244	Samples
SNJ54AC244FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87552012A SNJ54AC 244FK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AC244J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201RA SNJ54AC244J	Samples
SNJ54AC244W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201SA SNJ54AC244W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54AC244, SN54AC244-SP, SN74AC244 :

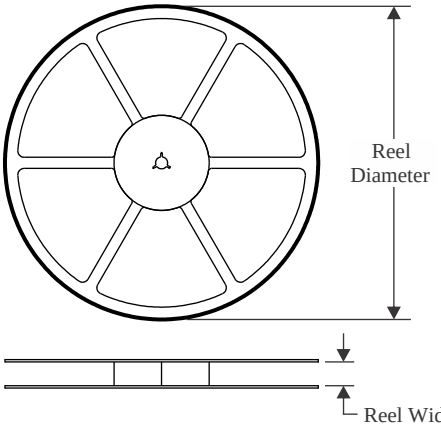
- Catalog : SN74AC244, SN54AC244
- Automotive : SN74AC244-Q1, SN74AC244-Q1
- Enhanced Product : SN74AC244-EP, SN74AC244-EP
- Military : SN54AC244
- Space : SN54AC244-SP

NOTE: Qualified Version Definitions:

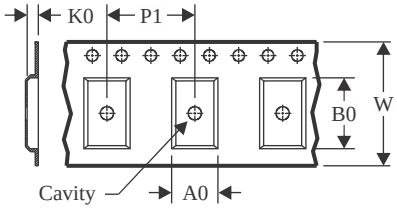
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

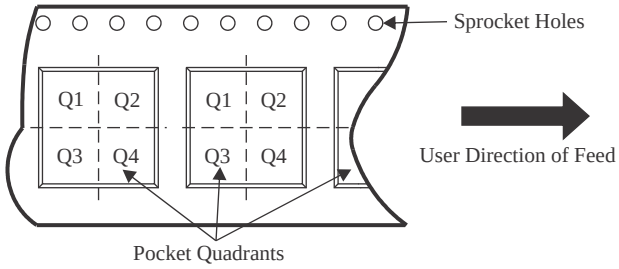


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

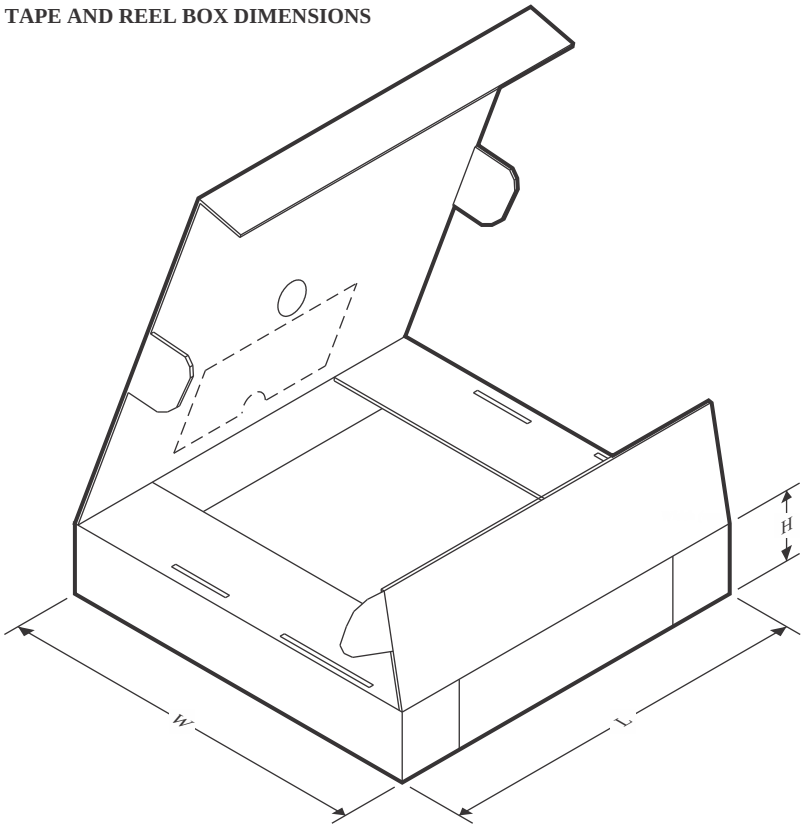
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC244DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AC244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC244DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AC244NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AC244NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AC244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AC244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AC244RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

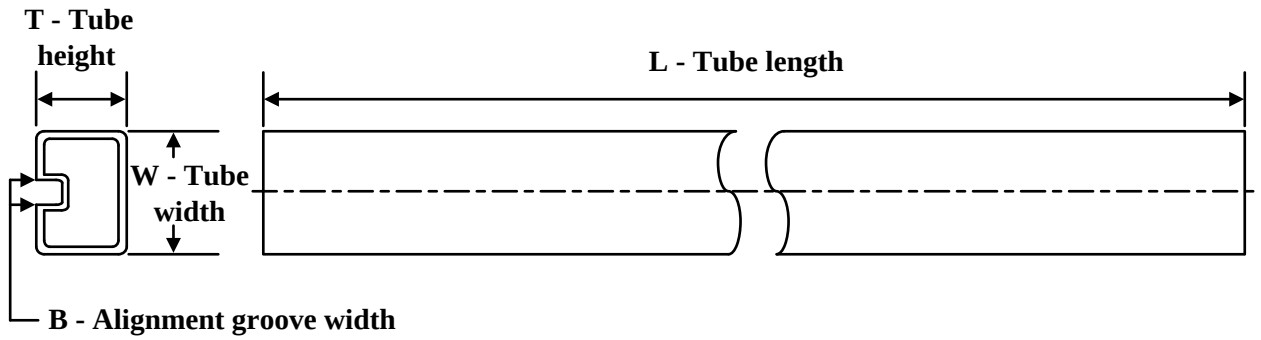
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AC244DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AC244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AC244DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC244NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74AC244NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AC244PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AC244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AC244RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

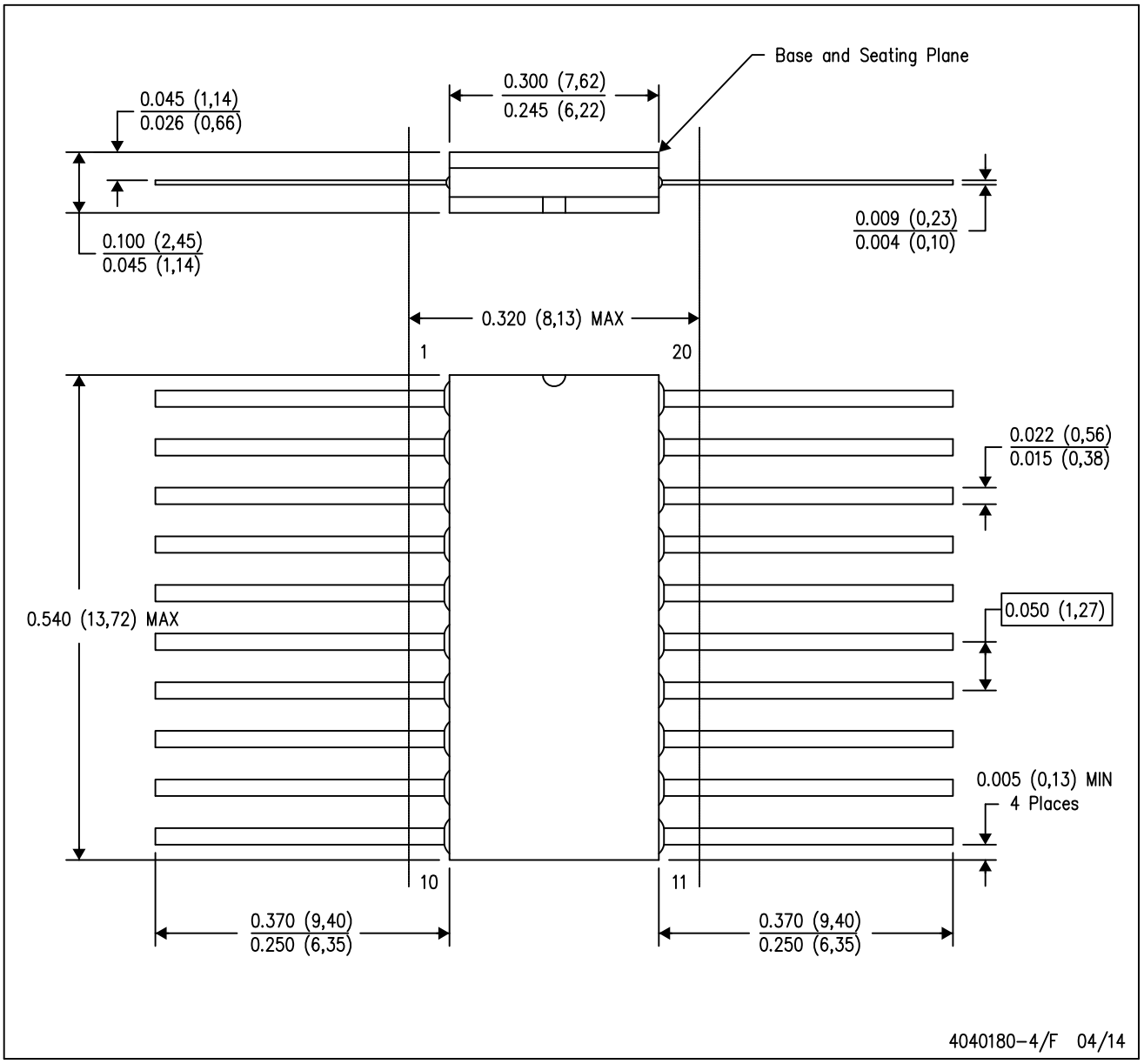
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87552012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8755201SA	W	CFP	20	25	506.98	26.16	6220	NA
5962-8755201VSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AC244N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AC244NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AC244FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC244W	W	CFP	20	25	506.98	26.16	6220	NA

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



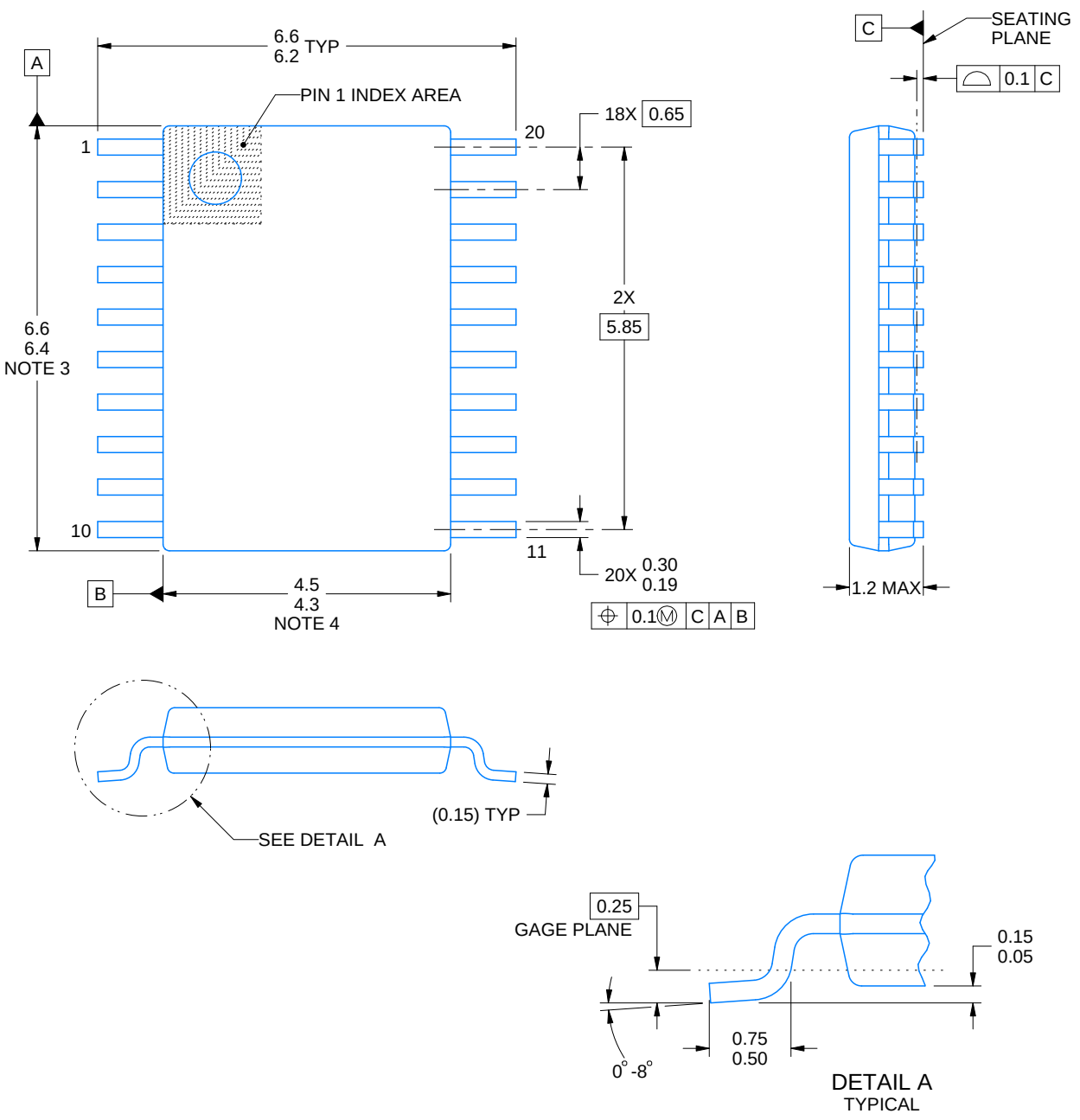
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

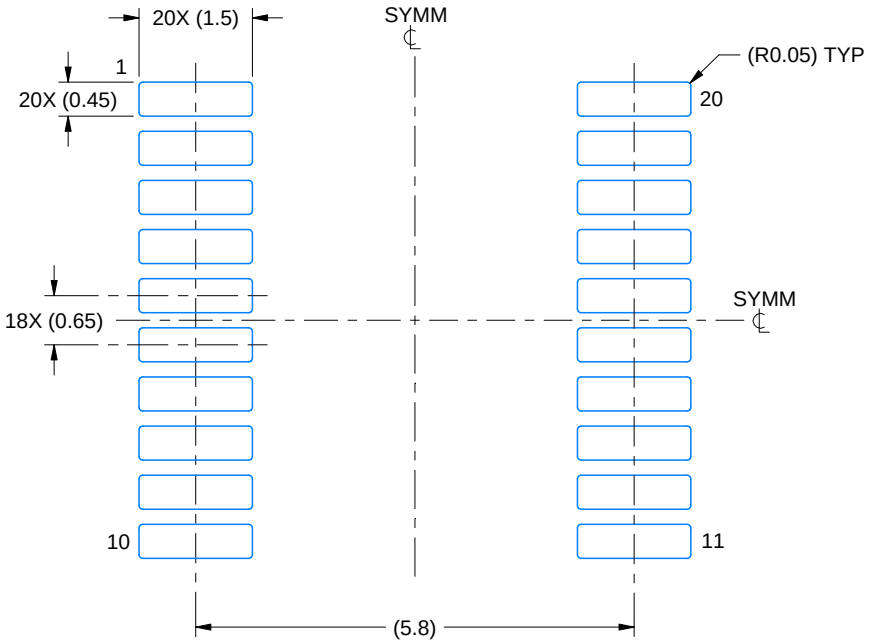
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



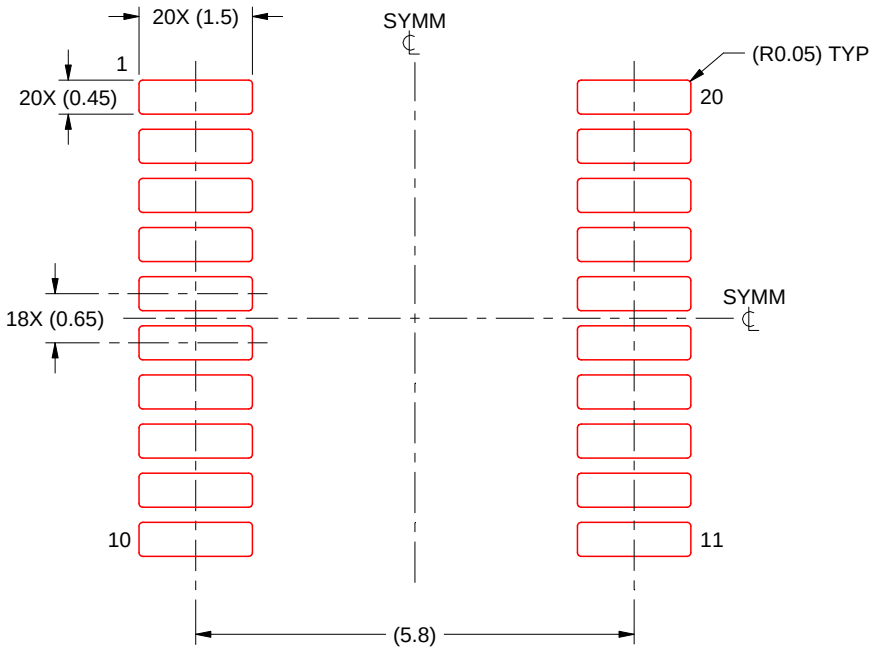
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

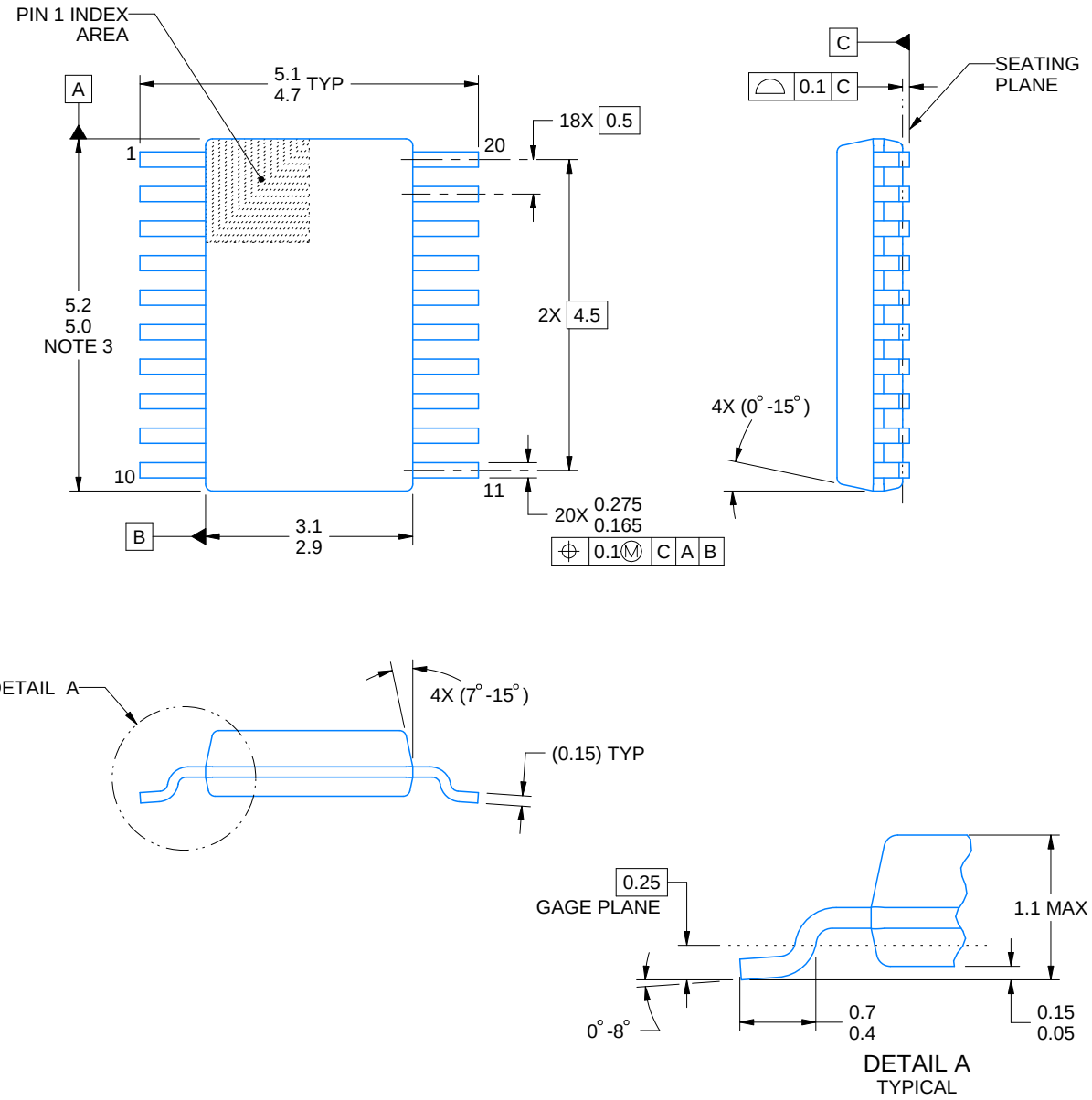
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

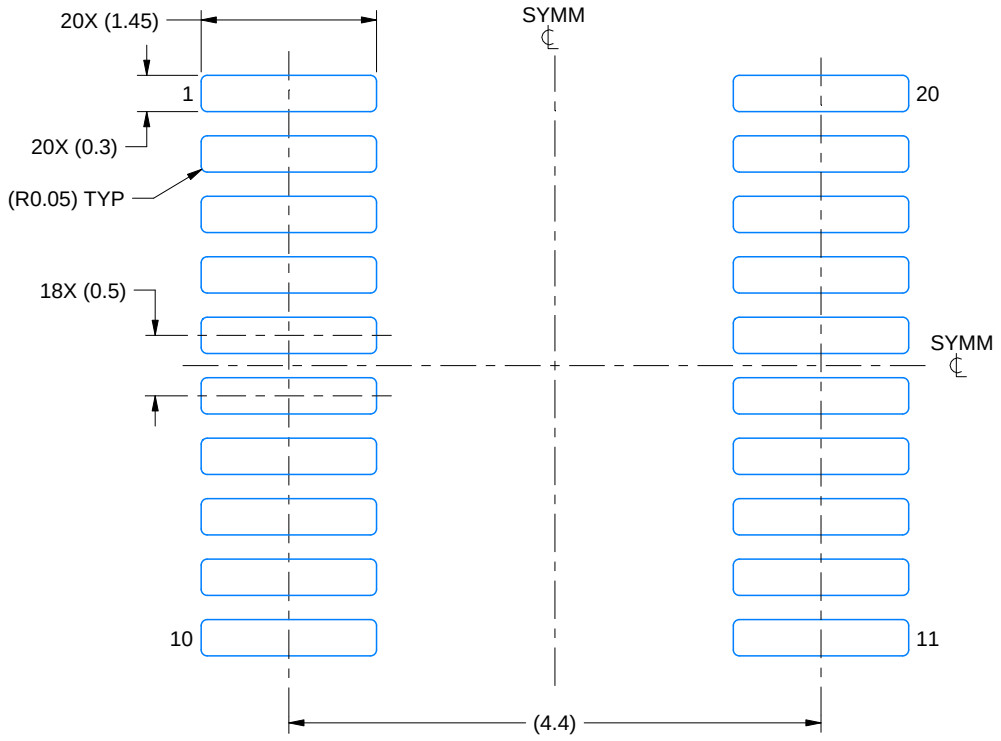
SMALL OUTLINE PACKAGE



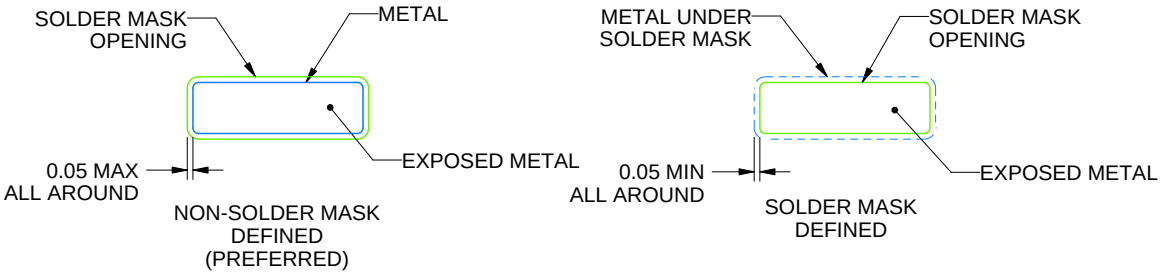
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

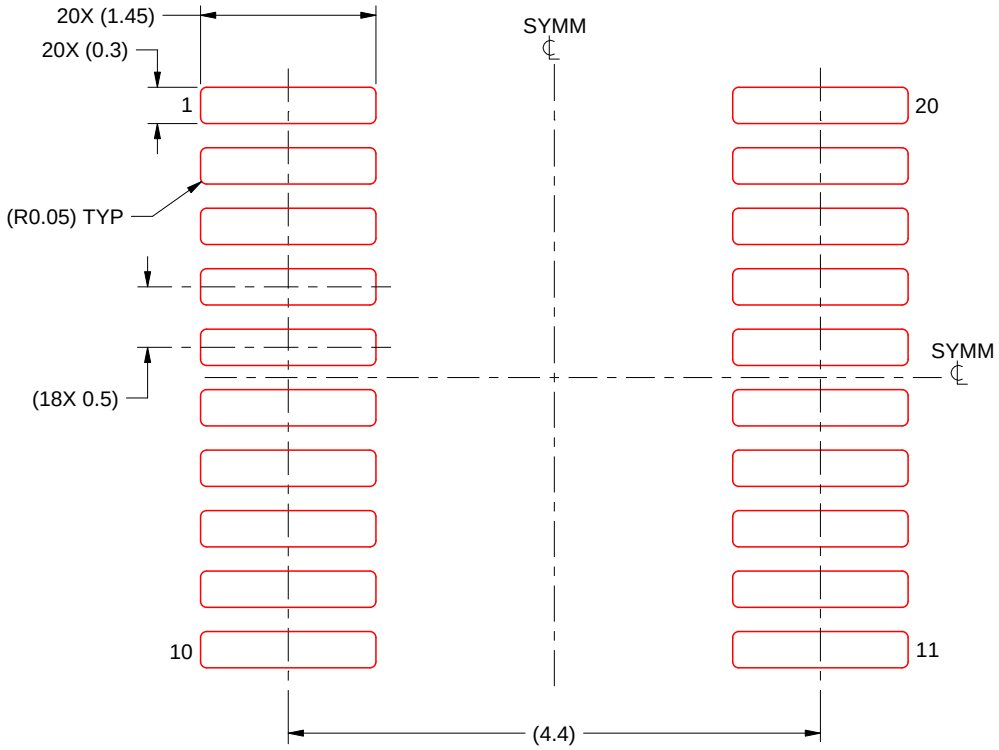


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

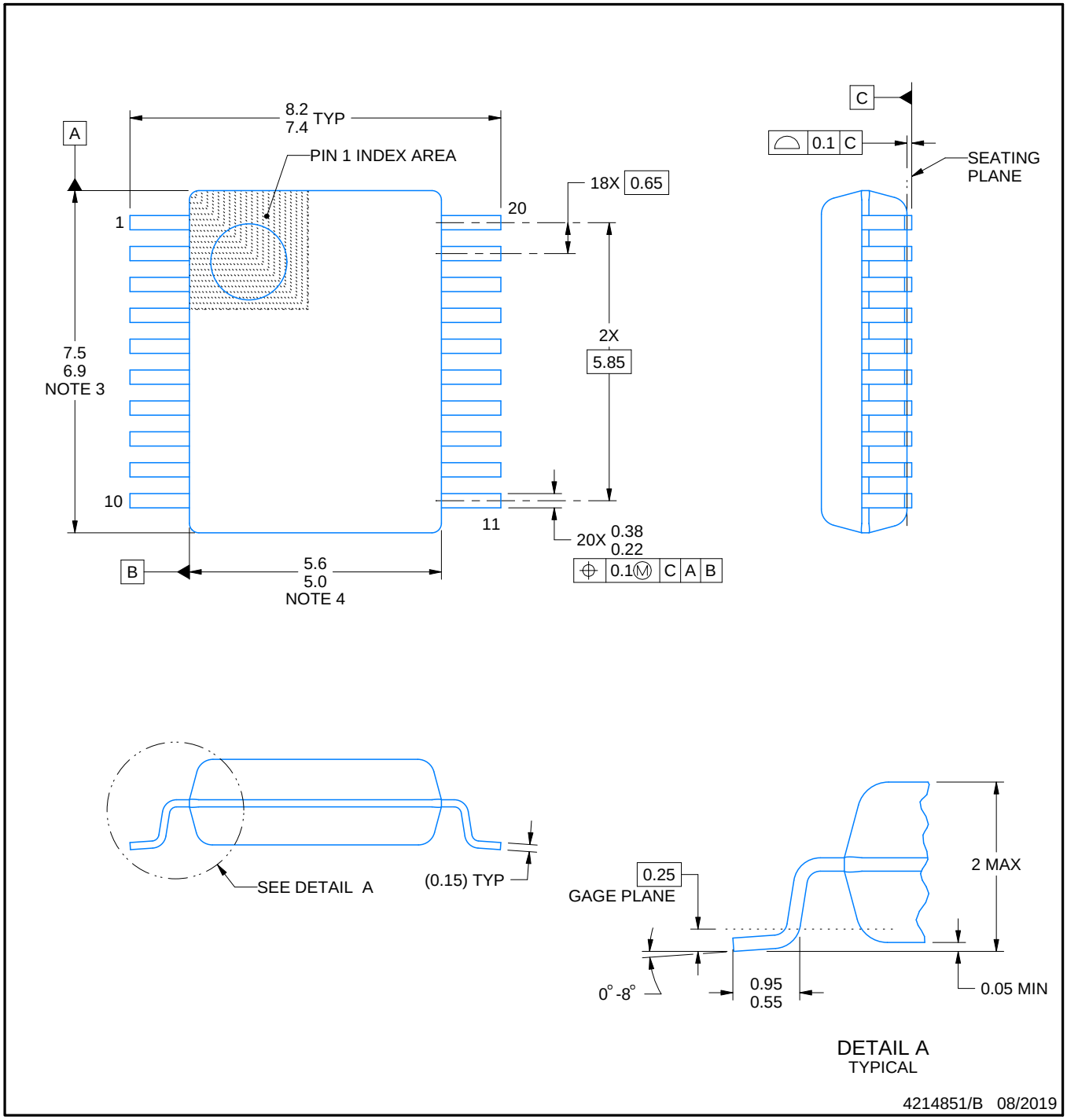
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0020A

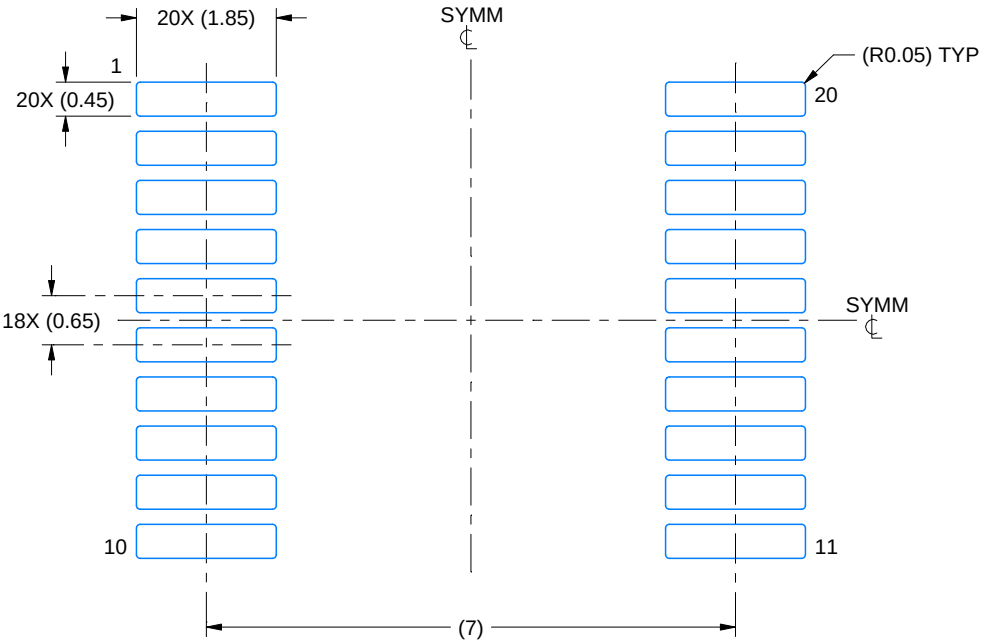
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

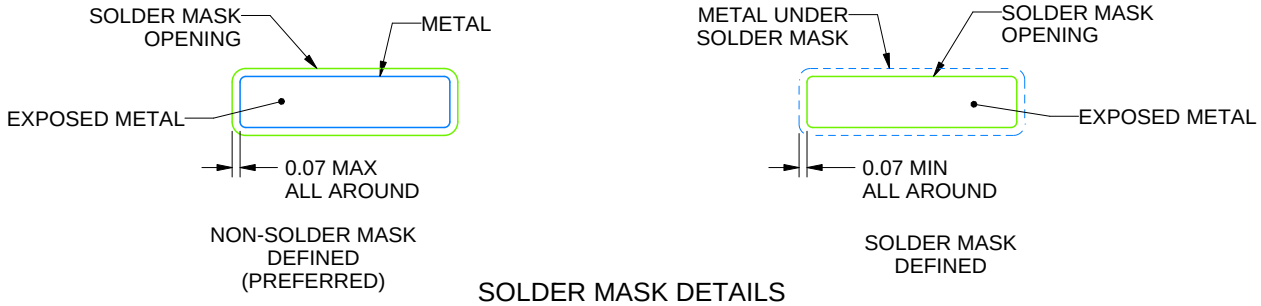


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

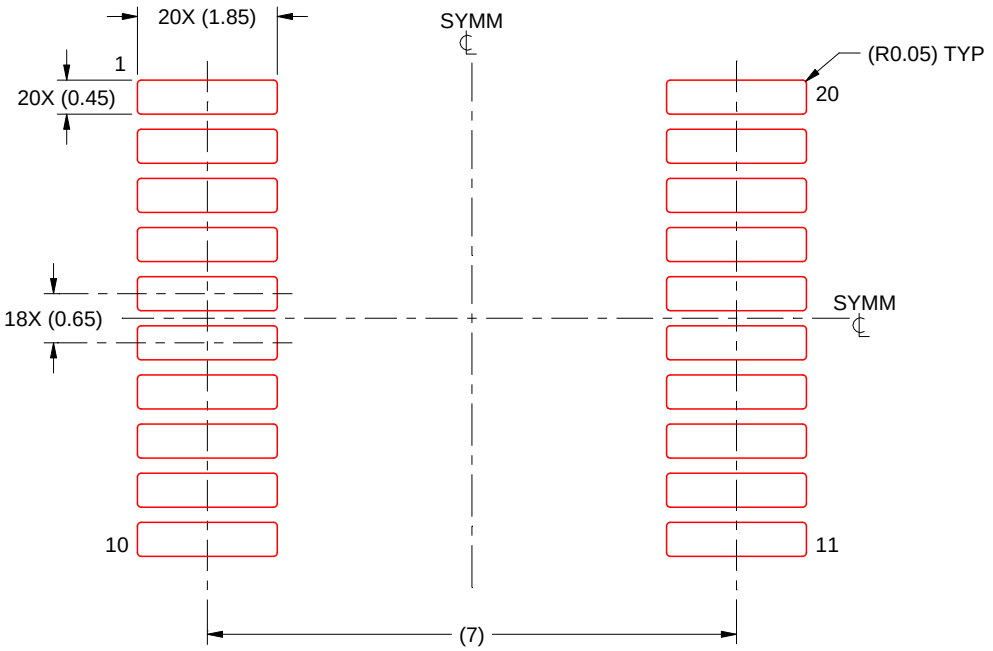
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

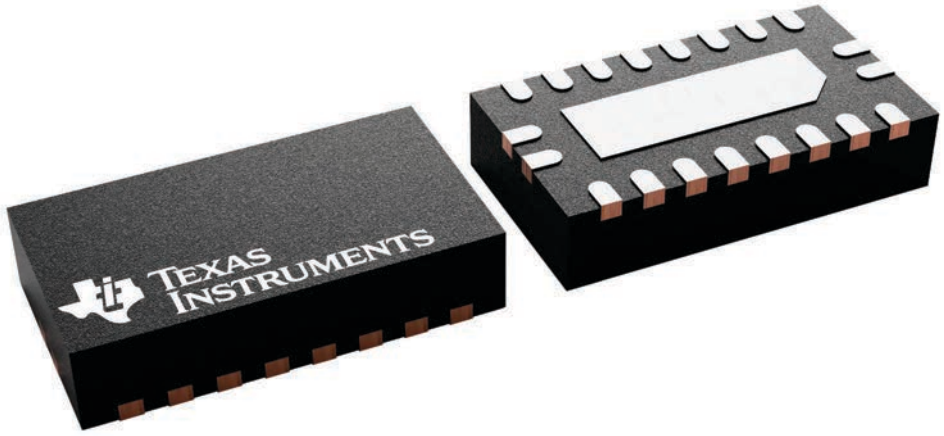
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

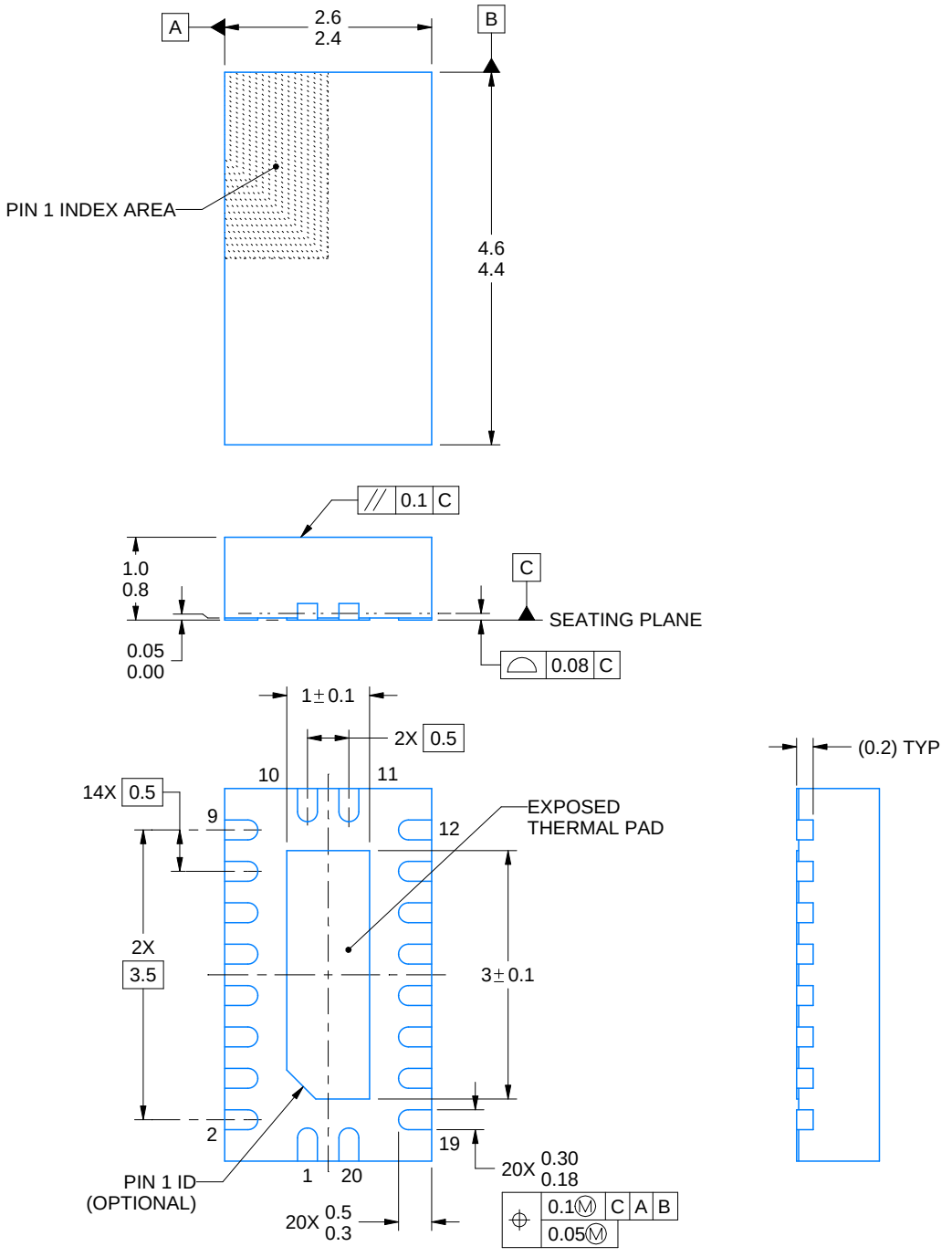


PACKAGE OUTLINE

RKS0020A

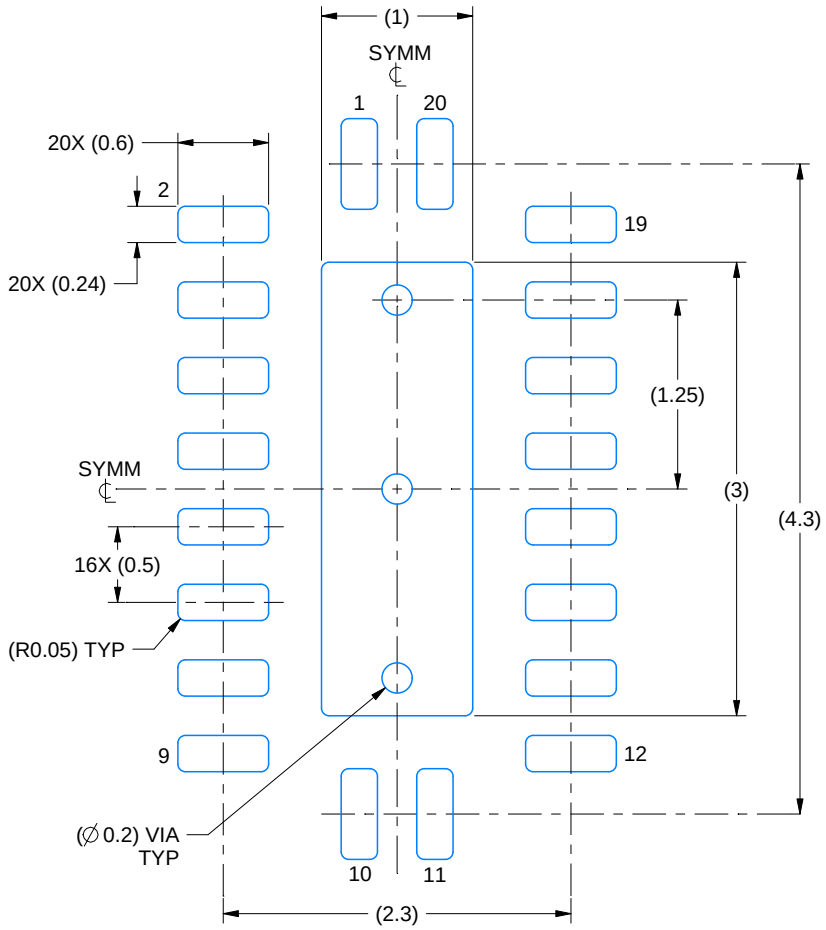
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

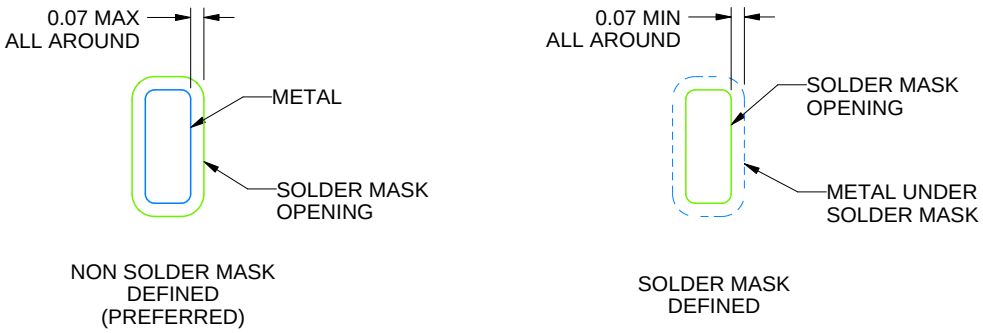


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

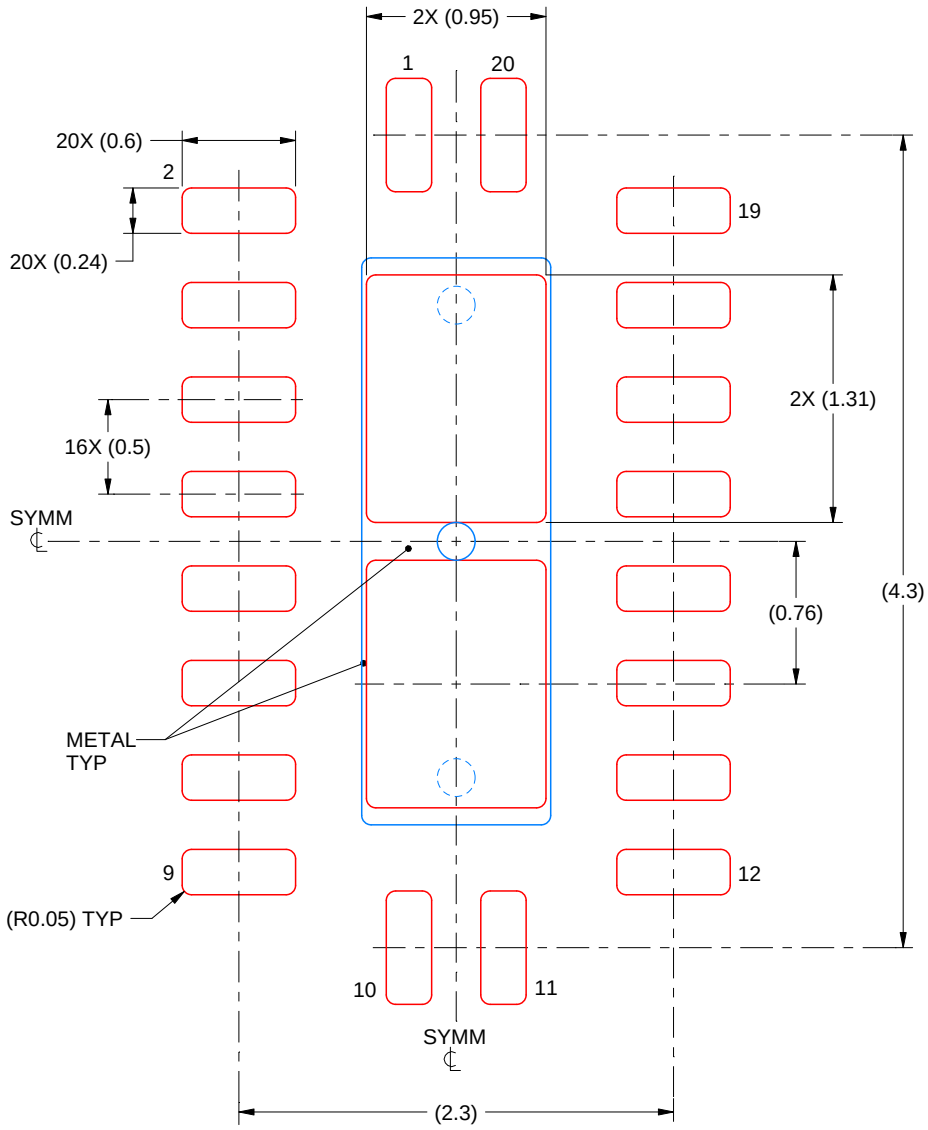


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

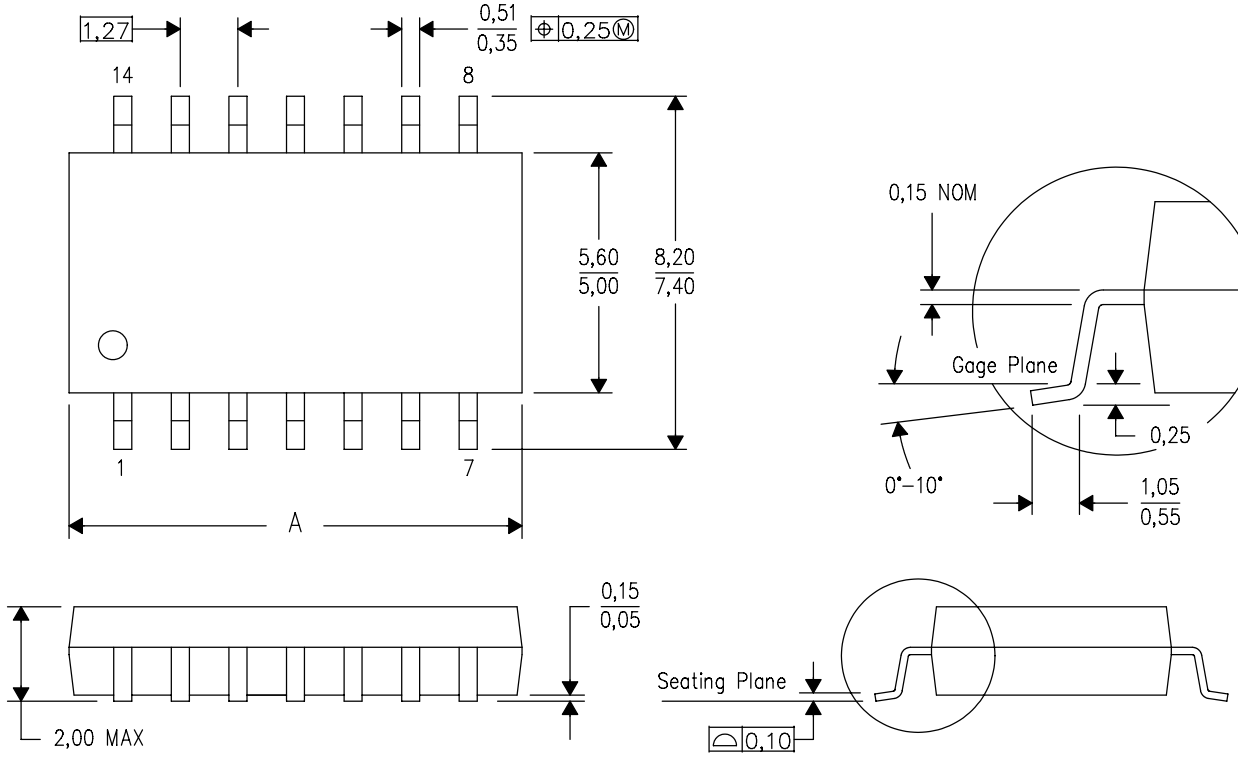
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

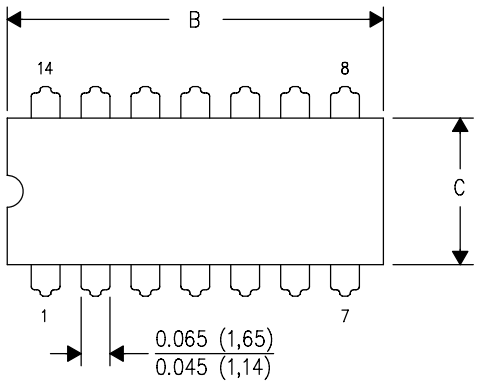
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

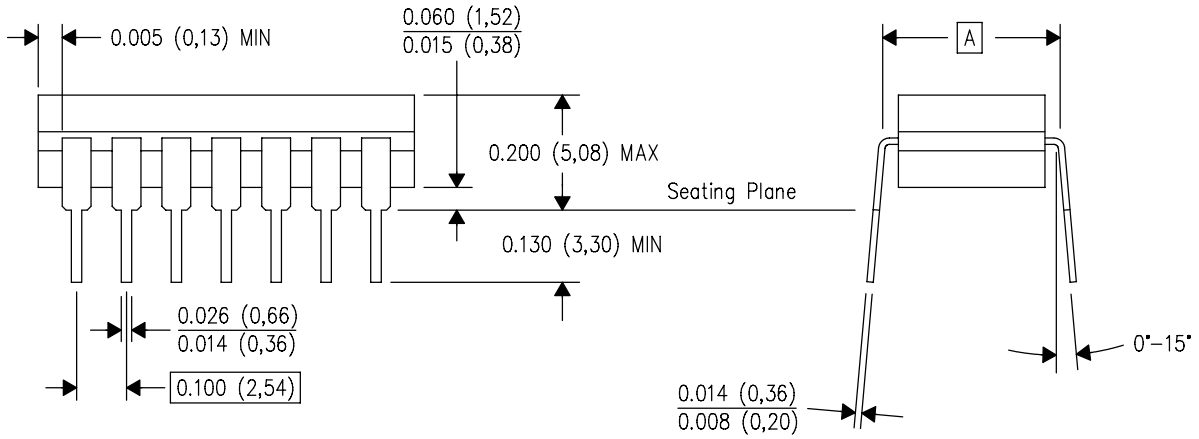
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

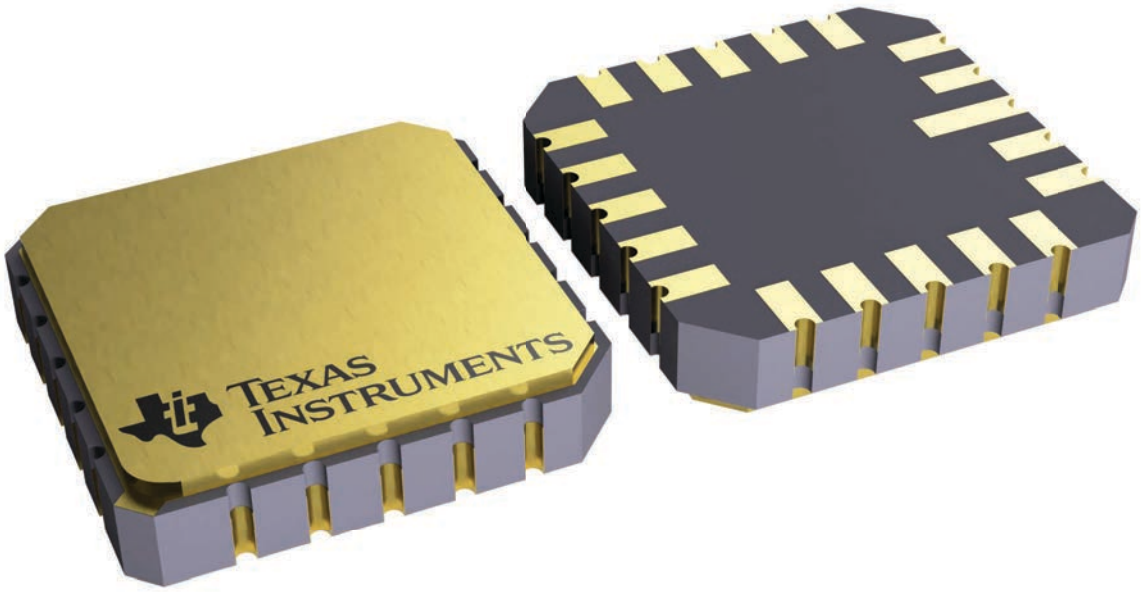
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

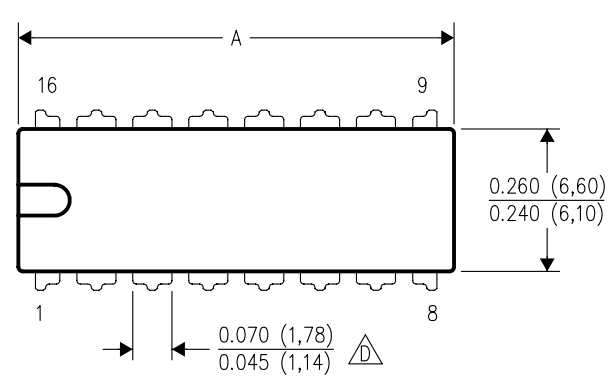


4229370VA\

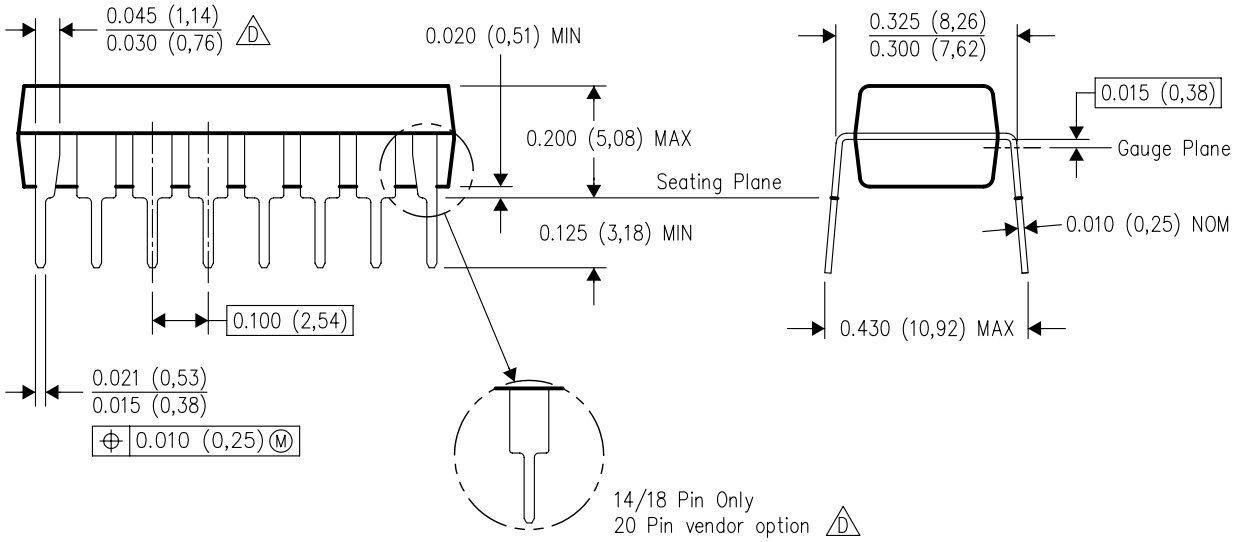
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

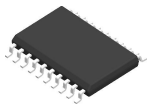


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

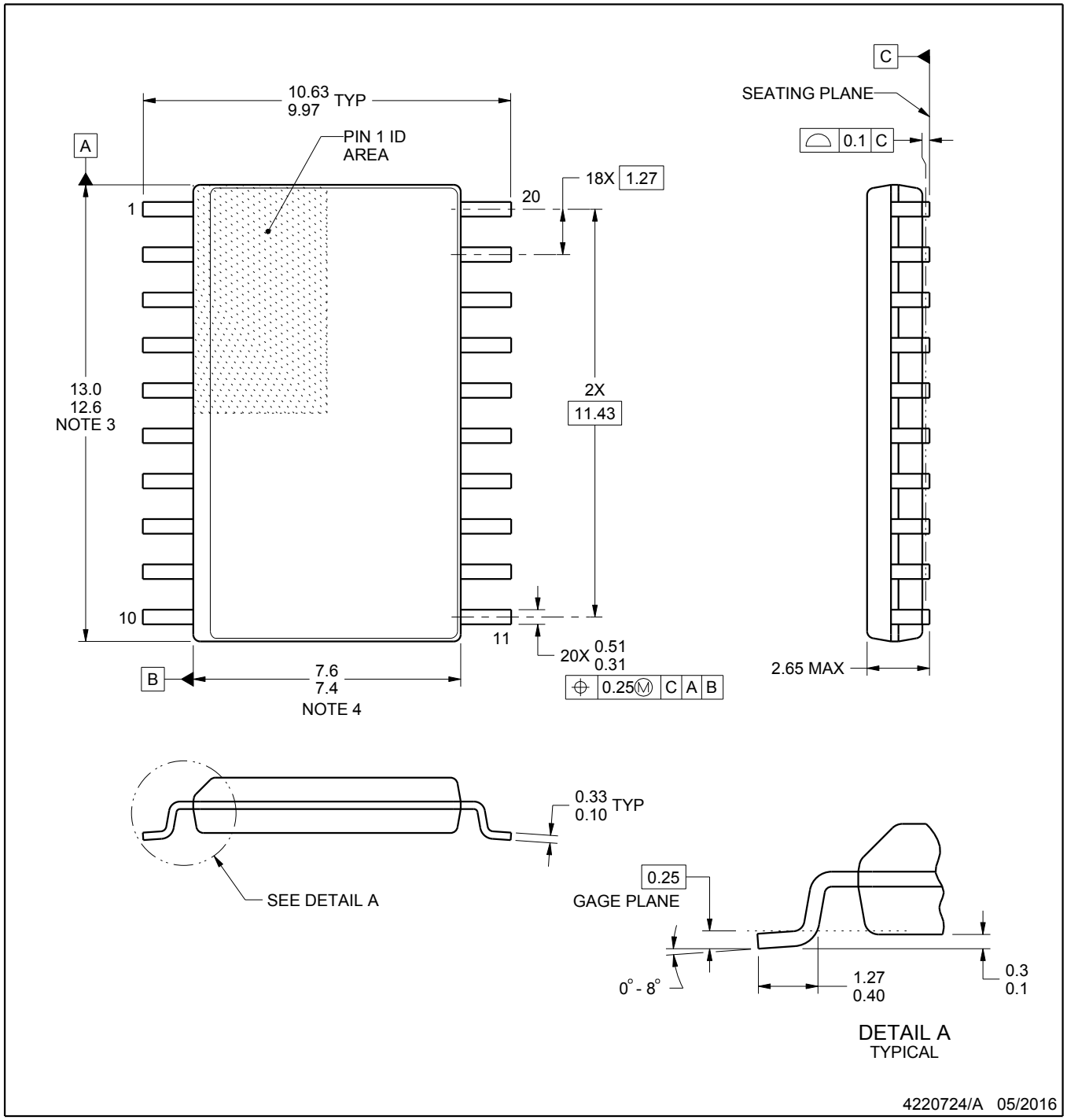


PACKAGE OUTLINE

DW0020A

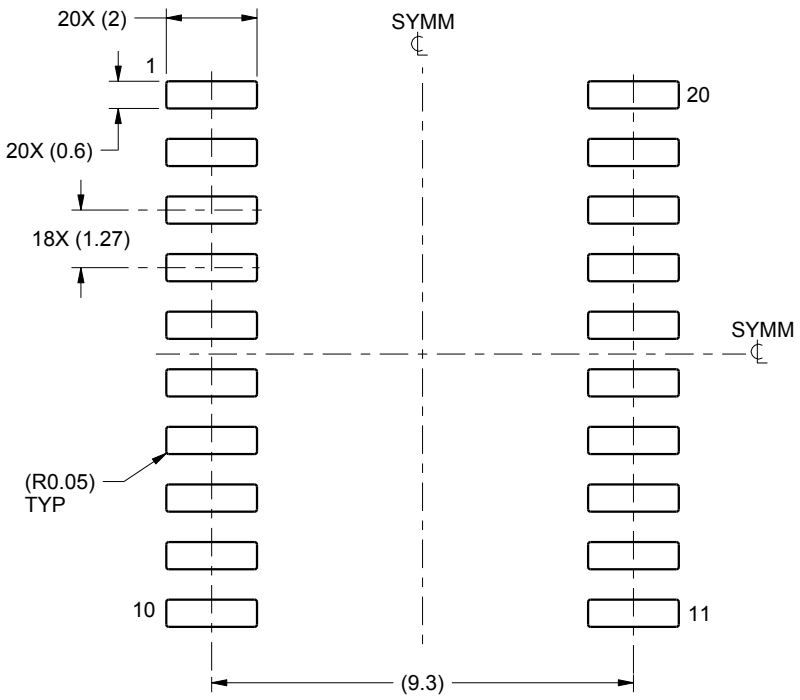
SOIC - 2.65 mm max height

SOIC

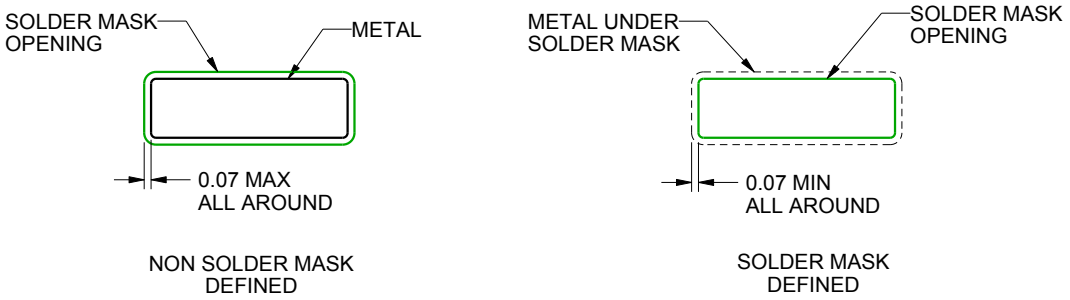


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

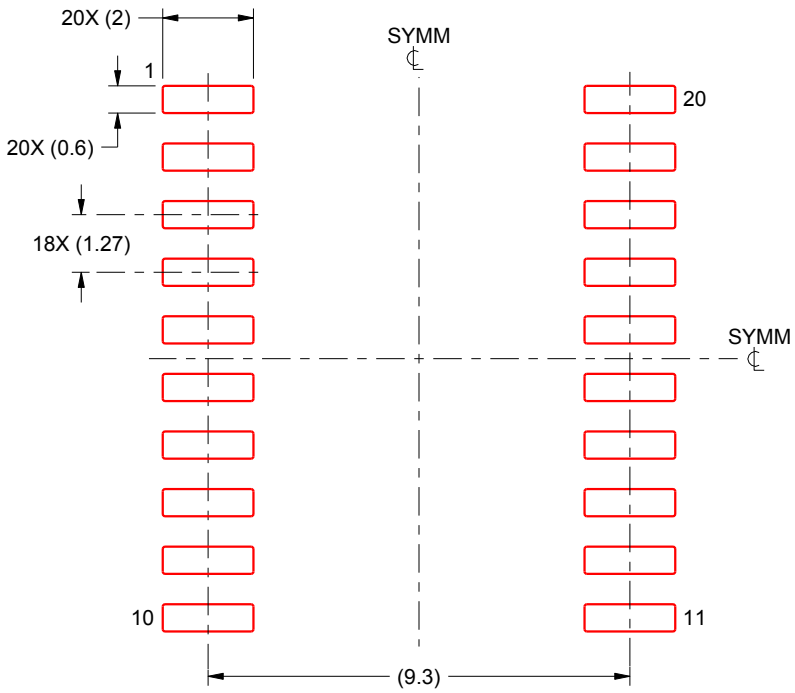


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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