

# SN54ALS574B, SN54AS574, SN54AS575 SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS165B – JUNE 1982 – REVISED JULY 1995

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- SN74ALS575A and 'AS575 Have Synchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N, NT) and Ceramic (J, JT) 300-mil DIPs, and Ceramic Flat (W) Packages

## description

These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN74ALS575A, SN54AS575, and SN74AS575 may be synchronously cleared by taking the clear ( $\overline{\text{CLR}}$ ) input low.

The output-enable ( $\overline{\text{OE}}$ ) input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS574B, SN54AS574, and SN54AS575 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS574B, SN74ALS575A, SN74AS574, and SN74AS575 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS574B, SN54AS574 . . . J OR W PACKAGE  
SN74ALS574B, SN74AS574 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS574B, SN54AS574 . . . FK PACKAGE  
(TOP VIEW)



SN54AS575 . . . JT OR W PACKAGE  
SN74ALS575A, SN74AS575 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54AS575 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

**SN54ALS574B, SN54AS574, SN54AS575**  
**SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

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**Function Tables**

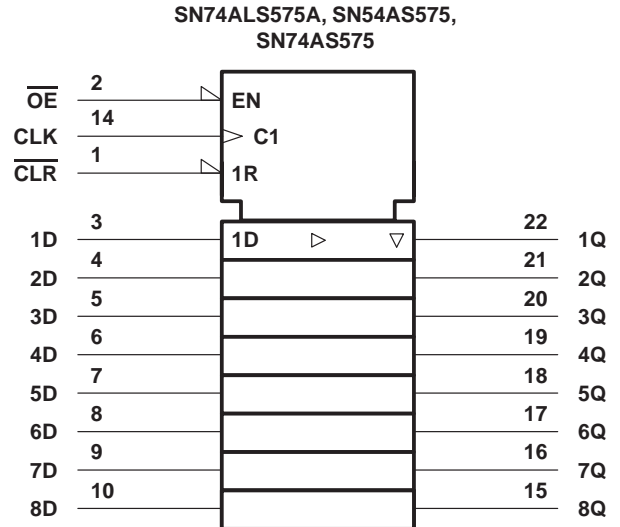
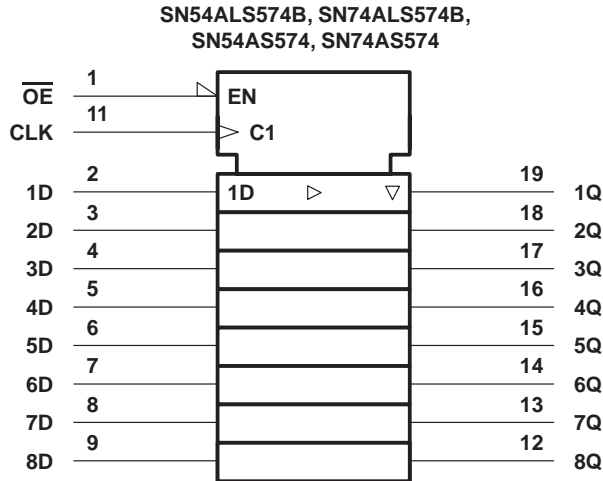
**SN54ALS574B, SN74ALS574B, SN54AS574, SN74AS574**  
 (each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

**SN74ALS575A, SN54AS575, SN74AS575**  
 (each flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	CLR	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	$Q_0$
H	X	H	X	Z

**logic symbol†**

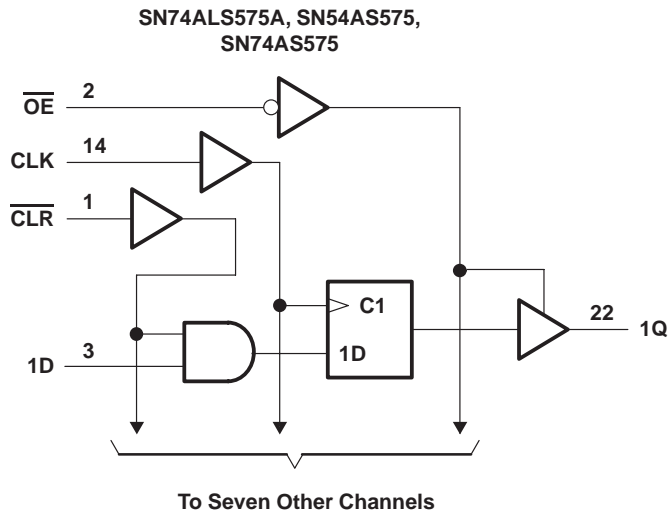


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, J, JT, N, and NT packages.

**SN54ALS574B, SN54AS574, SN54AS575**  
**SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

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**logic diagrams (positive logic)**



Pin numbers shown are for the DW, J, JT, N, and NT packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS574B	-55°C to 125°C
SN74ALS574B, SN74ALS575A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54ALS574B			SN74ALS574B SN74ALS575A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-1			-2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$f_{clock}$	Clock frequency	'ALS574B	0	28	0		35	MHz
		SN74ALS575A			0		30	
$t_w$	Pulse duration	'ALS574B, CLK high or low	16.5		14			ns
		SN74ALS575A, CLK high or low			16.5			
$t_{su}$	Setup time before CLK↑	Data	15		15			ns
		SN74ALS575A, $\overline{CLR}$			15			
$t_h$	Hold time after CLK↑	Data	4		0			ns
		SN74ALS575A, $\overline{CLR}$			0			
$T_A$	Operating free-air temperature	-55		125	0		70	°C



**SN54ALS574B, SN54AS574, SN54AS575**  
**SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54ALS574B			SN74ALS574B SN74ALS575A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.2			-1.2			V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.4	3.3					
		$I_{OH} = -2.6\text{ mA}$				2.4	3.2		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$		$I_{OL} = 12\text{ mA}$		0.25	0.4	0.25 0.4		V
			$I_{OL} = 24\text{ mA}$					0.35 0.5	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$		20			20			$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.4\text{ V}$		-20			-20			$\mu\text{A}$
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$		0.1			0.1			mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$		20			20			$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$		-0.2			-0.2			mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$		-20		-112	-30		-112	mA
$I_{CC}$	'ALS574B	$V_{CC} = 5.5\text{ V}$	Outputs high		11	18	11 18		mA
			Outputs low		17	27	17 27		
			Outputs disabled		17	28	17 28		
	SN74ALS575A	$V_{CC} = 5.5\text{ V}$	Outputs high		10	17	10 17		
			Outputs low		15	24	15 24		
			Outputs disabled		16	30	16 30		

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$						UNIT
			SN54ALS574B		SN74ALS574B		SN74ALS575A		
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			28		35		30		MHz
$t_{\text{PLH}}$	CLK	Q	4	22	3	14	4	14	ns
$t_{\text{PHL}}$			4	17	4	14	4	14	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	4	21	3	18	4	18	ns
$t_{\text{PZL}}$			4	26	4	18	4	18	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	2	16	1	10	2	10	ns
$t_{\text{PLZ}}$			2	25	2	12	3	13	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS574B, SN54AS574, SN54AS575**  
**SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ .....	7 V
Voltage applied to a disabled 3-state output .....	5.5 V
Operating free-air temperature range, $T_A$ : SN54AS574, SN54AS575 .....	–55°C to 125°C
SN74AS574, SN74AS575 .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			32			48	mA
$f_{clock}^*$	Clock frequency	0		100	0		90	MHz
$t_w^*$	Pulse duration	CLK high		5	5.5		ns	
		CLK low		4	5.5			
$t_{su}^*$	Setup time before CLK↑	Data		3	5.5		ns	
		'AS575, $\overline{CLR}$ high or low		6.5	6.5			
$t_h^*$	Hold time after CLK↑	Data		3	3		ns	
		'AS575, $\overline{CLR}$		0	0			
$T_A$	Operating free-air temperature	–55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



**SN54ALS574B, SN54AS574, SN54AS575**  
**SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54AS574 SN54AS575		SN74AS574 SN74AS575		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V	
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$		$V_{CC} - 2$		$V_{CC} - 2$		V	
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -12\text{ mA}$	2.4	3.2				
		$I_{OH} = -15\text{ mA}$			2.4	3.3		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 32\text{ mA}$	0.29	0.5			V	
		$I_{OL} = 48\text{ mA}$			0.34	0.5		
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$	50		50		$\mu\text{A}$		
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.4\text{ V}$	-50		-50		$\mu\text{A}$		
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$	0.1		0.1		mA		
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$	20		20		$\mu\text{A}$		
$I_{IL}$	$\overline{OE}$ , CLK, $\overline{CLR}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$	-0.5		-0.5		mA	
	D		-3		-2			
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-30	-112	-30	-112	mA		
$I_{CC}$	'AS574	$V_{CC} = 5.5\text{ V}$	Outputs high	73	116	73	116	mA
			Outputs low	85	134	85	134	
			Outputs disabled	84	134	84	134	
	'AS575	$V_{CC} = 5.5\text{ V}$	Outputs high	78	126	78	126	
			Outputs low	89	142	89	142	
			Outputs disabled	88	142	88	142	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$				UNIT
			SN54AS574 SN54AS575		SN74AS574 SN74AS575		
			MIN	MAX	MIN	MAX	
$f_{\text{max}}^*$			100		90	MHz	
$t_{PLH}$	CLK	Any Q	3	11	3	8	ns
$t_{PHL}$			4	11	4	9	
$t_{PZH}$	$\overline{OE}$	Any Q	2	7	2	6	ns
$t_{PZL}$			3	11	3	10	
$t_{PHZ}$	$\overline{OE}$	Any Q	2	7	2	6	ns
$t_{PLZ}$			2	7	2	6	

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

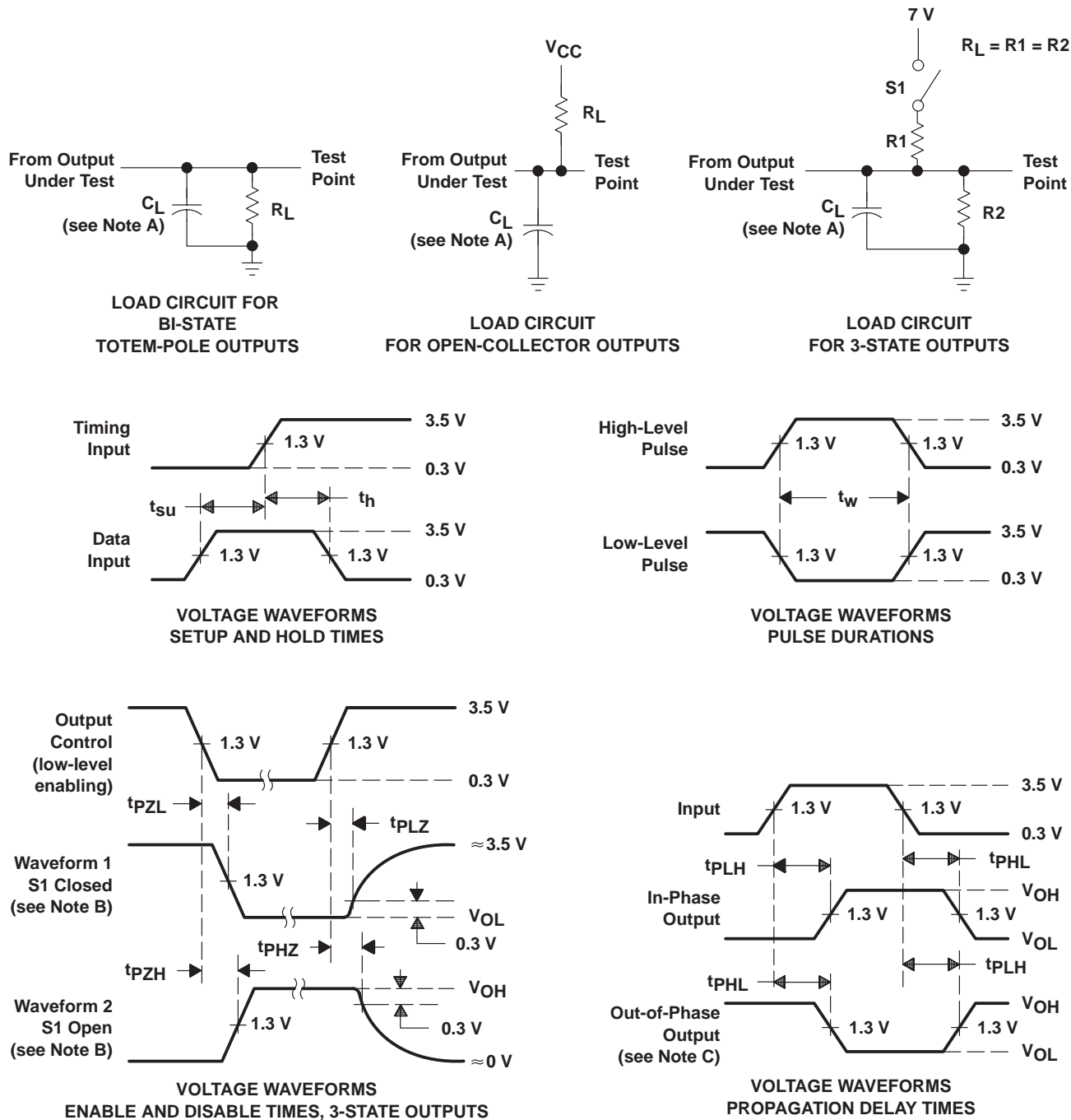
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS574B, SN54AS574, SN54AS575  
 SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575  
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**PARAMETER MEASUREMENT INFORMATION  
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84001012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84001012A SNJ54ALS 574BFK	<a href="#">Samples</a>
8400101RA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8400101RA SNJ54ALS574BJ	<a href="#">Samples</a>
8400101SA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8400101SA SNJ54ALS574BW	<a href="#">Samples</a>
JM38510/37104B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37104B2A	<a href="#">Samples</a>
JM38510/37104BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37104BRA	<a href="#">Samples</a>
M38510/37104B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37104B2A	<a href="#">Samples</a>
M38510/37104BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37104BRA	<a href="#">Samples</a>
SN54ALS574BJ	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54ALS574BJ	<a href="#">Samples</a>
SN54AS574J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54AS574J	<a href="#">Samples</a>
SN74ALS574BDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS574B	<a href="#">Samples</a>
SN74ALS574BN	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS574BN	<a href="#">Samples</a>
SN74ALS574BNE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS574BN	<a href="#">Samples</a>
SN74ALS574BNSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS574B	<a href="#">Samples</a>
SN74ALS575ADW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS575A	<a href="#">Samples</a>
SN74AS574DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS574	<a href="#">Samples</a>
SN74AS574N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS574N	<a href="#">Samples</a>
SNJ54ALS574BFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84001012A SNJ54ALS 574BFK	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54ALS574BJ	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8400101RA SNJ54ALS574BJ	<a href="#">Samples</a>
SNJ54ALS574BW	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8400101SA SNJ54ALS574BW	<a href="#">Samples</a>
SNJ54AS574J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54AS574J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ALS574B, SN54AS574, SN74ALS574B, SN74AS574 :**

- Catalog : [SN74ALS574B](#), [SN74AS574](#)
- Military : [SN54ALS574B](#), [SN54AS574](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS574BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS574BNSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AS574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS574BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS574BNSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AS574DWR	SOIC	DW	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84001012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8400101SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/37104B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/37104B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS574BN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS574BNE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS575ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74AS574N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS574BFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS574BW	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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