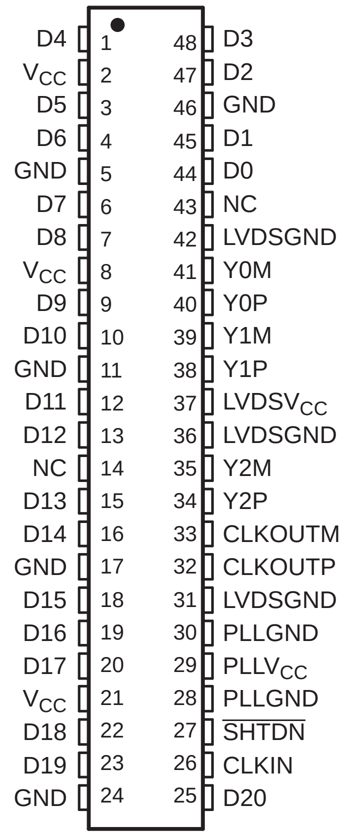
FlatLink™ TRANSMITTER

FEATURES

- **21:3 Data Channel Compression at up to 196 Mbytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Data Transmission From Controller to Display With Very Low EMI**
- **21 Data Channels Plus Clock In Low-Voltage TTL Inputs and 3 Data Channels Plus Clock Out Low-Voltage Differential Signaling (LVDS) Outputs**
- **Operates From a Single 3.3-V Supply and 89 mW (Typ)**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 0.54 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range: 31 MHz to 75 MHz**
- **No External Components Required for PLL**
- **Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **SSC Tracking Capability of 3% Center Spread at 50-kHz Modulation Frequency**
- **Improved Replacement for SN75LVDS84 and NSC DS90CF363A 3-V Device**
- **Qualified for Automotive Applications**

DGG PACKAGE
(TOP VIEW)



NC − Not Connected

DESCRIPTION/ORDERING INFORMATION

The SN65LVDS84AQ FlatLink™ transmitter contains three 7-bit parallel-load serial-out shift registers, and four low-voltage differential signaling (LVDS) line drivers in a single integrated circuit. These functions allow 21 bits of single-ended LVTTL data to be synchronously transmitted over 3 balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82 or SN75LVDS86/86A.

When transmitting, data bits D0–D20 are each loaded into registers of the SN65LVDS84AQ upon the falling edge. The internal PLL is frequency-locked to CLKIN and then used to unload the data registers in 7-bit slices. The three serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN65LVDS84AQ requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear ($\overline{SHTDN}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low level.

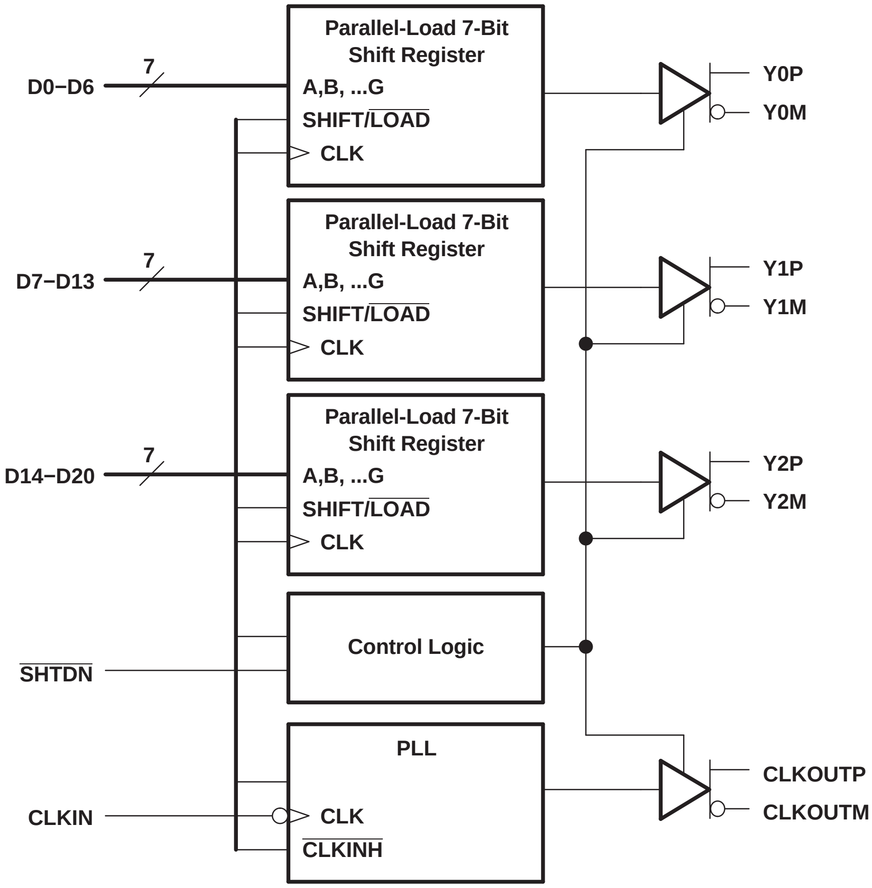
The SN65LVDS84AQ is characterized for operation over the full automotive temperature range of –40°C to 125°C.

ORDERING INFORMATION(1)

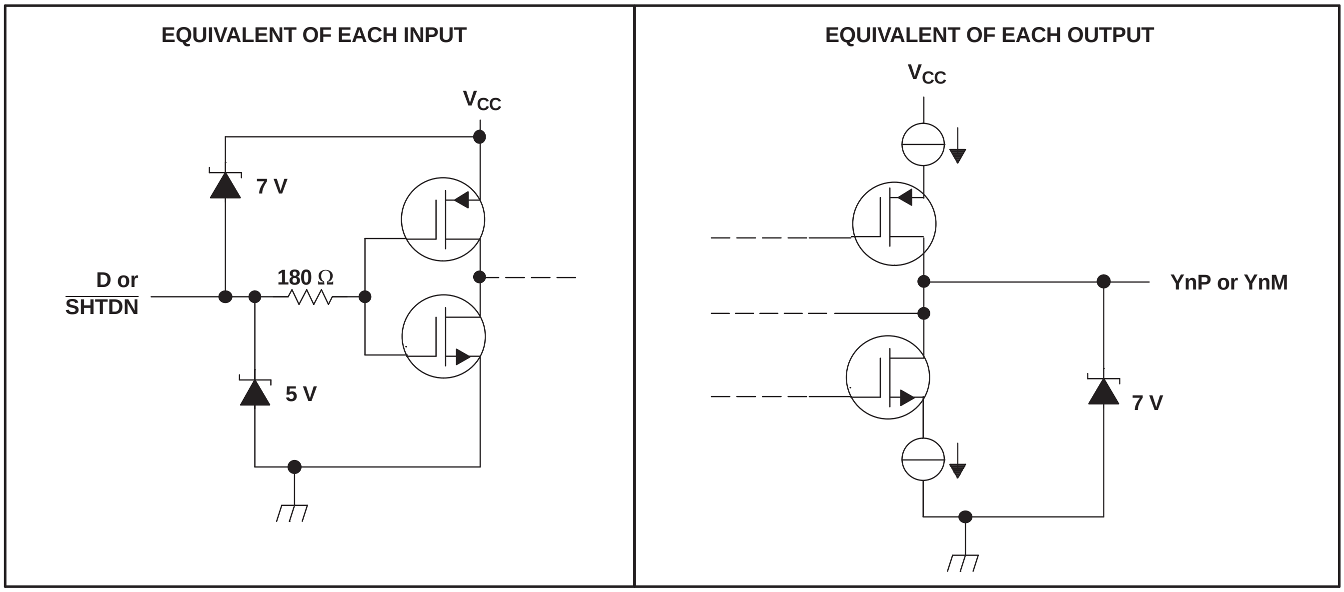
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – DGG	Reel of 2000	SN65LVDS84ADGGRQ1	65LVDS84AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM



SCHEMATICS OF INPUT AND OUTPUT



Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4	V
V_O V_I	Input and output voltage range (all terminals)		–0.5	V_{CC} + 0.5	V
	Continuous total power dissipation		See Dissipation Rating Table		
T_J	Operating virtual junction temperature range		–40	150	°C
ESD	Electrostatic discharge rating	Machine model		200	V
		Human-body model		6000	V
		Charged-device model		1500	V
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.

Dissipation Rating Table

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR[1] ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
DGG	1637 mW	13.1 mW/°C	1048 mW	327 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
Z_L	Differential load impedance	90		132	Ω
T_A	Operating free-air temperature	–40		125	°C

Timing Requirements

		MIN	NOM	MAX	UNIT
t_c	Input clock period	13.3	t_c	32.4	ns
t_w	Pulse duration, high-level input clock	0.4 t_c		0.6 t_c	ns
t_t	Transition time, input signal			5	ns
t_{su}	Setup time, data, D0–D20 valid before CLKIN↓ (see Figure 2)	3			ns
t_h	Hold time, data, D0–D20 valid after CLKIN↓ (see Figure 2)	1.5			ns

Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT}	Input threshold voltage				1.4		V
$\|V_{OD}\|$	Differential steady-state output voltage magnitude	R_L = 100 Ω, See Figure 3		247		454	mV
$\Delta\|V_{OD}\|$	Change in the steady-state differential output voltage magnitude between opposite binary states					50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	R_L = 100 Ω, See Figure 3		1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				80	150	mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$				25	μA
I_{IL}	Low-level input current	$V_{IL} = 0$				±10	μA
I_{OS}	Short-circuit output current	$V_{O(Yn)} = 0$			–6	±24	mA
		$V_{OD} = 0$			–6	±12	mA
I_{OZ}	High-impedance output current	V_O = 0 to V_{CC}				±10	μA
$I_{CC(AVG)}$	Quiescent supply current (average)	Disabled, All inputs at GND			15	170	μA
		Enabled, R_L = 100 Ω (4 places), Gray-scale pattern (see Figure 4)	f = 65 MHz		27	35	mA
			f = 75 MHz		30	38	mA
		Enabled, R_L = 100 Ω (4 places), Worst-case pattern (see Figure 5)	f = 65 MHz		28	36	mA
			f = 75 MHz		31	39	mA
C_I	Input capacitance				2		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{d0}	Delay time, CLKOUT↑ to serial bit position 0	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps(2), See Figure 6	–0.2		0.2	ns
t_{d1}	Delay time, CLKOUT↑ to serial bit position 1		$\frac{1}{7}t_C - 0.2$		$\frac{1}{7}t_C + 0.2$	
t_{d2}	Delay time, CLKOUT↑ to serial bit position 2		$\frac{2}{7}t_C - 0.2$		$\frac{2}{7}t_C + 0.2$	
t_{d3}	Delay time, CLKOUT↑ to serial bit position 3		$\frac{3}{7}t_C - 0.2$		$\frac{3}{7}t_C + 0.2$	
t_{d4}	Delay time, CLKOUT↑ to serial bit position 4		$\frac{4}{7}t_C - 0.2$		$\frac{4}{7}t_C + 0.2$	
t_{d5}	Delay time, CLKOUT↑ to serial bit position 5		$\frac{5}{7}t_C - 0.2$		$\frac{5}{7}t_C + 0.2$	
t_{d6}	Delay time, CLKOUT↑ to serial bit position 6		$\frac{6}{7}t_C - 0.2$		$\frac{6}{7}t_C + 0.2$	
$t_{sk(o)}$	Output skew, $t_n - \frac{n}{7}t_C$		–0.2		0.2	ns
t_{d7}	Delay time, CLKIN↓ to CLKOUT↑	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps(2), See Figure 6		2.7		ns
		t_c = 13.33 ns ~ 32.25 ns (±0.2%), |Input clock jitter| < 50 ps(2), See Figure 6	1		4.5	
$\Delta t_{c(o)}$	Cycle time, output clock jitter(3)	t_c = 15.38 + 0.308 sin(2π500E3t) ± 0.05 ns, See Figure 7		±62		ps
		t_c = 15.38 + 0.308 sin(2π3E6t) ±0.05 ns, See Figure 7		±121		
t_w	Pulse duration, high-level output clock			$\frac{4}{7}t_C$		ns
t_t	Transition time, differential output voltage (t_r or t_f)	See Figure 3		700	1500	ps
t_{en}	Enable time, $\overline{SHTDN}$↑ to phase lock (Yn valid)	See Figure 8		1		ms
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off state (CLKOUT low)	See Figure 9		6.5		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15000 cycles.

PARAMETER MEASUREMENT INFORMATION

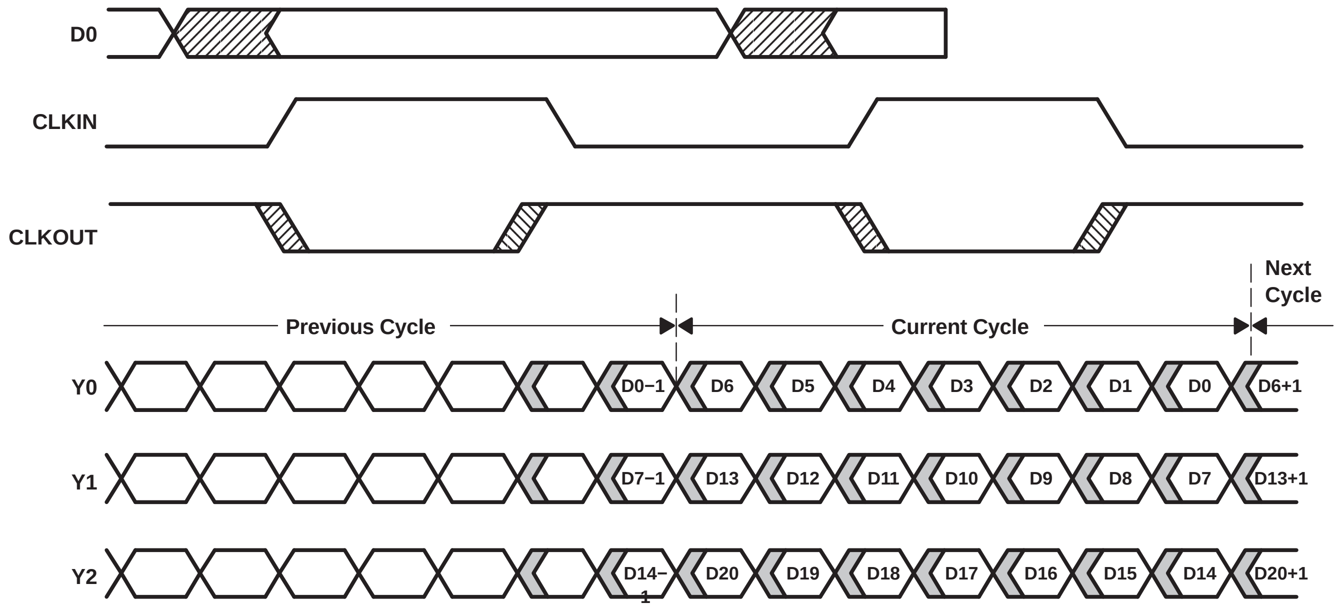
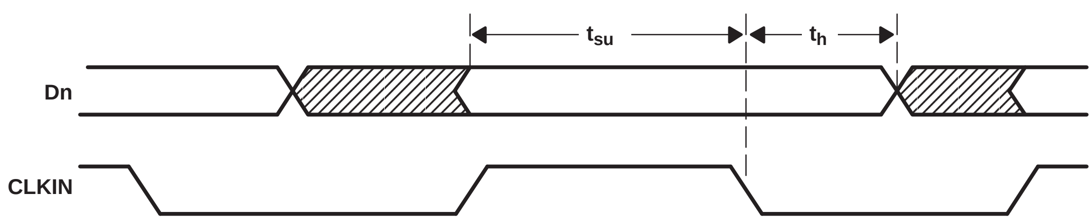


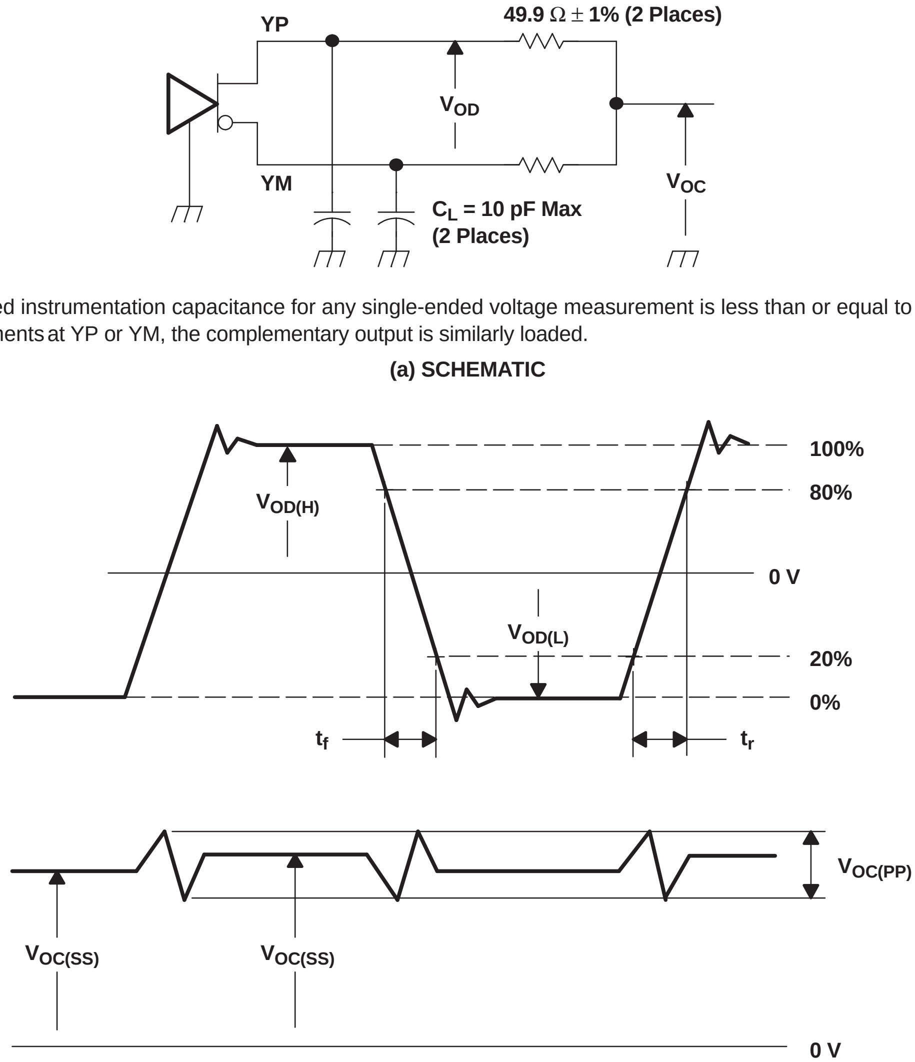
Figure 1. Typical Load and Shift Sequences



A. All input timing is defined at 1.4 V on an input signal with a 10%-to-90% rise or fall time of less than 5 ns.

Figure 2. Setup and Hold Time Definition

PARAMETER MEASUREMENT INFORMATION (continued)



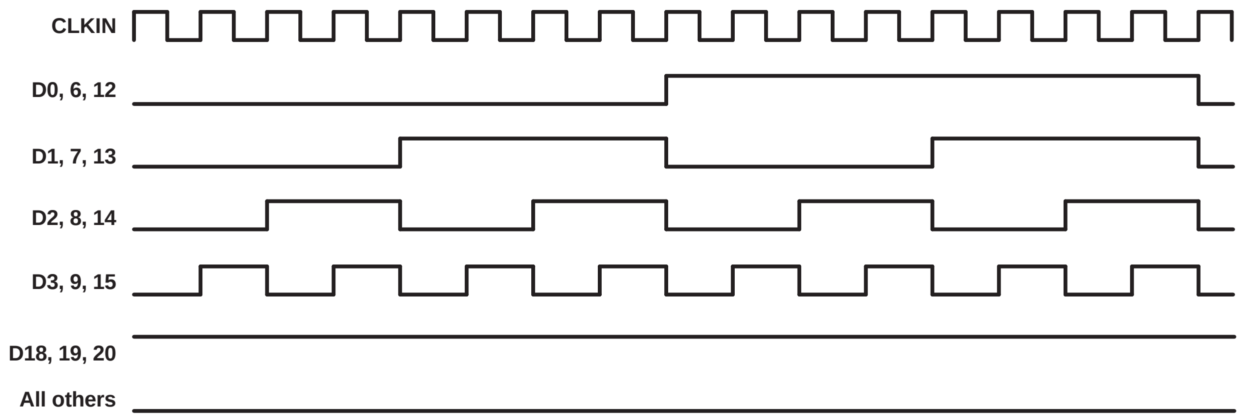
NOTE A: The lumped instrumentation capacitance for any single-ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output is similarly loaded.

(a) SCHEMATIC

(b) WAVEFORMS

Figure 3. Test Load and Voltage Definitions for LVDS Outputs

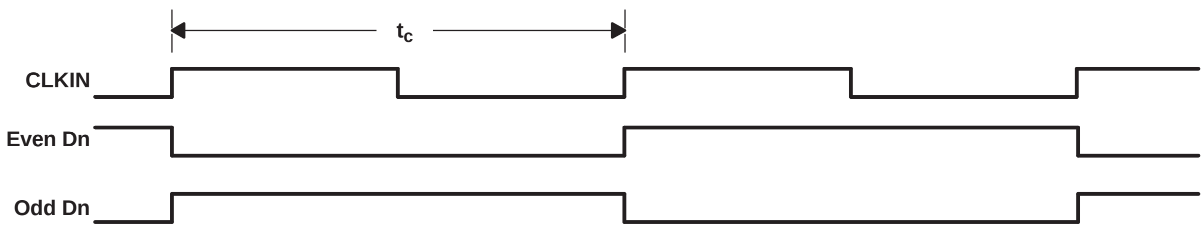
PARAMETER MEASUREMENT INFORMATION (continued)



A. The 16-grayscale test-pattern test device power consumption for a typical display pattern.

B. V_{IH} = 2 V and V_{IL} = 0.8 V

Figure 4. 16-Grayscale Test-Pattern Waveforms



A. The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

B. V_{IH} = 2 V and V_{IL} = 0.8 V

Figure 5. Worst-Case Test-Pattern Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

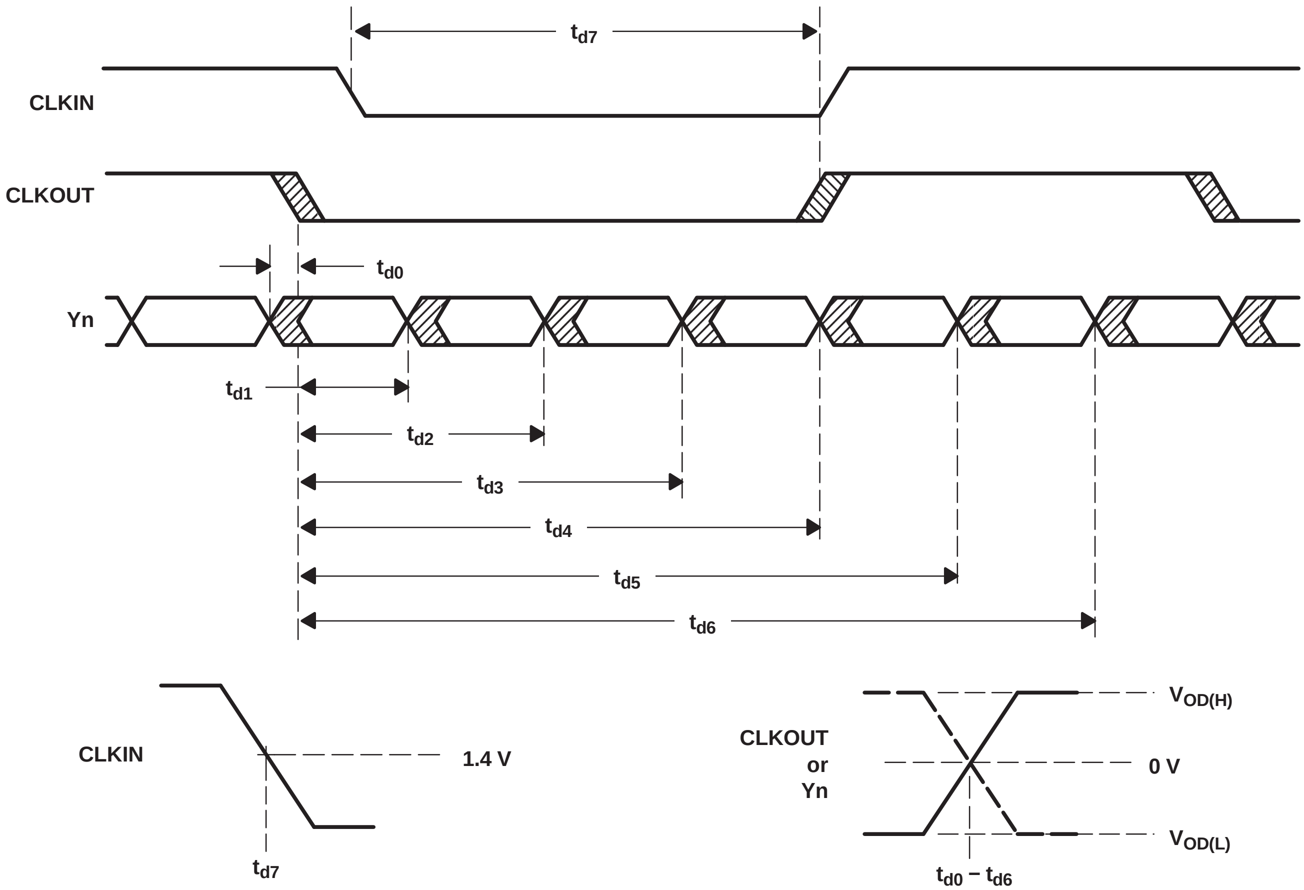
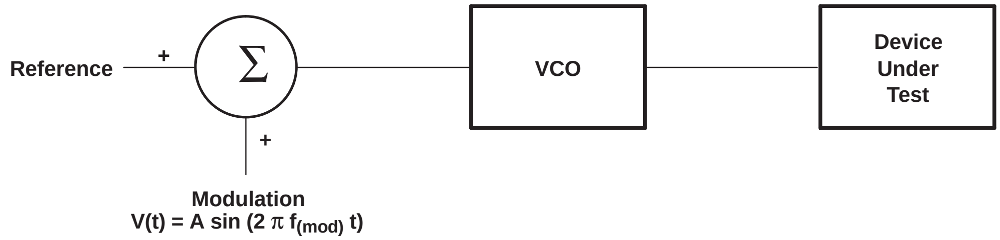


Figure 6. Timing Definitions



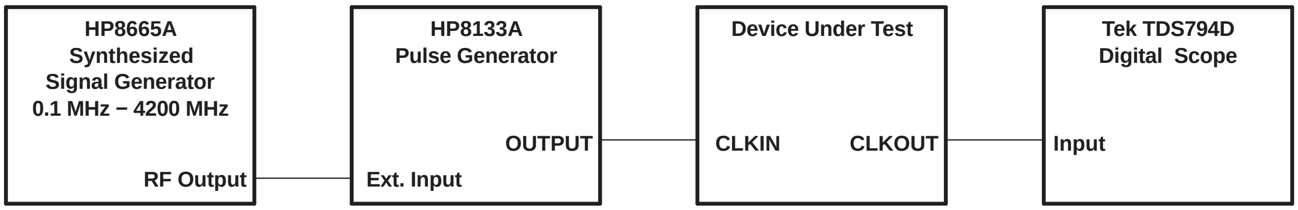


Figure 7. Clock Jitter Test Setup

TYPICAL CHARACTERISTICS

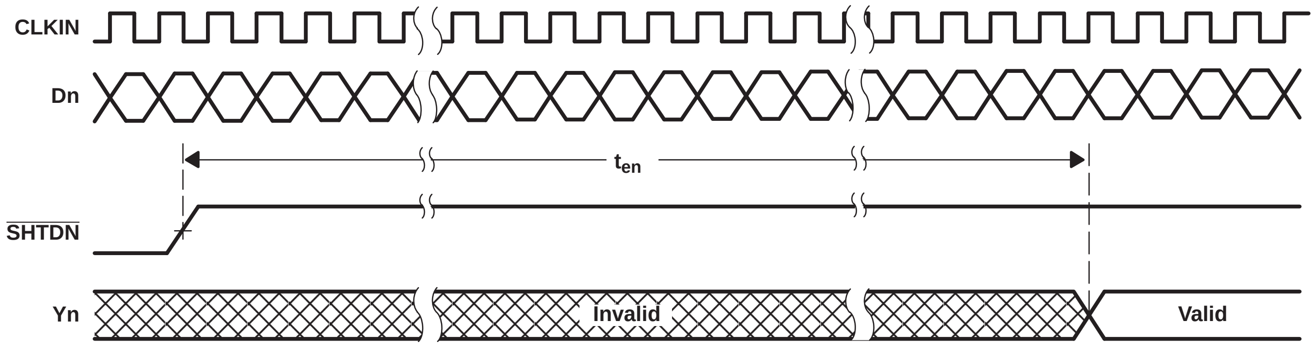


Figure 8. Enable Time Waveforms

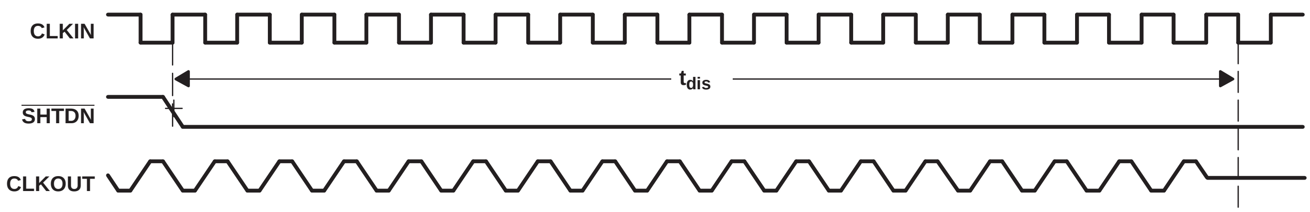


Figure 9. Disable Time Waveforms

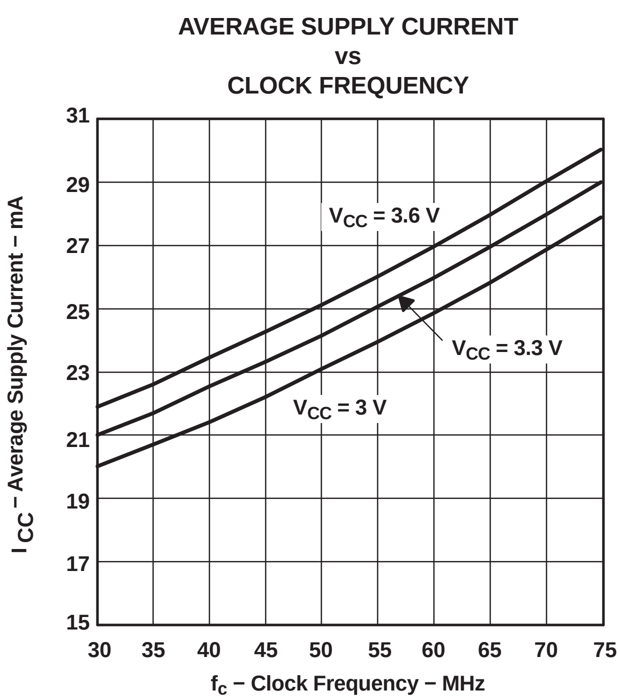


Figure 10. Grayscale Input Pattern

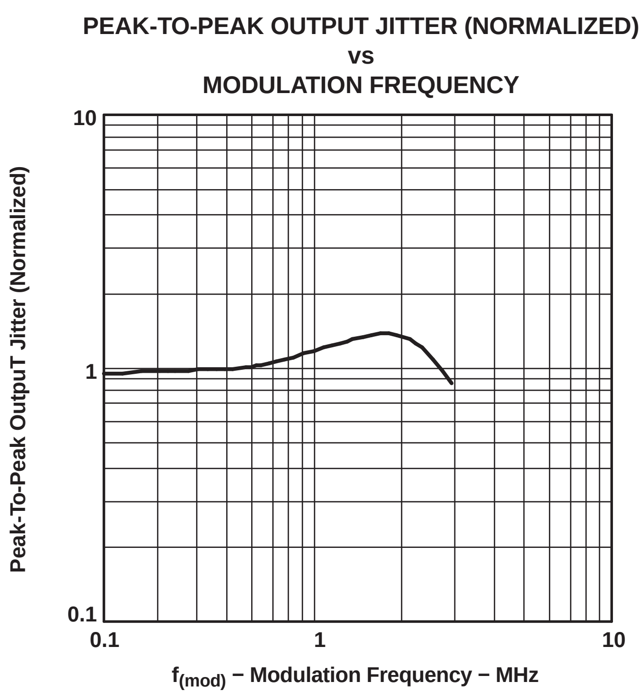
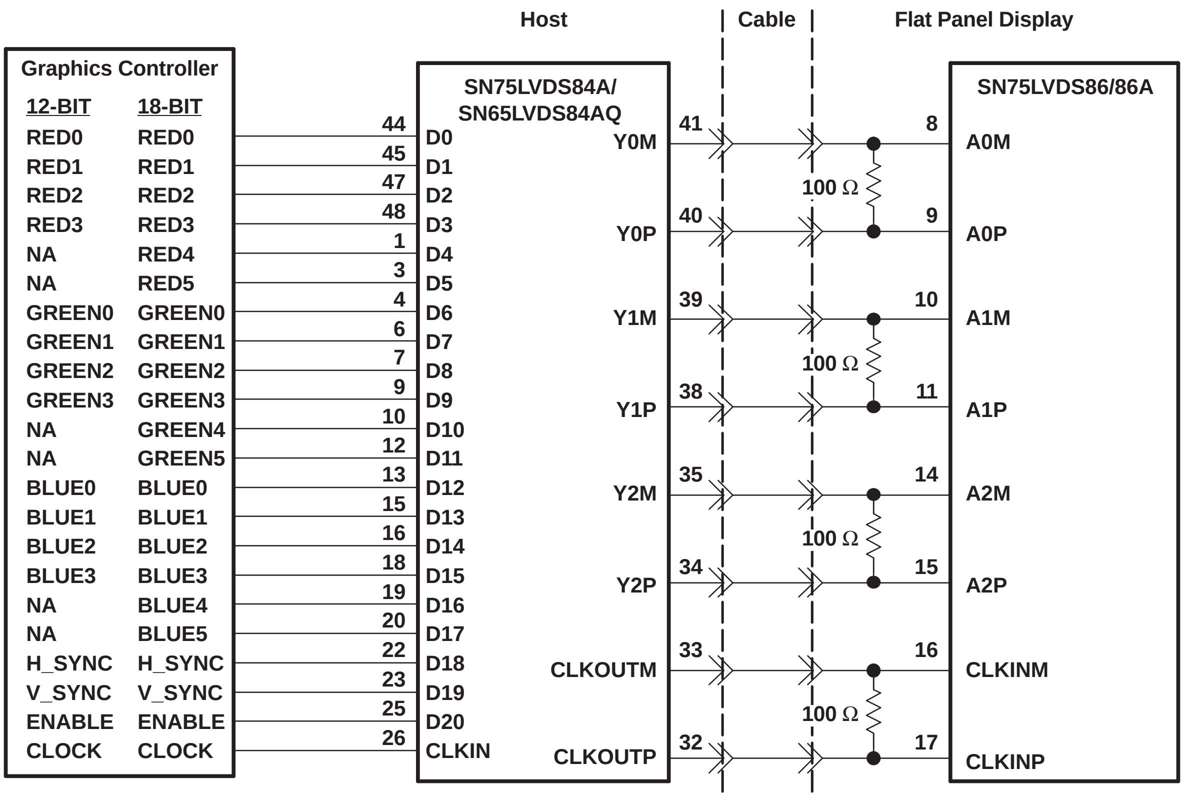


Figure 11. Output Period Jitter vs Modulation Frequency

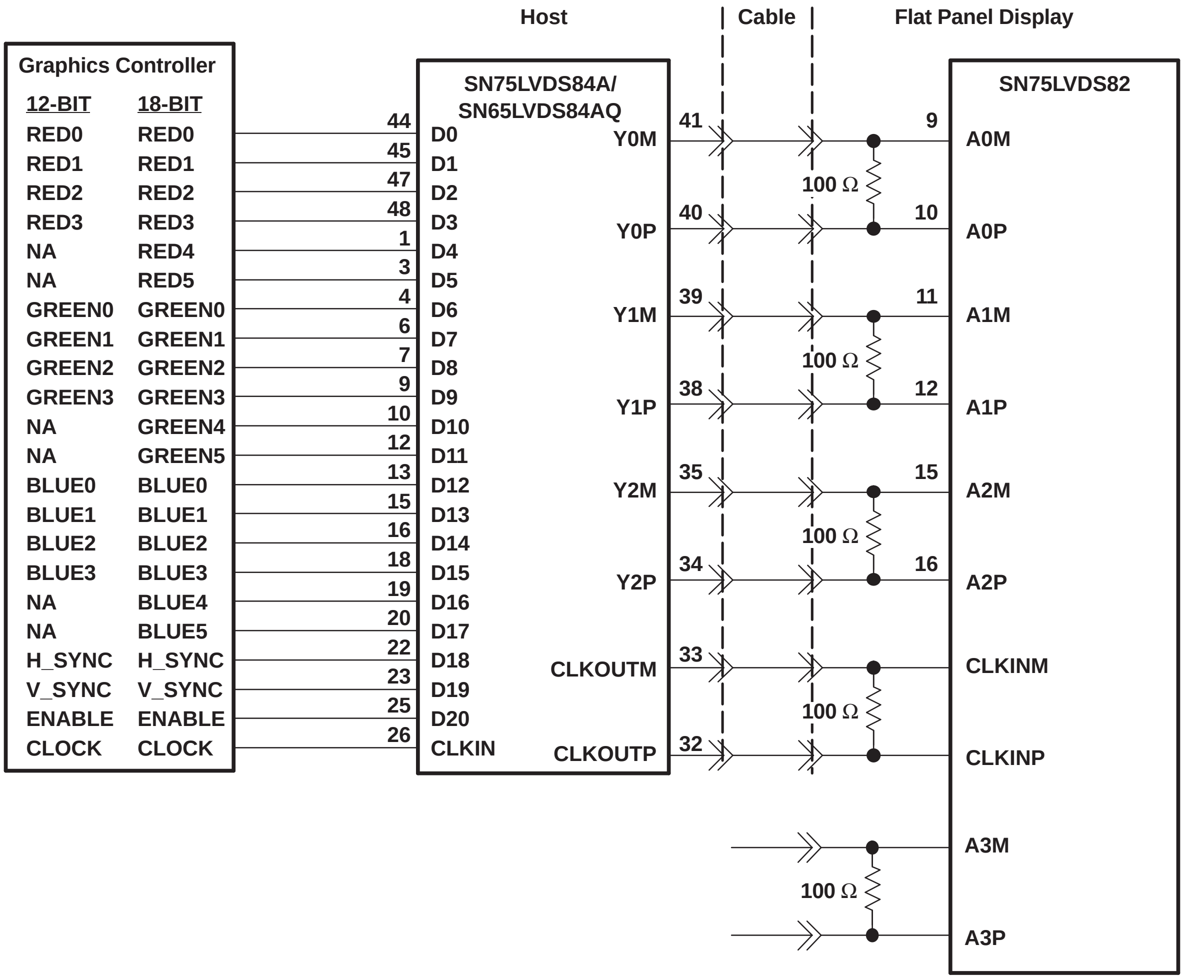
APPLICATION INFORMATION



A. The five 100-Ω terminating resistors are recommended to be 0603 types.

B. NA – not applicable, these unused inputs should be left open.

Figure 12. Color Host to LCD Panel Application



A. The four 100-Ω terminating resistors are recommended to be 0603 types.

B. NA – not applicable, these unused inputs should be left open.

Figure 13. 18-Bit Color Host to 24-Bit LCD Display Panel Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS84AQDGGRQ1	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS84AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

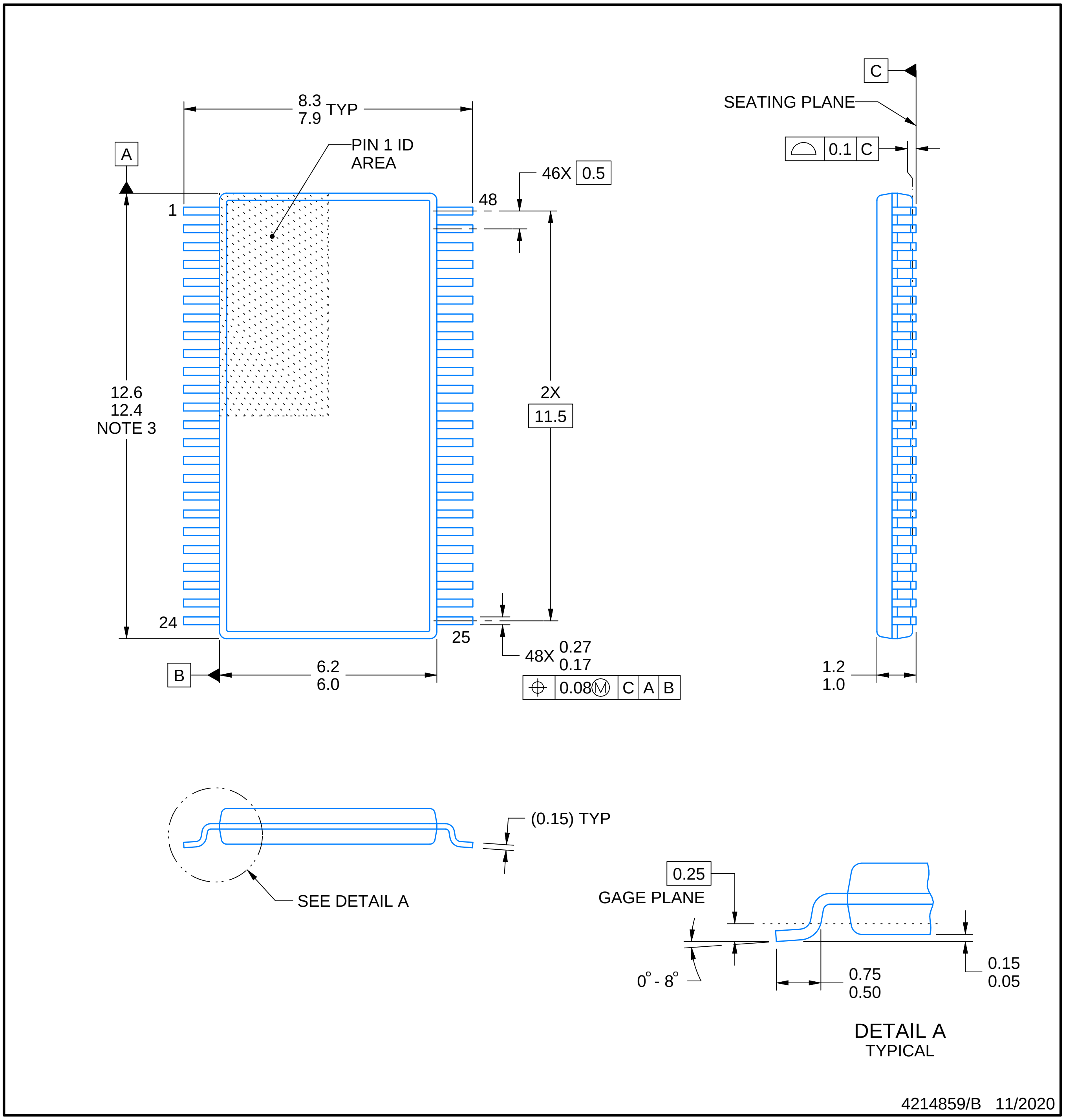
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

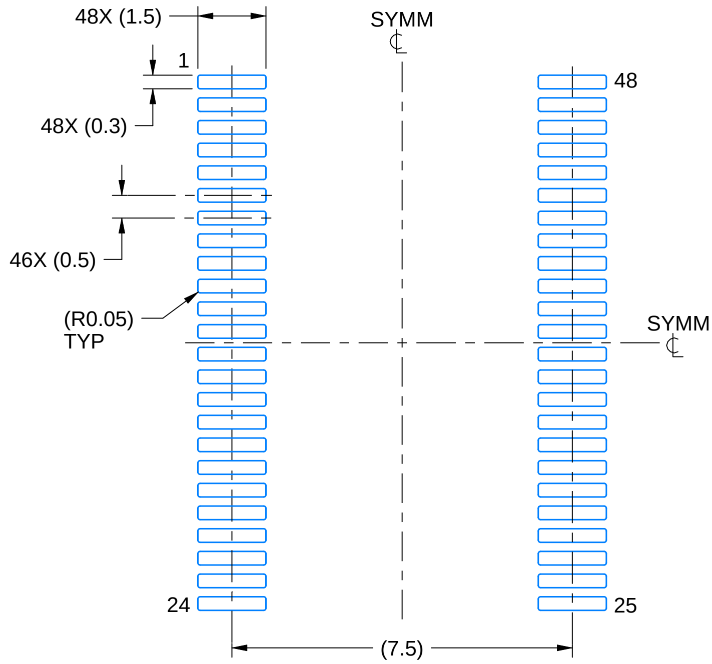
SMALL OUTLINE PACKAGE



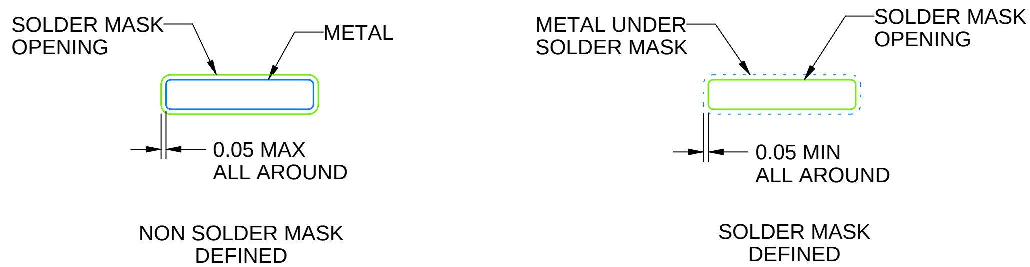
4214859/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

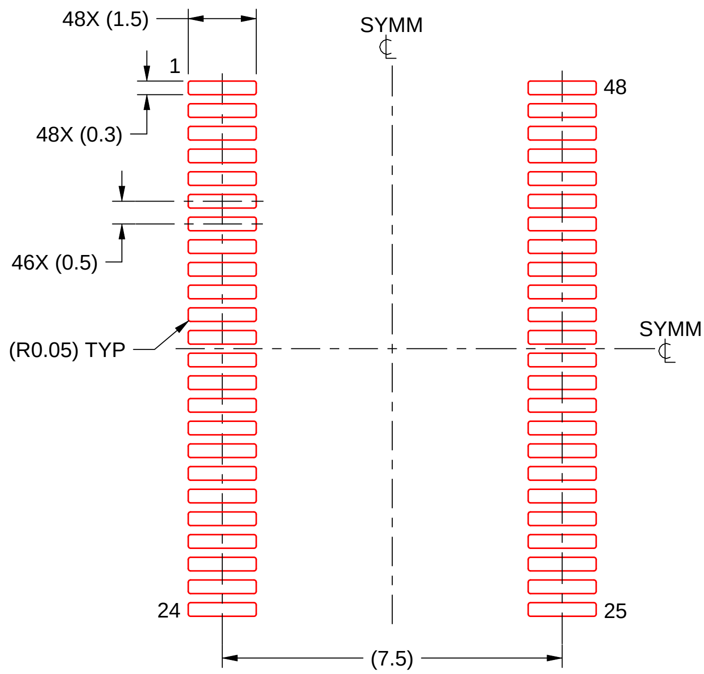


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

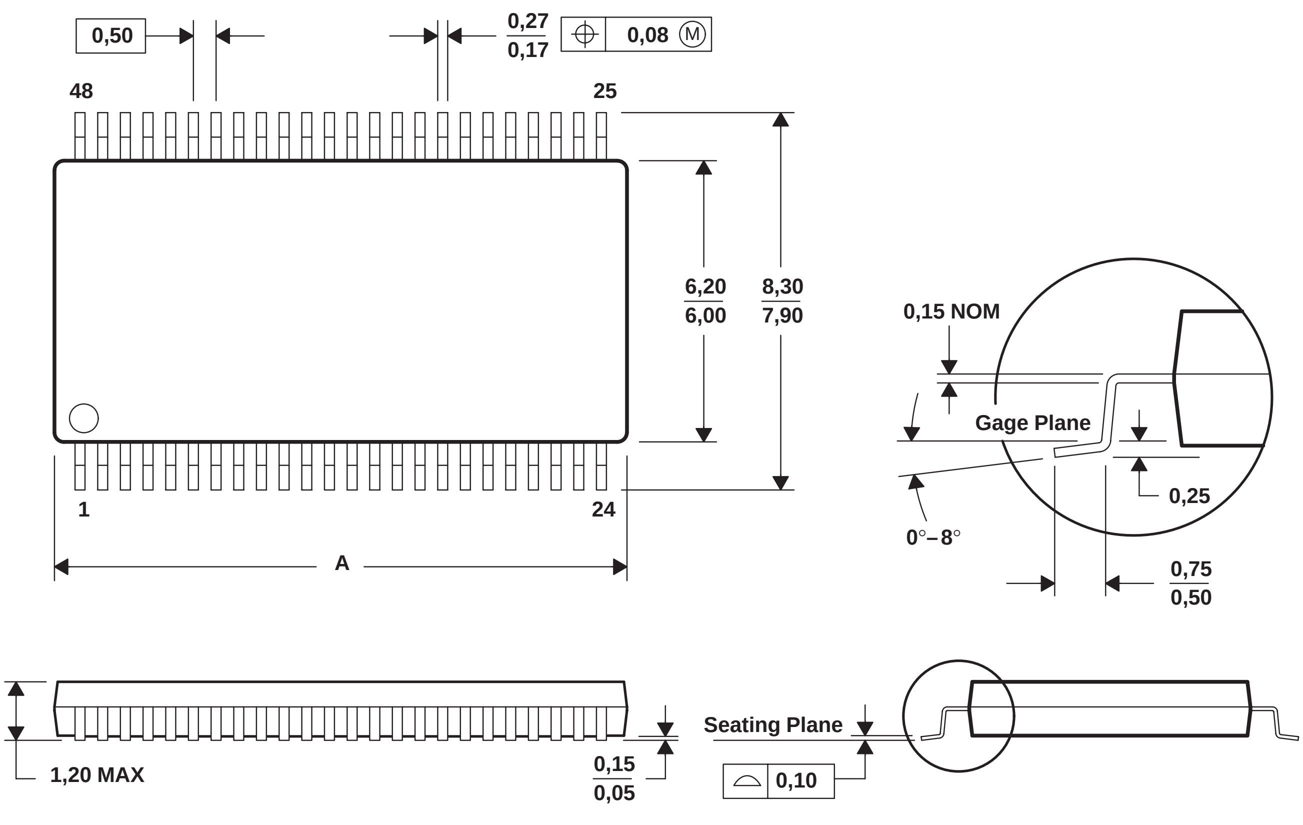
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153