

# SN74AC2G100 Dual Configurable Data Flip-Flops With Clear

## 1 Features

- Wide operating range of 1.5V to 6V
- Inputs accept voltages up to 6V
- Continuous  $\pm 24\text{mA}$  output drive at 5V
- Supports up to  $\pm 75\text{mA}$  output drive at 5V in short bursts
- Drives  $50\Omega$  transmission lines
- Maximum  $t_{pd}$  of 9.7ns at 5V, 50pF load

## 2 Applications

- [Hold a signal during controller reset](#)
- [Input slow edge-rate signals](#)
- [Operate in noisy environments](#)

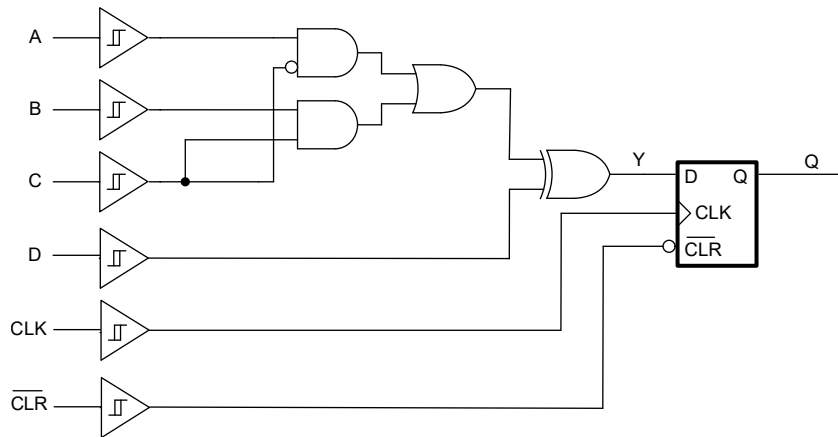
## 3 Description

The SN74AC2G100 contains two independent D-type flip-flops with rising edge triggered clock, active low clear, and configurable logic data inputs. The data inputs can be configured for many 1- and 2-input logic functions, including buffer, inverter, AND, OR, NAND, NOR, XOR, XNOR. All inputs have Schmitt-trigger architecture to support slow or noisy input signals.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SN74AC2G100	BQB (WQFN, 16)	3.6mm × 2.6mm	3.6mm × 2.6mm

- (1) For more information, see .
- (2) The package size (length × width) is a nominal value and includes pins, where applicable
- (3) The body size (length × width) is a nominal value and does not include pins.



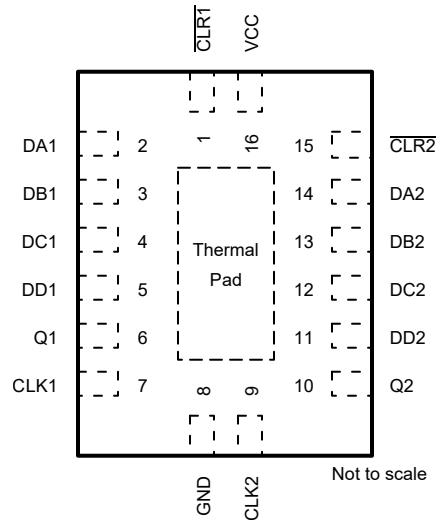
Logic Diagram (Positive Logic)



## Table of Contents

<b>1 Features</b> .....	1	7.5 Combinatorial Logic Configurations.....	13
<b>2 Applications</b> .....	1	<b>8 Application and Implementation</b> .....	15
<b>3 Description</b> .....	1	8.1 Application Information.....	15
<b>4 Pin Configuration and Functions</b> .....	3	8.2 Typical Application.....	15
<b>5 Specifications</b> .....	4	8.3 Application Curves.....	18
5.1 Absolute Maximum Ratings.....	4	8.4 Power Supply Recommendations.....	18
5.2 ESD Ratings.....	4	8.5 Layout.....	18
5.3 Recommended Operating Conditions.....	4	<b>9 Device and Documentation Support</b> .....	20
5.4 Thermal Information.....	4	9.1 Receiving Notification of Documentation Updates....	20
5.5 Electrical Characteristics.....	5	9.2 Support Resources.....	20
5.6 Timing Characteristics.....	6	9.3 Trademarks.....	20
5.7 Switching Characteristics.....	7	9.4 Electrostatic Discharge Caution.....	20
5.8 Typical Characteristics.....	7	9.5 Glossary.....	20
<b>6 Parameter Measurement Information</b> .....	10	<b>10 Revision History</b> .....	20
<b>7 Detailed Description</b> .....	11	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	20
7.1 Overview.....	11	11.1 Tape and Reel Information.....	21
7.2 Functional Block Diagram.....	11	11.2 Mechanical Data.....	23
7.3 Feature Description.....	11		
7.4 Device Functional Modes.....	13		

## 4 Pin Configuration and Functions



**Figure 4-1. BQB Package, 16-Pin WQFN (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
CLR1	1	I	Clear for Channel 1, active low
DA1	2	I	Channel 1, Data input A
DB1	3	I	Channel 1, Data input B
DC1	4	I	Channel 1, Data input C
DD1	5	I	Channel 1, Data input D
Q1	6	O	Channel 1, Output Q
CLK1	7	I	Clock for Channel 1, rising edge triggered
GND	8	G	Ground
CLK2	9	I	Clock for Channel 2, rising edge triggered
Q2	10	O	Channel 2, Output Q
DD2	11	I	Channel 2, Data input D
DC2	12	I	Channel 2, Data input C
DB2	13	I	Channel 2, Data input B
DA2	14	I	Channel 2, Data input A
CLR2	15	I	Clear for Channel 2, active low
V <sub>CC</sub>	16	P	Positive Supply
Thermal Pad <sup>(2)</sup>		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) BQB package only

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < -0.5V or V <sub>I</sub> > V <sub>CC</sub> + 0.5V		±20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < -0.5V or V <sub>O</sub> > V <sub>CC</sub> + 0.5V		±50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±50	mA
	Continuous output current through V <sub>CC</sub> or GND			±200	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.5	6	V
V <sub>I</sub>	Input Voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output Voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.8V		-1	mA
		V <sub>CC</sub> = 2.5V		-2	
		V <sub>CC</sub> = 3V		-12	
		V <sub>CC</sub> = 4.5V to 6V		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.8V		1	mA
		V <sub>CC</sub> = 2.5V		2	
		V <sub>CC</sub> = 3V		12	
		V <sub>CC</sub> = 4.5V to 6V		24	
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

### 5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC <sup>(1)</sup>						UNIT
		R <sub>θJA</sub>	R <sub>θJC(top)</sub>	R <sub>θJB</sub>	Ψ <sub>JT</sub>	Ψ <sub>JB</sub>	R <sub>θJC(bot)</sub>	
BQB (WQFN)	16	91.2	95.1	61.4	18.0	61.2	38.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>T+</sub>	Positive-going input threshold voltage	1.5V	0.71		1.06	V
		1.8V	0.82		1.22	
		2.5V	1.08		1.51	
		3V	1.19		1.72	V
		4.5V	1.61		2.37	
		6V	1.87		2.82	V
V <sub>T-</sub>	Negative-going input threshold voltage	1.5V	0.33		0.68	V
		1.8V	0.42		0.68	
		2.5V	0.59		0.8	
		3V	0.68		0.95	V
		4.5V	0.98		1.36	
		6V	1.14		1.63	V
ΔV <sub>T</sub>	Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	1.5V	0.31		0.66	V
		1.8V	0.37		0.66	
		2.5V	0.45		0.74	
		3V	0.47		0.84	V
		4.5V	0.62		1.06	
		6V	0.71		1.23	V
V <sub>OH</sub>	I <sub>OH</sub> = -50μA	1.5V	1.4	1.49		V
		1.8V	1.7	1.79		
		2.5V	2.4	2.49		
		3V	2.9	2.99		
		4.5V	4.4	4.49		
		6V	5.4	5.99		
	I <sub>OH</sub> = -1mA	1.8V	1.44			
	I <sub>OH</sub> = -2mA	2.5V	2			
	I <sub>OH</sub> = -12mA	3V	2.4			
	I <sub>OH</sub> = -24mA	4.5V	3.7			
I <sub>OH</sub> = -24mA	6V	4.7				
I <sub>OH</sub> = -75mA	6V	3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50μA	1.5V		0.01	0.1	V
		1.8V		0.01	0.1	
		2.5V		0.01	0.1	
		3V		0.01	0.1	
		4.5V		0.01	0.1	
		6V		0.01	0.1	
	I <sub>OL</sub> = 1mA	1.8V			0.36	
	I <sub>OL</sub> = 2mA	2.5V			0.5	
	I <sub>OL</sub> = 12mA	3V			0.5	
	I <sub>OL</sub> = 24mA	4.5V			0.5	
	I <sub>OL</sub> = 24mA	6V			0.5	
	I <sub>OL</sub> = 75mA	6V			1.65	
I <sub>I</sub>	V <sub>I</sub> = 6V or GND	0V to 6V			±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	6V			20	μA

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5V		2		pF

## 5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V <sub>CC</sub>	-40°C to 125°C		UNIT
				MIN	MAX	
f <sub>clock</sub>	Clock frequency		1.5V	22		MHz
			3.3V ± 0.3V	80		
			5V ± 0.5V	140		
			6V	175		
t <sub>w</sub>	Pulse duration	CL $\bar{R}$ low	1.5V	4.1		ns
			3.3V ± 0.3V	3.3		
			5V ± 0.5V	3.3		
			6V	3.3		
		CLK	1.5V	4.1		
			3.3V ± 0.3V	3.3		
			5V ± 0.5V	3.3		
			6V	3.3		
t <sub>su</sub>	Set up time, data before CLK $\uparrow$	DAx, DBx and DCx	1.5V	6.6		ns
			3.3V ± 0.3V	5.3		
			5V ± 0.5V	5.3		
			6V	5.3		
		DDx	1.5V	4.6		
			3.3V ± 0.3V	3.3		
			5V ± 0.5V	3.3		
			6V	3.3		
		CL $\bar{R}$ inactive	1.5V	2.7		
			3.3V ± 0.3V	2		
			5V ± 0.5V	1.9		
			6V	1.1		
t <sub>H</sub>	Hold time, data after CLK $\uparrow$	DAx, DBx and DCx	1.5V	1		ns
			3.3V ± 0.3V	1		
			5V ± 0.5V	1		
			6V	1		
		DDx	1.5V	0.7		
			3.3V ± 0.3V	0.7		
			5V ± 0.5V	0.7		
			6V	0.7		

### 5.7 Switching Characteristics

over operating free-air temperature range;  $C_L = 50\text{pF}$  typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
$t_{pd}$	CLK	Q	1.5V			41	ns
			$3.3V \pm 0.3V$			13.9	ns
			$5V \pm 0.5V$			9.7	ns
			6V			8	ns
	CLR	Q	1.5V			36	ns
			$3.3V \pm 0.3V$			13.1	ns
			$5V \pm 0.5V$			9.6	ns
			6V			8.2	ns
$t_{sk(o)}$		Q	1.5V			4	ns
			6V			1	ns
$C_{PD}^{(1)}$	CLK or CLK INH	$Q_H$	5V			50	pF

(1) Power dissipation capacitance measured with  $C_L = 50\text{pF}$ ,  $F = 1\text{MHz}$

### 5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

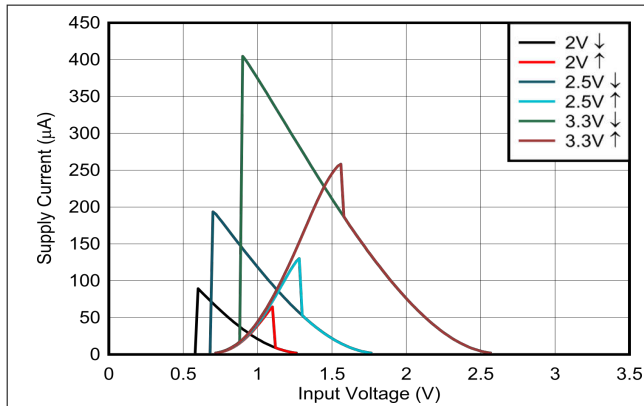


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

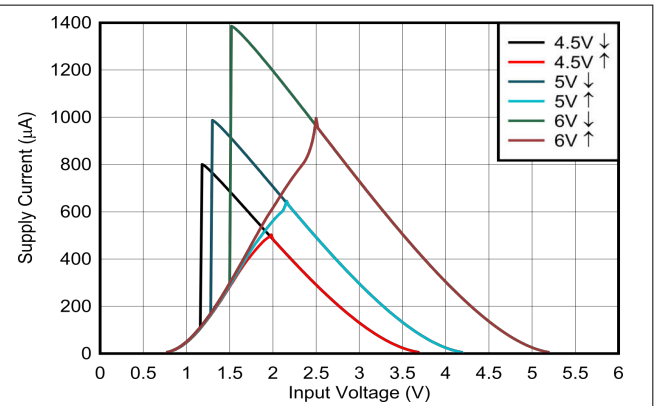


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

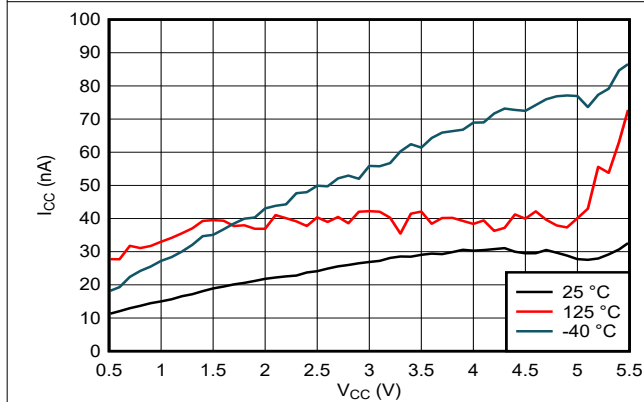


Figure 5-3. Supply Current Across Supply Voltage

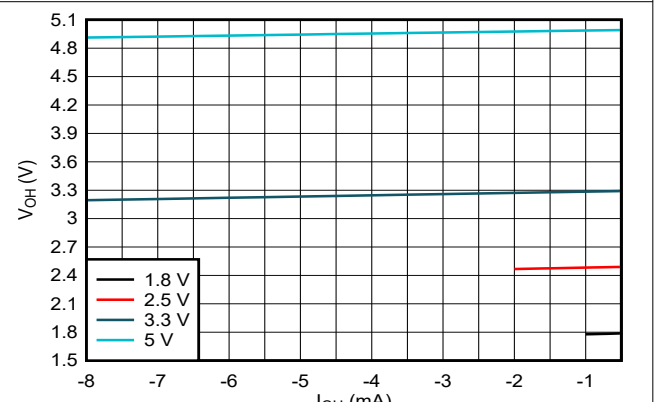


Figure 5-4. Output Voltage vs Current in HIGH State

## 5.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

ADVANCE INFORMATION

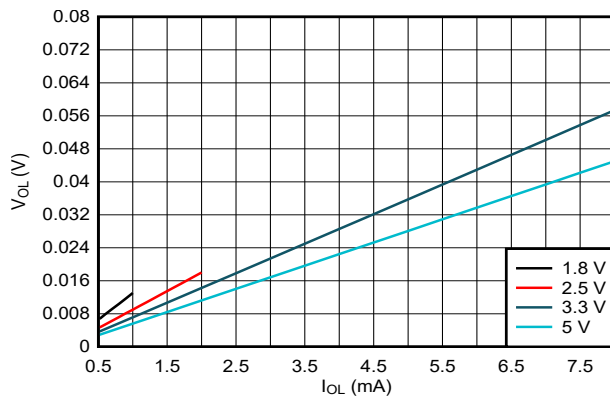


Figure 5-5. Output Voltage vs Current in LOW State

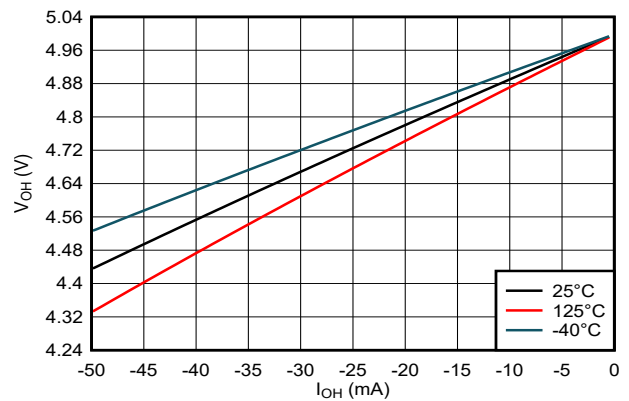


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

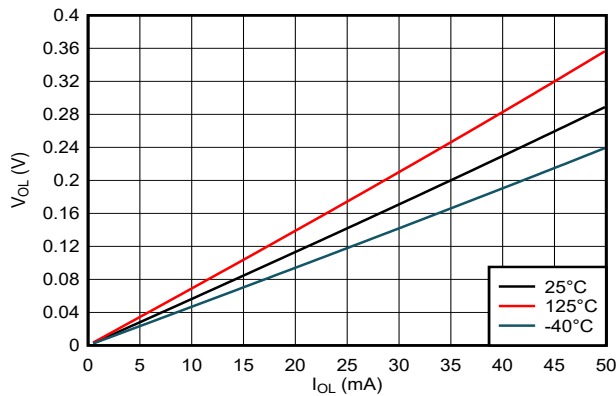


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

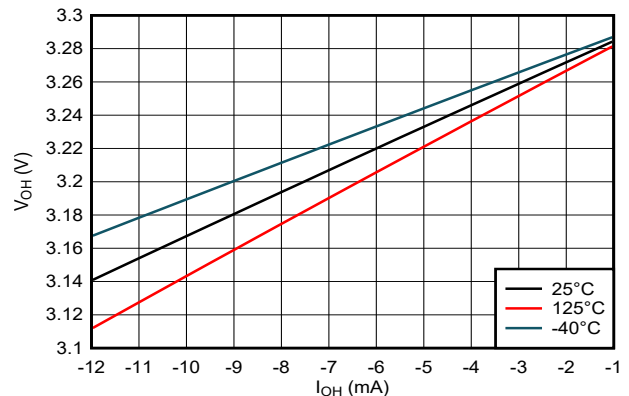


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

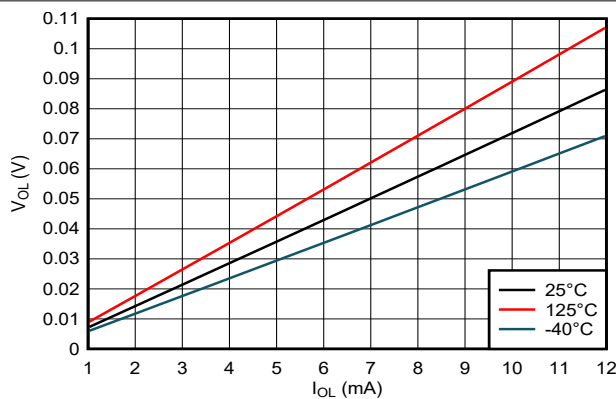


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

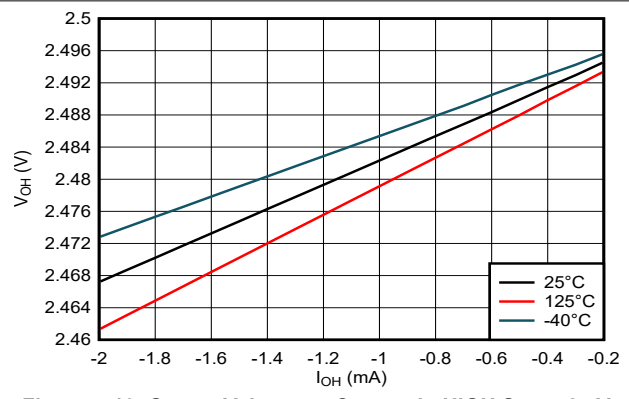
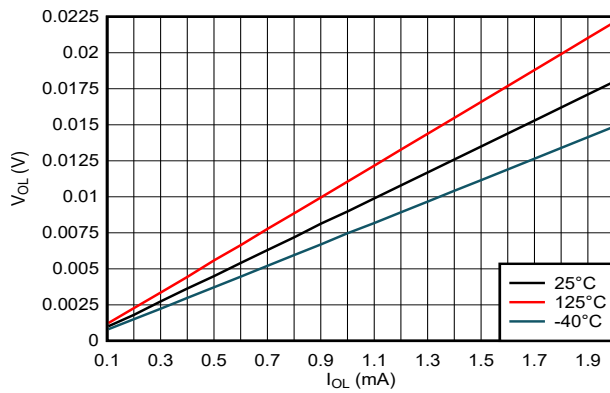


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

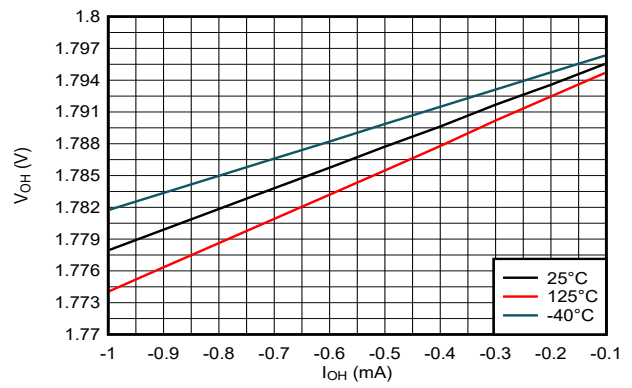


### 5.8 Typical Characteristics (continued)

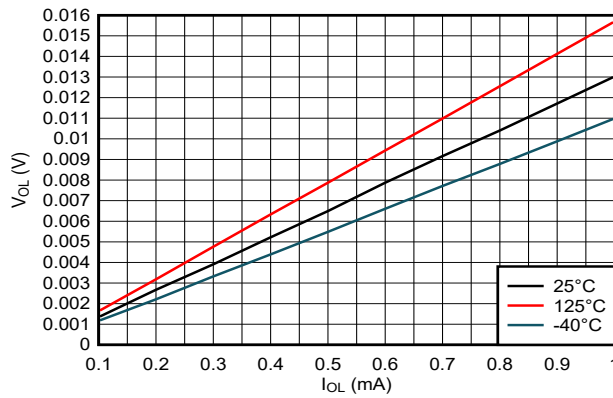
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



**Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply**



**Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply**



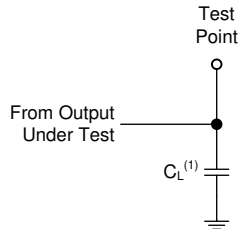
**Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply**

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_f < 2.5\text{ns}$ .

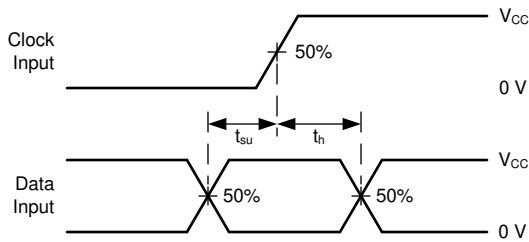
For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.

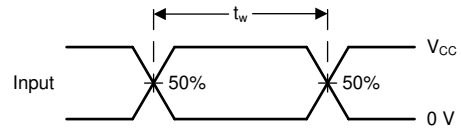


(1)  $C_L$  includes probe and test-fixture capacitance.

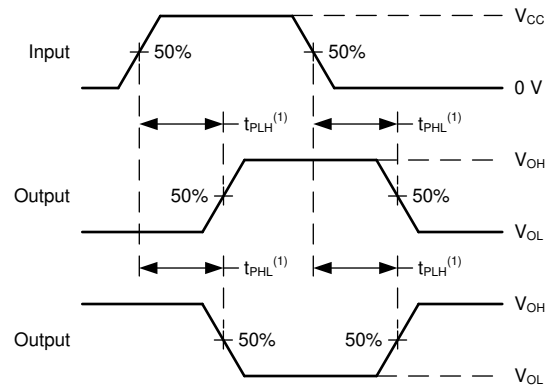
**Figure 6-1. Load Circuit for Push-Pull Outputs**



**Figure 6-3. Voltage Waveforms, Setup and Hold Times**

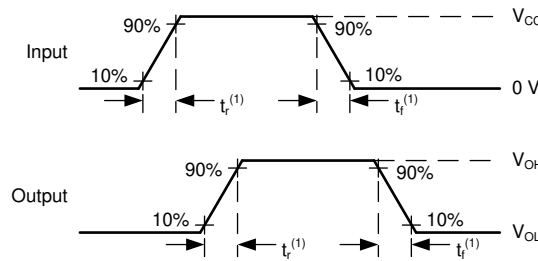


**Figure 6-2. Voltage Waveforms, Pulse Duration**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 6-4. Voltage Waveforms Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

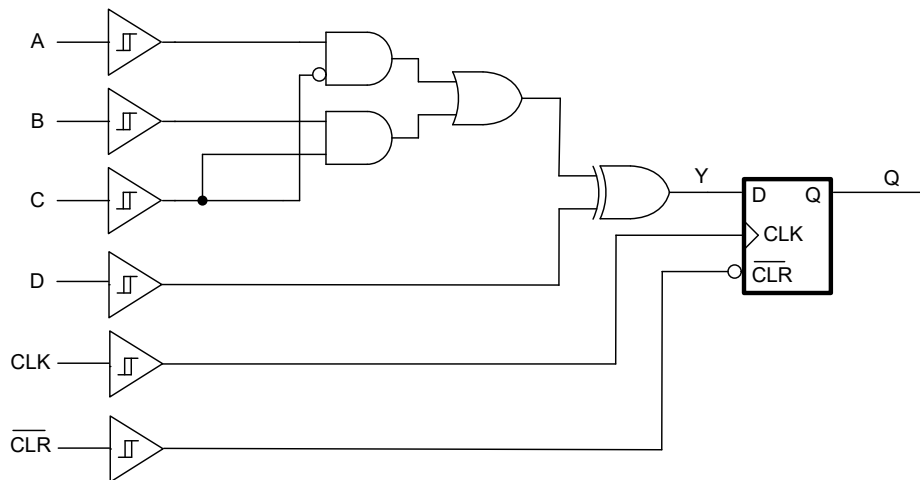
**Figure 6-5. Voltage Waveforms, Input and Output Transition Times**

## 7 Detailed Description

### 7.1 Overview

The SN74AC2G100 is a dual, sequential, configurable multiple function device with Schmitt-trigger inputs. A 4-input combinational logic block provides a wide range of configurable data input logic. The output of the configurable logic block is the data input to a D-Flip Flop, which is transferred to the Q output on the positive going CLK edge. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and buffer.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

#### 7.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ( $R = V \div I$ ).

The Schmitt-trigger input architecture provides hysteresis as defined by  $\Delta V_T$  in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

#### 7.3.3 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

### 7.3.4 Clamp Diode Structure

As shown in [Figure 7-1](#), the inputs and outputs to this device have both positive and negative clamping diodes.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

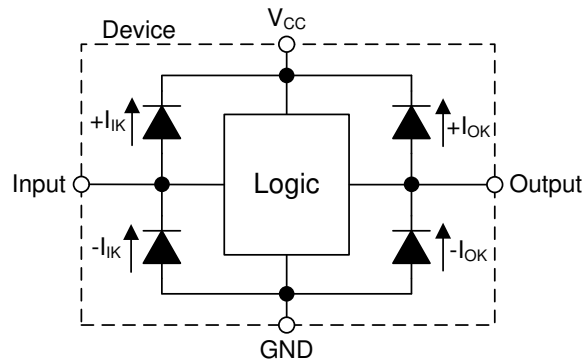


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

### 7.4 Device Functional Modes

**Table 7-1. Function Table**

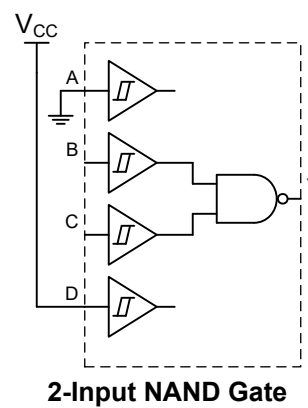
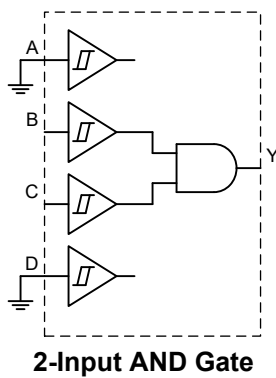
INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	L
L	L	L	H	H
L	L	H	L	L
L	L	H	H	H
L	H	L	L	L
L	H	L	H	H
L	H	H	L	H
L	H	H	H	L
H	L	L	L	H
H	L	L	H	L
H	L	H	L	L
H	L	H	H	H
H	H	L	L	H
H	H	L	H	L
H	H	H	L	H
H	H	H	H	L

**Table 7-2. Function Table**

INPUTS <sup>(1) (2)</sup>			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

- (1) H = high voltage level, L = low voltage level, X = don't care
- (2) This configuration is nonstable; that is, it does not persist when CLR returns to its inactive (high) level.

### 7.5 Combinatorial Logic Configurations



ADVANCE INFORMATION

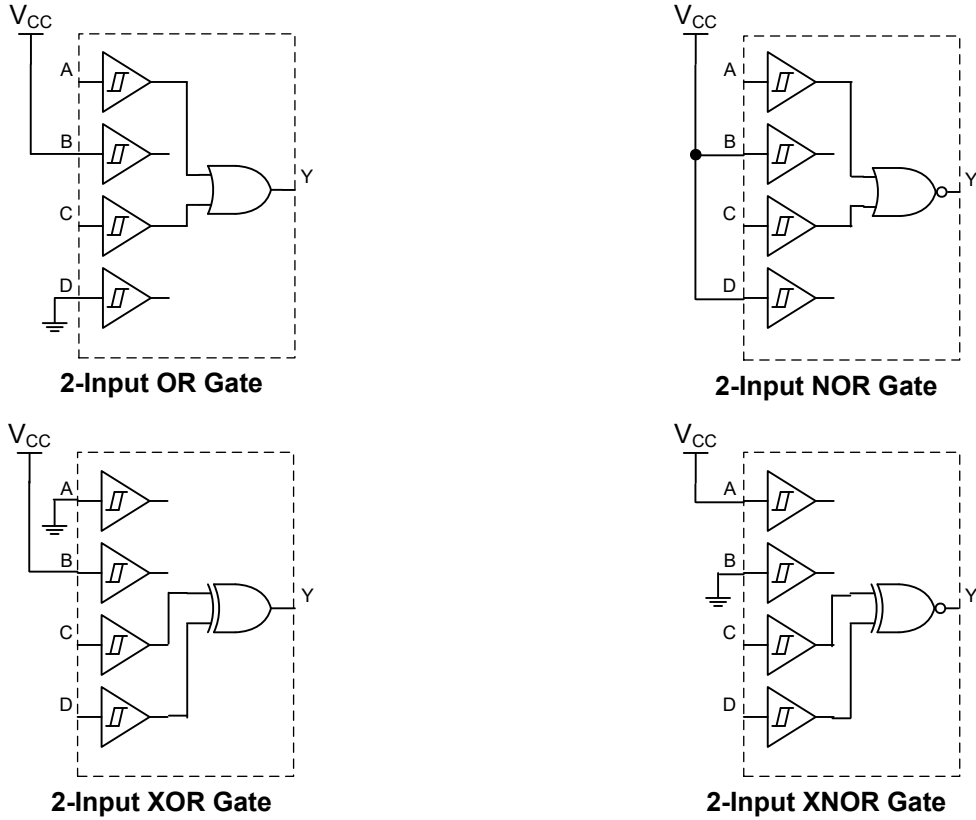


Figure 7-2. Logic Configurations

ADVANCE INFORMATION

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The SN74AC2G100 device offers flexible configuration for many design applications. The following example shows one way to hold the power supply operating mode while the system controller is put into a low power or disabled state. It is often beneficial to reduce the power consumption of a system controller when it is not required. The SN74AC2G100 provides a highly configurable D-type flip-flop to maintain a valid logic state to control a variety of system components when the controller is disabled.

### 8.2 Typical Application

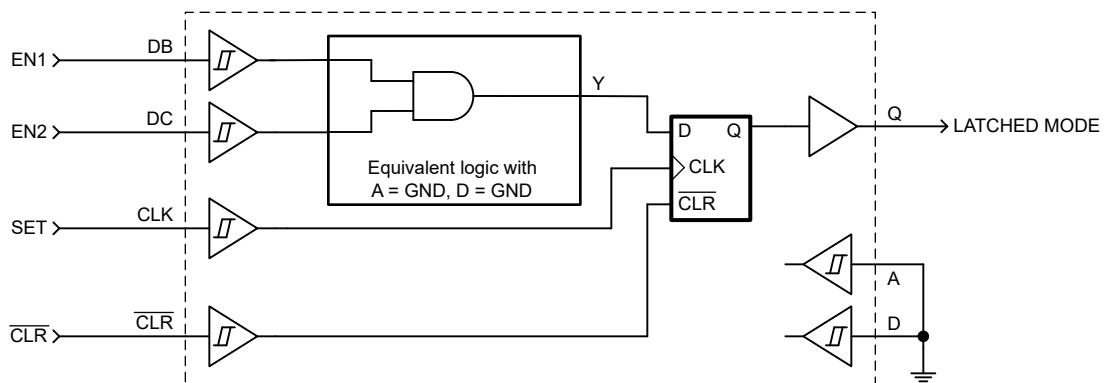


Figure 8-1. Typical Application Schematic

## 8.2.1 Design Requirements

### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AC2G100 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AC2G100 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AC2G100 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AC2G100 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.



### 8.2.1.2 Input Considerations

Input signals must cross  $V_{t-(\min)}$  to be considered a logic LOW, and  $V_{t+(\max)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AC2G100 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k $\Omega$  resistor value is often used due to these factors.

The SN74AC2G100 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the  $\Delta V_{T(\min)}$  in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than  $V_{CC}$  or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

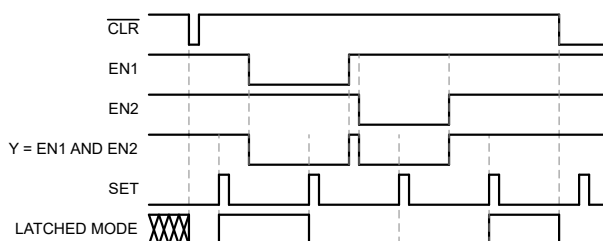
Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50\text{pF}$ . This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AC2G100 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(\text{max})})\Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in  $\text{M}\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 8.3 Application Curves



**Figure 8-2. Typical Application Timing Diagram**

### 8.4 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\mu\text{F}$  and  $1\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 8.5 Layout

#### 8.5.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid  $90^\circ$  corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

8.5.2 Layout Example

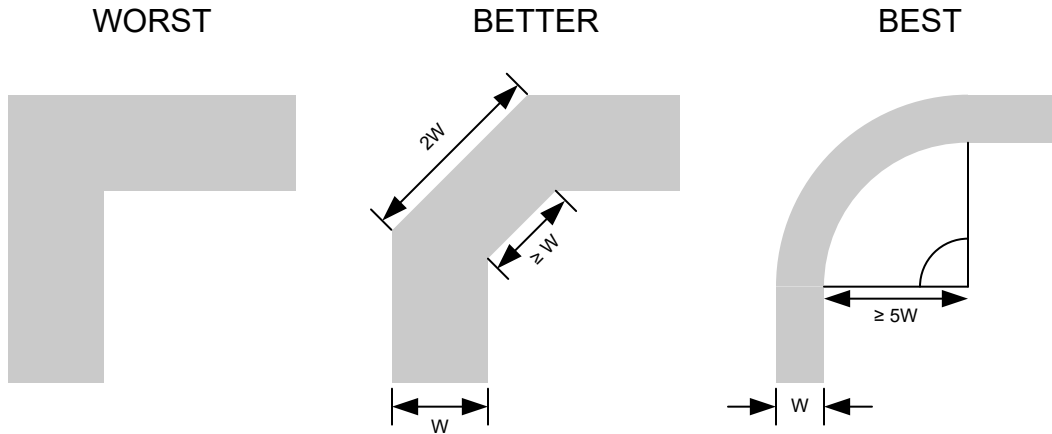


Figure 8-3. Example Trace Corners for Improved Signal Integrity

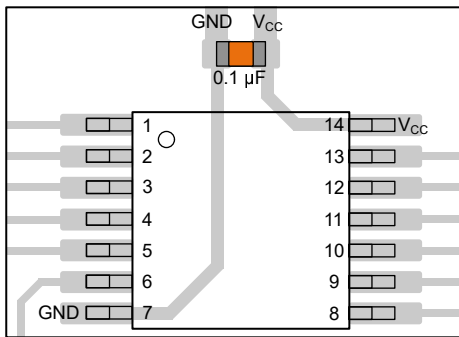


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

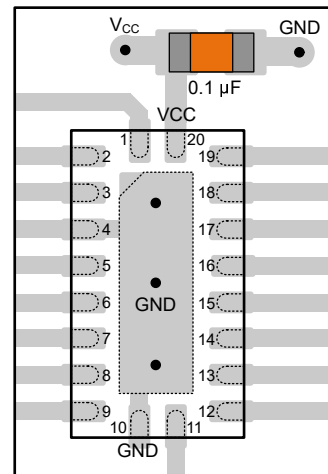


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

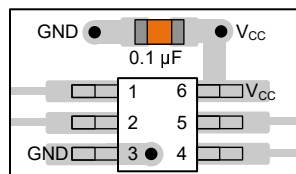


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

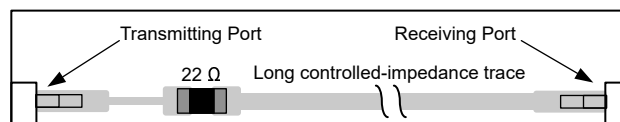


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

ADVANCE INFORMATION

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

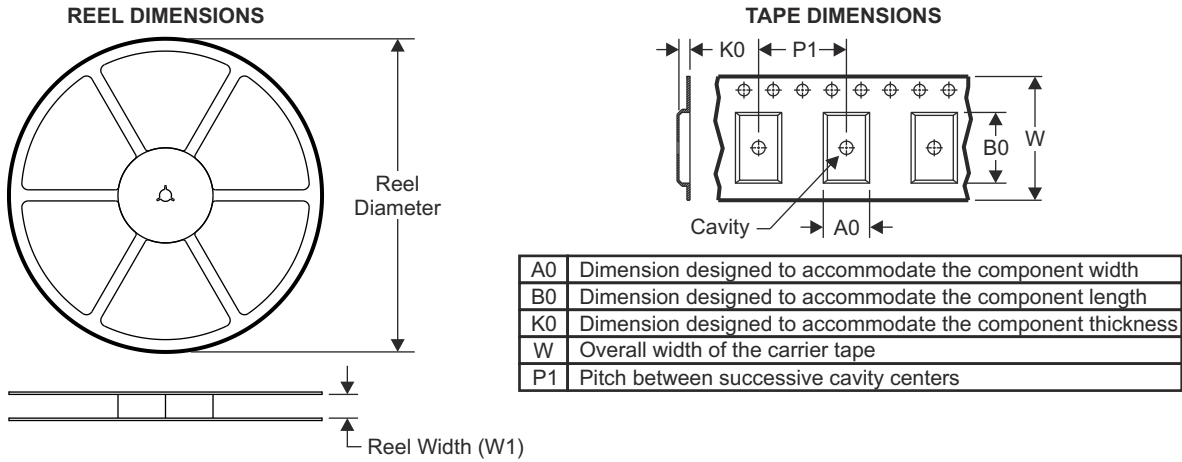
## 10 Revision History

DATE	REVISION	NOTES
September 2024	*	Advance Information Release

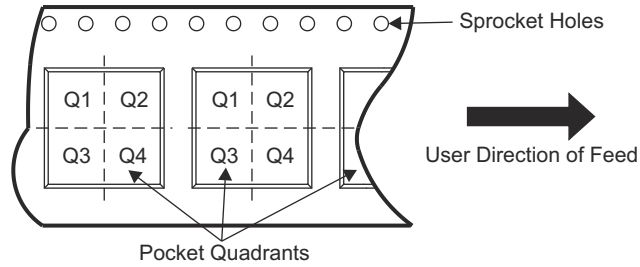
## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 11.1 Tape and Reel Information



#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



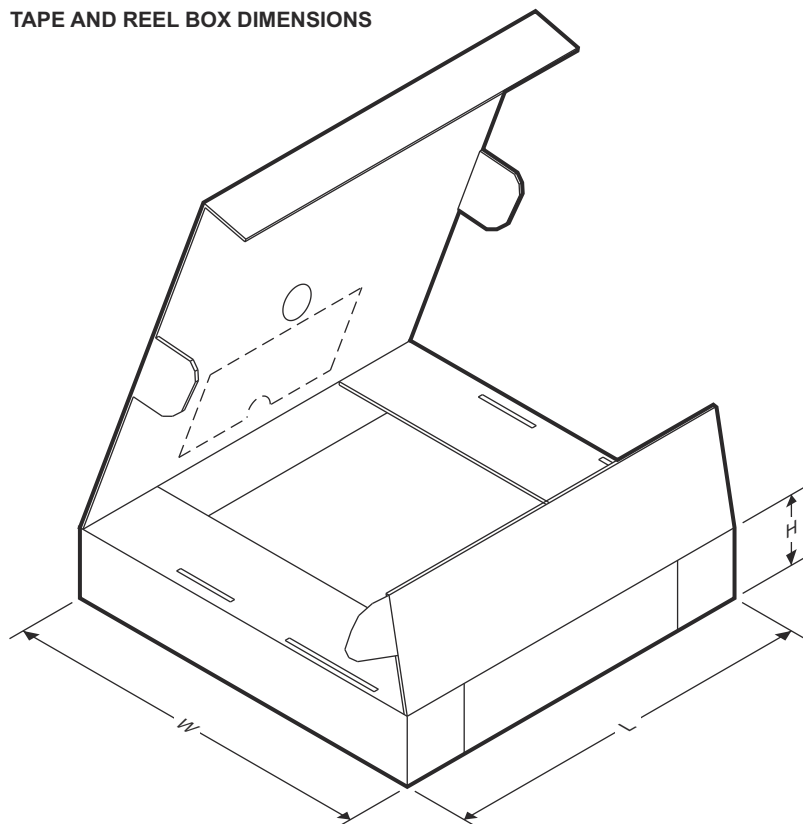
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC165BQBR	WQFN	BQB	16	SPQ	180mm	12.4mm	2.8mm	3.8mm	1.2mm	P1	W	Q1

**ADVANCE INFORMATION**

**SN74AC2G100**

SCASE16 – SEPTEMBER 2024

**TAPE AND REEL BOX DIMENSIONS**



**ADVANCE INFORMATION**

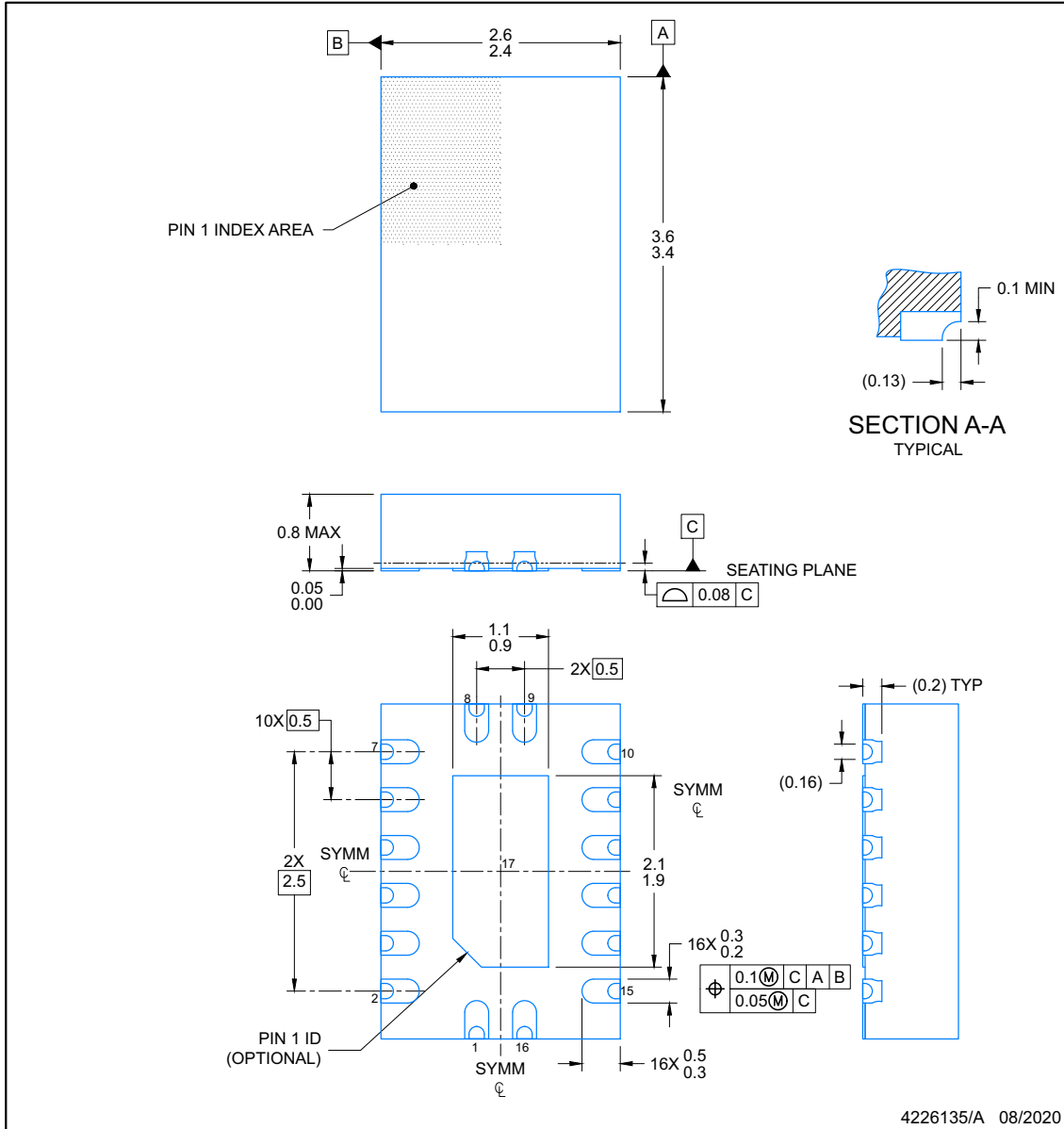
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC165BQBR	WQFN	BQB	16	SPQ	210mm	185mm	35mm

11.2 Mechanical Data

**PACKAGE OUTLINE**  
**WQFN - 0.8 mm max height**

**BQB0016B**

INDSTNAME



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

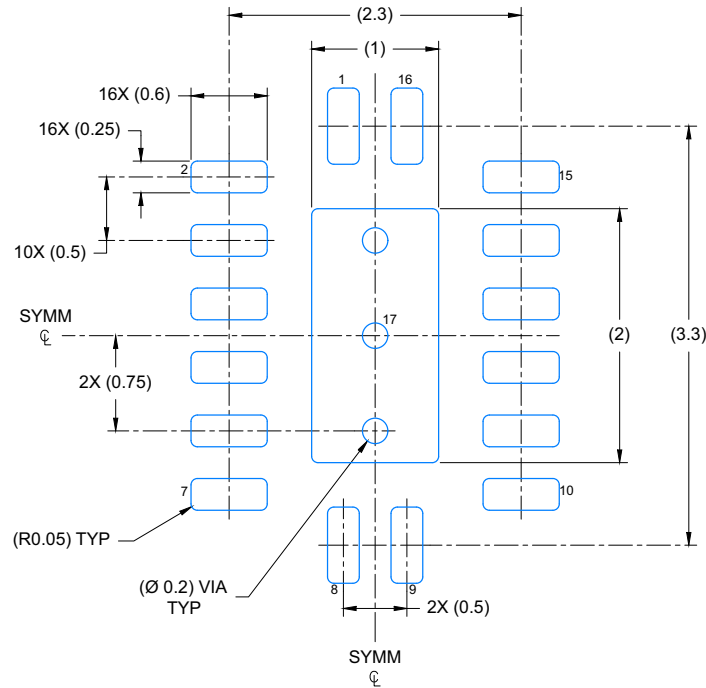
ADVANCE INFORMATION

## EXAMPLE BOARD LAYOUT

**BQB0016B**

**WQFN - 0.8 mm max height**

INDSTNAME



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

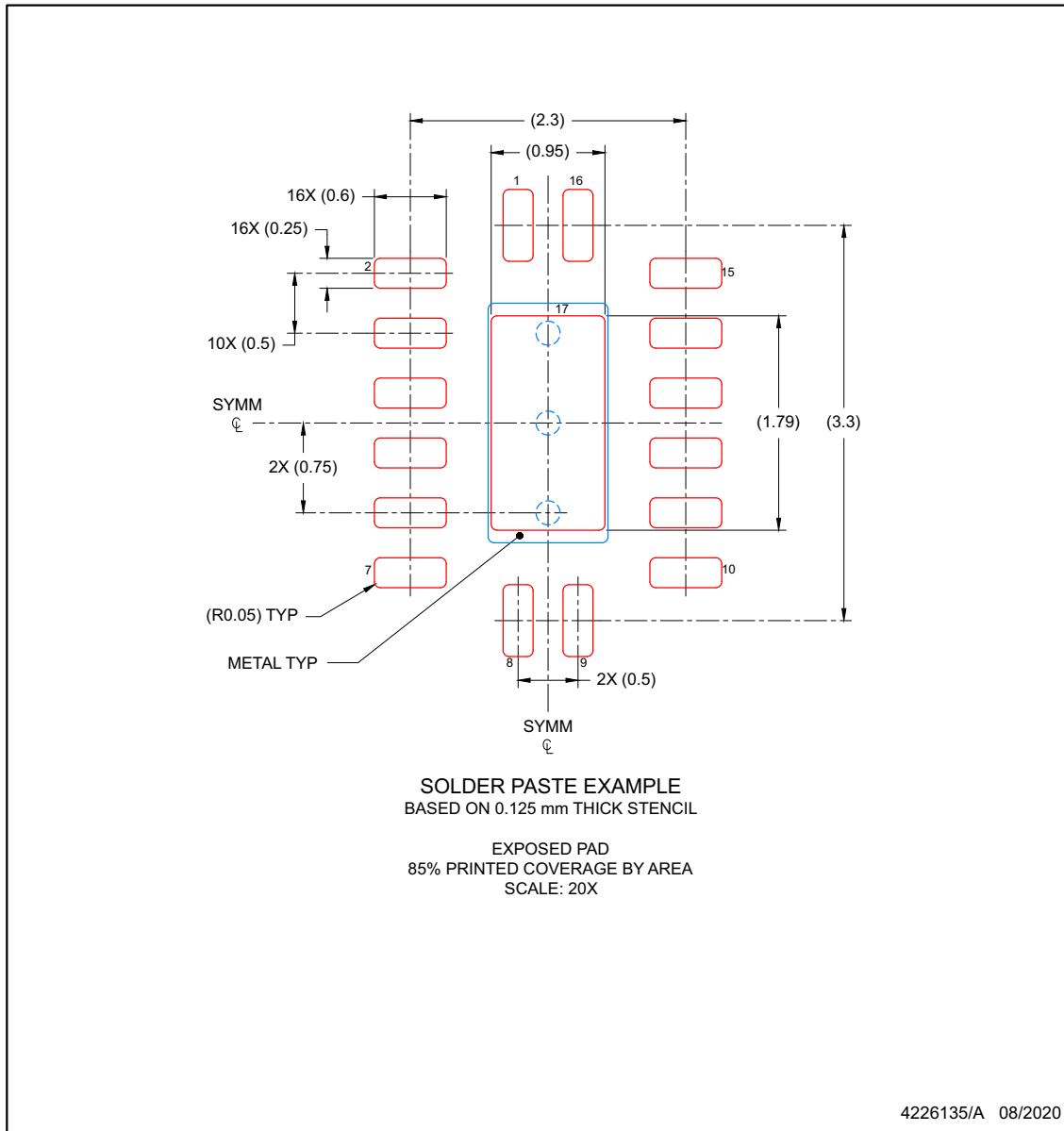


**EXAMPLE STENCIL DESIGN**

**BQB0016B**

**WQFN - 0.8 mm max height**

INDSTNAME



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**ADVANCE INFORMATION**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PSN74AC2G100BQBR	ACTIVE	WQFN	BQB	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## GENERIC PACKAGE VIEW

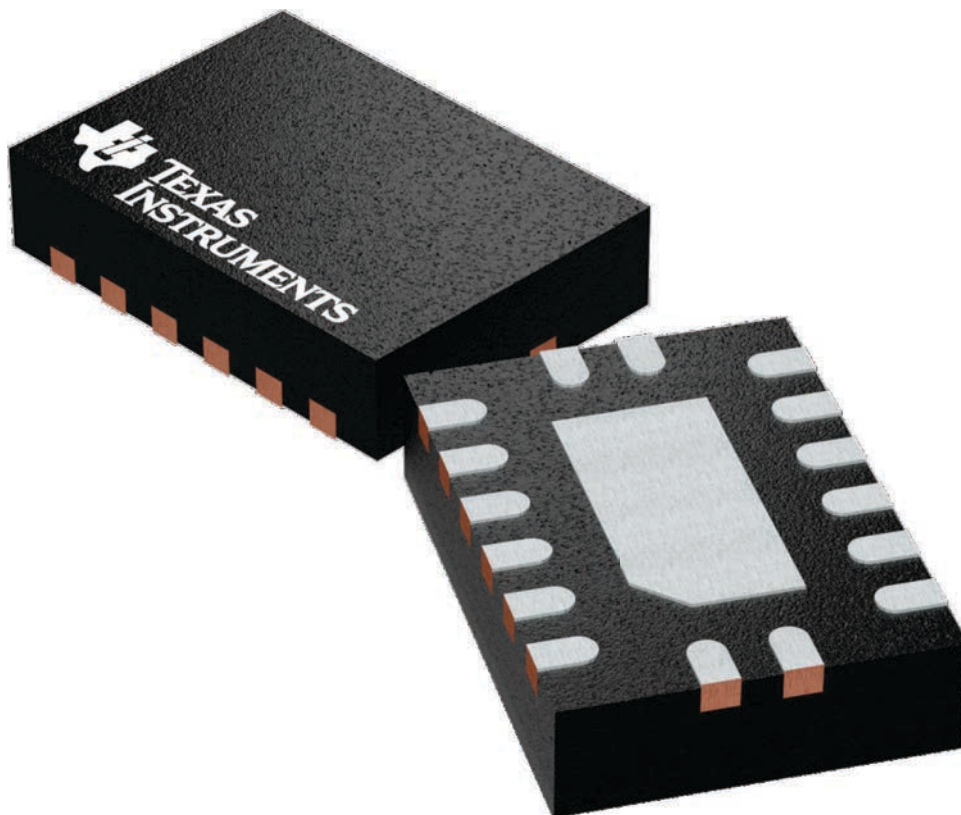
**BQB 16**

**WQFN - 0.8 mm max height**

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226161/A

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated