

SN74AHC595-Q1 Automotive 8-Bit Shift Register With 3-State Output Registers

1 Features

- Qualified for automotive applications
- Operating range 2V to 5.5V V_{CC}
- 8-bit serial-in, parallel-out shift
- Shift register has direct clear

2 Applications

- [Enable or disable a digital signal](#)
- [Controlling an indicator LED](#)
- [Translation between communication modules and system controllers](#)

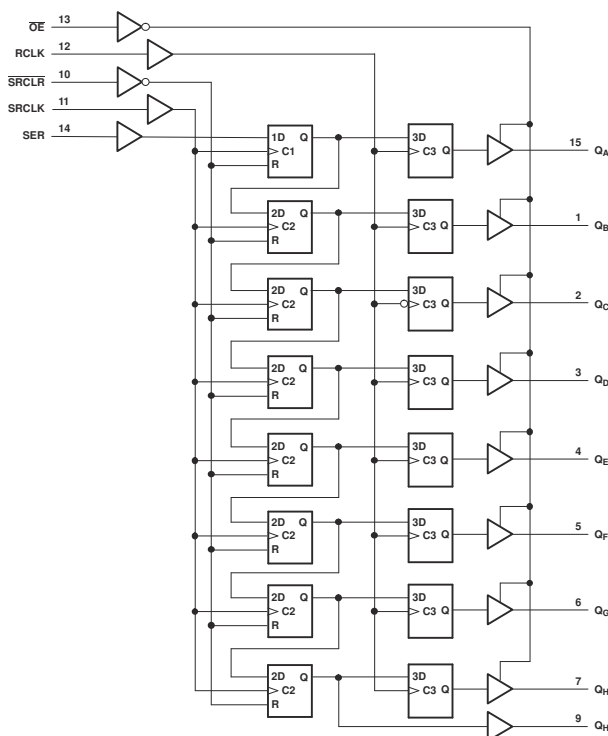
3 Description

The SN74AHC595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74AHC595-Q1	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	PW (TSSOP, 16)	5.00mm × 6.40mm	5.00mm × 4.4mm

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

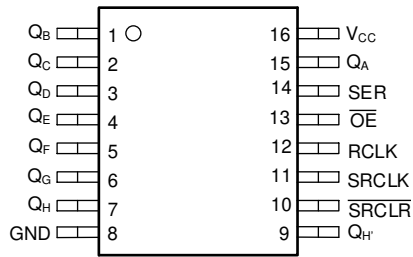


Figure 4-1. PW Package, 16-PIN TSSOP (Top View)

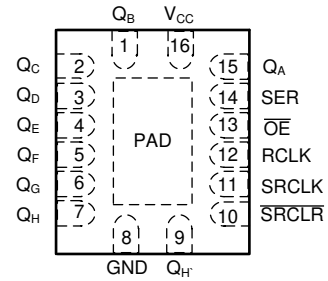


Figure 4-2. BQB Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
Q _B	1	O	Q _B Output
Q _C	2	O	Q _C Output
Q _D	3	O	Q _D Output
Q _E	4	O	Q _E Output
Q _F	5	O	Q _F Output
Q _G	6	O	Q _G Output
Q _H	7	O	Q _H Output
GND	8	G	Ground Pin
Q _H '	9	O	Q _H ' Output
SRCLR	10	I	SRCLR Input
SRCLK	11	I	SRCLK Input
RCLK	12	I	RCLK Input
OE	13	I	Output Enable Pin. Active LOW
SER	14	I	SER Input
Q _A	15	O	Q _A Output
V _{CC}	16	P	Power Pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)	-20 mA	mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})	±20 mA	mA
I _O	Continuous output current	(V _O = 0 to V _{CC})	±25 mA	mA
	Continuous current through V _{CC} or GND		±75 mA	mA
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 3 V	2.1	
		V _{CC} = 5.5 V	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 3 V	0.9	
		V _{CC} = 5.5 V	1.65	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	μA
		V _{CC} = 3.3 V ± 0.3 V	-4	
		V _{CC} = 5 V ± 0.5 V	-8	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 3.3 V ± 0.3 V	4	
		V _{CC} = 5 V ± 0.5 V	8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	ns/V
		V _{CC} = 5 V ± 0.5 V	20	
T _A	Operating free-air temperature	I-suffix devices	-40	85
		Q-suffix devices	-40	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾	BQB (WQFN)	PW (TSSOP)	UNIT	
	16 PINS	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	91.8	135.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9	V	
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1	0.1	V	
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36	0.44		
	I _{OL} = 8 mA	4.5 V			0.36	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1	±1	μA	
I _{OZ}	Q _A -Q _H , V _I = V _{CC} or GND, V _O = V _{CC} or GND, \overline{OE} = V _{IH} or V _{IL}	5.5 V			±0.25	±10	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4	40	μA	
C _i	V _I = V _{CC} or GND	5 V		3	10	10	pF	
C _o	V _O = V _{CC} or GND	5 V		5.5			pF	

5.5 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

V_{CC} = 3.3 V ± 0.3 V, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration	SRCLK high or low	5.5		6.5	ns
		RCLK high or low	5.5		6.5	
		SRCLR low	5		6	
t _{su}	Setup time	SER before SRCLK↑	3.5		4.5	ns
		SRCLK↑ before RCLK↑ ⁽¹⁾	8		9.5	
		SRCLR low before RCLK↑	8		10	
		SRCLR high (inactive) before SRCLK↑	3		4	
t _h	Hold time	SER after SRCLK↑	1.5		2.5	ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.6 Timing Requirements, V_{CC} = 5 V ± 0.5 V

V_{CC} = 5 V ± 0.5 V, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration	SRCLK high or low	5		6	ns
		RCLK high or low	5		6	
		SRCLR low	5.2		6.2	

SN74AHC595-Q1

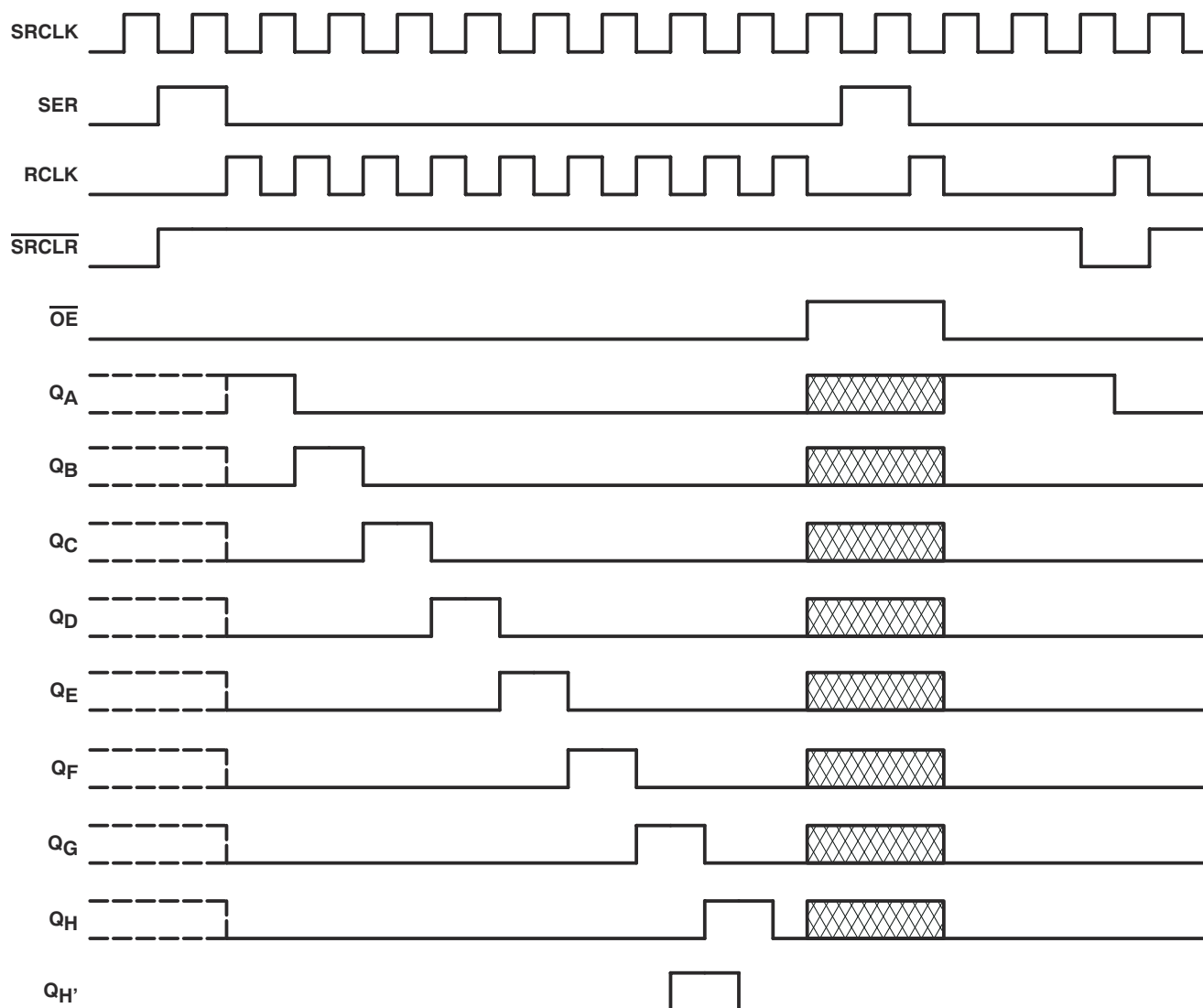
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 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
t_{su}	Setup time	SER before SRCLK \uparrow	3	4	ns	
		SRCLK \uparrow before RCLK \uparrow ⁽¹⁾	5	6		
		SRCLR low before RCLK \uparrow	5	6		
		SRCLR high (inactive) before SRCLK \uparrow	2.5	3.5		
t_h	Hold time	SER after SRCLK \uparrow	2	3	ns	

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.7 Timing Diagrams



NOTE:  implies that the output is in 3-State mode.

5.8 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

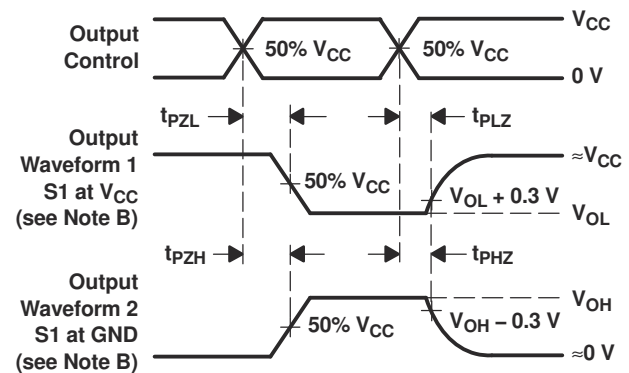
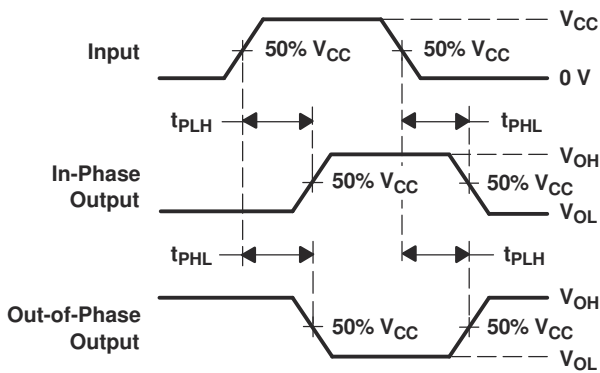
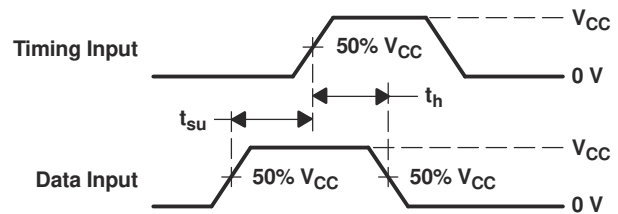
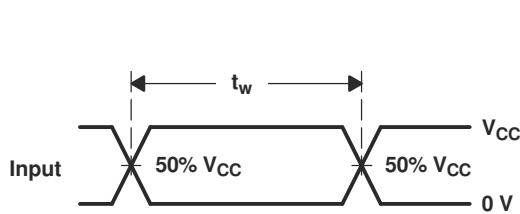
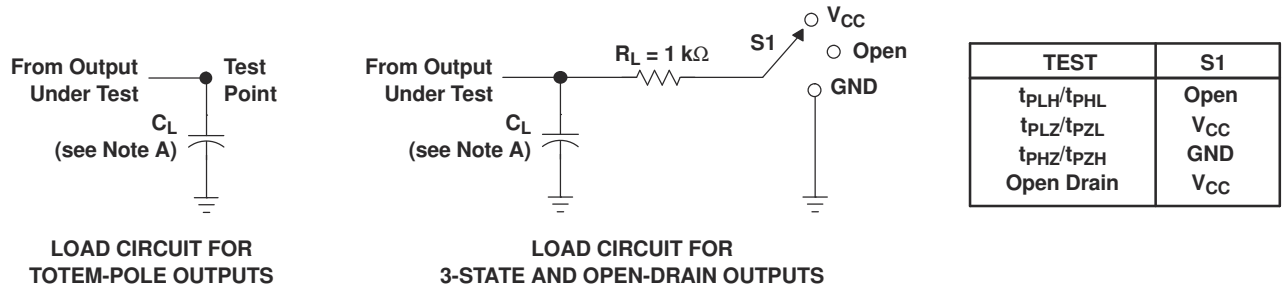
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{\max}			$C_L = 50\text{ pF}$	55	105		40		MHz
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 50\text{ pF}$		7.9	15.4	1	20	ns
t_{PHL}					7.9	15.4	1	20	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$		9.2	16.5	1	21.5	ns
t_{PHL}					9.2	16.5	1	21.5	
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$		9	16.3	1	20.2	ns
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H	$C_L = 50\text{ pF}$		7.8	15	1	20	ns
t_{PZL}					9.6	15	1	20	
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H	$C_L = 50\text{ pF}$		8.1	15.7	1	19.2	ns
t_{PLZ}					9.3	15.7	1	19.2	

5.9 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{\max}			$C_L = 50\text{ pF}$	95	140		75		MHz
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 50\text{ pF}$		5.6	9.4	1	13.5	ns
t_{PHL}					5.6	9.4	1	13.5	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$		6.4	10.2	1	14.4	ns
t_{PHL}					6.4	10.2	1	14.4	
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$		6.4	10	1	14.1	ns
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H	$C_L = 50\text{ pF}$		5.7	10.6	1	15	ns
t_{PZL}					6.8	10.6	1	15	
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H	$C_L = 50\text{ pF}$		3.5	10.3	1	14	ns
t_{PLZ}					3.4	10.3	1	14	

6 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time, with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AHC595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers.

The shift register has a direct overriding clear ($\overline{\text{SRCLR}}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{\text{OE}}$) input is high, all outputs, except Q_H , are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

7.2 Functional Block Diagram

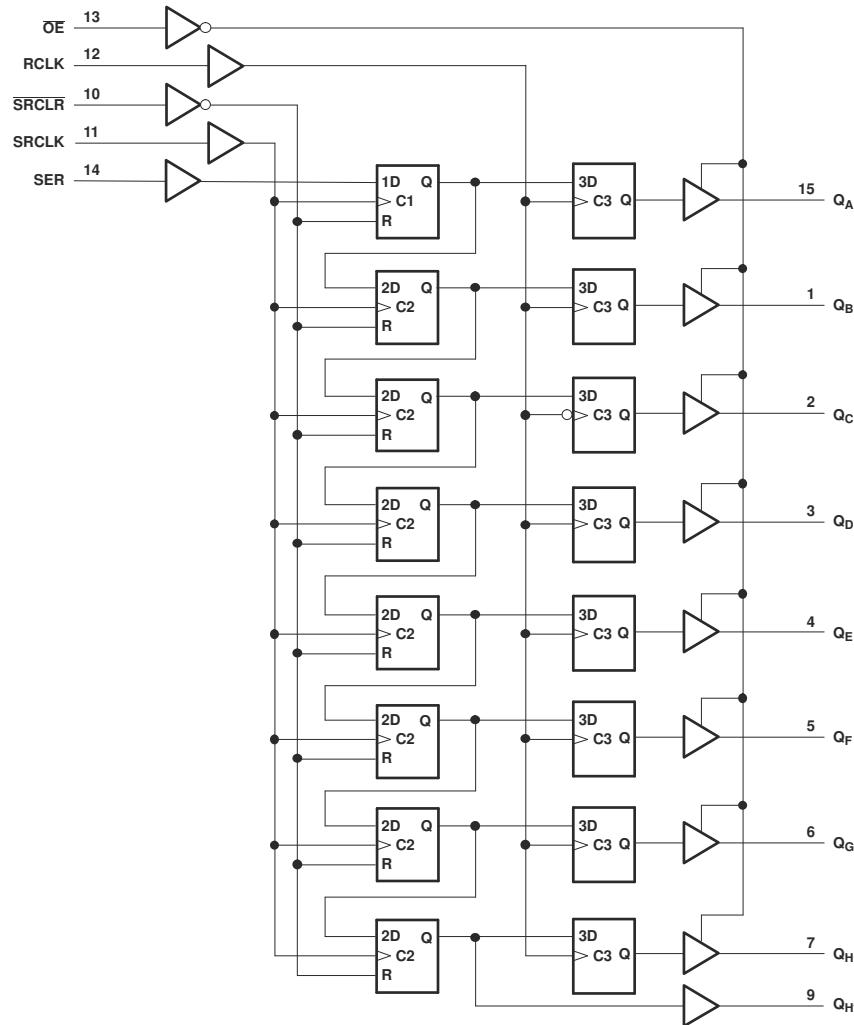


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

Table 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	\overline{OE}	
X	X	X	X	H	Outputs Q _A –Q _H are disabled.
X	X	X	X	L	Outputs Q _A –Q _H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored into the storage register.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.2.2 Layout Example

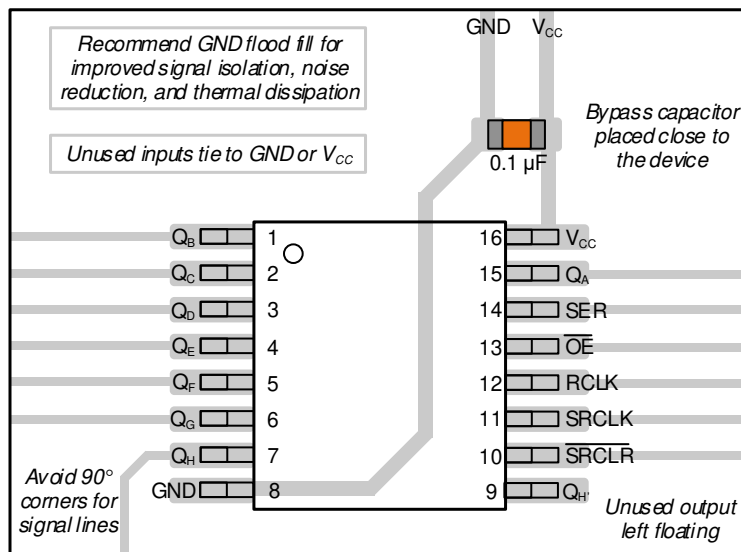


Figure 8-1. Example Layout for the SN74AHC595-Q1

9 Device and Documentation Support

9.1 Document Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC595-Q1	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2024) to Revision E (April 2024)	Page
• Updated thermal values for PW package from RθJA = 108 to 135.9, all values in °C/W	4

Changes from Revision C (November 2023) to Revision D (March 2024)	Page
• Added BQB package to <i>Package Information</i> table, <i>Pin Configuration and Functions</i> section, and <i>Thermal Information</i> table.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC595QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595Q	Samples
SN74AHC595QWBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH595Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC595-Q1 :

- Catalog : [SN74AHC595](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC595QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC595QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC595QWBQRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC595QPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHC595QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHC595QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0



4220204/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

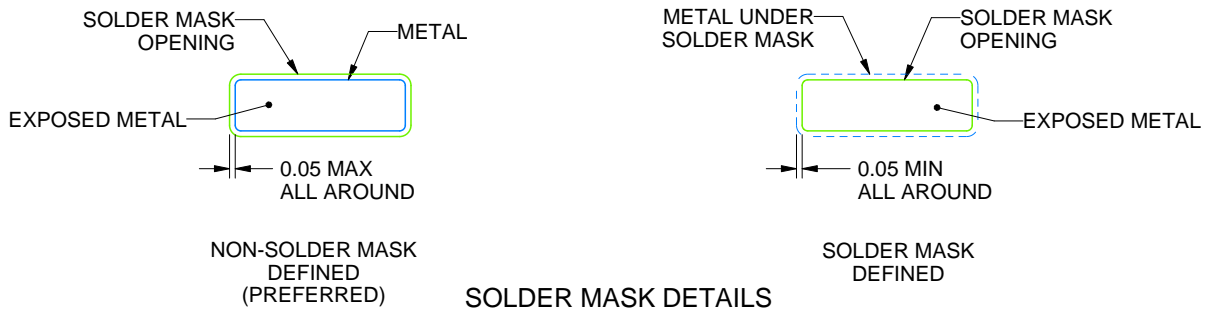
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

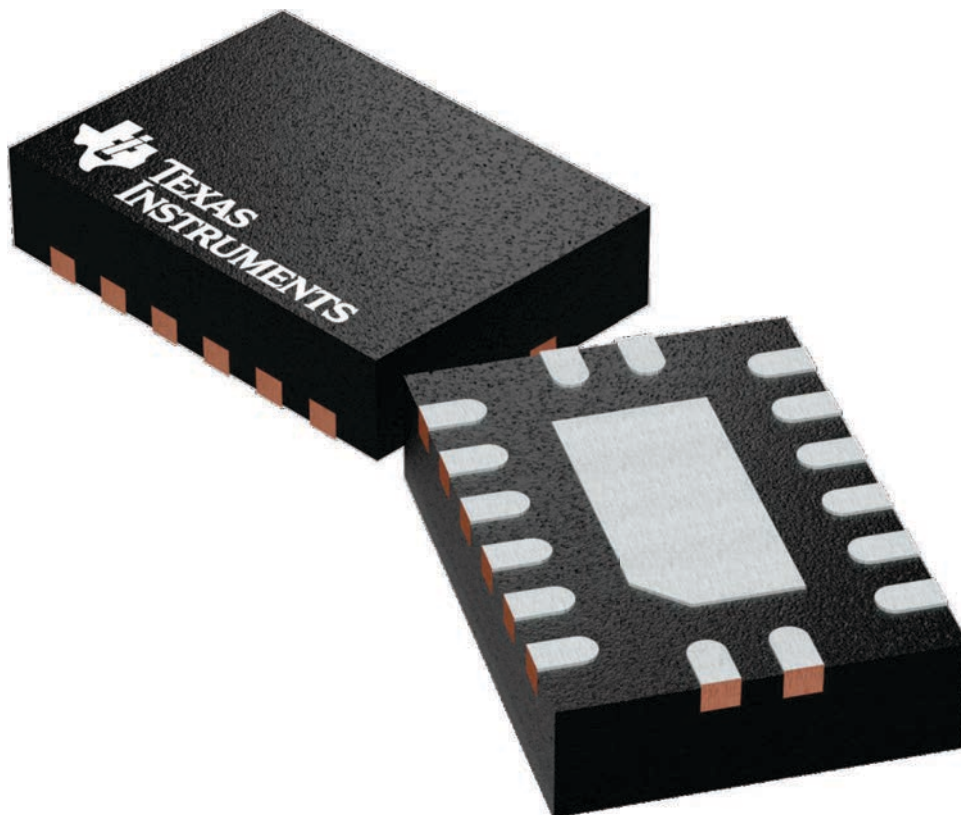
BQB 16

WQFN - 0.8 mm max height

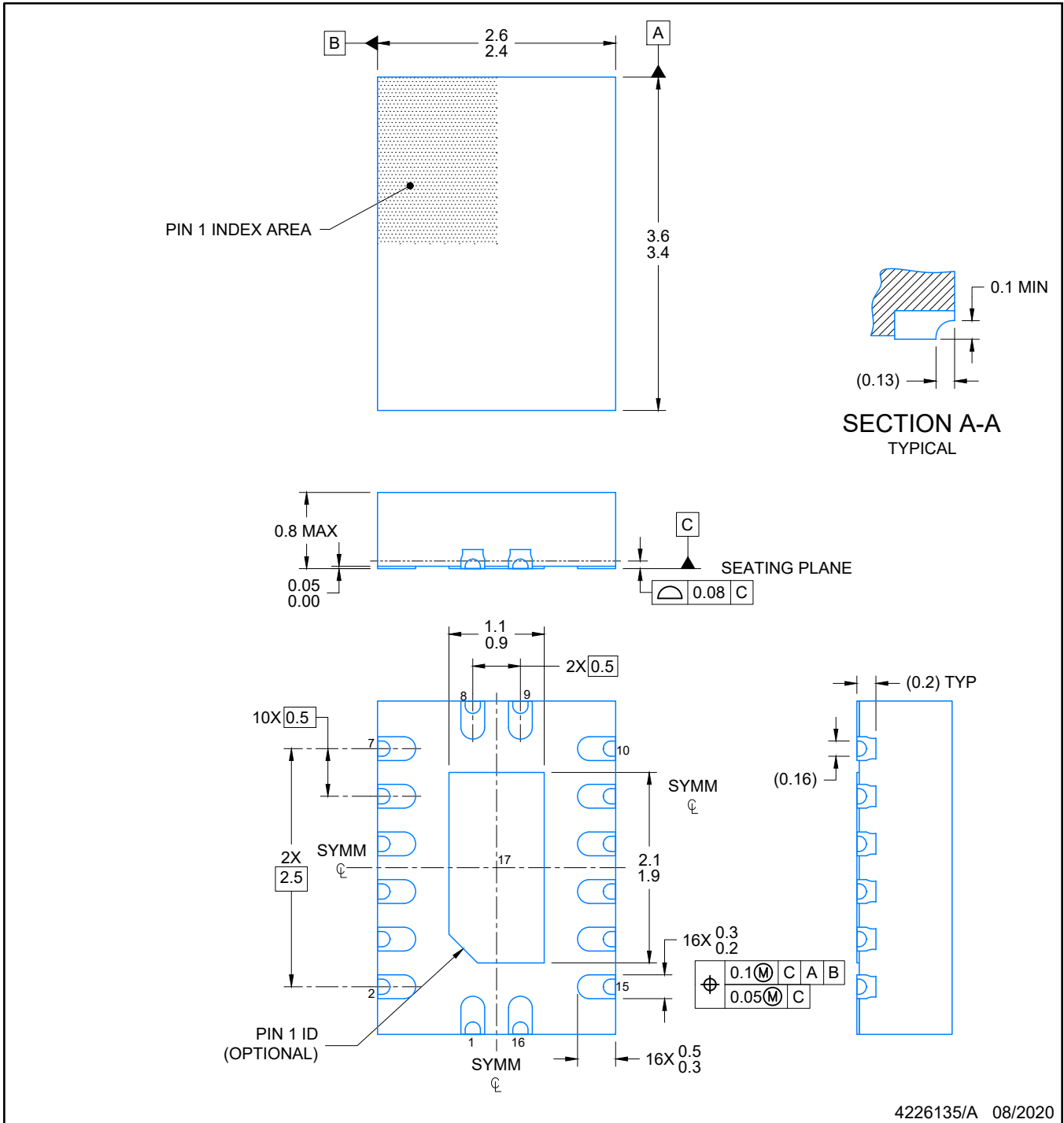
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



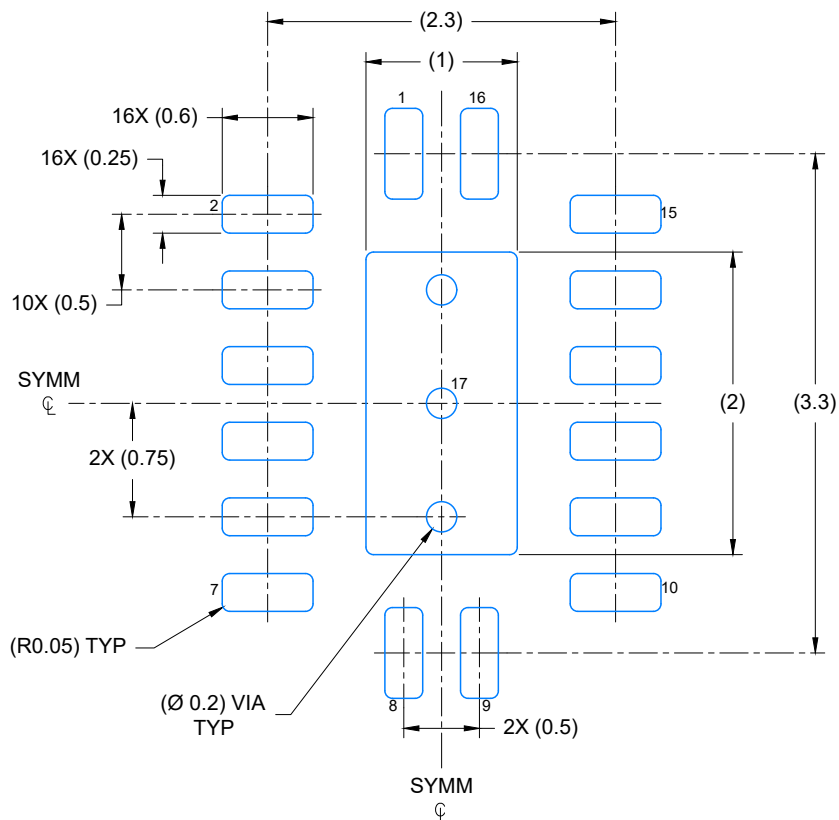
4226161/A



4226135/A 08/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

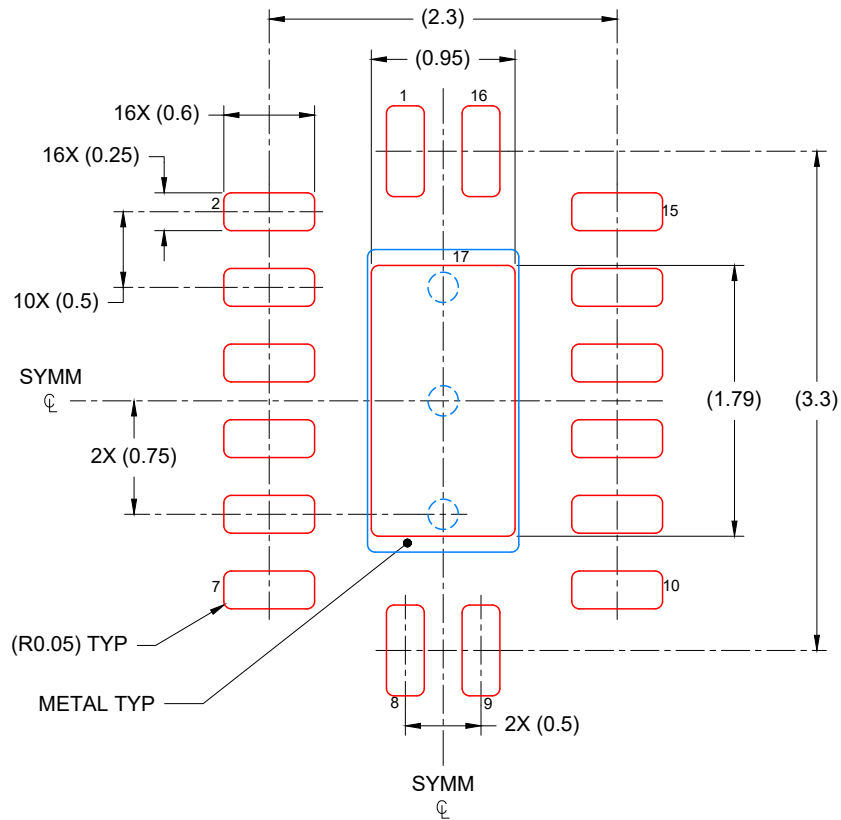


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 85% PRINTED COVERAGE BY AREA
 SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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