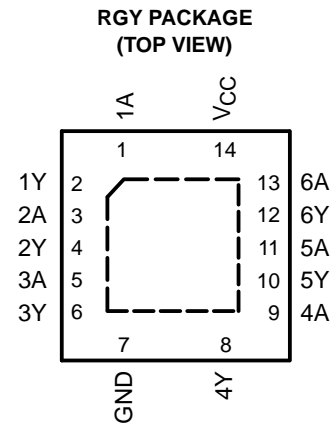


FEATURES

- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 2.2 ns at 1.8 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This hex buffer/driver is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The outputs of the SN74AUC07 are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

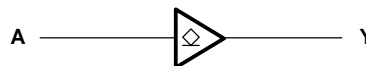
T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AUC07RGYR	MS07

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH BUFFER/DRIVER)

INPUT A	OUTPUT Y
H	H
L	L

LOGIC DIAGRAM, EACH BUFFER/DRIVER (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74AUC07

HEX BUFFER/DRIVER

WITH OPEN-DRAIN OUTPUT

SCES472–AUGUST 2003–REVISED NOVEMBER 2005

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	3.6	V
V_I	Input voltage range ⁽²⁾	-0.5	3.6	V
V_O	Output voltage range ⁽²⁾	-0.5	3.6	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		±20	mA
	Continuous current through V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance ⁽³⁾		47	°C/W
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	2.7	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8$ V	V_{CC}	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	1.7	
V_{IL}	Low-level input voltage	$V_{CC} = 0.8$ V	0	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	3.6	V
I_{OL}	Low-level output current	$V_{CC} = 0.8$ V	0.7	mA
		$V_{CC} = 1.1$ V	3	
		$V_{CC} = 1.4$ V	5	
		$V_{CC} = 1.65$ V	8	
		$V_{CC} = 2.3$ V	9	
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OL}		I _{OL} = 100 μA	0.8 V to 2.7 V			0.2	V
		I _{OL} = 0.7 mA	0.8 V		0.25		
		I _{OL} = 3 mA	1.1 V			0.3	
		I _{OL} = 5 mA	1.4 V			0.4	
		I _{OL} = 8 mA	1.65 V			0.45	
		I _{OL} = 9 mA	2.3 V			0.6	
I _I	A inputs	V _I = V _{CC} or GND	0 to 2.7 V			±5	μA
I _{off}		V _I or V _O = 2.7 V	0			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V			10	μA
C _i		V _I = V _{CC} or GND	2.5 V		2.5		pF

(1) All typical values are at T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	4.5	0.9	3.5	0.7	2.8	0.6	1.4	2.8	0.6	2.3	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 1)

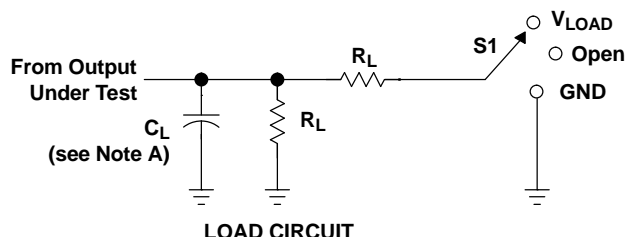
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	0.8	1.4	2.3	0.2	1.3	ns

Operating Characteristics

T_A = 25°C

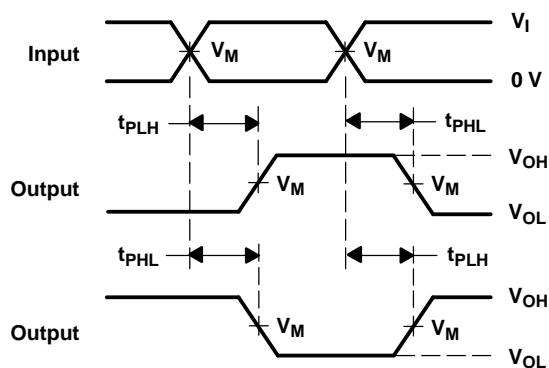
PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT
		TYP	TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance f = 10 MHz	2	2	2	3	3	pF

PARAMETER MEASUREMENT INFORMATION
 (Open Drain)

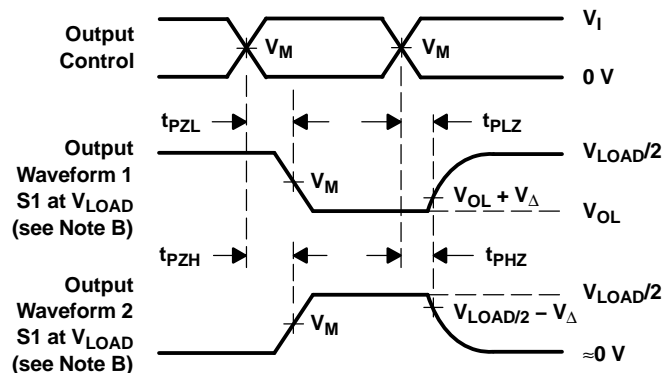


TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
0.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
1.2 V \pm 0.1 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.15 V
1.8 V \pm 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 - t_{PZL} is measured at V_M .
 - t_{PLZ} is measured at $V_{OL} + V_{\Delta}$.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUC07RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MS07	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC07RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC07RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

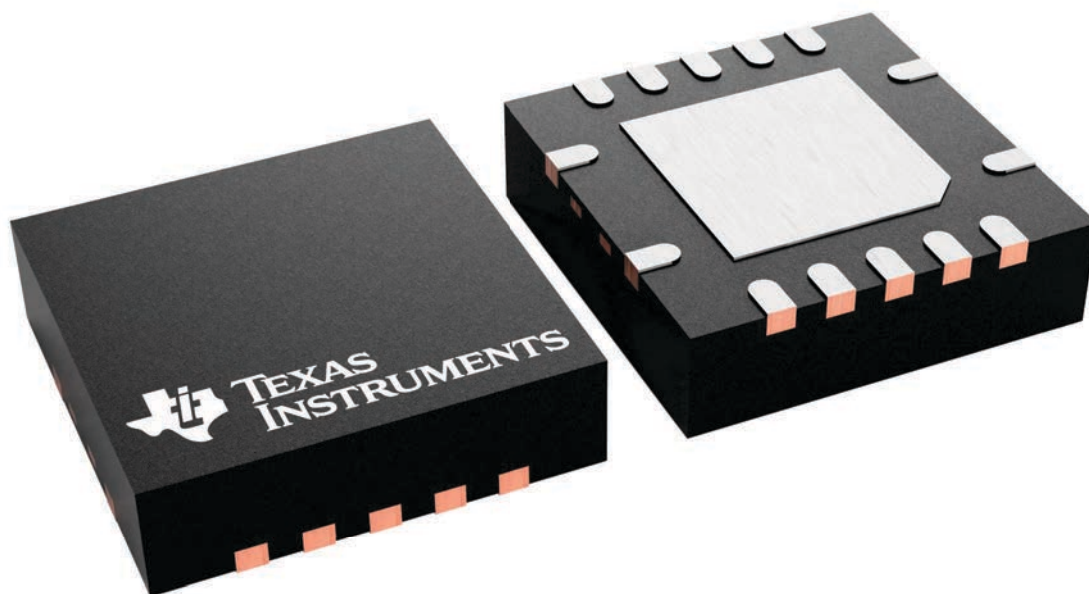
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

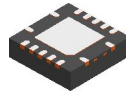
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

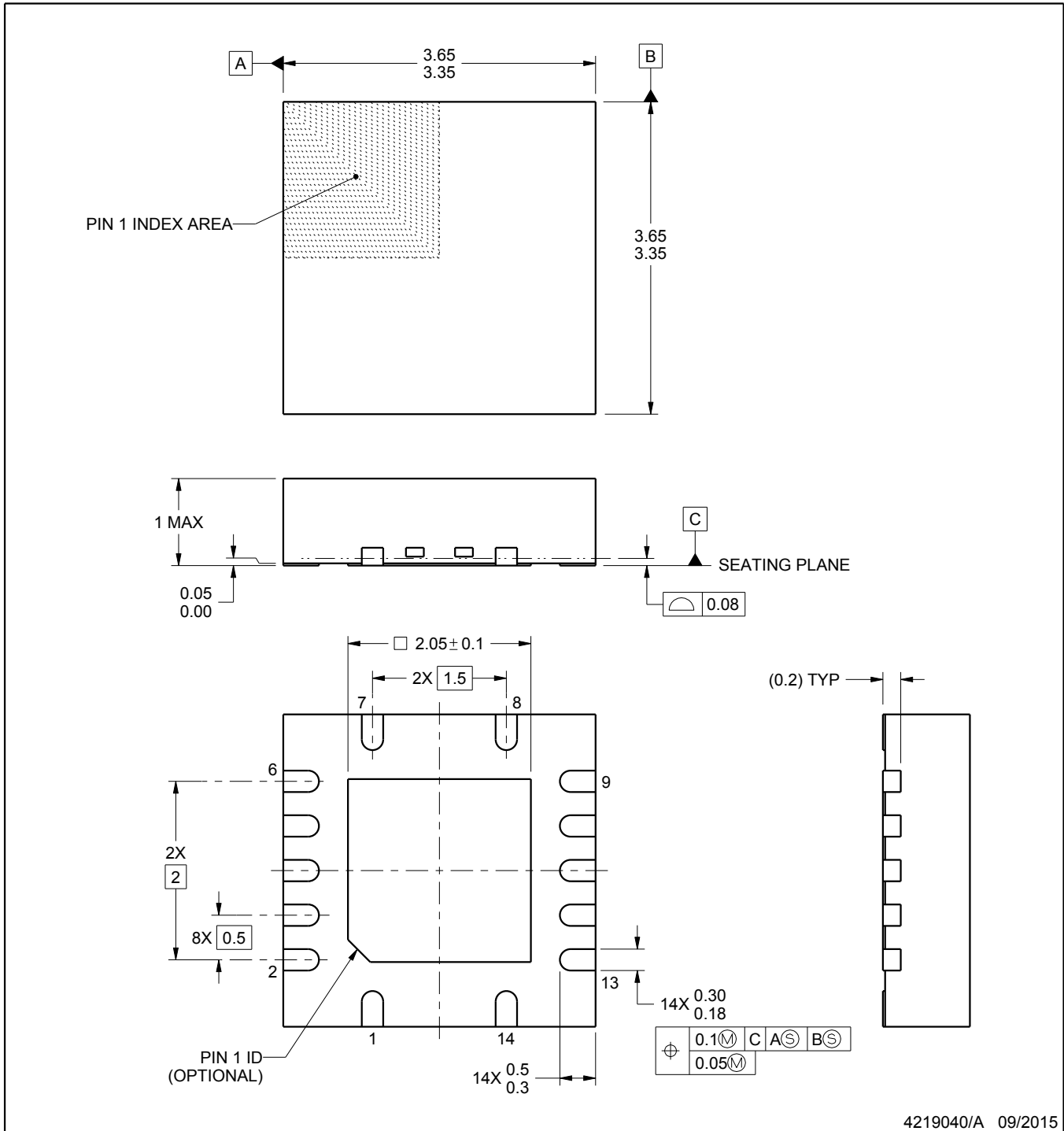
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES:

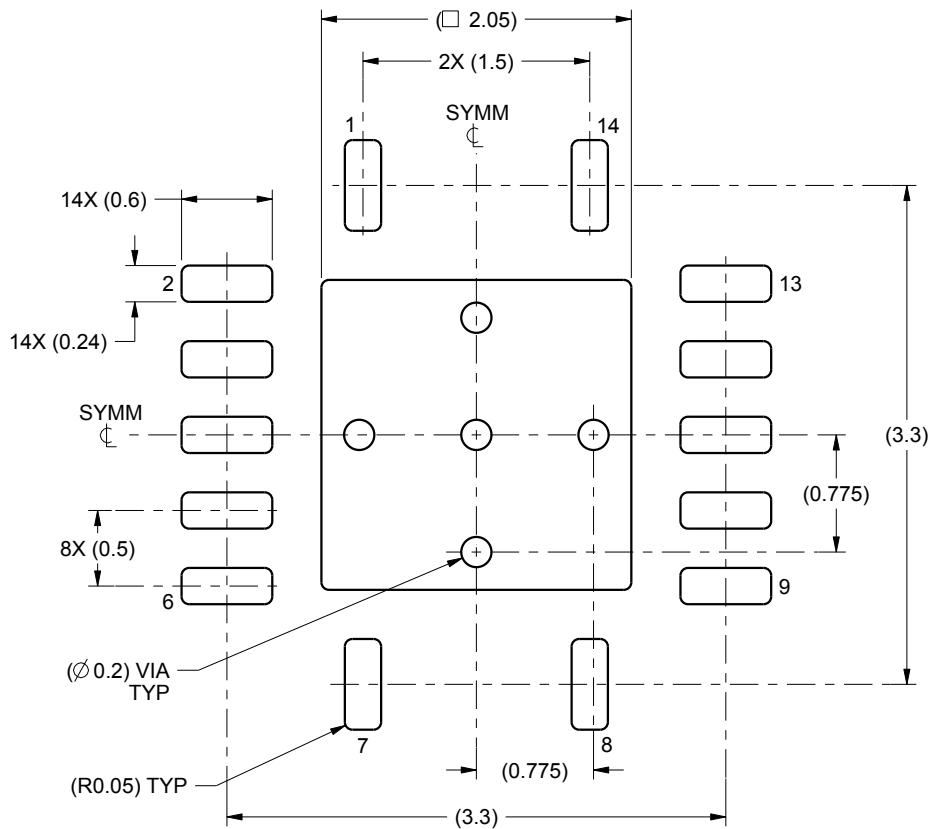
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

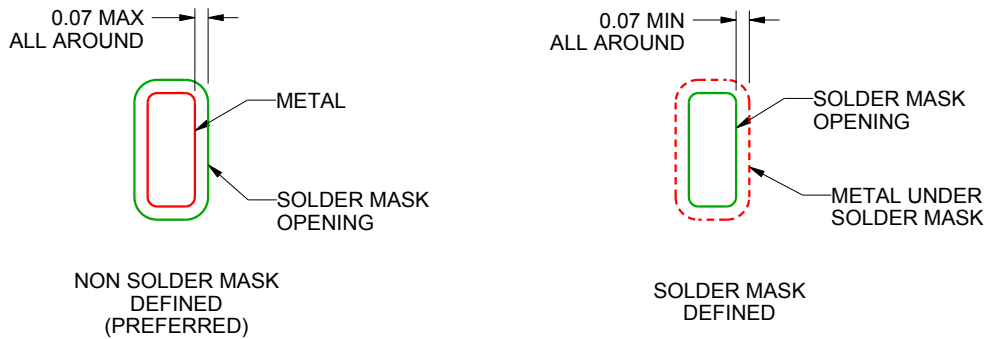
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

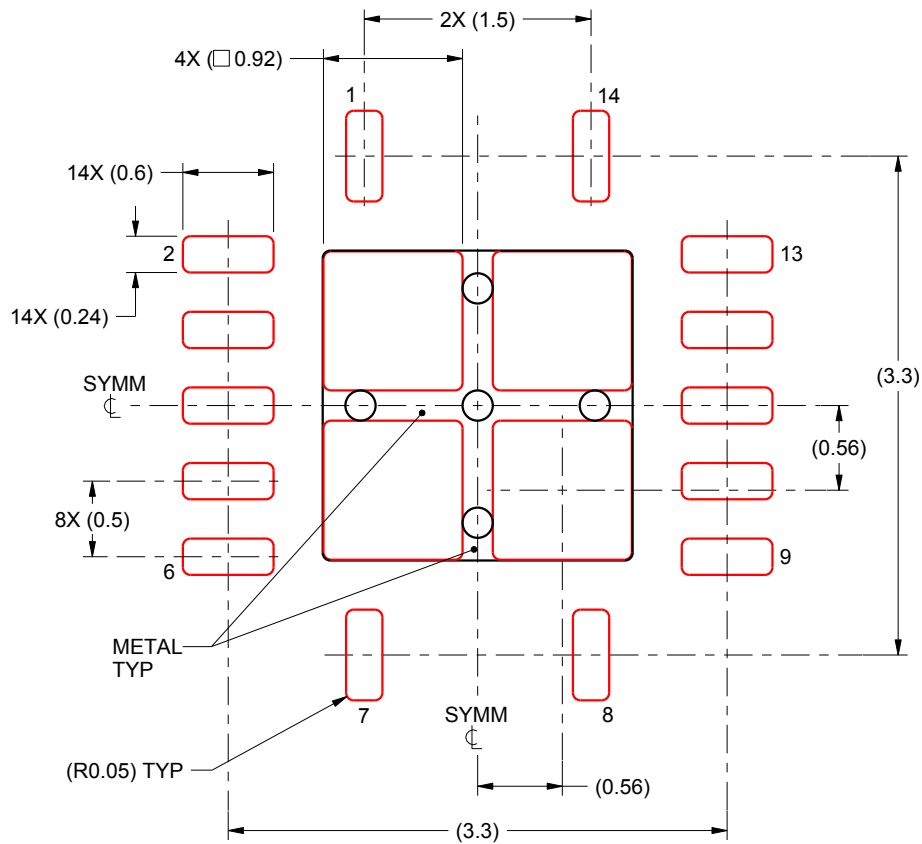
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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