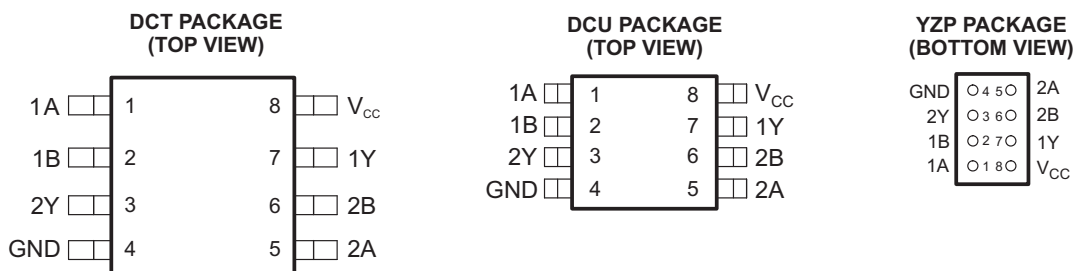


## FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max  $t_{pd}$  of 1.7 ns at 1.8 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

This dual 2-input exclusive-OR gate is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC2G86 performs the Boolean function  $Y = A \oplus B$  or  $Y = \bar{A}B + A\bar{B}$  in positive logic.

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G86YZPR	__ _UH_
	SSOP – DCT	Reel of 3000	SN74AUC2G86DCTR	U86_ _ _
	VSSOP – DCU	Reel of 3000	SN74AUC2G86DCUR	U86_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.  
DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

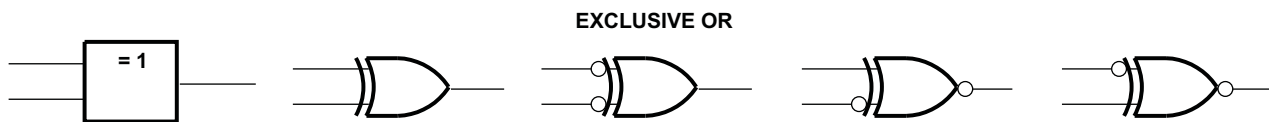
NanoFree is a trademark of Texas Instruments.

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

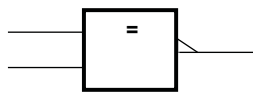
## EXCLUSIVE-OR LOGIC

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



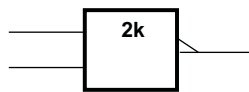
These are five equivalent exclusive-OR symbols valid for an SN74AUC2G86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



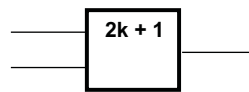
The output is active (low) if all inputs stand at the same logic level (i.e.,  $A = B$ ).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	3.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	3.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	3.6	V
$V_O$	Output voltage range <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		-50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50 mA
$I_O$	Continuous output current			$\pm 20$ mA
	Continuous current through $V_{CC}$ or GND			$\pm 100$ mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DCT package		220
		DCU package		227
		YZP package		102
$T_{stg}$	Storage temperature range	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	0.8	2.7	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.65 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 0.8 V	0	V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.35 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
V <sub>I</sub>	Input voltage	0	3.6	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 0.8 V	–0.7	mA
		V <sub>CC</sub> = 1.1 V	–3	
		V <sub>CC</sub> = 1.4 V	–5	
		V <sub>CC</sub> = 1.65 V	–8	
		V <sub>CC</sub> = 2.3 V	–9	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 0.8 V	0.7	mA
		V <sub>CC</sub> = 1.1 V	3	
		V <sub>CC</sub> = 1.4 V	5	
		V <sub>CC</sub> = 1.65 V	8	
		V <sub>CC</sub> = 2.3 V	9	
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	0.8 V to 2.7 V	V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –0.7 mA	0.8 V		0.55		
	I <sub>OH</sub> = –3 mA	1.1 V		0.8		
	I <sub>OH</sub> = –5 mA	1.4 V		1		
	I <sub>OH</sub> = –8 mA	1.65 V		1.2		
	I <sub>OH</sub> = –9 mA	2.3 V		1.8		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V			0.2	V
	I <sub>OL</sub> = 0.7 mA	0.8 V		0.25		
	I <sub>OL</sub> = 3 mA	1.1 V			0.3	
	I <sub>OL</sub> = 5 mA	1.4 V			0.4	
	I <sub>OL</sub> = 8 mA	1.65 V			0.45	
	I <sub>OL</sub> = 9 mA	2.3 V			0.6	
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	0 to 2.7 V		±5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 2.7 V	0		±10	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	0.8 V to 2.7 V		10	μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V		2.5	pF

(1) All typical values are at T<sub>A</sub> = 25°C.

# SN74AUC2G86

## DUAL 2-INPUT EXCLUSIVE-OR GATE

SCES479B – AUGUST 2003 – REVISED JANUARY 2007

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 15$  pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V $\pm 0.1$ V		$V_{CC} = 1.5$ V $\pm 0.1$ V		$V_{CC} = 1.8$ V $\pm 0.15$ V			$V_{CC} = 2.5$ V $\pm 0.2$ V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	5.3	0.8	3.8	0.5	2.6	0.4	1	1.7	0.3	1.3	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30$  pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V $\pm 0.15$ V			$V_{CC} = 2.5$ V $\pm 0.2$ V		UNIT
			MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8	1.5	2.6	0.7	2	ns

### Operating Characteristics

$T_A = 25^\circ\text{C}$

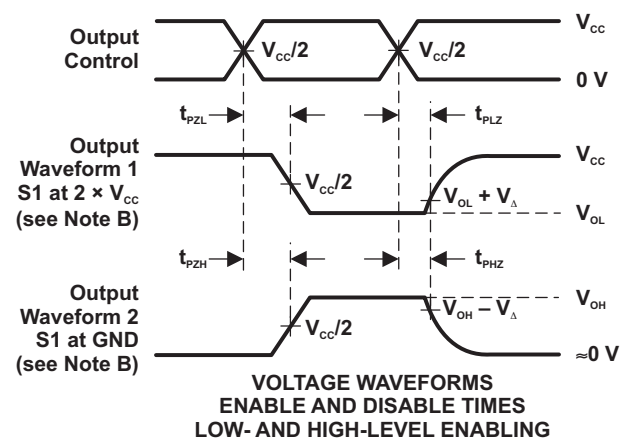
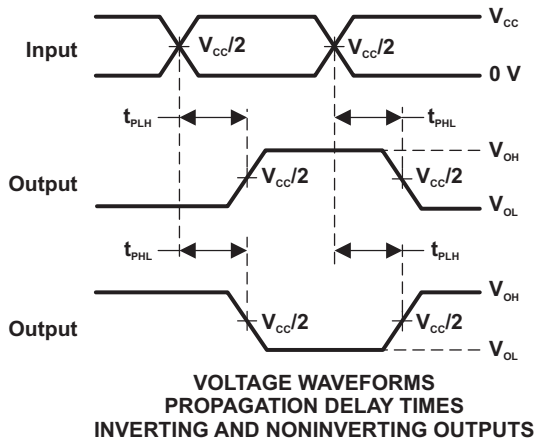
PARAMETER	TEST CONDITIONS	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V	$V_{CC} = 1.5$ V	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	UNIT
		TYP	TYP	TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance	f = 10 MHz	15	15	16	19	27	pF

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PZL}/t_{PZH}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_A$
0.8 V	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
1.8 V $\pm$ 0.15 V	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50 \Omega$ , slew rate  $\geq$  1 V/ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PZL}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUC2G86DCTR	ACTIVE	SSOP	DCT	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(2XF5, U86) (R, Z)	<a href="#">Samples</a>
SN74AUC2G86DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(U86Q, U86R)	<a href="#">Samples</a>
SN74AUC2G86DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U86R	<a href="#">Samples</a>
SN74AUC2G86YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UHN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G86DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC2G86DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G86DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G86DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G86YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G86DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AUC2G86DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G86DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G86DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G86YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

# DCU0008A



# PACKAGE OUTLINE

## VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

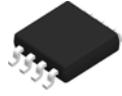


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

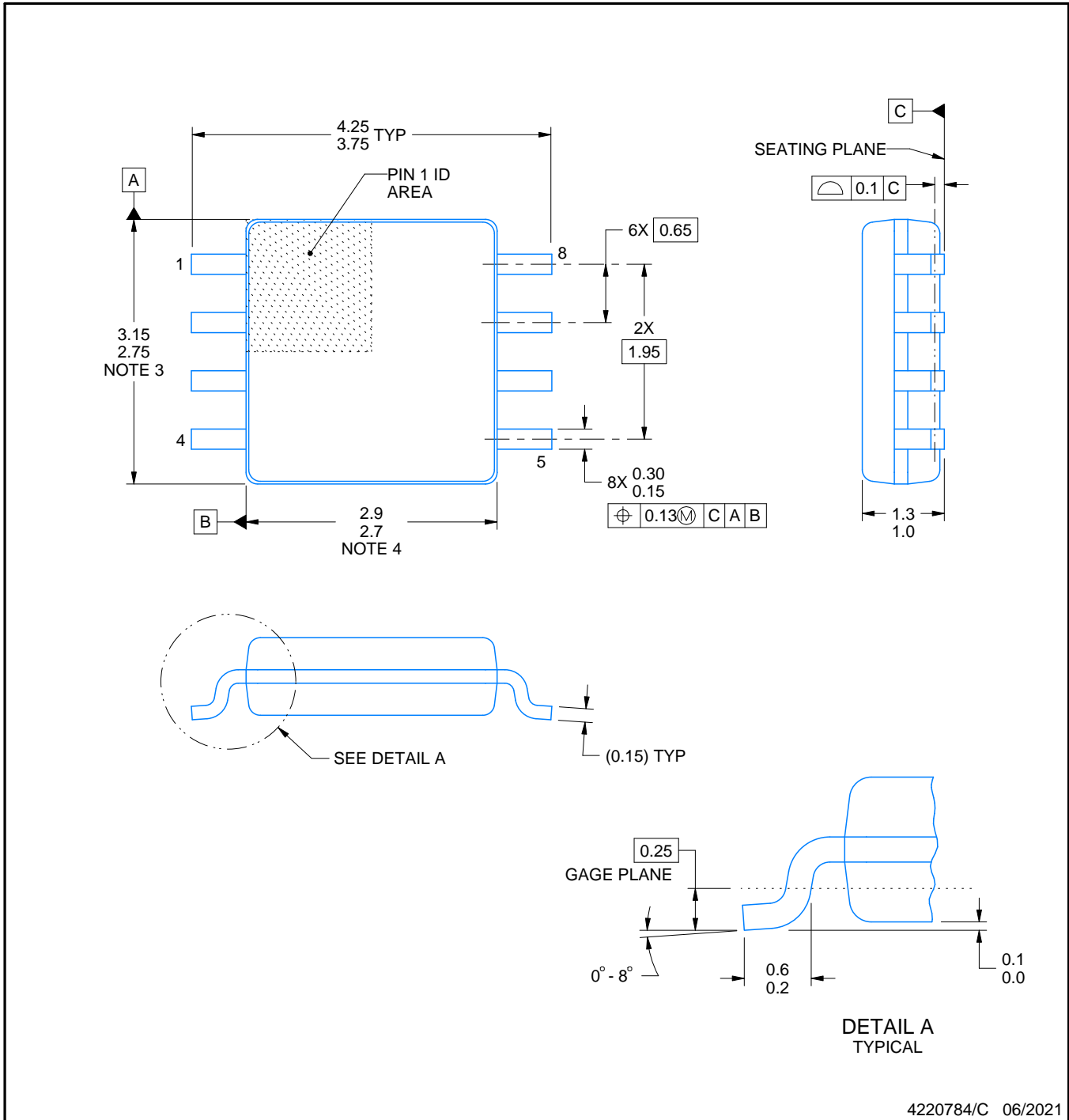


# DCT0008A

# PACKAGE OUTLINE

## SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



4220784/C 06/2021

### NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

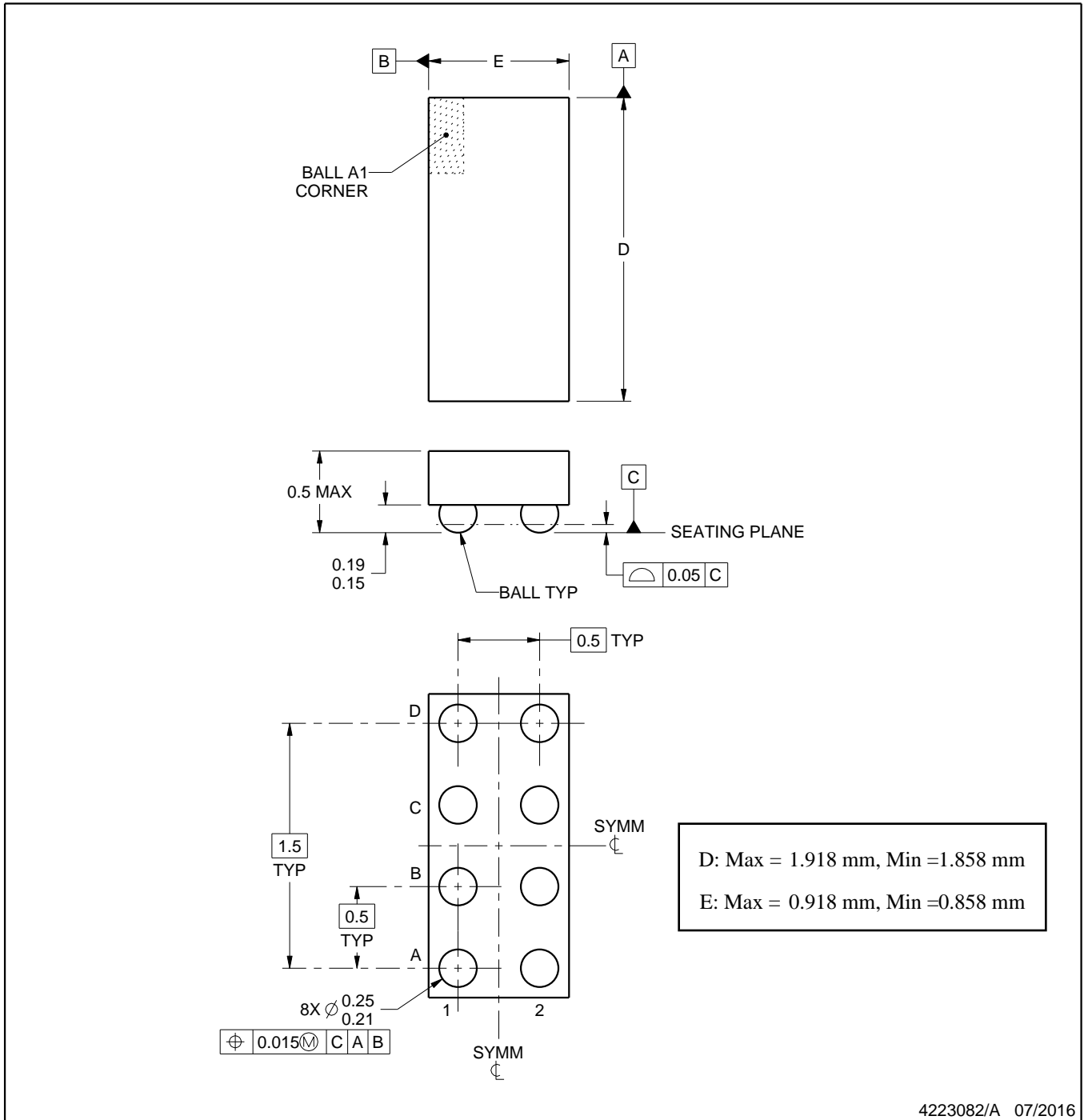
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



# EXAMPLE BOARD LAYOUT

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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