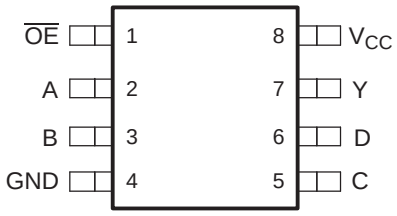
SN74AUP1G99
LOW-POWER ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE WITH 3-STATE OUTPUTS

SCES594C–JULY 2004–REVISED DECEMBER 2007

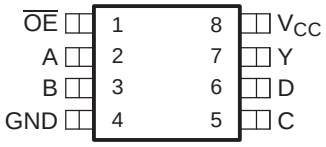
FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Low Static-Power Consumption (I_{CC} = 0.9 μA Max)**
- **Low Dynamic-Power Consumption (C_{pd} = 5 pF Typ at 3.3 V)**
- **Low Input Capacitance (C_I = 1.5 pF)**
- **Low Noise – Overshoot and Undershoot <10% of V_{CC}**
- **Input-Disable Feature Allows Floating Input Conditions**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Includes Schmitt-Trigger Inputs**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**
- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 7.4 ns Max at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

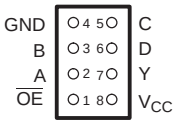
DCT PACKAGE
(TOP VIEW)



DCU PACKAGE
(TOP VIEW)



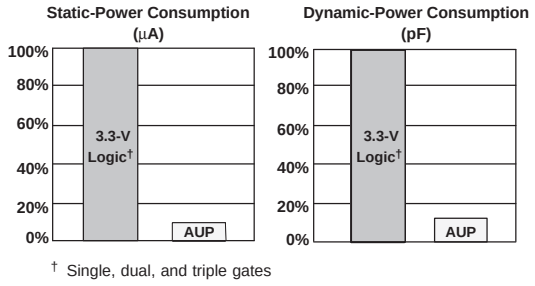
YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.

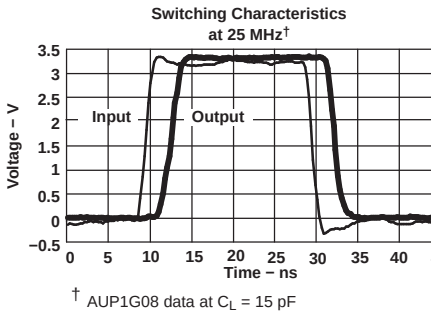
DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figures 1 and 2).



† Single, dual, and triple gates

Figure 1. AUP - The Lowest-Power Family



† AUP1G08 data at C_L = 15 pF

Figure 2. Excellent Signal Integrity

DESCRIPTION/ORDERING INFORMATION

The SN74AUP1G99 features configurable multiple functions with a 3-state output. This device has the input-disable feature, which allows floating input signals. The inputs and output are disabled when the output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the output state is determined by 16 patterns of 4-bit input. The user can choose the logic functions, such as MUX, AND, OR, NAND, NOR, XOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching noise immunity at the input.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	SN74AUP1G99YZPR	_ _ HY_
	SSOP – DCT	Tape and reel	SN74AUP1G99DCTR	H99_ _ _
	VSSOP – DCU	Tape and reel	SN74AUP1G99DCUR	H99_

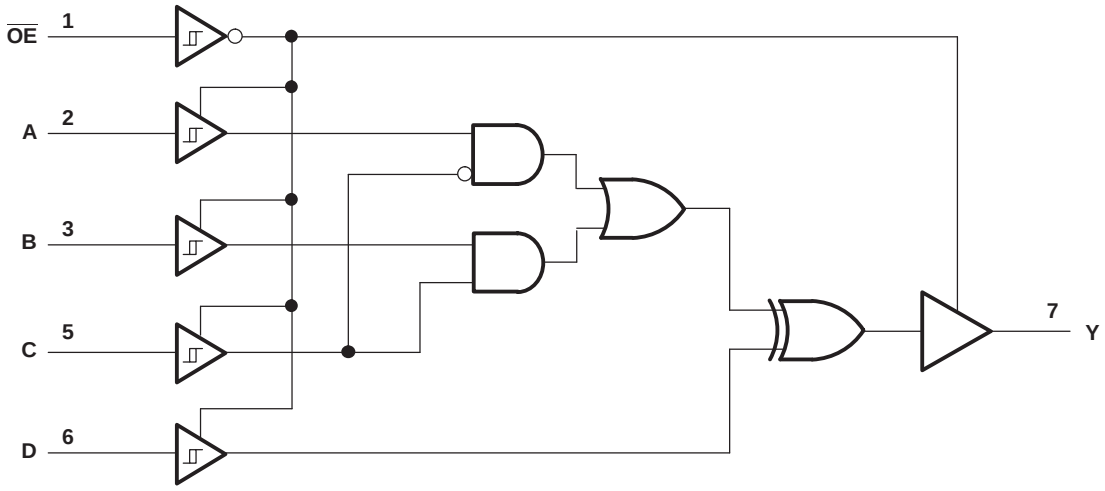
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OE}$	D	C	B	A	Y
L	L	L	L	L	L
L	L	L	L	H	H
L	L	L	H	L	L
L	L	L	H	H	H
L	L	H	L	L	L
L	L	H	L	H	L
L	L	H	H	L	H
L	L	H	H	H	H
L	H	L	L	L	H
L	H	L	L	H	L
L	H	L	H	L	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	L	H	H
L	H	H	H	L	L
L	H	H	H	H	L
H	X(1)	X(1)	X(1)	X(1)	Z

(1) Floating inputs allowed.

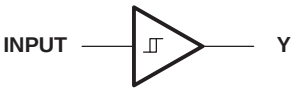
LOGIC DIAGRAM (POSITIVE LOGIC)



FUNCTION SELECTION TABLE

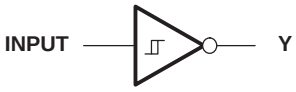
PRIMARY FUNCTION	COMPLEMENTARY FUNCTION	PAGE
3-state buffer		4
3-state inverter		4
3-state 2-to-1 data selector MUX		5
3-state 2-to-1 data selector MUX, inverted out		5
3-state 2-input AND	3-state 2-input NOR, both inputs inverted	5
3-state 2-input AND, 1 input inverted	3-state 2-input NOR, 1 input inverted	5
3-state 2-input AND, both inputs inverted	3-state 2-input NOR	5
3-state 2-input NAND	3-state 2-input OR, both inputs inverted	6
3-state 2-input NAND, 1 input inverted	3-state 2-input OR, 1 input inverted	6
3-state 2-input NAND, both inputs inverted	3-state 2-input OR	6
3-state 2-input XOR		6
3-state 2-input XNOR	3-state 2-input XOR, 1 input inverted	7

3-STATE BUFFER FUNCTIONS AVAILABLE



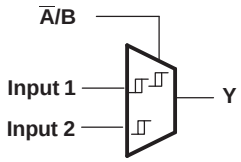
FUNCTION	$\overline{OE}$	A	B	C	D
3-state buffer	L	Input	X	L	L
		X	Input	H	L
		L	H	Input	L
		H	L	Input	H
		H	X	L	Input
		X	L	H	Input
		L	L	X	Input

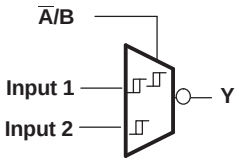
3-STATE INVERTER FUNCTIONS AVAILABLE



FUNCTION	$\overline{OE}$	A	B	C	D
3-state inverter	L	Input	X	L	H
		X	Input	H	H
		L	H	Input	H
		H	L	Input	L
		H	X	L	Input
		X	H	H	Input
		H	H	X	Input

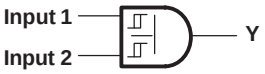
3-STATE MUX FUNCTIONS AVAILABLE

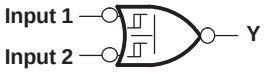




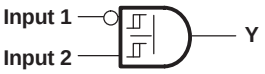
FUNCTION	$\overline{OE}$	A	B	C	D
3-state 2-to-1, data selector MUX	L	Input 1	Input 2	$\overline{\text{Input 1}}$ or Input 2	L
3-state 2-to-1, data selector MUX		Input 2	Input 1	$\overline{\text{Input 2}}$ or Input 1	L
3-state 2-to-1, data selector MUX, inverted out		Input 1	Input 2	$\overline{\text{Input 1}}$ or Input 2	H
3-state 2-to-1, data selector MUX, inverted out		Input 2	Input 1	$\overline{\text{Input 2}}$ or Input 1	H

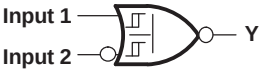
3-STATE AND/NOR FUNCTIONS AVAILABLE



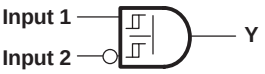


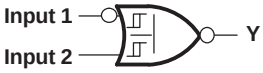
NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	$\overline{OE}$	A	B	C	D
2	3-state AND	3-state NOR, both inputs inverted	L	L	Input 1	Input 2	L
2	3-state AND	3-state NOR, both inputs inverted		L	Input 2	Input 1	L



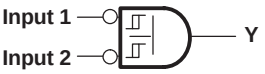


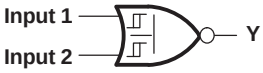
NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	$\overline{OE}$	A	B	C	D
2	3-state AND, with A inverted	3-state NOR, with B inverted	L	Input 2	L	Input 1	L
2	3-state AND, with A inverted	3-state NOR, with B inverted		H	Input 1	Input 2	H





NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	$\overline{OE}$	A	B	C	D
2	3-state AND, with B inverted	3-state NOR, with A inverted	L	Input 1	L	Input 2	L
2	3-state AND, with B inverted	3-state NOR, with A inverted		H	Input 2	Input 1	H





NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	$\overline{OE}$	A	B	C	D
2	3-state AND, both inverted inputs	3-state NOR	L	Input 1	H	Input 2	H
2	3-state AND, both inverted inputs	3-state NOR		Input 2	H	Input 1	H

3-STATE NAND/OR FUNCTIONS AVAILABLE

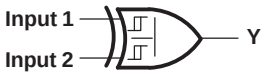
NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	$\overline{OE}$	A	B	C	D
2	3-state NAND	3-state OR, with both inputs inverted	L	L	Input 1	Input 2	H
2	3-state NAND	3-state OR, with both inputs inverted		L	Input 2	Input 1	H

NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	$\overline{OE}$	A	B	C	D
2	3-state NAND, with A inverted	3-state OR, with B inverted	L	Input 2	L	Input 1	H
2	3-state NAND, with A inverted	3-state OR, with B inverted		H	Input 1	Input 2	L

NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	$\overline{OE}$	A	B	C	D
2	3-state NAND, with B inverted	3-state OR, with A inverted	L	Input 1	L	Input 2	H
2	3-state NAND, with B inverted	3-state OR, with A inverted		H	Input 2	Input 1	L

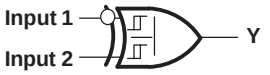
NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	$\overline{OE}$	A	B	C	D
2	3-state NAND, with both inputs inverted	3-state OR	L	Input 1	H	Input 2	L
2	3-state NAND, with both inputs inverted	3-state OR		Input 2	H	Input 1	L

3-STATE XOR/XNOR FUNCTIONS AVAILABLE

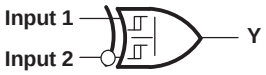


FUNCTION	$\overline{OE}$	A	B	C	D
3-state XOR	L	Input 1	X	L	Input 2
		Input 2	X	L	Input 1
		X	Input 1	H	Input 2
		X	Input 2	H	Input 1
		L	H	Input 1	Input 2
		L	H	Input 2	Input 1

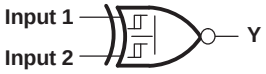
3-STATE XOR/XNOR FUNCTIONS AVAILABLE (continued)



FUNCTION	$\overline{OE}$	A	B	C	D
3-state XOR, with A inverted	L	H	L	Input 1	Input 2



FUNCTION	$\overline{OE}$	A	B	C	D
3-state XOR, with B inverted	L	H	L	Input 1	Input 2



FUNCTION	$\overline{OE}$	A	B	C	D
3-state XNOR	L	H	L	Input 1	Input 2
3-state XNOR		H	L	Input 2	Input 1

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage range in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	DCT package		220	°C/W
		DCU package		227	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_I	Input voltage		0	3.6	V
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	μA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65 V		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage			0.8 V	0.3		0.6	0.3	0.6	V
			1.1 V	0.53		0.9	0.53	0.9	
			1.4 V	0.74		1.11	0.74	1.11	
			1.65 V	0.91		1.29	0.91	1.29	
			2.3 V	1.37		1.77	1.37	1.77	
			3 V	1.88		2.29	1.88	2.29	
$V_{T–}$ Negative-going input threshold voltage			0.8 V	0.1		0.6	0.1	0.6	V
			1.1 V	0.26		0.65	0.26	0.65	
			1.4 V	0.39		0.75	0.39	0.75	
			1.65 V	0.47		0.84	0.47	0.84	
			2.3 V	0.69		1.04	0.69	1.04	
			3 V	0.88		1.24	0.88	1.24	
ΔV_T Hysteresis ($V_{T+} – V_{T–}$)			0.8 V	0.07		0.5	0.07	0.5	V
			1.1 V	0.08		0.46	0.08	0.46	
			1.4 V	0.18		0.56	0.18	0.56	
			1.65 V	0.27		0.66	0.27	0.66	
			2.3 V	0.53		0.92	0.53	0.92	
			3 V	0.79		1.31	0.79	1.31	
V_{OH}		I_{OH} = –20 µA	0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
		I_{OH} = –1.7 mA	1.4 V	1.11			1.03		
		I_{OH} = –1.9 mA	1.65 V	1.32			1.3		
		I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
		I_{OH} = –3.1 mA		1.9			1.85		
		I_{OH} = –2.7 mA	3 V	2.72			2.67		
		I_{OH} = –4 mA		2.6			2.55		
V_{OL}		I_{OL} = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
		I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	All inputs	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	µA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	µA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	µA
I_{OZ}		V_O = V_{CC} or GND	3.6 V			0.1		0.5	µA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), $\overline{OE}$ = GND, I_O = 0	0.8 V to 3.6 V			0.5		0.9	µA

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
ΔI_{CC}	Data inputs	$V_I = V_{CC} - 0.6$ V,(1) $I_O = 0$	3.3 V			40		50	µA
	$\overline{OE}$				110			120	
	All inputs	V_I = GND to 3.6 V, $\overline{OE} = V_{CC}$(2)	0.8 V to 3.6 V		0				nA
C_I		$V_I = V_{CC}$ or GND	0 V		1.5				pF
			3.6 V		1.5				
C_o		$V_O = V_{CC}$ or GND	3.6 V		3				pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND
(2) To show I_{CC} is very low when the input-disable feature is enabled.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	0.8 V		32				ns
			1.2 V ± 0.1 V	0.5	9.9	20.1	0.5	26.6	
			1.5 V ± 0.1 V	1.4	6.6	11.9	0.5	16.8	
			1.8 V ± 0.15 V	1.8	5.3	8.9	1	13	
			2.5 V ± 0.2 V	2.1	3.9	5.8	1.3	8.9	
			3.3 V ± 0.3 V	1.9	3.3	4.8	1.2	7.4	
t_{en}	$\overline{OE}$	Y	0.8 V		35				ns
			1.2 V ± 0.1 V	0.6	11.1	21.7	0.5	25.2	
			1.5 V ± 0.1 V	2.3	7.4	12.6	1.4	16.4	
			1.8 V ± 0.15 V	2	5.7	9.4	1.1	12.8	
			2.5 V ± 0.2 V	2.1	4.1	6.2	1.2	8.5	
			3.3 V ± 0.3 V	1.9	3.4	5	1.1	6.7	
t_{dis}	$\overline{OE}$	Y	0.8 V		9.8				ns
			1.2 V ± 0.1 V	1.4	4.5	7.7	1.5	8.2	
			1.5 V ± 0.1 V	1.7	3.2	4.8	1.7	6	
			1.8 V ± 0.15 V	1.5	3	4.7	1.3	6.1	
			2.5 V ± 0.2 V	0.9	1.9	3	0.7	4.2	
			3.3 V ± 0.3 V	0.8	2.5	4.4	0.7	4.5	

Switching Characteristics

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	0.8 V		36				ns
			1.2 V ± 0.1 V	0.4	10.7	21.1	0.7	29.8	
			1.5 V ± 0.1 V	2	7.2	12.6	1.1	18.5	
			1.8 V ± 0.15 V	2.3	5.8	9.5	1.5	14.5	
			2.5 V ± 0.2 V	2.5	4.4	6.3	1.7	10.5	
			3.3 V ± 0.3 V	2.3	3.7	5.2	1.5	8.4	
t_{en}	$\overline{OE}$	Y	0.8 V		0				ns
			1.2 V ± 0.1 V	1.4	12.1	22.8	0.8	29.3	
			1.5 V ± 0.1 V	2.8	8	13.3	2	18.7	
			1.8 V ± 0.15 V	2.5	6.2	10	1.6	14.8	
			2.5 V ± 0.2 V	2.5	4.5	6.7	1.6	9.9	
			3.3 V ± 0.3 V	2.3	3.8	5.4	1.5	8.2	
t_{dis}	$\overline{OE}$	Y	0.8 V		0				ns
			1.2 V ± 0.1 V	2	5.6	9.3	2	10	
			1.5 V ± 0.1 V	2.5	4.1	5.8	2.4	7.6	
			1.8 V ± 0.15 V	2.9	4.2	5.7	2.7	7.9	
			2.5 V ± 0.2 V	1.1	2.7	4.4	1.1	5.5	
			3.3 V ± 0.3 V	1.9	3.5	5.2	1.9	5.8	

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	0.8 V		38				ns
			1.2 V ± 0.1 V	0.9	11.4	22	0.5	30.8	
			1.5 V ± 0.1 V	2.5	7.8	13.2	1.6	19.2	
			1.8 V ± 0.15 V	2.7	6.3	10	1.9	15.1	
			2.5 V ± 0.2 V	2.8	4.7	6.6	2	10.8	
			3.3 V ± 0.3 V	2.6	4	5.5	1.8	8.8	
t_{en}	$\overline{OE}$	Y	0.8 V		44				ns
			1.2 V ± 0.1 V	1.8	13	24.2	1.3	30.6	
			1.5 V ± 0.1 V	3.2	8.6	14.1	2.4	19.5	
			1.8 V ± 0.15 V	2.9	6.7	10.6	2	15.4	
			2.5 V ± 0.2 V	2.8	4.9	7	1.9	10.3	
			3.3 V ± 0.3 V	2.6	4.1	5.7	1.8	8.6	
t_{dis}	$\overline{OE}$	Y	0.8 V		13				ns
			1.2 V ± 0.1 V	2.7	6.3	9.9	2.8	10.7	
			1.5 ± 0.1 V	3.2	4.6	6.1	3.1	8	
			1.8 V ± 0.15 V	3.2	4.8	6.6	3	8.8	
			2.5 V ± 0.2 V	2.2	3.4	4.7	2	6	
			3.3 V ± 0.3 V	2.4	4.4	6.5	2.3	7.2	

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

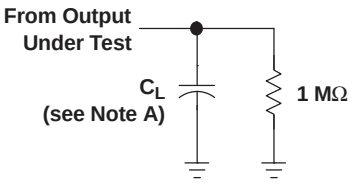
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A - 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	0.8 V		48				ns
			1.2 V ± 0.1 V	3.1	14	24.9	2.6	36.1	
			1.5 V ± 0.1 V	4.2	9.6	15.1	3.3	23.1	
			1.8 V ± 0.15 V	4.1	7.9	11.7	3.3	18	
			2.5 V ± 0.2 V	4.1	5.9	7.9	3.1	12.7	
			3.3 V ± 0.3 V	3.7	5.1	6.7	2.8	10.4	
t_{en}	$\overline{OE}$	Y	0.8 V		50				ns
			1.2 V ± 0.1 V	4.4	16	27.6	3.9	36.8	
			1.5 V ± 0.1 V	5.3	10.7	16.2	4.3	23.6	
			1.8 V ± 0.15 V	4.6	8.5	12.4	3.6	18.6	
			2.5 V ± 0.2 V	4.2	6.3	8.5	3.2	12.6	
			3.3 V ± 0.3 V	3.8	5.4	7.1	2.9	10.2	
t_{dis}	$\overline{OE}$	Y	0.8 V		19				ns
			1.2 V ± 0.1 V	6	10.1	14.2	6	14.6	
			1.5 V ± 0.1 V	5.1	7.4	10.6	5	10.1	
			1.8 V ± 0.15 V	5.5	8.6	11.6	5.5	12.1	
			2.5 V ± 0.2 V	3.3	5.9	8.3	3.3	8.9	
			3.3 V ± 0.3 V	6	8.7	10.9	5.9	11.8	

Operating Characteristics

T_A = 25°C

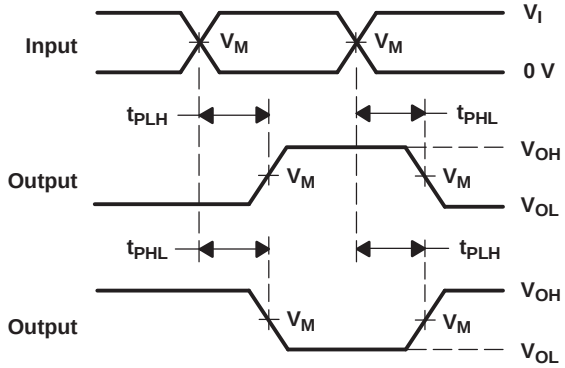
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	f = 10 MHz	0.8 V	4	pF
			1.2 ± 0.1 V	4	
			1.5 ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	5	
			3.3 V ± 0.3 V	5	
	Outputs disabled		0.8 V	0	
			1.2 ± 0.1 V	0	
			1.5 ± 0.1 V	0	
			1.8 V ± 0.15 V	0	
			2.5 V ± 0.2 V	0	
			3.3 V ± 0.3 V	0	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)

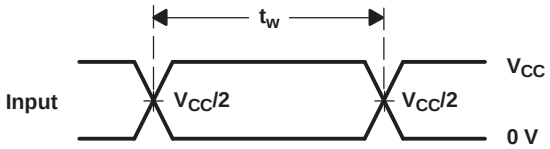


LOAD CIRCUIT

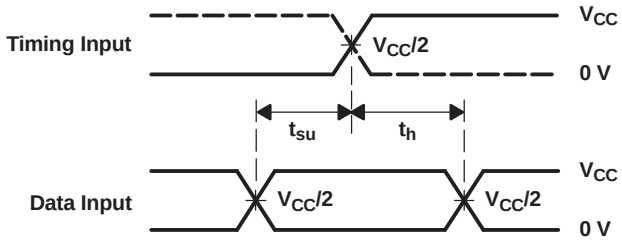
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

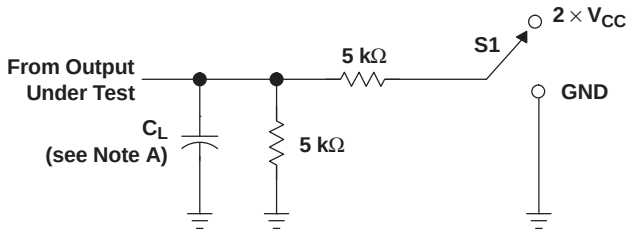


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, for propagation delays t_r/t_f = 3 ns, for setup and hold times and pulse width t_r/t_f = 1.2 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

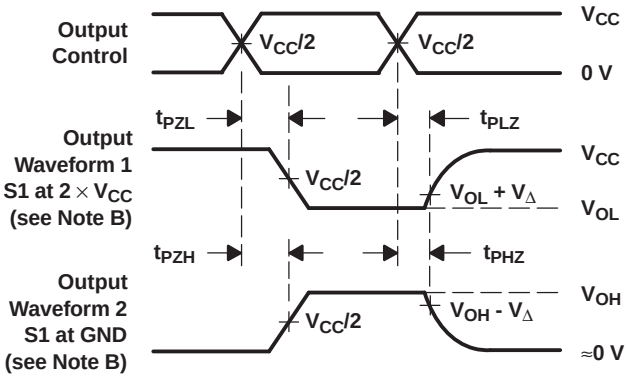
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	$2 \times V_{CC}$ GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G99DCTR	ACTIVE	SSOP	DCT	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(2XG5, H99) (R, Z)	Samples
SN74AUP1G99DCTT	ACTIVE	SSOP	DCT	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(2XG5, H99) (R, Z)	Samples
SN74AUP1G99DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(H99Q, H99R)	Samples
SN74AUP1G99DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(H99Q, H99R)	Samples
SN74AUP1G99YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HYN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

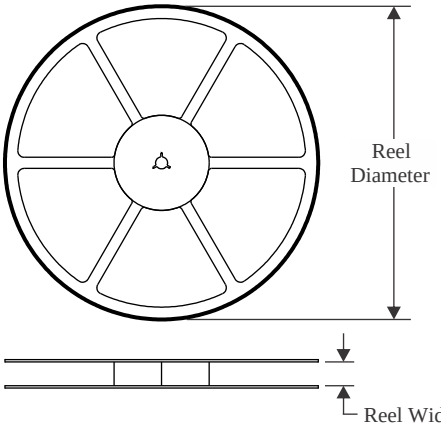
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

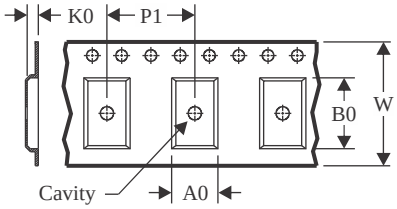
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

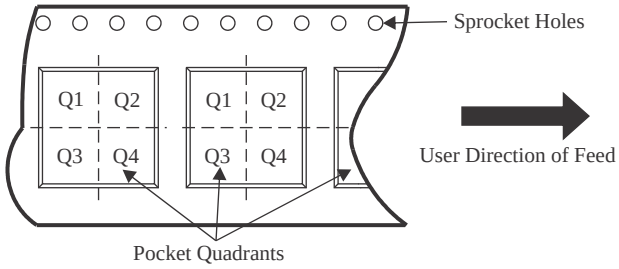


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

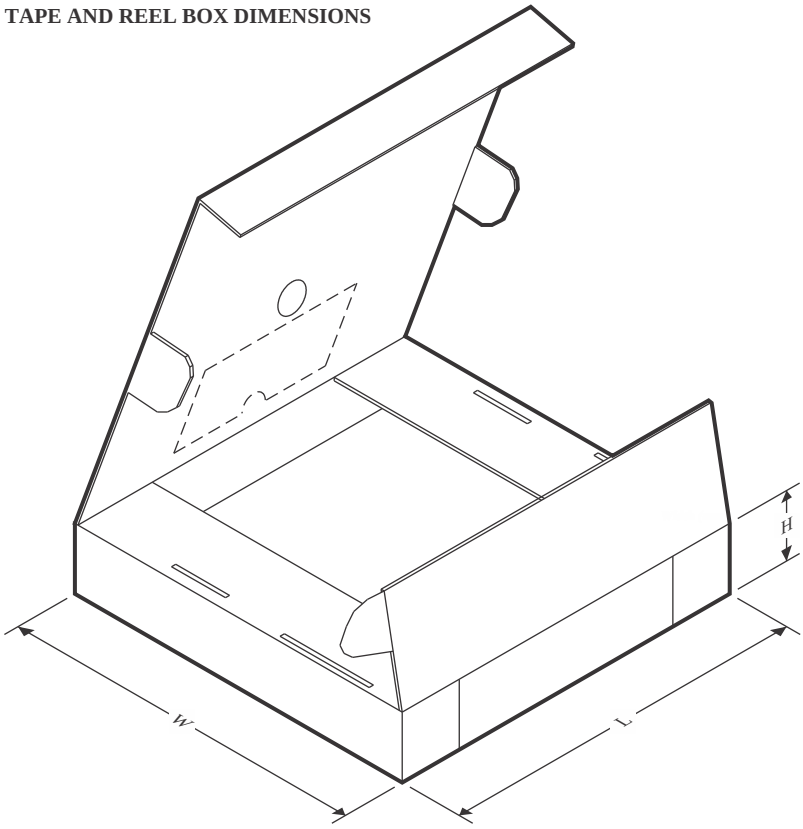
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G99DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUP1G99DCTR	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74AUP1G99DCTT	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74AUP1G99DCTT	SSOP	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUP1G99DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP1G99DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP1G99DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP1G99YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

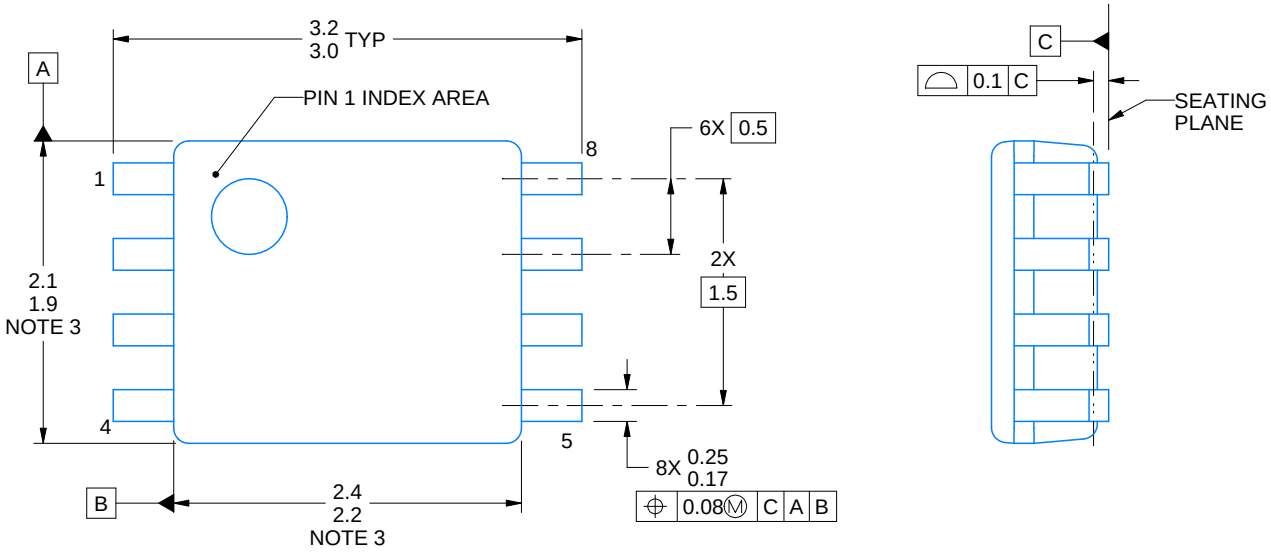
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G99DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AUP1G99DCTR	SSOP	DCT	8	3000	183.0	183.0	20.0
SN74AUP1G99DCTT	SSOP	DCT	8	250	183.0	183.0	20.0
SN74AUP1G99DCTT	SSOP	DCT	8	250	182.0	182.0	20.0
SN74AUP1G99DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP1G99DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP1G99DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74AUP1G99YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

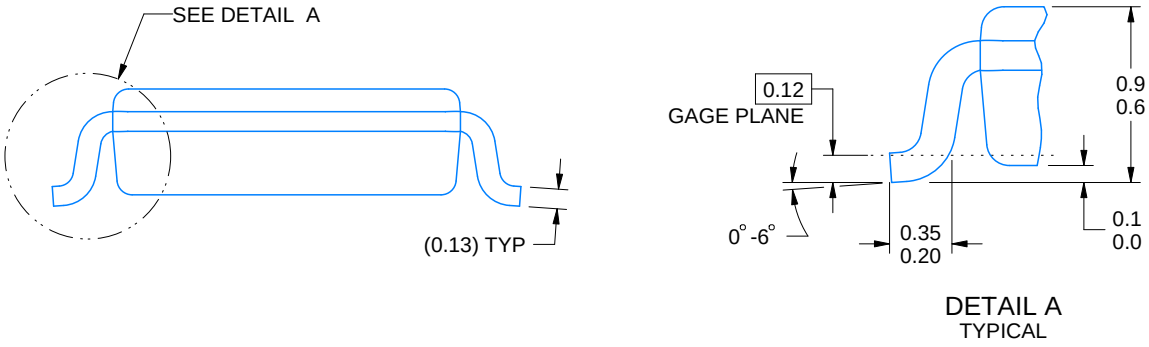
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

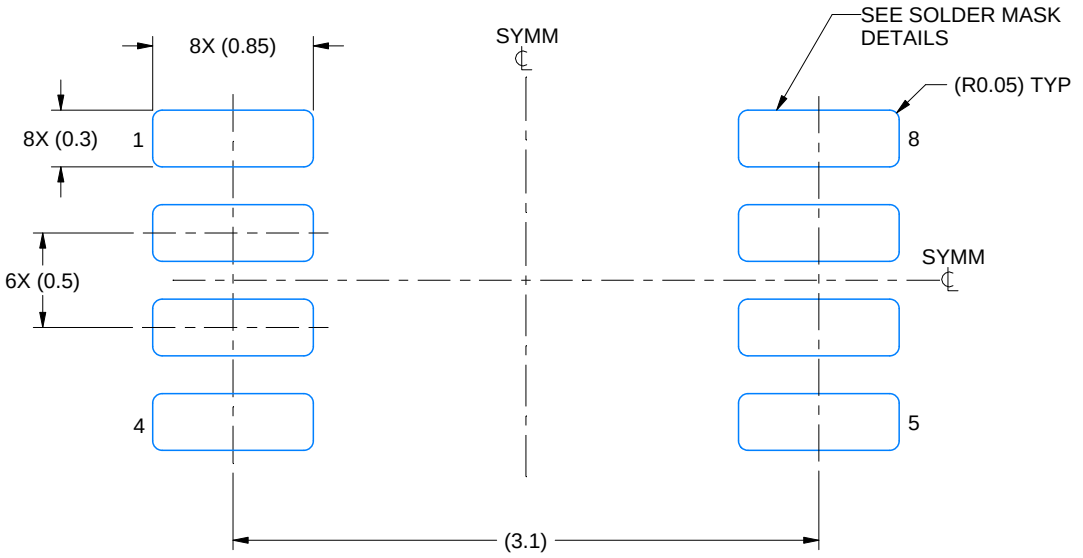




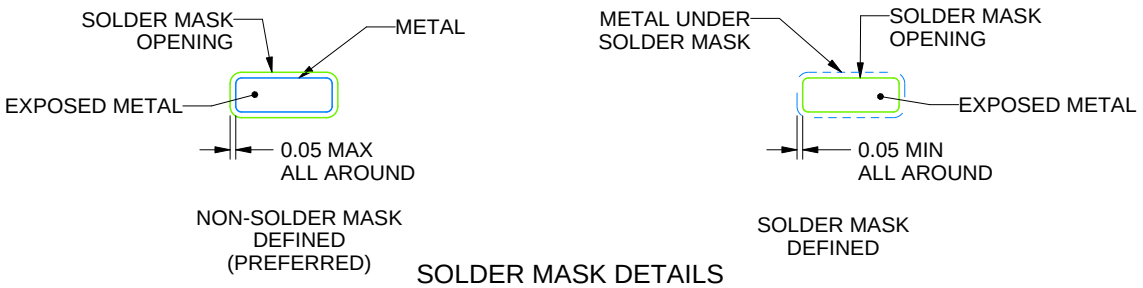
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

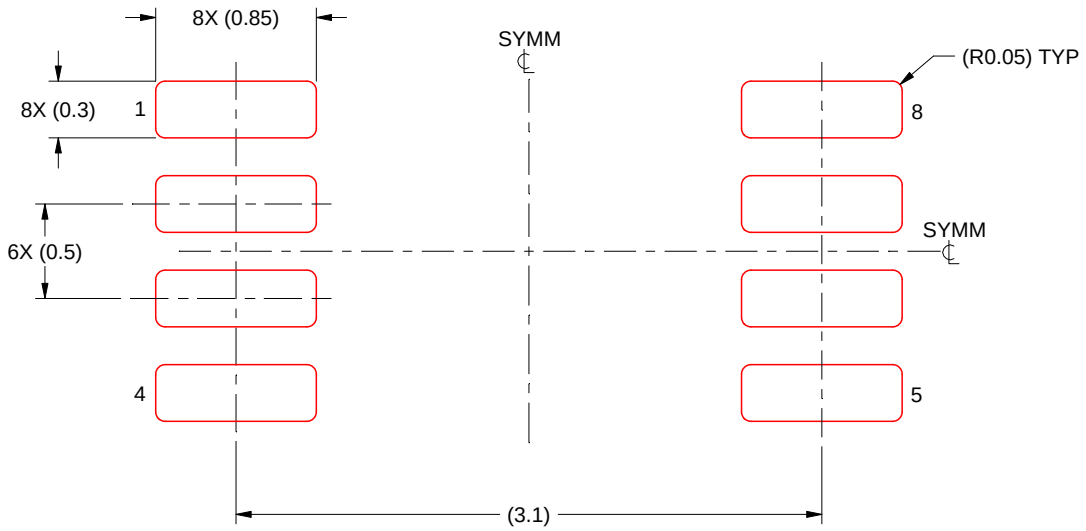


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

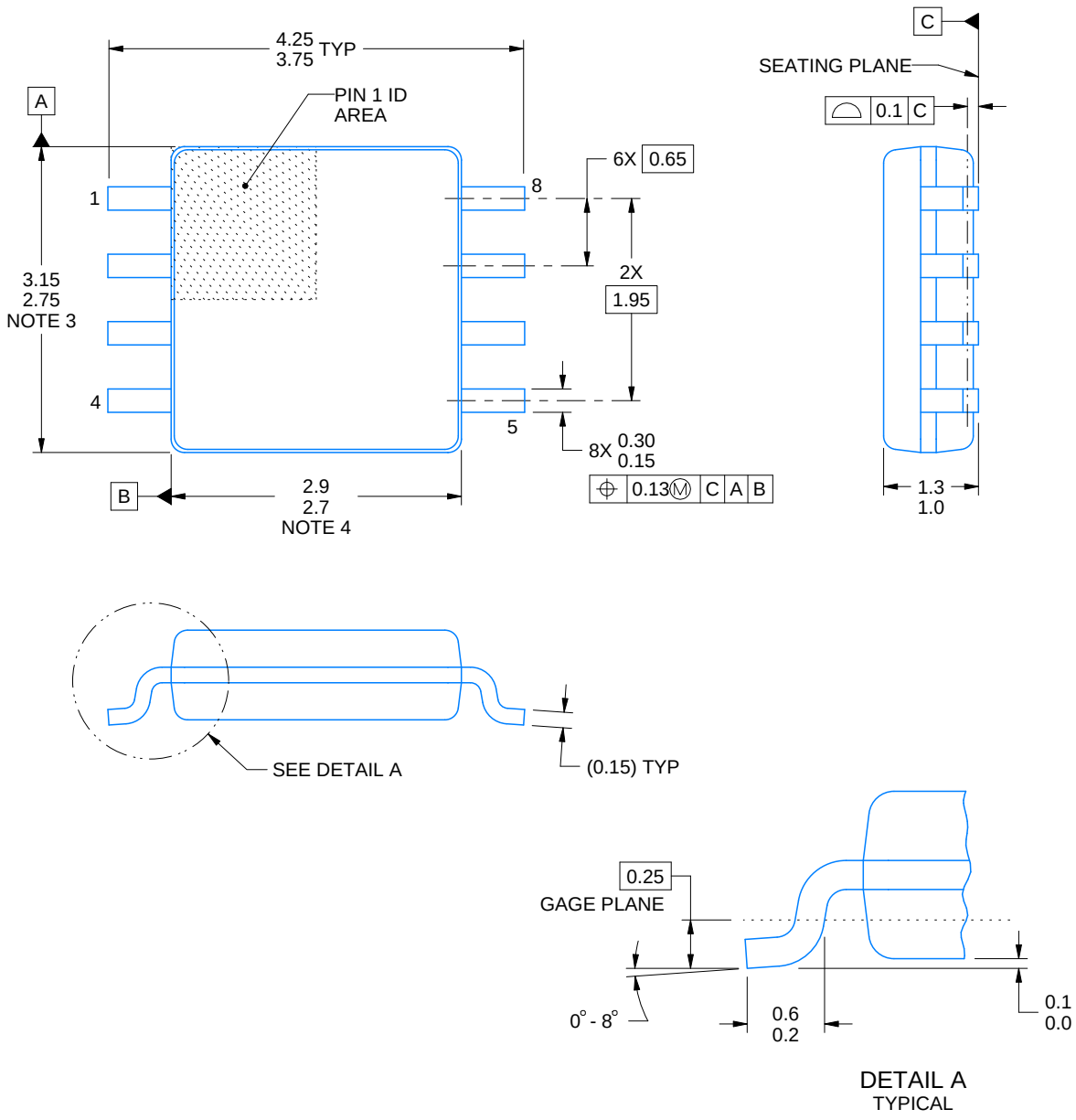
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

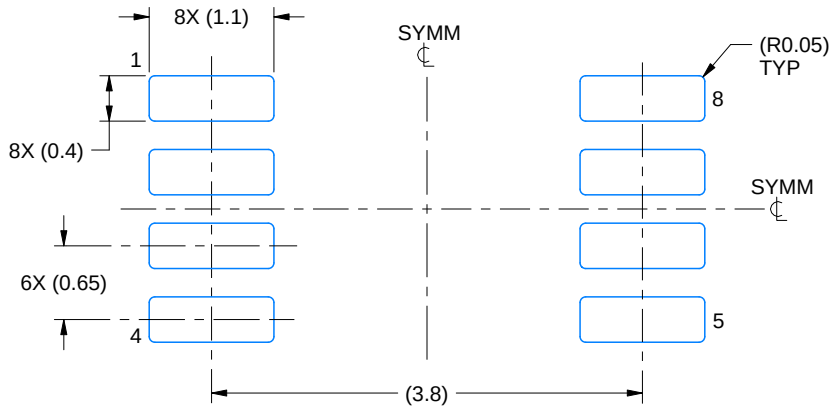
SMALL OUTLINE PACKAGE



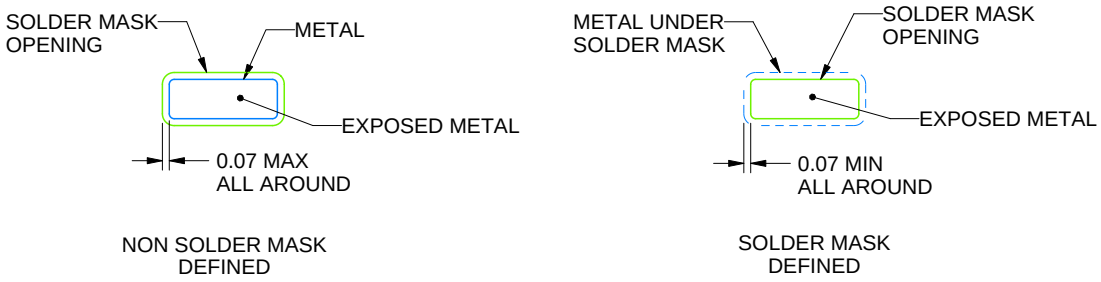
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

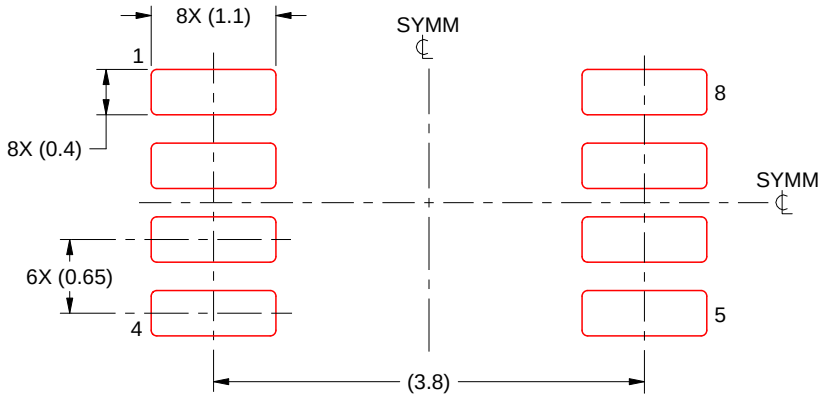


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

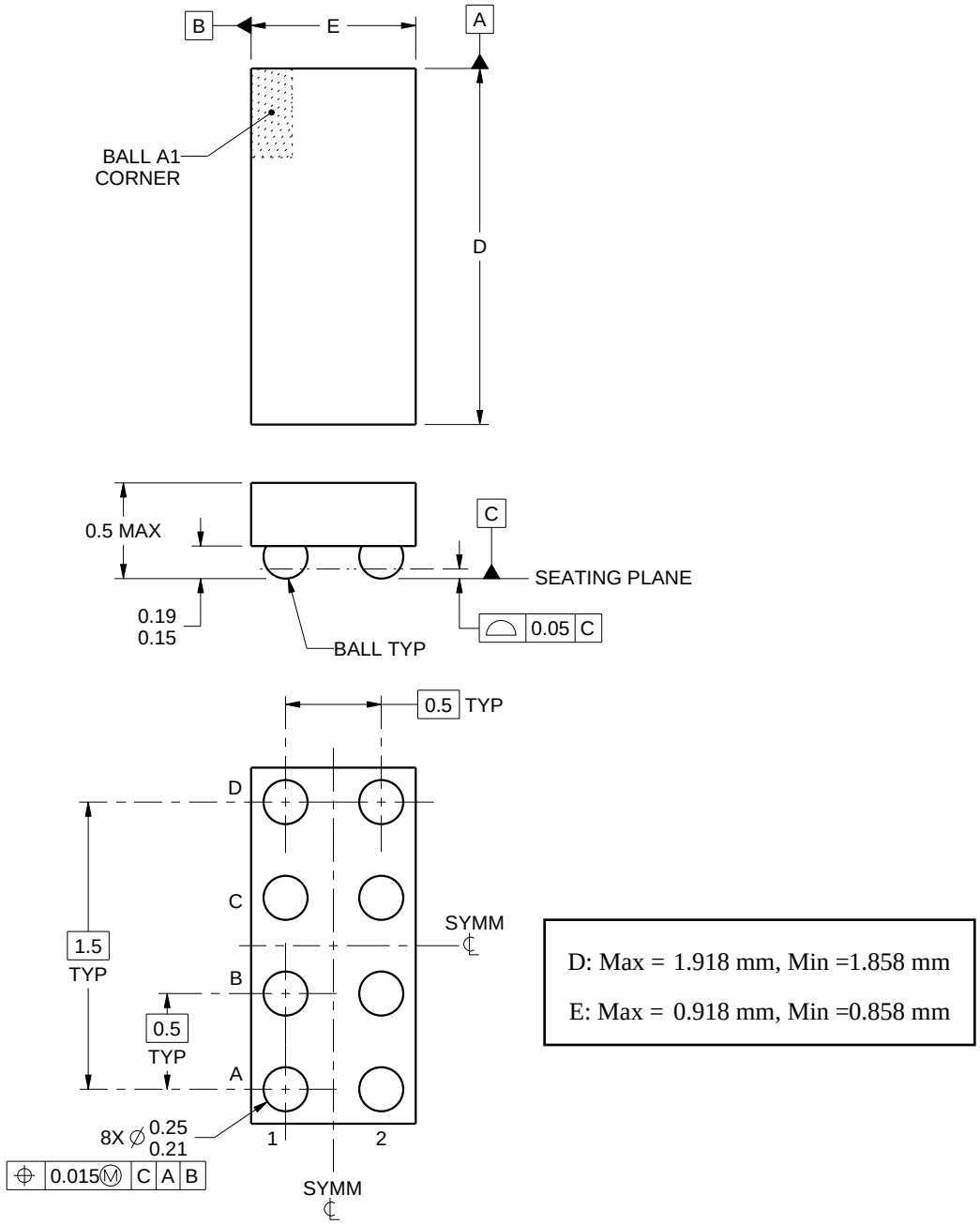
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

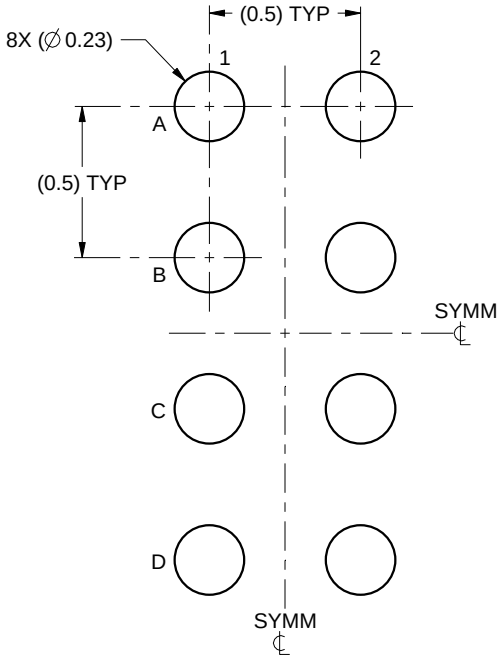
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

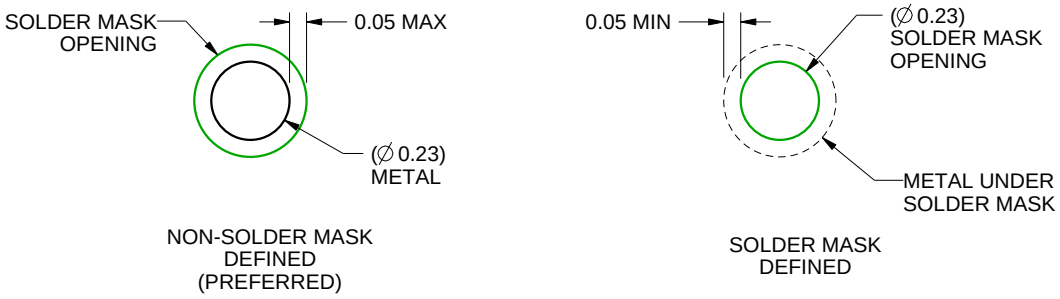


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

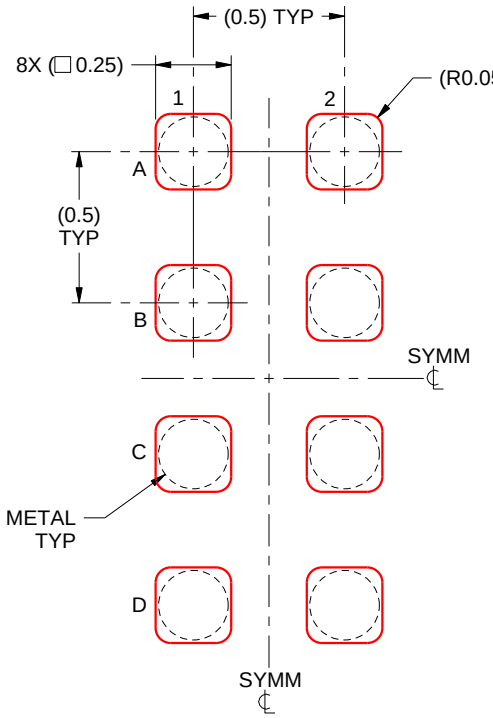


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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