

SN74AUP2G08 Low-Power Dual 2-Input Positive-AND Gate

1 Features

- Wide operating V_{CC} range of 0.8V to 3.6V
- Low static-power consumption ($I_{CC} = 0.9\mu\text{A max}$)
- Low dynamic-power consumption ($C_{pd} = 4.3\text{pF typ at } 3.3\text{V}$)
- Low noise – overshoot and undershoot <math><10\% \text{ of } V_{CC}</math>
- I_{off} supports partial-power-down mode operation
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the input ($V_{hys} = 250\text{mV Typ at } 3.3\text{V}$)
- 3.6V I/O tolerant to support mixed-mode signal operation
- $t_{pd} = 5.9\text{ns max at } 3.3\text{V}$
- Latch-up performance exceeds 100mA per JESD 78, Class II

2 Applications

- [Combine power good signals](#)
- [Combine enable signals](#)

3 Description

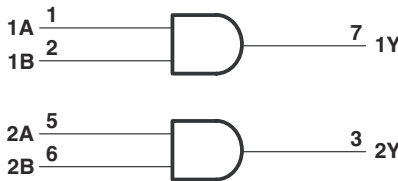
This dual 2-input positive-AND gate is designed for 0.8V to 3.6V V_{CC} operation and performs the Boolean function $Y = A \bullet B$ in positive logic.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when $V_{CC} = 0\text{V}$, preventing damaging current backflow through the device when it is powered down.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM) ⁽³⁾
SN74AUP2G08	DCU (VSSOP, 8)	3.1mm × 2mm	2.3mm × 2mm
	DQE (X2SON, 8)	1mm × 1.4mm	1mm × 1.4mm
	RSE (UQFN, 8)	1.5mm × 1.5mm	1.5mm × 1.5mm
	YFP (DSBGA, 8)	0.76mm × 1.56mm	0.76mm × 1.56mm
	YZP (DSBGA, 8)	0.89mm × 1.89mm	0.89mm × 1.89mm

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Simplified Logic Diagram (Positive Logic)



Table of Contents

1 Features	1	7.1 Overview.....	11
2 Applications	1	7.2 Functional Block Diagram.....	11
3 Description	1	7.3 Feature Description.....	11
4 Pin Configuration and Functions	3	7.4 Device Functional Modes.....	12
5 Specifications	4	8 Application and Implementation	13
5.1 Absolute Maximum Ratings.....	4	8.1 Application Information.....	13
5.2 ESD Ratings.....	4	8.2 Typical Application.....	13
5.3 Recommended Operating Conditions.....	5	8.3 Power Supply Recommendations.....	16
5.4 Thermal Resistance Characteristics.....	5	8.4 Layout.....	16
5.5 Electrical Characteristics.....	6	9 Device and Documentation Support	18
5.6 Switching Characteristics - $C_L = 5\text{pF}$	7	9.1 Receiving Notification of Documentation Updates....	18
5.7 Switching Characteristics - $C_L = 10\text{pF}$	7	9.2 Support Resources.....	18
5.8 Switching Characteristics - $C_L = 15\text{pF}$	7	9.3 Trademarks.....	18
5.9 Switching Characteristics - $C_L = 30\text{pF}$	8	9.4 Electrostatic Discharge Caution.....	18
5.10 Operating Characteristics.....	8	9.5 Glossary.....	18
5.11 Typical Characteristics.....	8	10 Revision History	18
6 Parameter Measurement Information	9	11 Mechanical, Packaging, and Orderable Information	18
6.1 Load Circuit And Voltage Waveforms.....	10		
7 Detailed Description	11		

4 Pin Configuration and Functions

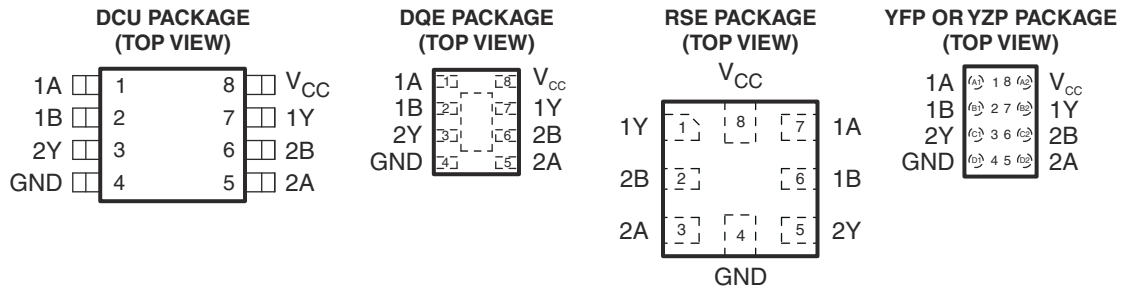


Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1 logic input A
1B	2	I	Channel 1 logic input B
2Y	3	O	Channel 2 output
GND	4	G	Ground
2A	5	I	Channel 2 logic input A
2B	6	I	Channel 2 logic input B
1Y	7	O	Channel 1 output
V _{CC}	8	P	Power Supply

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	4.6	V
V _I	Input voltage range ⁽²⁾	-0.5	4.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V _O	Output voltage range in the high or low state ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-50	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
I _O	Continuous output current		±20	mA
	Continuous current through V _{CC} or GND		±50	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 0.8V	V _{CC}	V
		V _{CC} = 1.1V to 1.95V	0.65 × V _{CC}	
		V _{CC} = 2.3V to 2.7V	1.6	
		V _{CC} = 3V to 3.6V	2	
V _{IL}	Low-level input voltage	V _{CC} = 0.8V	0	V
		V _{CC} = 1.1V to 1.95V	0.35 × V _{CC}	
		V _{CC} = 2.3V to 2.7V	0.7	
		V _{CC} = 3V to 3.6V	0.9	
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8V	-20	μA
		V _{CC} = 1.1V	-1.1	
		V _{CC} = 1.4V	-1.7	
		V _{CC} = 1.65V	-1.9	
		V _{CC} = 2.3V	-3.1	
		V _{CC} = 3V	-4	
I _{OL}	Low-level output current	V _{CC} = 0.8V	20	μA
		V _{CC} = 1.1V	1.1	
		V _{CC} = 1.4V	1.7	
		V _{CC} = 1.65V	1.9	
		V _{CC} = 2.3V	3.1	
		V _{CC} = 3V	4	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8V to 3.6V	200	ns/V
T _A	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#)

5.4 Thermal Resistance Characteristics

THERMAL METRIC ⁽¹⁾		DCU (VSSOP)	DQE (X2SON)	RSE (UQFN)	YPF (DSBGA)	YZP (DSBGA)	UNIT
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	227	261	253	98.8	102	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = –20μA	0.8 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
	I _{OH} = –1.1mA	1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		
	I _{OH} = –1.7mA	1.4 V	1.11			1.03		
	I _{OH} = –1.9mA	1.65 V	1.32			1.3		
	I _{OH} = –2.3mA	2.3 V	2.05			1.97		
	I _{OH} = –3.1mA		1.9			1.85		
	I _{OH} = –2.7mA	3 V	2.72			2.67		
	I _{OH} = –4mA		2.6			2.55		
V _{OL}	I _{OL} = 20μA	0.8 V to 3.6 V	0.1			0.1		V
	I _{OL} = 1.1mA	1.1 V	0.3 × V _{CC}			0.3 × V _{CC}		
	I _{OL} = 1.7mA	1.4 V	0.31			0.37		
	I _{OL} = 1.9mA	1.65 V	0.31			0.35		
	I _{OL} = 2.3mA	2.3 V	0.31			0.33		
	I _{OL} = 3.1mA		0.44			0.45		
	I _{OL} = 2.7mA	3 V	0.31			0.33		
	I _{OL} = 4mA		0.44			0.45		
I _I	A or B input	V _I = GND to 3.6V	0 V to 3.6 V			0.1	0.5	μA
I _{off}		V _I or V _O = 0V to 3.6V	0 V			0.2	1.3	μA
ΔI _{off}		V _I or V _O = 0V to 3.6V	0 V to 0.2 V			0.2	2	μA
I _{CC}		V _I = GND or (V _{CC} to 3.6V), I _O = 0	0.8 V to 3.6 V			0.5	1.7	μA
ΔI _{CC}		V _I = V _{CC} – 0.6V#none#, I _O = 0	3.3 V			40	50	μA
C _i	V _I = V _{CC} or GND	0 V			1.5		pF	
		3.6 V			1.5			
C _o	V _O = GND	0 V			3		pF	

5.6 Switching Characteristics - $C_L = 5\text{pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit And Voltage Waveforms Section 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8V	19.8					ns
			$1.2\text{V} \pm 0.1\text{V}$	2.6	7.8	18.8	2.1	20.9	
			$1.5\text{V} \pm 0.1\text{V}$	1.4	5.4	11.8	0.9	12.7	
			$1.8\text{V} \pm 0.15\text{V}$	1	4.3	9	0.5	9.5	
			$2.5\text{V} \pm 0.2\text{V}$	1	3	5.9	0.5	6.4	
			$3.3\text{V} \pm 0.3\text{V}$	1	2.4	5.2	0.5	5.7	

5.7 Switching Characteristics - $C_L = 10\text{pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit And Voltage Waveforms Section 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8V	23.1					ns
			$1.2\text{V} \pm 0.1\text{V}$	1.5	8.9	21.1	1	22.1	
			$1.5\text{V} \pm 0.1\text{V}$	1	6.3	13.2	0.5	13.7	
			$1.8\text{V} \pm 0.15\text{V}$	1	5	10.1	0.5	10.6	
			$2.5\text{V} \pm 0.2\text{V}$	1	3.6	7.4	0.5	7.9	
			$3.3\text{V} \pm 0.3\text{V}$	1	2.9	5.5	0.5	6	

5.8 Switching Characteristics - $C_L = 15\text{pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit And Voltage Waveforms Section 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8V	24.7					ns
			$1.2\text{V} \pm 0.1\text{V}$	3.6	9.8	21.7	3.1	24.8	
			$1.5\text{V} \pm 0.1\text{V}$	2.3	4.6	14	1.8	15.8	
			$1.8\text{V} \pm 0.15\text{V}$	1.6	5.5	10.6	1.1	11.7	
			$2.5\text{V} \pm 0.2\text{V}$	1	4	7	0.5	7.5	
			$3.3\text{V} \pm 0.3\text{V}$	1	3.3	5.9	0.5	6.4	

5.9 Switching Characteristics - $C_L = 30\text{pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit And Voltage Waveforms Section 6)

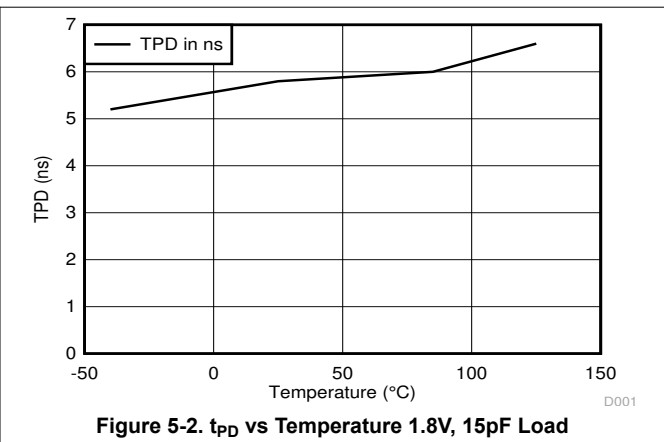
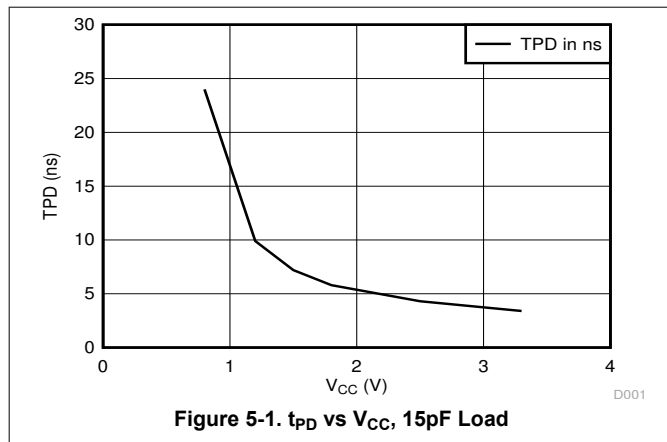
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8V	31.8					ns
			$1.2\text{V} \pm 0.1\text{V}$	4.9	12.6	26.3	4.4	29	
			$1.5\text{V} \pm 0.1\text{V}$	3.4	9	16.6	2.9	20	
			$1.8\text{V} \pm 0.15\text{V}$	2.5	7.3	12.9	2	15.7	
			$2.5\text{V} \pm 0.2\text{V}$	1.8	5.4	8.8	1.3	11.4	
			$3.3\text{V} \pm 0.3\text{V}$	1.5	4.5	7	1	9.5	

5.10 Operating Characteristics

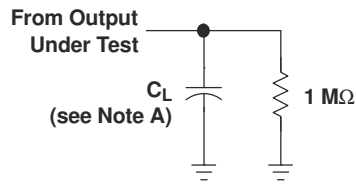
$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10\text{MHz}$	0.8V	4	pF
			$1.2\text{V} \pm 0.1\text{V}$	4	
			$1.5\text{V} \pm 0.1\text{V}$	4	
			$1.8\text{V} \pm 0.15\text{V}$	4	
			$2.5\text{V} \pm 0.2\text{V}$	4.1	
			$3.3\text{V} \pm 0.3\text{V}$	4.3	

5.11 Typical Characteristics

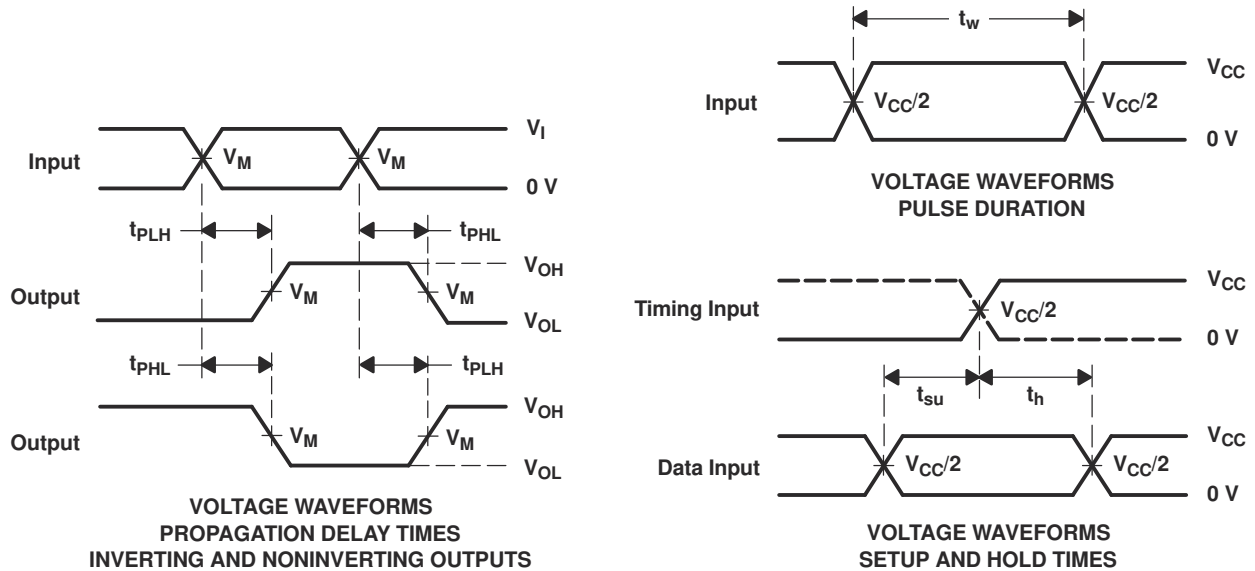


6 Parameter Measurement Information



LOAD CIRCUIT

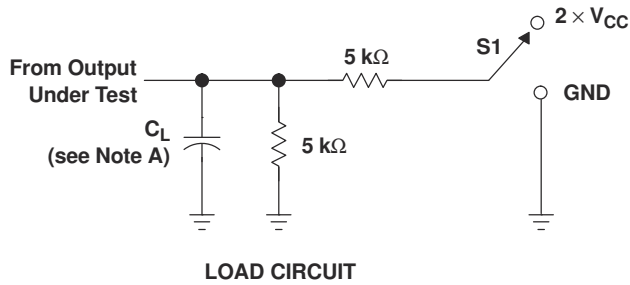
	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, slew rate ≥ 1 V/ns.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 E. All parameters and waveforms are not applicable to all devices.

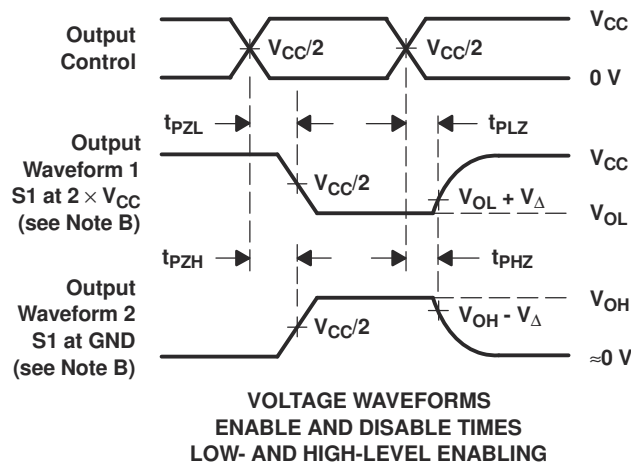
Figure 6-1. Load Circuit And Voltage Waveforms

6.1 Load Circuit And Voltage Waveforms



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, slew rate \geq 1 V/ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit And Voltage Waveforms

7 Detailed Description

7.1 Overview

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8V to 3.6V, resulting in increased battery life. This product also maintains excellent signal integrity.

This dual 2-input positive-AND gate is designed for 0.8V to 3.6V V_{CC} operation and performs the Boolean function $Y = A \bullet B$ in positive logic.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

7.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.4 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this

specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k Ω resistor, however, is recommended and will typically meet all requirements.

7.3.5 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

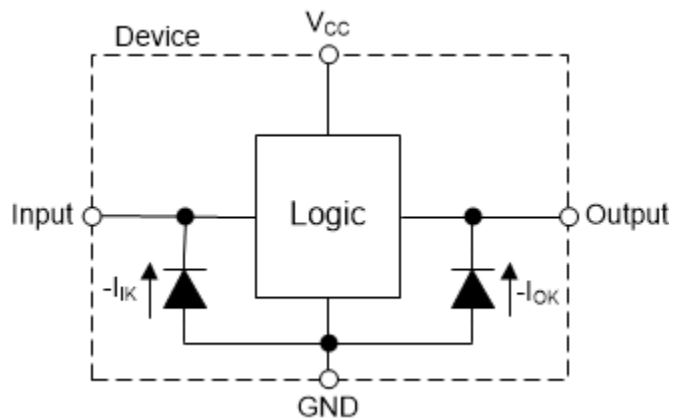


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in Figure 8-1. Multiple SN74AUP2G08 are used to directly control the $\overline{\text{RESET}}$ pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

(1)

8.2 Typical Application

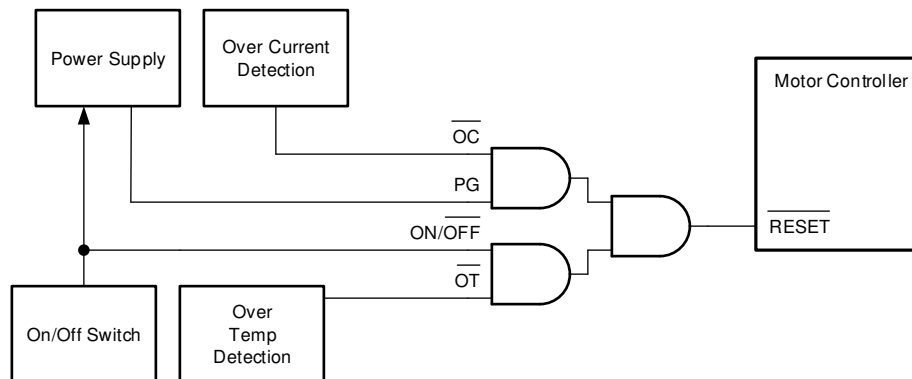


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AUP2G08 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AUP2G08 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AUP2G08 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AUP2G08 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)} V_{t-(min)}$ to be considered a logic LOW, and $V_{IH(min)} V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AUP2G08 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN74AUP2G08 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

The SN74AUP2G08 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is $\leq 50\text{pF}$. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AUP2G08 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(\text{max})})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in $\text{M}\Omega$; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

8.2.3 Application Curves

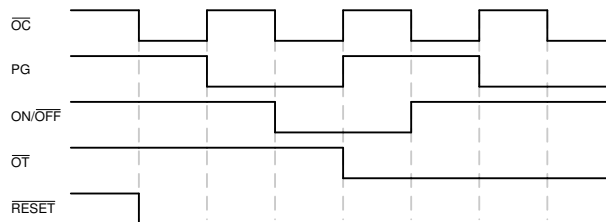


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

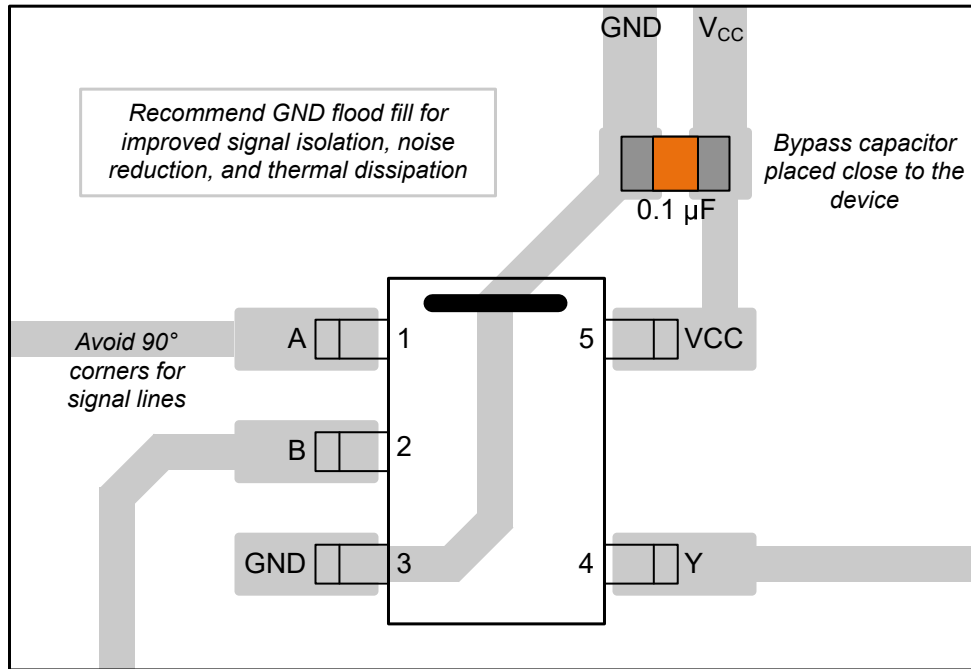


Figure 8-3. Example Layout

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2024) to Revision F (May 2025)	Page
• Updated SN74AUP2G08 operating temperature to 125°C and respective values in <i>Electrical Characteristics</i> table, <i>Recommended Operating Conditions</i> table, and <i>Switching Characteristics</i> tables.....	1

Changes from Revision D (October 2010) to Revision E (April 2024)	Page
• Added <i>Applications</i> , <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Increased Operating free-air temperature from 85°C max to 125°C max	5
• Added column to reflect performance at $T_A = -40^\circ\text{C}$ to 125°C to <i>Electrical Characteristics</i> and <i>Switching Characteristics</i> tables	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP2G08DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H08R
SN74AUP2G08DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H08R
SN74AUP2G08DCUR1G4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H08R
SN74AUP2G08DCUR1G4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H08R
SN74AUP2G08DQER	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	PR
SN74AUP2G08DQER.B	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	PR
SN74AUP2G08RSER	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	PR
SN74AUP2G08RSER.B	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	PR
SN74AUP2G08YFPR	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	HEN
SN74AUP2G08YFPR.B	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	HEN
SN74AUP2G08YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	HEN
SN74AUP2G08YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	HEN

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G08DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G08DCUR1G4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G08DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP2G08RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
SN74AUP2G08YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1
SN74AUP2G08YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G08DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G08DCUR1G4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G08DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP2G08RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP2G08YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0
SN74AUP2G08YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

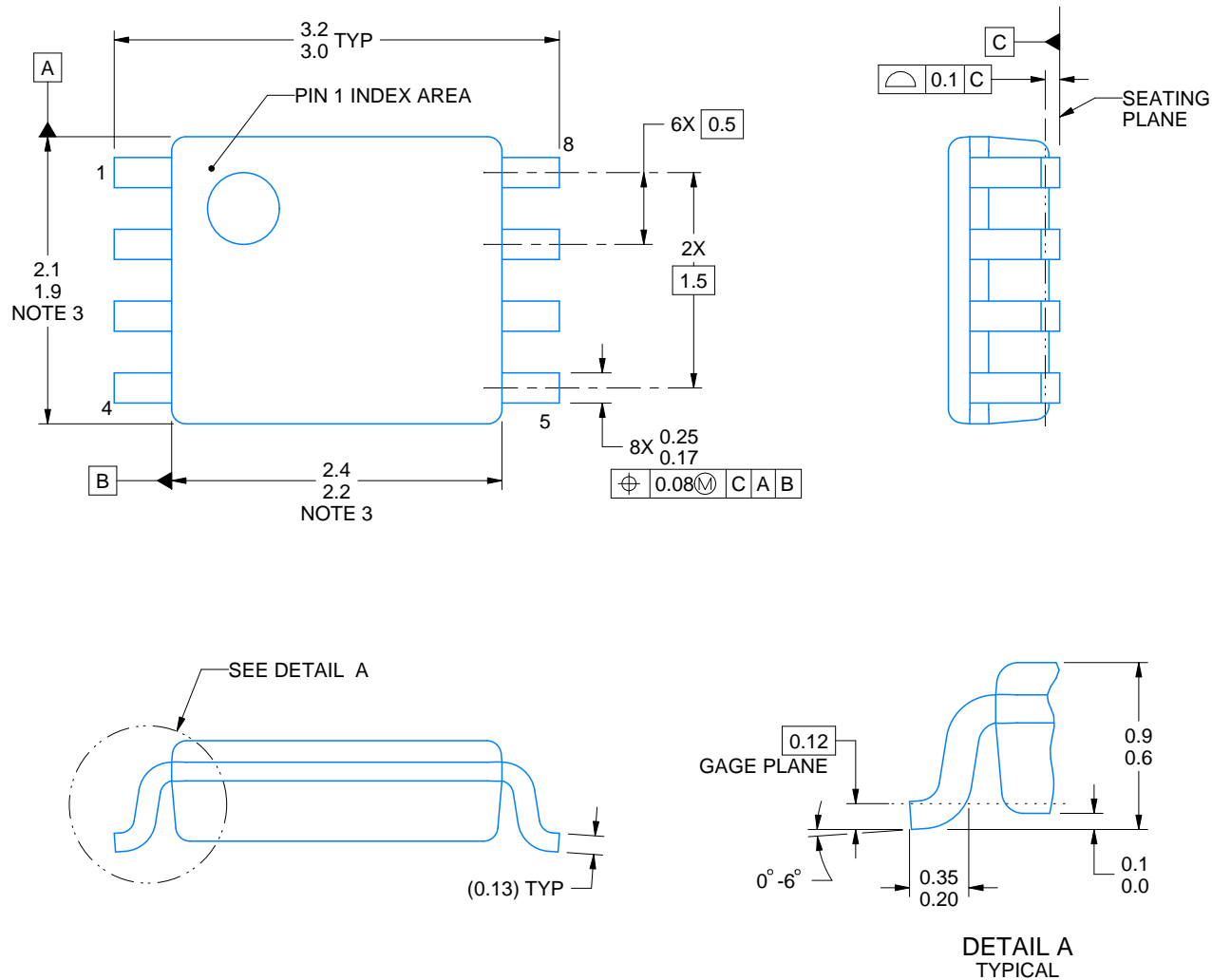
DCU0008A



PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

NOTES:

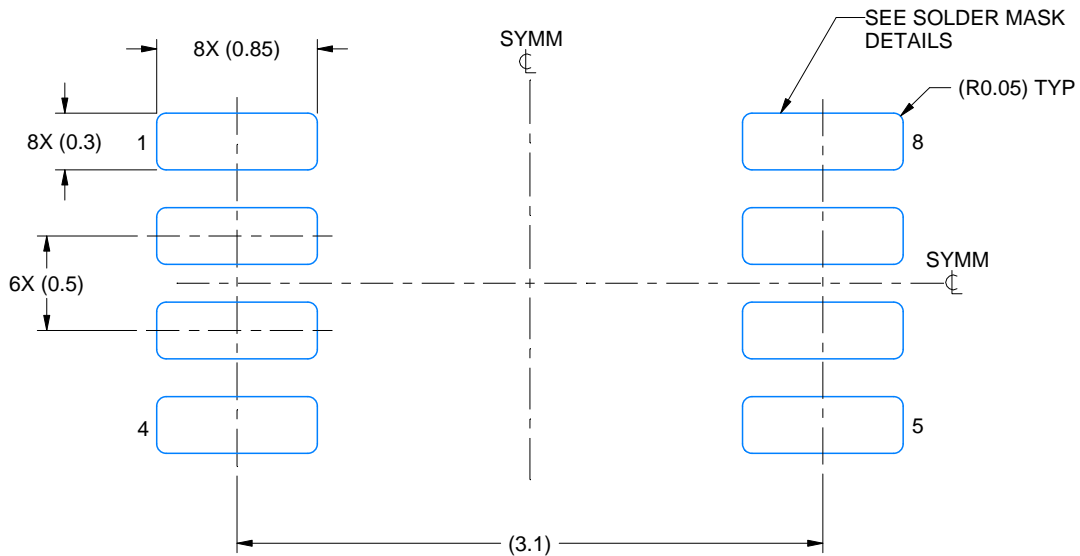
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.

EXAMPLE BOARD LAYOUT

DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



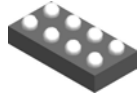
SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

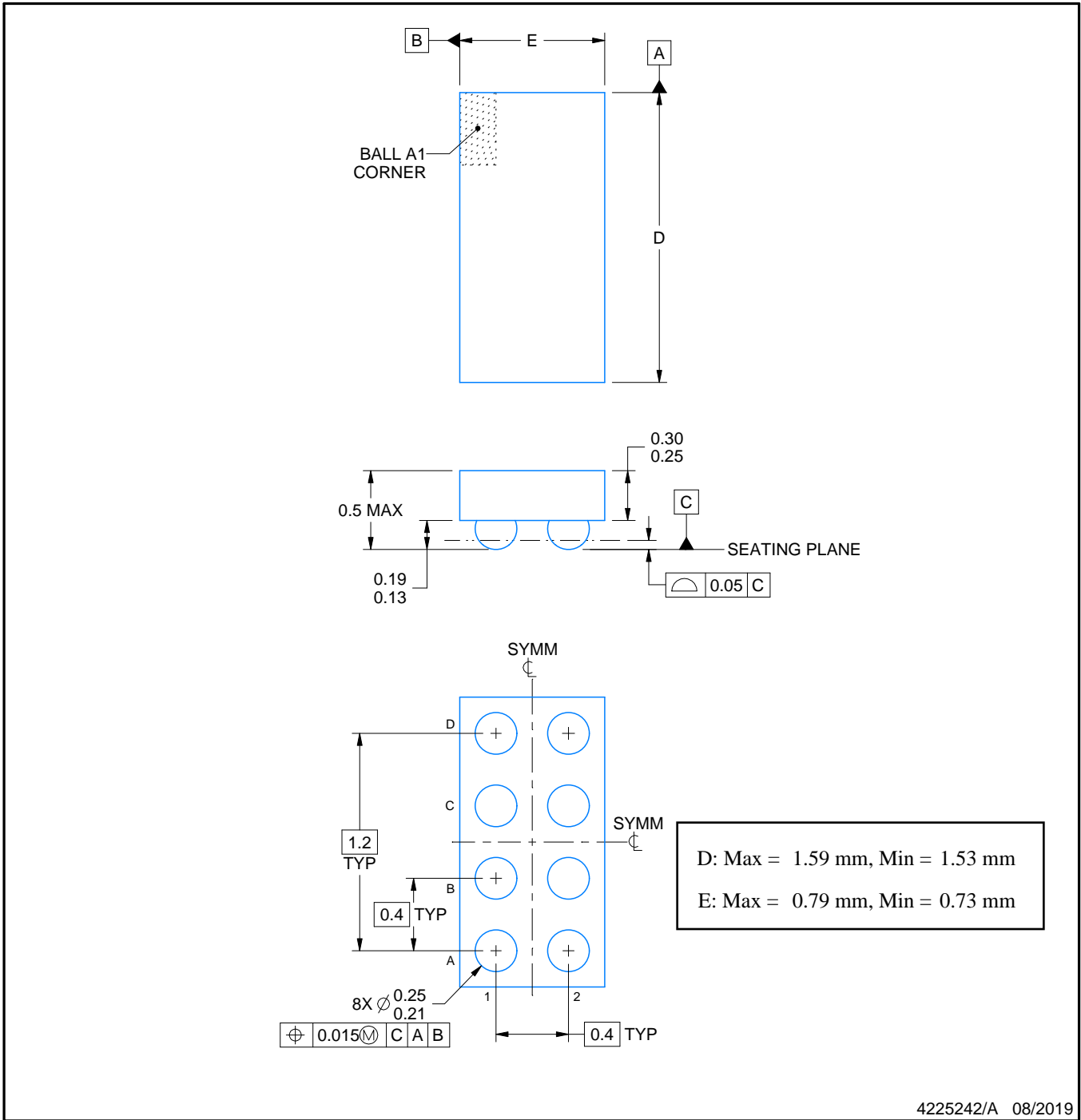
YFP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4225242/A 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YFP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4225242/A 08/2019

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

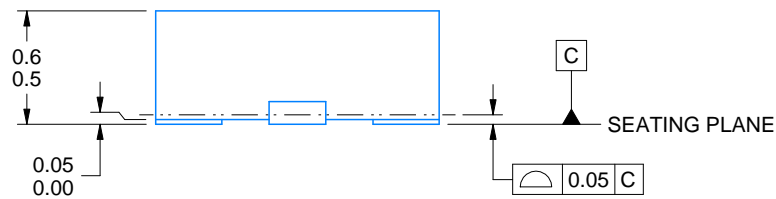


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4225242/A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4220323/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

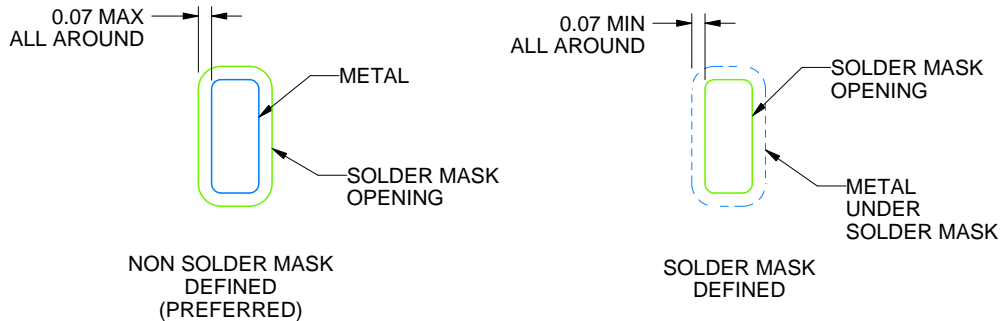
RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



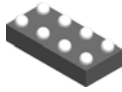
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/B 03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

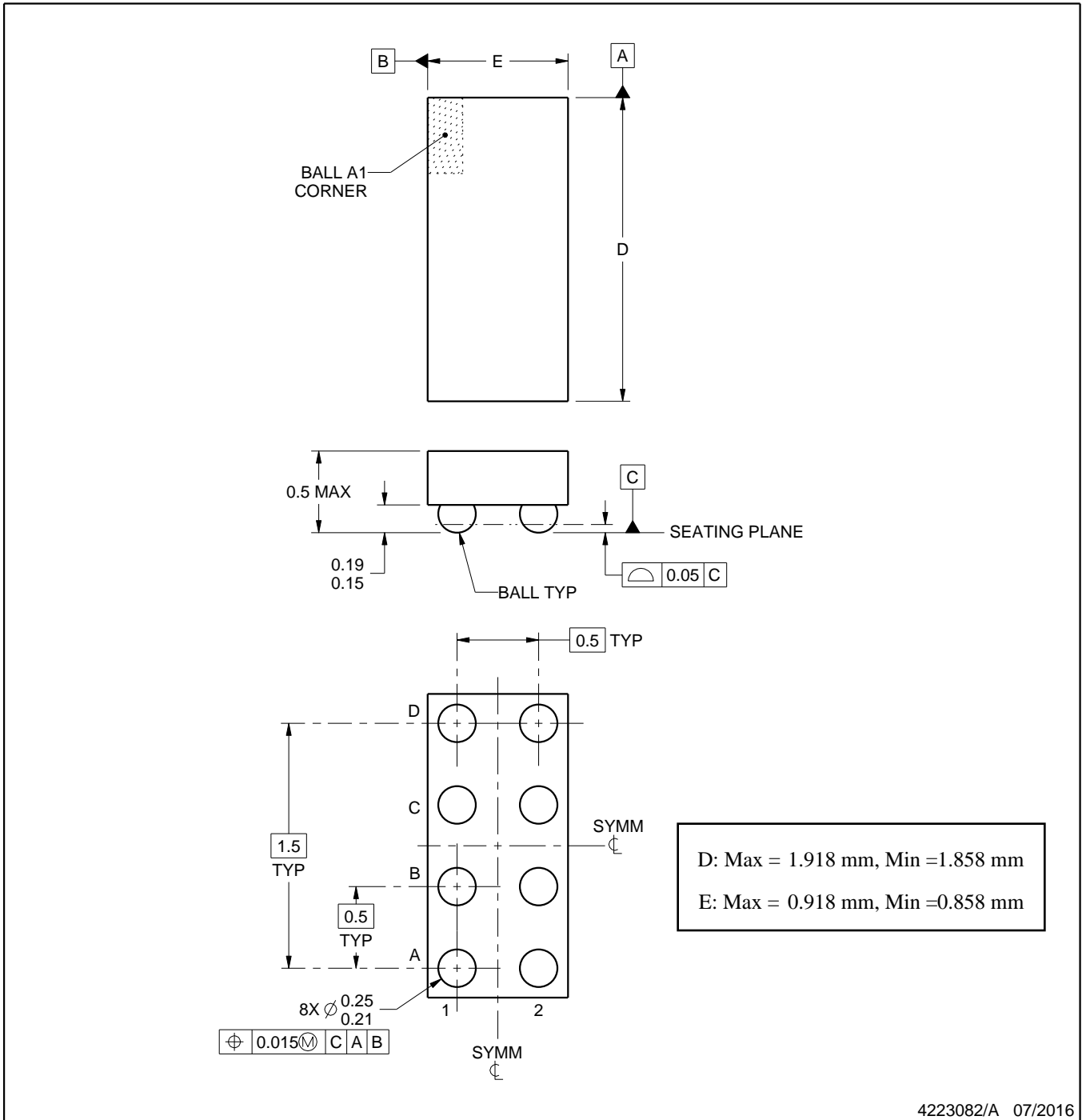
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

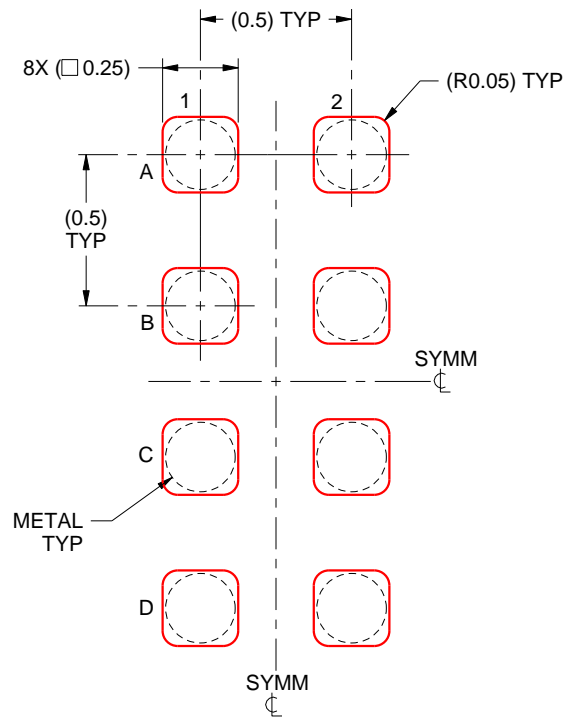
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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Last updated 10/2025