

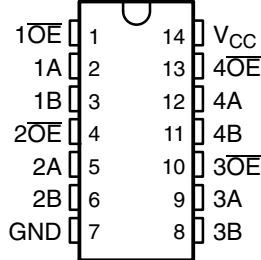
# SN74CBT3125 QUADRUPLE FET BUS SWITCH

SCDS0211 – MAY 1995 – REVISED SEPTEMBER 2002

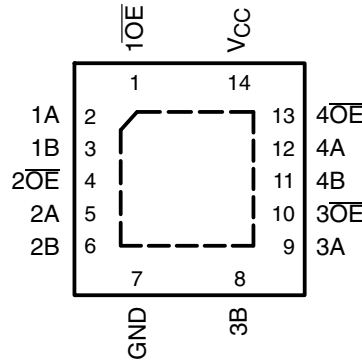
- Standard '125-Type Pinout (D, DB, DGV, and PW Packages)

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

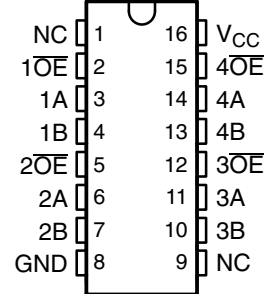
**D, DB, DGV, OR PW PACKAGE  
(TOP VIEW)**



**RGY PACKAGE  
(TOP VIEW)**



**DBQ PACKAGE  
(TOP VIEW)**



NC – No internal connection

## description/ordering information

The SN74CBT3125 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74CBT3125RGYR	CU125
	SOIC – D	Tube	SN74CBT3125D	CBT3125
		Tape and reel	SN74CBT3125DR	
	SSOP – DB	Tape and reel	SN74CBT3125DBR	CU125
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3125DBQR	CU125
	TSSOP – PW	Tape and reel	SN74CBT3125PWR	CU125
TVSOP – DGV	Tape and reel	SN74CBT3125DGVR	CU125	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect



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**TEXAS  
INSTRUMENTS**

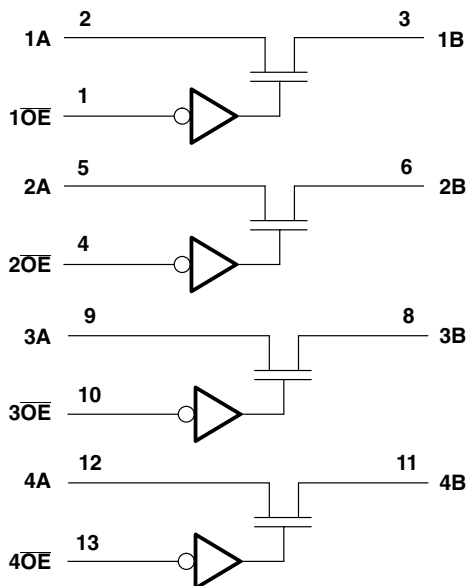
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# SN74CBT3125 QUADRUPLE FET BUS SWITCH

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## logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_K$ ( $V_{I/O} < 0$ )	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

## recommended operating conditions (see Note 4)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$I_I$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 5.5\text{ V}$ or GND			$\pm 1$	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	$I_O = 0$ , $V_I = V_{CC}$ or GND			3	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2.5	mA
$C_i$	Control inputs	$V_I = 3\text{ V}$ or 0				3	pF
$C_{io(OFF)}$		$V_O = 3\text{ V}$ or 0,	$\overline{OE} = V_{CC}$			4	pF
$r_{on}^\S$		$V_{CC} = 4\text{ V}$ , TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$ ,	$I_I = 15\text{ mA}$	16	22	$\Omega$
			$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	
		$I_I = 30\text{ mA}$			5	7	
		$V_I = 2.4\text{ V}$ ,	$I_I = 15\text{ mA}$	10	15		

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

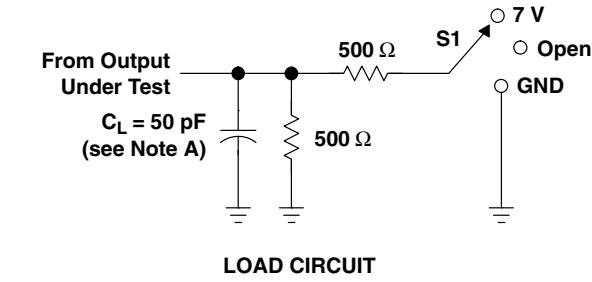
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{\parallel}$	A or B	B or A	0.35		0.25		ns
$t_{en}$	$\overline{OE}$	A or B	6		1.6	5.4	ns
$t_{dis}$	$\overline{OE}$	A or B	5.1		1	4.7	ns

<sup>||</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

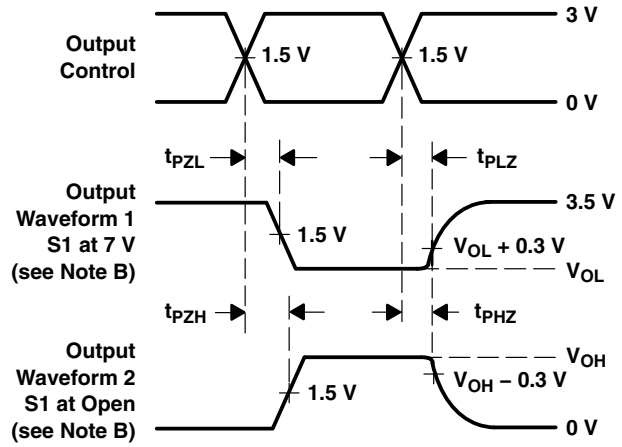
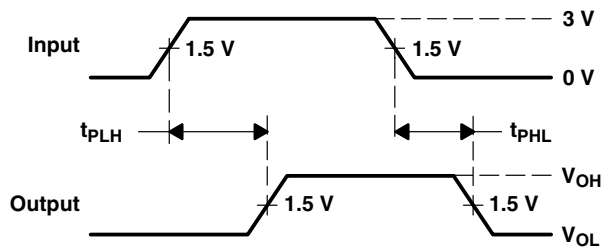
# SN74CBT3125 QUADRUPLE FET BUS SWITCH

SCDS0211 – MAY 1995 – REVISED SEPTEMBER 2002

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT3125D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	CBT3125	
SN74CBT3125DBQR	NRND	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU125	
SN74CBT3125DBR	NRND	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU125	
SN74CBT3125DGVR	NRND	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU125	
SN74CBT3125PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	CU125	
SN74CBT3125RGYR	OBSOLETE	VQFN	RGY	14		TBD	Call TI	Call TI	-40 to 85	CU125	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3125DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3125DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74CBT3125DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBT3125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3125DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBT3125DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74CBT3125DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74CBT3125DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74CBT3125PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74CBT3125RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT3125D	D	SOIC	14	50	506.6	8	3940	4.32
SN74CBT3125PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74CBT3125PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - ⚠ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.







# DBQ0016A

# PACKAGE OUTLINE

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



### NOTES:

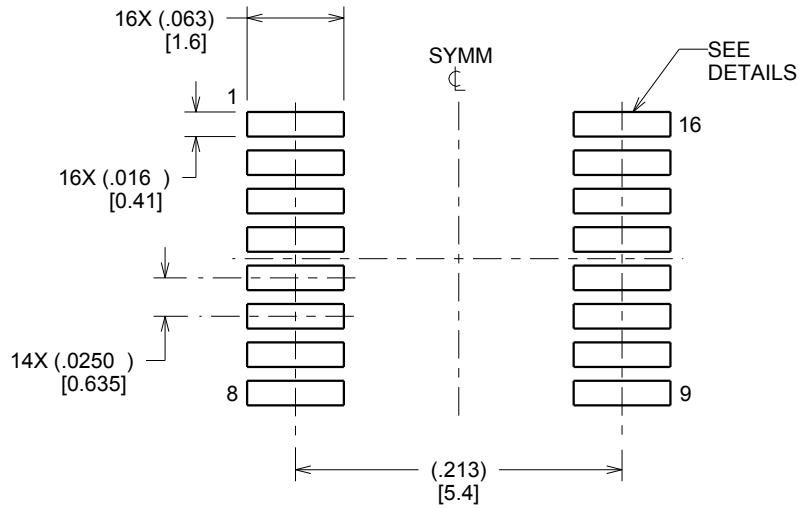
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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