

## SN74LV393A Dual 4-Bit Binary Counters

### 1 Features

- $V_{CC}$  operation of 2 V to 5.5 V
- Max  $t_{pd}$  of 10 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  supports Partial-Power-Down-Mode operation
- Dual 4-bit binary counters with individual clocks
- Direct clear for each 4-bit counter
- Can significantly improve system densities by reducing counter package count by 50 percent
- Latch-Up performance exceeds 100 mA per JESD 78, Class II

### 2 Applications

- [Synchronize inverted clock inputs](#)
- [Debounce a switch](#)
- Invert a digital signal

### 3 Description

The 'LV393A devices contain eight flip-flops and additional gating to implement two individual 4-bit counters in a single package. These devices are designed for 2 V to 5.5 V  $V_{CC}$  operation.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
SN74LV393A	D (SOIC, 14)	8.65 mm x 3.9 mm
	NS (SOP, 14)	10.3 mm x 5.3 mm
	DB (SSOP, 14)	6.2 mm x 5.3 mm
	PW (TSSOP, 14)	5 mm x 4.4 mm
	DGV (TVSOP, 14)	3.6 mm x 4.4 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

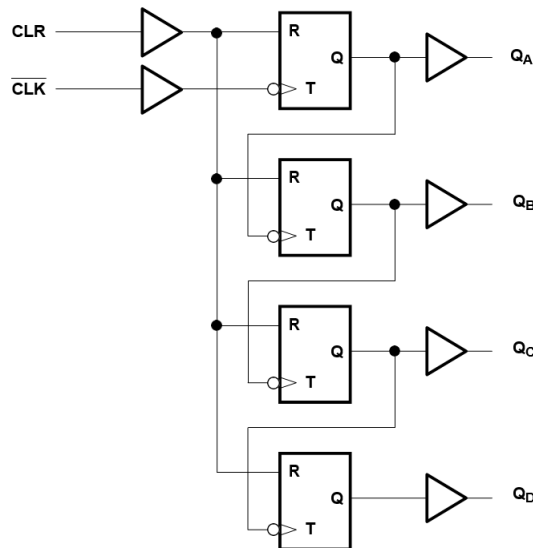


Figure 3-1. Logic Diagram, Each Counter (Positive Logic)



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## 4 Revision History

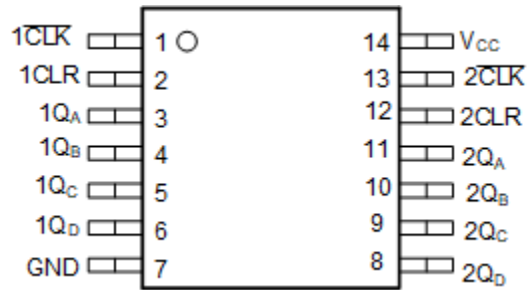
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (February 2001) to Revision E (March 2023)

Page

- Added *Applications*, *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... 1

## 5 Pin Configuration and Functions



**Figure 5-1. D, DB, DGV, NS, or PW Package (Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1CLK	1	I	Counter 1 Clock Input
1CLR	2	I	Counter 1 Clear Input
1Q <sub>A</sub>	3	O	Counter 1 A Output
1Q <sub>B</sub>	4	O	Counter 1 B Output
1Q <sub>C</sub>	5	O	Counter 1 B Output
1Q <sub>D</sub>	6	O	Counter 1 B Output
GND	7	G	Ground
2Q <sub>D</sub>	8	O	Counter 2 D Output
2Q <sub>C</sub>	9	O	Counter 2 C Output
2Q <sub>B</sub>	10	O	Counter 2 B Output
2Q <sub>A</sub>	11	O	Counter 2 A Output
2CLR	12	I	Counter 2 Clear Input
2CLK	13	I	Counter 2 Clock Input
V <sub>CC</sub>	14	P	V <sub>CC</sub>

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
V <sub>I</sub>	Input voltage <sup>(1)</sup>	-0.5	7	V
V <sub>O</sub>	Output voltage range applied in high or low state <sup>(1)</sup> <sup>(1)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage range applied in power-off state <sup>(1)</sup>	-0.5	7	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±25	mA
Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>stg</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- This value is limited to 7 V maximum.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-Body Model (A114-A) <sup>(1)</sup>	±2000
		Charged-Device Model (C101) <sup>(2)</sup>	±1000
		Machine Model (A115-A)	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V		V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		-2	
		V <sub>CC</sub> = 3 V to 3.6 V		-6	
		V <sub>CC</sub> = 4.5 V to 5.5 V		-12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2	
		V <sub>CC</sub> = 3 V to 3.6 V		6	
		V <sub>CC</sub> = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V		200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V		100	
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LV393A					UNIT
		D (SOIC)	NS (SOP)	DB (SSOP)	PW (TSSOP)	DGV (TVSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	86	96	127	76	113	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> - 0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			
	I <sub>OH</sub> = -6 mA	3 V	2.48			
	I <sub>OH</sub> = -12 mA	4.5 V	3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V	0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			
	I <sub>OL</sub> = 6 mA	3 V	0.44			
	I <sub>OL</sub> = 12 mA	4.5 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V	±1			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	1.8			pF

## 6.6 Timing Requirements, V<sub>CC</sub> = 2.5 V ± 0.2 V

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted)

			T <sub>A</sub> = 25°C		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t <sub>su</sub>	Setup time	CLR inactive before CLK↓	6		6		ns

## 6.7 Timing Requirements, V<sub>CC</sub> = 3.3 V ± 0.3 V

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted)

			T <sub>A</sub> = 25°C		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t <sub>su</sub>	Setup time	CLR inactive before CLK↓	5		5		ns

## 6.8 Timing Requirements, V<sub>CC</sub> = 5 V ± 0.5 V

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted)

			T <sub>A</sub> = 25°C		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t <sub>su</sub>	Setup time	CLR inactive before CLK↓	4		4		ns

## 6.9 Switching Characteristics, V<sub>CC</sub> = 2.5 V ± 0.2 V

over operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			C <sub>L</sub> = 15 pF	50 <sup>1</sup>	90 <sup>1</sup>		40		MHz
			C <sub>L</sub> = 50 pF	30	70		25		

### 6.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (continued)

over operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	$\overline{\text{CLK}}$	$Q_A$	$C_L = 15\text{ pF}$		7.1 <sup>1</sup>	17.7 <sup>1</sup>	1	20.5	ns
		$Q_B$			8.5 <sup>1</sup>	20.3 <sup>1</sup>	1	23.5	
		$Q_C$			10 <sup>1</sup>	122.5 <sup>1</sup>	1	26	
		$Q_D$			11.1 <sup>1</sup>	24.2 <sup>1</sup>	1	28	
$t_{PHL}$	CLR	$Q_n$		6.7 <sup>1</sup>	14.8 <sup>1</sup>	1	17		
$t_{pd}$	$\overline{\text{CLK}}$	$Q_A$	$C_L = 50\text{ pF}$		9.3	21.3	1	24.5	ns
		$Q_B$			10.9	23.9	1	27.5	
		$Q_C$			12.3	26.1	1	30	
		$Q_D$			13.4	27.8	1	32	
$t_{PHL}$	CLR	$Q_n$		9.1	17.4	1	20		

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 6.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}$	75 <sup>1</sup>	130 <sup>1</sup>		65	MHz	
			$C_L = 50\text{ pF}$	45	105		35		
$t_{pd}$	$\overline{\text{CLK}}$	$Q_A$	$C_L = 15\text{ pF}$		5.1 <sup>1</sup>	13.2 <sup>1</sup>	1	15.5	ns
		$Q_B$			6 <sup>1</sup>	15.8 <sup>1</sup>	1	18.5	
		$Q_C$			7 <sup>1</sup>	18 <sup>1</sup>	1	21	
		$Q_D$			7.7 <sup>1</sup>	19.7 <sup>1</sup>	1	23	
$t_{PHL}$	CLR	$Q_n$		5.1 <sup>1</sup>	12.3 <sup>1</sup>	1	14.5		
$t_{pd}$	$\overline{\text{CLK}}$	$Q_A$	$C_L = 50\text{ pF}$		6.7	16.7	1	19	ns
		$Q_B$			7.8	19.3	1	22	
		$Q_C$			8.7	21.5	1	24.5	
		$Q_D$			9.5	23.2	1	26.5	
$t_{PHL}$	CLR	$Q_n$		6.8	15.8	1	18		

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 6.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}$	125 <sup>1</sup>	185 <sup>1</sup>		105	MHz	
			$C_L = 50\text{ pF}$	85	150		75		
$t_{pd}$	$\overline{\text{CLK}}$	$Q_A$	$C_L = 15\text{ pF}$		3.7 <sup>1</sup>	8.5 <sup>1</sup>	1	10	ns
		$Q_B$			4.3 <sup>1</sup>	9.8 <sup>1</sup>	1	11.5	
		$Q_C$			4.9 <sup>1</sup>	11.2 <sup>1</sup>	1	13	
		$Q_D$			5.3 <sup>1</sup>	12.5 <sup>1</sup>	1	14.5	
$t_{PHL}$	CLR	$Q_n$		3.9 <sup>1</sup>	8.1 <sup>1</sup>	1	9.5		

## 6.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (continued)

over operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	CLK	Q <sub>A</sub>	C <sub>L</sub> = 50 pF		4.9	10.5	1	12	ns
		Q <sub>B</sub>		5.6	11.8	1	13.5		
		Q <sub>C</sub>		6.2	13.2	1	15		
		Q <sub>D</sub>		6.6	14.5	1	16.5		
$t_{PHL}$	CLR	Q <sub>n</sub>		5.2	10.1	1	11.5		

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.12 Timing Diagrams

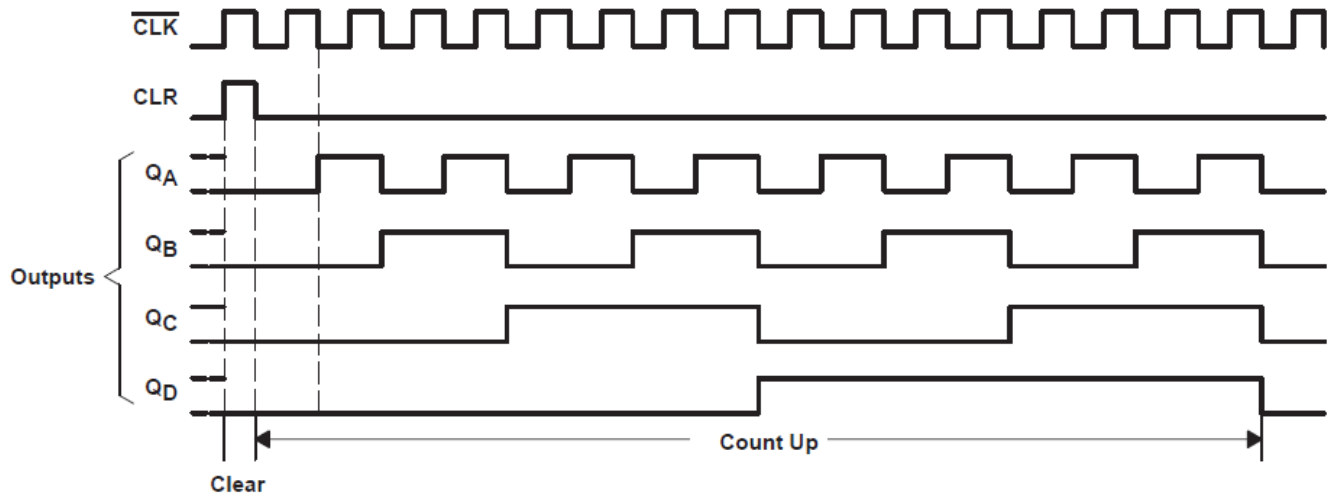


Figure 6-1. Timing Diagram

## 6.13 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER <sup>(1)</sup>		SN74LV393A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.2	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics for surface-mount packages only.

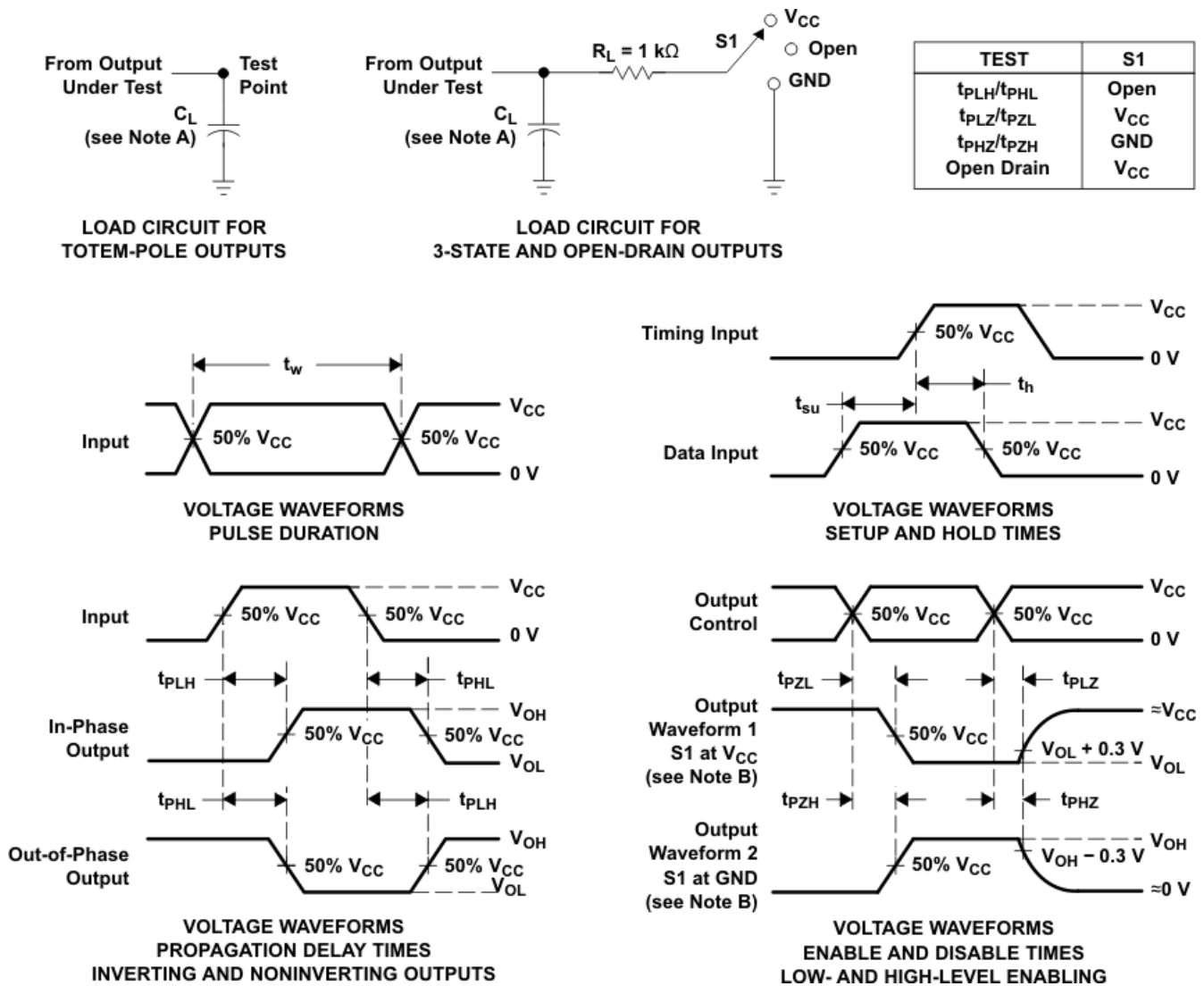
## 6.14 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance (outputs enabled)	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	15.2	pF
			5 V	17.3	



## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns, and  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

These devices comprise two independent 4-bit binary counters, each having a clear (CLR) and a clock ( $\overline{\text{CLK}}$ ) input. These devices change state on the negative-going transition of the  $\overline{\text{CLK}}$  pulse. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The 'LV393A devices have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

These devices are fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### 8.2 Functional Block Diagram

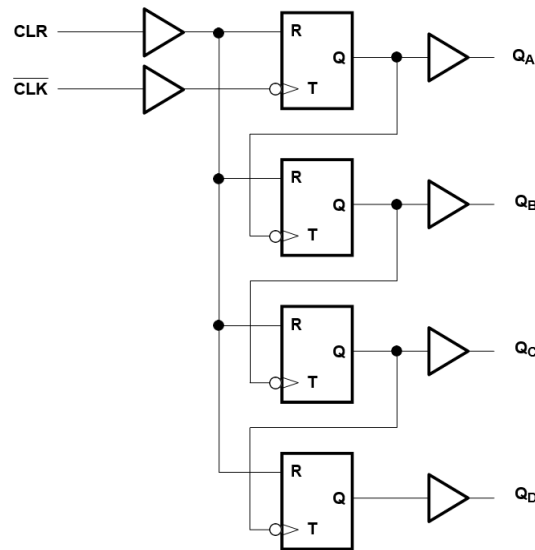


Figure 8-1. Logic Diagram, Each Counter (Positive Logic)

### 8.3 Device Functional Modes

Table 8-1. Function Table

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu\text{F}$  capacitor; if there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

### 9.2 Layout

#### 9.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

##### 9.2.1.1 Layout Example

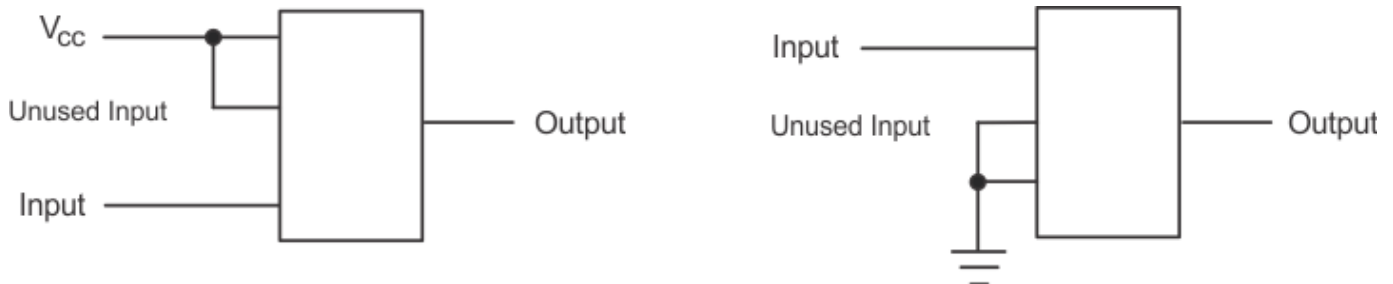


Figure 9-1. Layout Diagram

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 10-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV393A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV393AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	LV393A	
SN74LV393ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV393A	Samples
SN74LV393APW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	LV393A	
SN74LV393APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV393A :**

- Automotive : [SN74LV393A-Q1](#)
- Enhanced Product : [SN74LV393A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV393ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV393ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV393ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV393ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV393APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV393APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV393APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV393APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV393ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV393ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV393ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV393ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV393APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV393APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV393APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV393APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0





4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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