

SN74LV4051A-Q1 Automotive 8-Channel Analog Multiplexer or Demultiplexer

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- 1.65V to 5.5V V_{CC} operation
- Supports mixed-mode voltage operation on all ports
- High on-off output-voltage ratio
- Low crosstalk between switches
- Individual switch controls
- Extremely low input current
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Applications

- [Automotive infotainment and cluster](#)
- [Telematics, eCall](#)

3 Description

This 8-channel CMOS analog multiplexer and demultiplexer is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LV4051A-Q1 handles analog and digital signals. Each channel permits signals with amplitudes up to 5.5V (peak) to be transmitted in either direction.

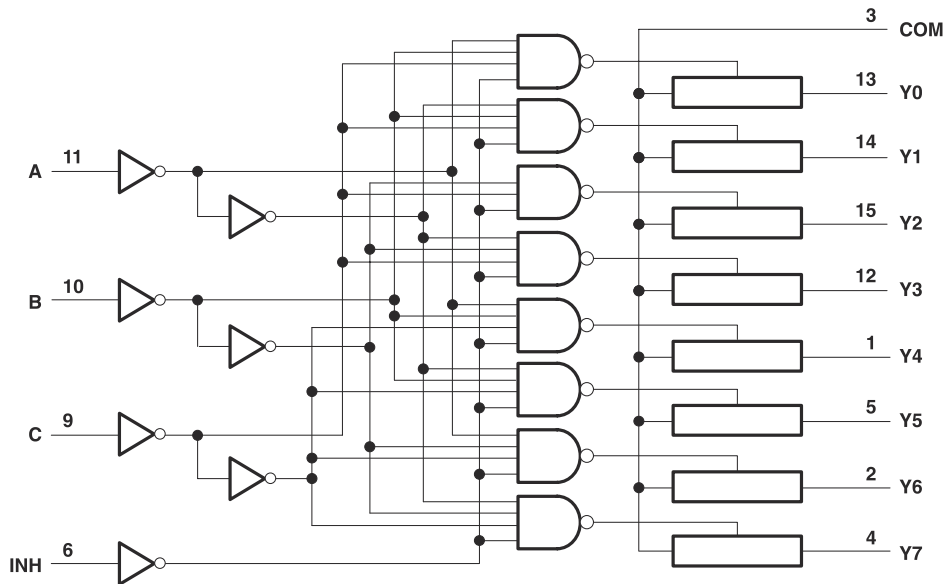
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN74LV4051A-Q1	PW (TSSOP, 16)	5mm × 6.4mm
	D (SOIC, 16)	9.9mm × 6mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

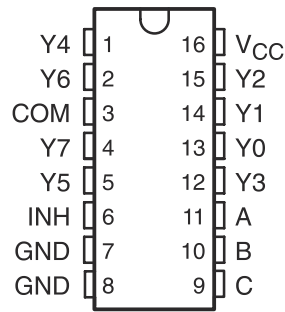


Figure 4-1. D or PW Package, 16-Pin SOIC or TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
Y4	1	I ⁽²⁾	Input to mux
Y6	2	I ⁽²⁾	Input to mux
COM	3	O ⁽²⁾	Output of mux
Y7	4	I ⁽²⁾	Input to mux
Y5	5	I ⁽²⁾	Input to mux
INH	6	I ⁽²⁾	Enables the outputs of the device. Logic low level will turn the outputs on, high level will turn them off.
GND	7	—	Ground
GND	8	—	Ground
C	9	I	Selector line for outputs (see Section 7.4 for specific information)
B	10	I	Selector line for outputs (see Section 7.4 for specific information)
A	11	I	Selector line for outputs (see Section 7.4 for specific information)
Y3	12	I ⁽²⁾	Input to mux
Y0	13	I ⁽²⁾	Input to mux
Y1	14	I ⁽²⁾	Input to mux
Y2	15	I ⁽²⁾	Input to mux
Vcc	16	I	Device power input

(1) I = input, O = output

(2) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins Y0-Y7 may be considered outputs (O) and the COM pin may be considered inputs (I).

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7.0	V
V _I	Logic input voltage range	-0.5	7.0	V
V _{IO}	Switch I/O voltage range ^{(2) (3)}	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		mA
I _{IOK}	Switch IO diode clamp current	V _{IO} < 0 or V _{IO} > V _{CC}		mA
I _T	Switch continuous current	V _{IO} = 0 to V _{CC}	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5V maximum

5.2 ESD Ratings

				VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	All pins	±2000	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	All pins	±500	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information: SN74LV4051A-Q1

THERMAL METRIC ⁽¹⁾		SN74LV4051A-Q1	UNIT
		PW (TSSOP)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	140.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	72.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	98.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	13.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	97.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	1 ⁽²⁾		5.5	V
V _{IH}	High-level input voltage, logic control inputs	V _{CC} = 1.65		5.5	V
		V _{CC} = 2V		5.5	
		V _{CC} = 2.3V to 2.7V	V _{CC} × 0.7	5.5	
		V _{CC} = 3V to 3.6V	V _{CC} × 0.7	5.5	
		V _{CC} = 4.5V to 5.5V	V _{CC} × 0.7	5.5	
V _{IL}	Low-level input voltage, logic control inputs	V _{CC} = 1.65V to 2.7V	0	0.4	V
		V _{CC} = 1.65V to 2.7V	0	0.5	
		V _{CC} = 1.65V to 2.7V	0	V _{CC} × 0.3	
		V _{CC} = 3V to 3.6V	0	V _{CC} × 0.3	
		V _{CC} = 4.5V to 5.5V	0	V _{CC} × 0.3	
V _I	Logic control input voltage	0		5.5	V
V _{IO}	Switch input or output voltage	0		V _{CC}	V
Δt/ΔV	Logic input transition rise or fall rate	V _{CC} = 1.0V to 2.0V		500	ns/V
		V _{CC} = 2.0V to 2.7V		200	
		V _{CC} = 3V to 3.6V		100	
		V _{CC} = 4.5V to 5.5V		20	
T _A	Ambient temperature	−40		125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
- (2) When using a V_{CC} of ≤1.2 V, it is recommended to use these devices only for transmitting digital signals. When supply voltage is near 1.2 V the analog switch ON resistance becomes very non-linear

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT	
r _{ON}	ON-state switch resistance	I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	1.65V	25°C		60	150	Ω
				−40°C to 85°C			225	
				−40°C to 125°C			225	
			2.3V	25°C		38	180	
				−40°C to 85°C			225	
				−40°C to 125°C			225	
			3V	25°C		30	150	
				−40°C to 85°C			190	
				−40°C to 125°C			190	
			4.5V	25°C		22	75	
				−40°C to 85°C			100	
				−40°C to 125°C			100	

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON(p)}	Peak ON-state resistance	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65V		220	600	Ω
			-40°C to 85°C				700	
			-40°C to 125°C				700	
			25°C	2.3V		113	500	
			-40°C to 85°C				600	
			-40°C to 125°C				600	
			25°C	3V		54	180	
			-40°C to 85°C				225	
			-40°C to 125°C				225	
			25°C	4.5V		31	100	
			-40°C to 85°C				125	
			-40°C to 125°C				125	
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65V				Ω
			-40°C to 85°C					
			-40°C to 85°C					
			-40°C to 85°C	2.3V		2.1	30	
			-40°C to 85°C				40	
			-40°C to 125°C				40	
			25°C	3V		1.4	20	
			-40°C to 85°C				30	
			-40°C to 125°C				30	
			25°C	4.5V		1.3	15	
			-40°C to 85°C				20	
			-40°C to 125°C				20	
I _{IH} I _{IL}	Control input current	V _I = 5.5V or GND	25°C	0 to 5.5V	-0.1		0.1	μA
			-40°C to 85°C		-1		1	
			-40°C to 125°C		-2		2	
I _{S(off)}	OFF-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH}	25°C	5.5V	-0.1		0.1	μA
			-40°C to 85°C		-1		1	
			-40°C to 125°C		-2		2	
I _{S(on)}	ON-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL}	25°C	5.5V	-0.1		0.1	μA
			-40°C to 85°C		-1		1	
			-40°C to 125°C		-2		2	
I _{CC}	Supply current	V _I = V _{CC} or GND V _{INH} = 0V	25°C	5.5V				μA
			-40°C to 85°C				20	
			-40°C to 125°C				40	
C _{IC}	Control input capacitance	f = 10MHz	25°C	3.3V		2		pF
C _{IS}	Common terminal capacitance	f = 10MHz	25°C	3.3V		23.4		pF
C _{OS}	Switch terminal capacitance	f = 10MHz	25°C	3.3V		5.7		pF
C _F	Feedthrough capacitance	f = 10MHz	25°C	3.3V		0.5		pF

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
C _{PD}	Power dissipation capacitance	C _L = 50pF, f = 10MHz	25°C	3.3V		5.9		pF

5.6 Timing Characteristics V_{CC} = 2.5V ± 0.2V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15pF	25°C		1.9	10	ns
					-40°C to 85°C			16	
					-40°C to 125°C			18	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15pF	25°C		6.6	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15pF	25°C		7.4	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50pF	25°C		3.8	12	ns
					-40°C to 85°C			18	
					-40°C to 125°C			20	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 50pF	25°C		7.8	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 50pF	25°C		11.5	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	

5.7 Timing Characteristics V_{CC} = 3.3V ± 0.3V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50pF	25°C		2.5	9	ns
					-40°C to 85°C			12	
					-40°C to 125°C			14	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 50pF	25°C		5.5	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 50pF	25°C		8.8	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	

5.8 Timing Characteristics V_{CC} = 5V ± 0.5V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50pF	25°C		1.5	6	ns
					-40°C to 85°C			8	
					-40°C to 125°C			10	

5.8 Timing Characteristics $V_{CC} = 5V \pm 0.5V$ (continued)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		4	14	ns
					-40°C to 85°C			18	
					-40°C to 125°C			18	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		6.2	14	ns
					-40°C to 85°C			18	
					-40°C to 125°C			18	

5.9 AC Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	SN74LV4051	$C_L = 50pF$, $R_L = 600\Omega$, $F_{in} = 1MHz$ (sine wave)	$V_{CC} = 2.3V$		20	MHz	
					$V_{CC} = 3V$		25		
					$V_{CC} = 4.5V$		35		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	ALL	$C_L = 50pF$, $R_L = 600\Omega$, $F_{in} = 1MHz$ (sine wave)	$V_{CC} = 2.3V$		-45	dB	
					$V_{CC} = 3V$		-45		
					$V_{CC} = 4.5V$		-45		
Crosstalk (between any switches)	COM or Yn	Yn or COM	ALL	$C_L = 50pF$, $R_L = 600\Omega$, $F_{in} = 1MHz$ (sine wave)	$V_{CC} = 2.3V$		20	mV	
					$V_{CC} = 3V$		35		
					$V_{CC} = 4.5V$		60		
Sine-wave distortion	COM or Yn	Yn or COM	ALL	$C_L = 50pF$, $R_L = 10k\Omega$, $F_{in} = 1kHz$ (sine wave)	$V_I = 2V_{p-p}$ $V_{CC} = 2.3V$		0.1	%	
					$V_I = 2.5V_{p-p}$ $V_{CC} = 3V$		0.1		
					$V_I = 4V_{p-p}$ $V_{CC} = 4.5V$		0.1		

6 Parameter Measurement Information

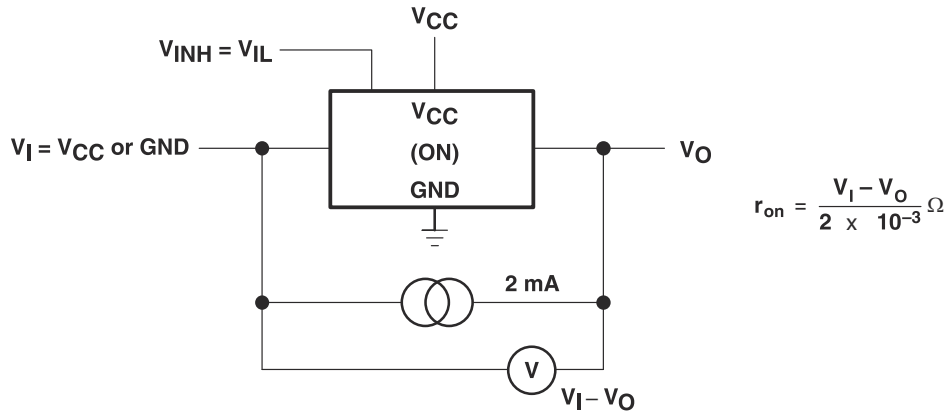


Figure 6-1. On-State Resistance Test Circuit

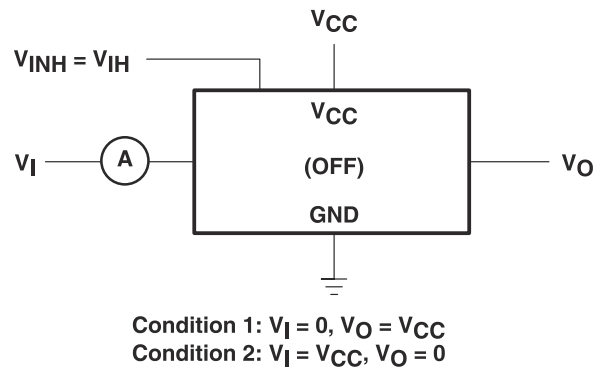


Figure 6-2. Off-State Switch Leakage-Current Test Circuit

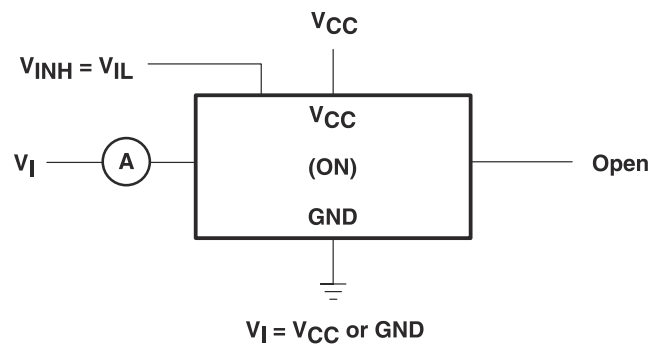


Figure 6-3. On-State Switch Leakage-Current Test Circuit

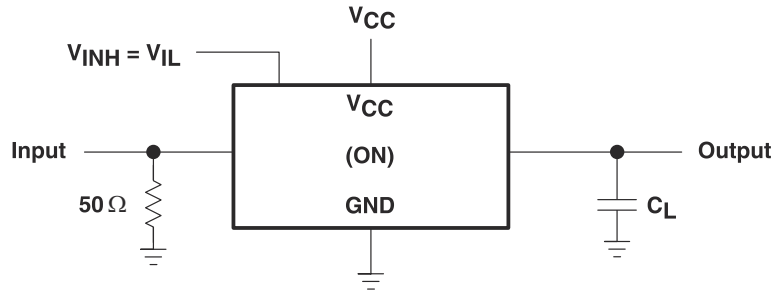
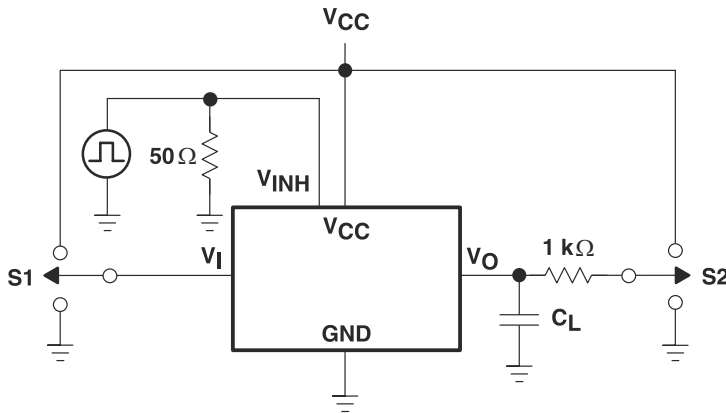


Figure 6-4. Propagation Delay Time, Signal Input to Signal Output



TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

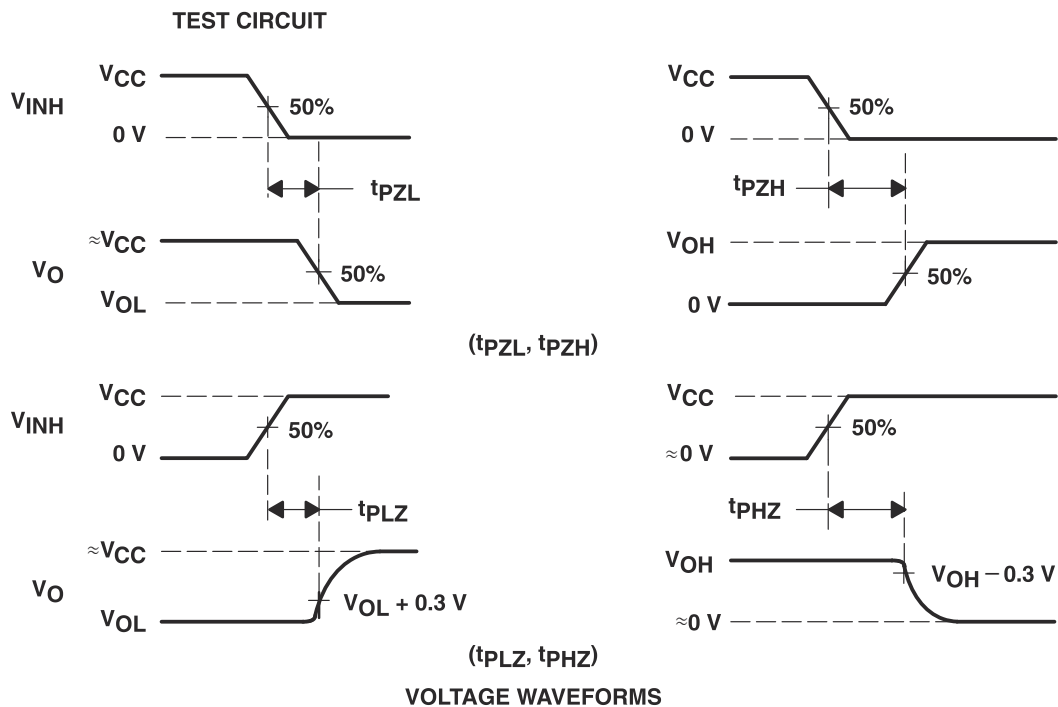
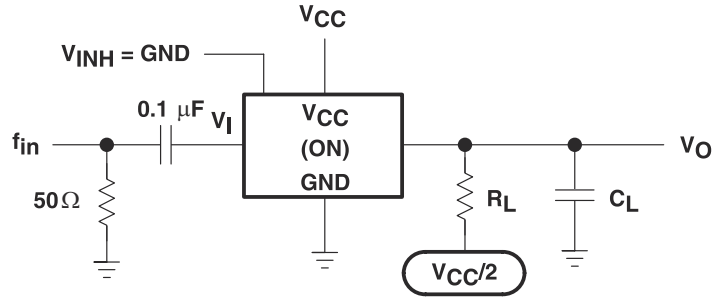


Figure 6-5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6-6. Frequency Response (Switch On)

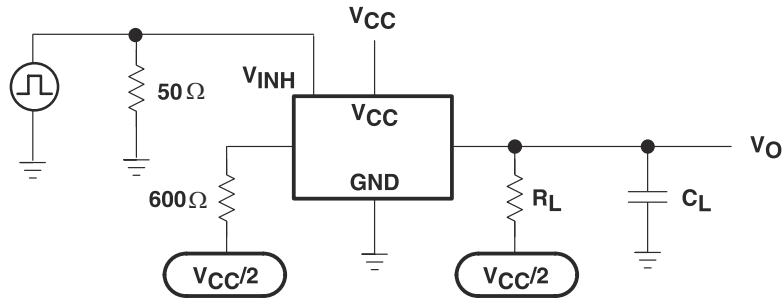


Figure 6-7. Crosstalk (Control Input, Switch Output)

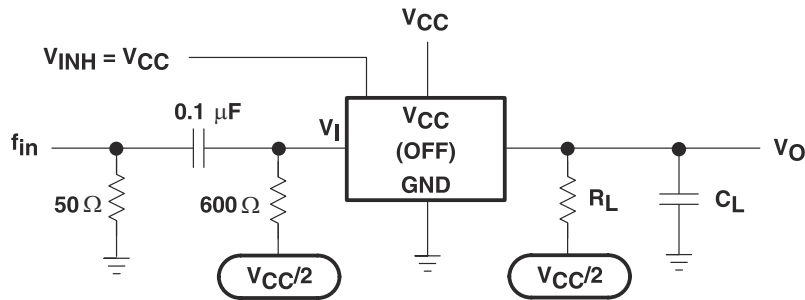


Figure 6-8. Feedthrough Attenuation (Switch Off)

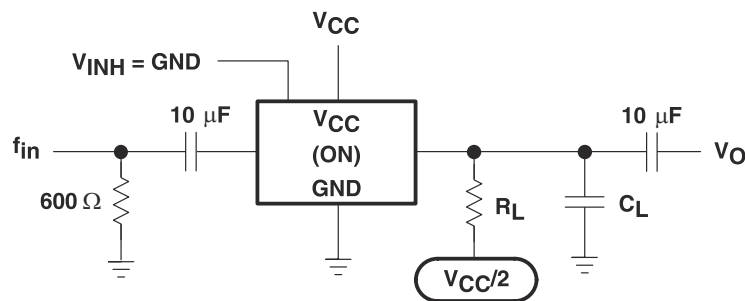


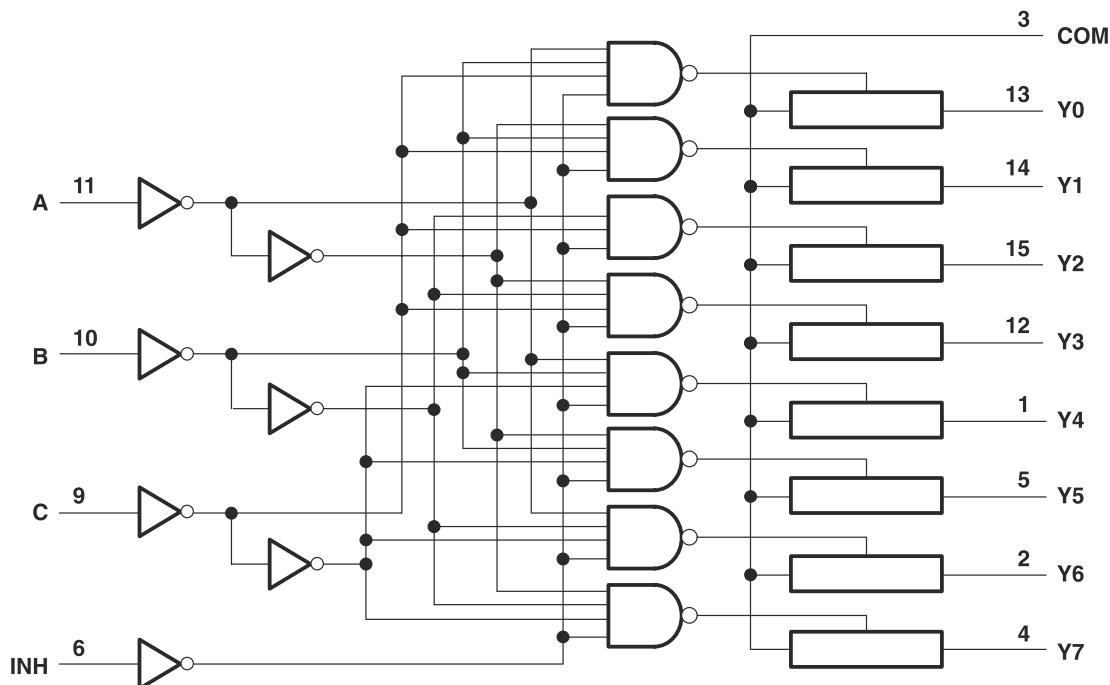
Figure 6-9. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

This device is an 8-channel analog multiplexer. A multiplexer is used when several signals must share the same device or resource. This device allows the selection of one of these signals at a time, for analysis or propagation.

7.2 Functional Block Diagram



7.3 Feature Description

This device contains one 8-channel multiplexer for use in a variety of applications, and can also be configured as demultiplexer by using the COM pin as an input and the Yx pins as outputs. This device is qualified for automotive applications and has an extended temperature range of -40°C to 125°C (maximum depends on package type).

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A multiplexer is used in applications where multiple signals share a resource. In the example below, several different sensors are connected to the analog-to-digital converter (ADC) of a microcontroller unit (MCU).

8.2 Typical Application

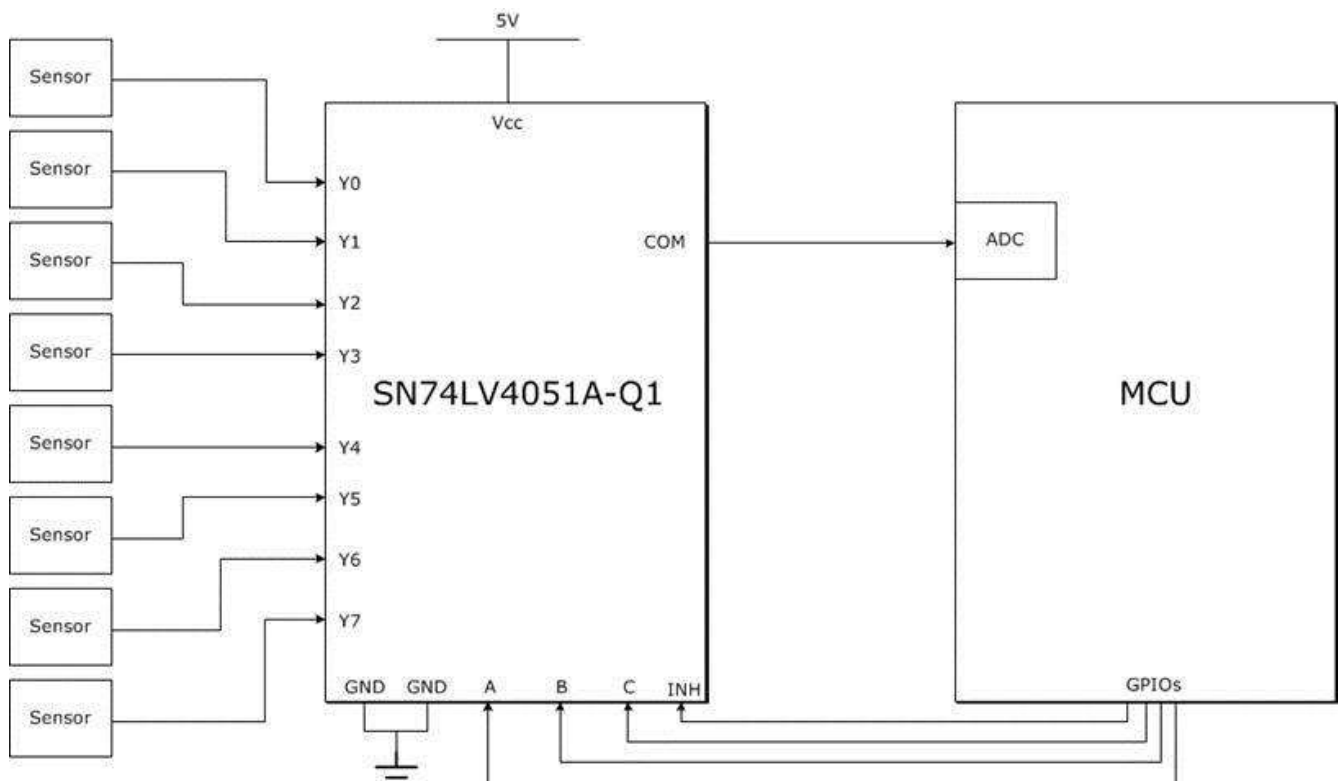


Figure 8-1. Example of Multiplexer Use With Analog Sensors and the ADC of an MCU

8.2.1 Design Requirements

Designing with the SN74LV4051A-Q1 device requires a stable input voltage between 2 V (see *Recommended Operating Conditions* for details) and 5.5V. Another important design consideration are the characteristics of the signal being multiplexed—ensure no important information is lost due to timing or incompatibility with this device.

8.2.2 Detailed Design Procedure

Processing eight different analog signals would normally require eight separate ADCs, but [Figure 8-1](#) shows how to achieve this using only one ADC and four GPIOs (general-purpose input/outputs).

8.3 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the Vcc pin of this device. If this is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher voltage rail.

8.4 Layout

8.4.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are more than 1 inch long. These traces must be designed with a characteristic impedance of either 50Ω or 75Ω, as required by the application. Do not place this device too close to high-voltage switching components, as they may cause interference.

8.4.2 Layout Example

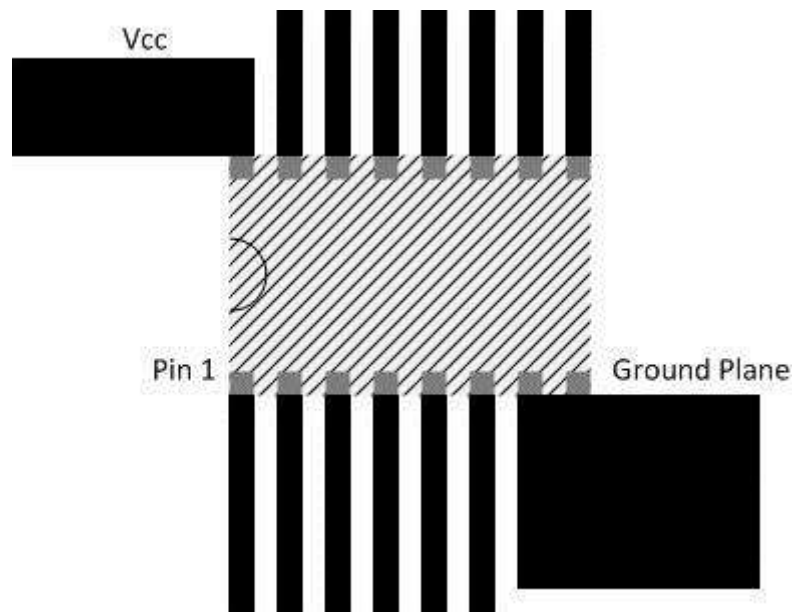


Figure 8-2. Layout Schematic

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2015) to Revision F (June 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated the <i>Package Information</i> table to include package lead size.....	1
• Added new VIH and VIL Specifications at 1.65V Vcc.....	5
• Added Ron, Ron Peak, and Delta Ron Specifications at 1.65V Vcc.....	5

Changes from Revision D (June 2011) to Revision E (January 2015)	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes, Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLV4051ATDWRG4Q1	NRND	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ	
SN74LV4051AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4051AQ1	Samples
SN74LV4051ATDRQ1	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ	
SN74LV4051ATDWRQ1	NRND	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ	
SN74LV4051ATPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4051A-Q1 :

- Catalog : [SN74LV4051A](#)
- Enhanced Product : [SN74LV4051A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLV4051ATDWRG4Q1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CLV4051ATPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051ATDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN74LV4051ATPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLV4051ATDWRG4Q1	SOIC	DW	16	2000	350.0	350.0	43.0
CLV4051ATPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4051AQPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV4051ATDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
SN74LV4051ATPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



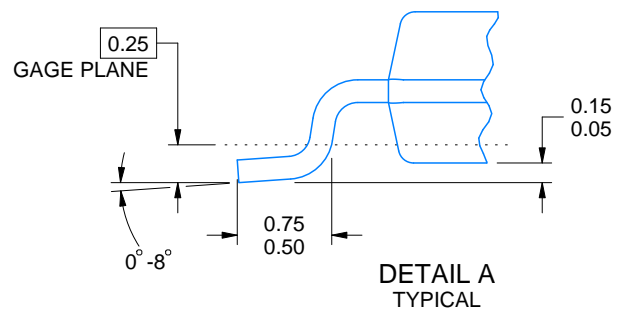
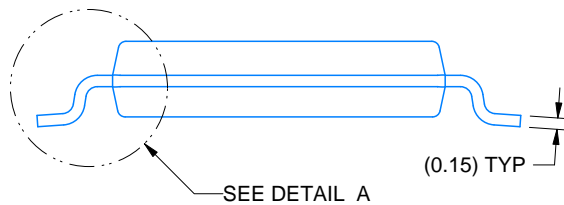
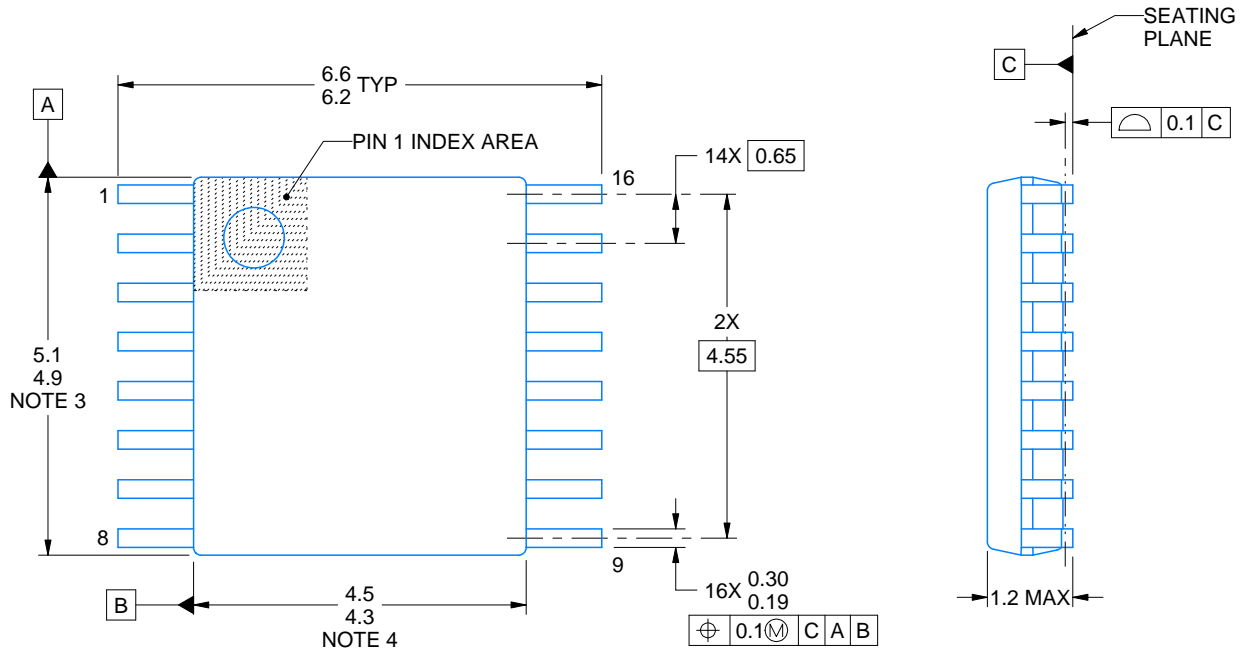
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

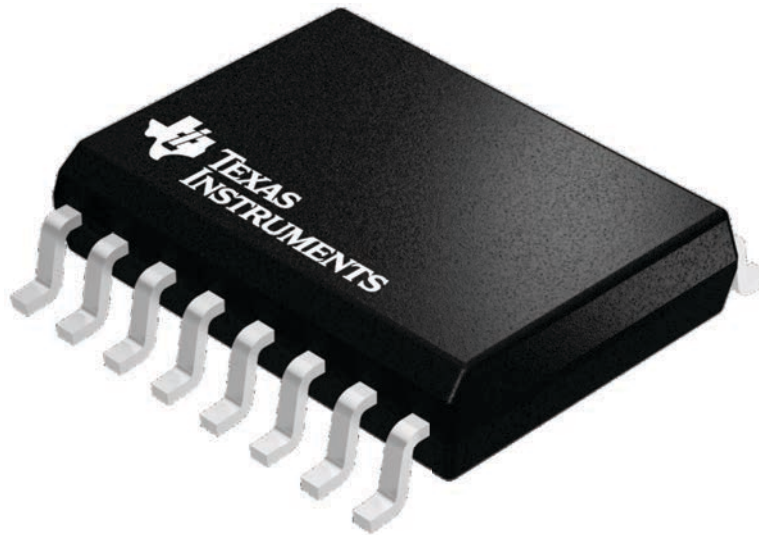
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A



DW0016A

PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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