

SN74LV6T06-Q1 Automotive Hex Open-Drain Inverters with Integrated Translation

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- Available in *wettable flank* QFN package
- Wide operating range of 1.65 V to 5.5 V
- 5.5-V tolerant input pins
- *LVxT enhanced inputs* combined with *open-drain outputs* provide maximum voltage translation flexibility:
 - Over 6.67-Mbps operation, ($R_{PU} = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$)
 - Up translation from 1.2 V to 5 V with 1.8-V supply
 - Down translation from 5 V to 0.8 V or even less with any valid supply
- 5.5-V tolerant input pins
- Supports standard function pinout
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- [Enable or disable a digital signal](#)
- [Controlling an indicator LED](#)
- [Translation between communication modules and system controllers](#)

3 Description

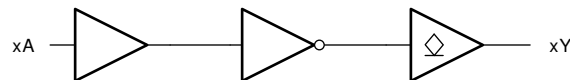
The SN74LV6T06-Q1 device contains six independent inverters with open-drain outputs. Each inverter performs the Boolean function $Y = \bar{A}$ in positive logic.

The input is designed with a lower threshold circuit to support up translation for lower voltage CMOS inputs (for example, 1.2 V input to 1.8 V output or 1.8 V input to 3.3 V output). In addition, the 5-V tolerant input pins enable down translation (for example, 3.3 V to 2.5 V output).

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM) ⁽³⁾
SN74LV6T06-Q1	BQA (WQFN, 14)	3 mm × 2.5 mm	3 mm × 2.5 mm
	PW (TSSOP, 14)	5 mm × 6.4 mm	5 mm × 4.4 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Simplified Logic Diagram (Positive Logic)

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4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

5 Pin Configuration and Functions

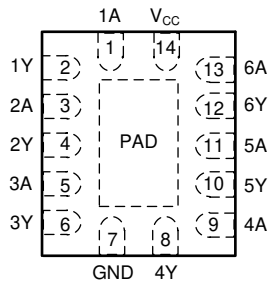


Figure 5-1. SN74LV6T06-Q1 BQA Package, 14-Pin WQFN (Top View)

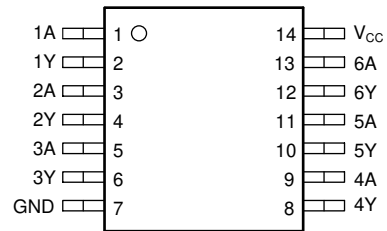


Figure 5-2. SN74LV6T06-Q1 PW Package, 14-Pin TSSOP (Top View)

Table 5-1. Pin Functions

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	BQA	PW		
1A	1	1	I	Channel 1, A input
1Y	2	2	O	Channel 1, Y output
2A	3	3	I	Channel 2, A input
2Y	4	4	O	Channel 2, Y output
3A	5	5	I	Channel 3, A input
3Y	6	6	O	Channel 3, Y output
GND	7	7	G	Ground
4Y	8	8	O	Channel 4, Y output
4A	9	9	I	Channel 4, A input A
5Y	10	10	O	Channel 5, Y output
5A	11	11	I	Channel 5, A input
6Y	12	12	O	Channel 6, Y output
6A	13	13	I	Channel 6, A input
V _{CC}	14	14	P	Positive supply
Thermal Pad ⁽²⁾			—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

(2) BQA package only.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Output voltage range ⁽²⁾	-0.5	7	V
I _{IK}	Input clamp current	V _I < -0.5 V	-20	mA
I _{OK}	Output clamp current	V _O < -0.5 V	-20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	5.5	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage in the high-impedance state		0	5.5	V
V _O	Output voltage in the active state		0	V _{CC}	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 2 V	1.1		V
		V _{CC} = 2.25 V to 2.75 V	1.28		
		V _{CC} = 3 V to 3.6 V	1.45		
		V _{CC} = 4.5 V to 5.5 V	2		
V _{IL}	Low-Level input voltage	V _{CC} = 1.65 V to 2 V		0.5	V
		V _{CC} = 2.25 V to 2.75 V		0.65	
		V _{CC} = 3 V to 3.6 V		0.75	
		V _{CC} = 4.5 V to 5.5 V		0.85	
I _O	Output current	V _{CC} = 1.65 V to 2 V		3	mA
		V _{CC} = 2.25 V to 2.75 V		7	
		V _{CC} = 3.3 V to 5.0 V		15	
Δt/Δv	Input transition rise or fall rate			20	ns/V
T _A	Operating free-air temperature		-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		BQA (WQFN)	PW (TSSOP)	UNIT
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	88.3	151.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	90.9	80.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.8	94.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	9.9	28.0	°C/W
Y _{JB}	Junction-to-board characterization parameter	56.7	93.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	33.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OL}	I _{OL} = 50 μA	1.65 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	1.65 V to 2 V		0.1 ⁽¹⁾	0.2		0.25		
	I _{OL} = 3 mA	2.25 V to 2.75 V		0.1 ⁽¹⁾	0.15		0.2		
	I _{OL} = 5.5 mA	3 V to 3.6 V		0.2 ⁽¹⁾	0.2		0.25		
	I _{OL} = 8 mA	4.5 V to 5.5 V		0.3 ⁽¹⁾	0.3		0.35		
I _{OZ}	V _O = V _{CC} or GND and V _{CC} = 5.5 V	5.5 V			±0.25		±2.5	μA	
I _I	V _I = 0 V or V _{CC}	0 V to 5.5 V			±0.1		±1	μA	
I _{CC}	V _I = 0 V or V _{CC} , I _O = 0; open on loading	1.65 V to 5.5 V			2		20	μA	
ΔI _{CC}	One input at 0.3 V or 3.4 V, other inputs at 0 or V _{CC} , I _O = 0	5.5 V			1.35		1.5	mA	
	One input at 0.3 V or 1.1 V, other inputs at 0 or V _{CC} , I _O = 0	1.8 V			10		20	μA	
C _I	V _I = V _{CC} or GND	5 V			4	10		pF	
C _O	V _O = V _{CC} or GND	5 V			3			pF	
C _{PD}	No load, F = 1 MHz	5 V			14			pF	

(1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)

6.6 Switching Characteristics

$C_L = 50\text{ pF}$; over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PZL}	A	Y	$C_L = 15\text{ pF}$	1.8 V	10.7	23	1	26.6	ns		
t_{PLZ}	A	Y	$C_L = 15\text{ pF}$	1.8 V	10.7	23	1	26.6	ns		
t_{PZL}	A	Y	$C_L = 50\text{ pF}$	1.8 V	15	28	1	32	ns		
t_{PLZ}	A	Y	$C_L = 50\text{ pF}$	1.8 V	15	28	1	32	ns		
t_{PZL}	A	Y	$C_L = 15\text{ pF}$	2.5 V	7.3	12.9	1	15.9	ns		
t_{PLZ}	A	Y	$C_L = 15\text{ pF}$	2.5 V	7.3	12.9	1	15.9	ns		
t_{PZL}	A	Y	$C_L = 50\text{ pF}$	2.5 V	9.9	16.3	1	18.8	ns		
t_{PLZ}	A	Y	$C_L = 50\text{ pF}$	2.5 V	9.9	16.3	1	18.8	ns		
t_{PZL}	A	Y	$C_L = 15\text{ pF}$	3.3 V	5.6	9.7	1	11.9	ns		
t_{PLZ}	A	Y	$C_L = 15\text{ pF}$	3.3 V	5.6	9.7	1	11.9	ns		
t_{PZL}	A	Y	$C_L = 50\text{ pF}$	3.3 V	7.7	12.3	1	14.8	ns		
t_{PLZ}	A	Y	$C_L = 50\text{ pF}$	3.3 V	7.7	12.3	1	14.8	ns		
t_{PZL}	A	Y	$C_L = 15\text{ pF}$	5 V	4.3	7.2	1	9.1	ns		
t_{PLZ}	A	Y	$C_L = 15\text{ pF}$	5 V	4.3	7.2	1	9.1	ns		
t_{PZL}	A	Y	$C_L = 50\text{ pF}$	5 V	5.9	9.4	1	11.5	ns		
t_{PLZ}	A	Y	$C_L = 50\text{ pF}$	5 V	5.9	9.4	1	11.5	ns		

6.7 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.1			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.5	V

6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

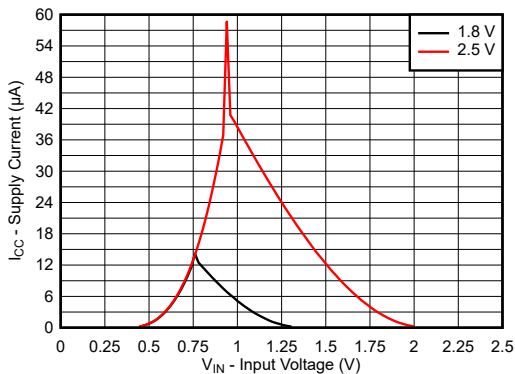


Figure 6-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

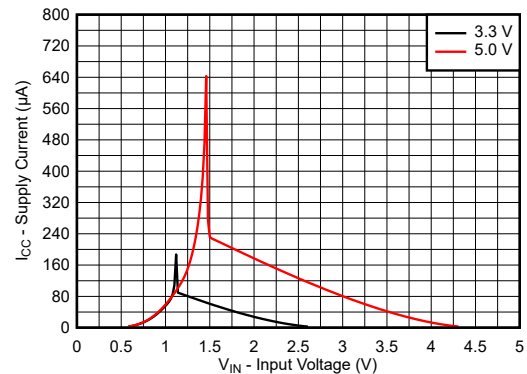


Figure 6-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply

6.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

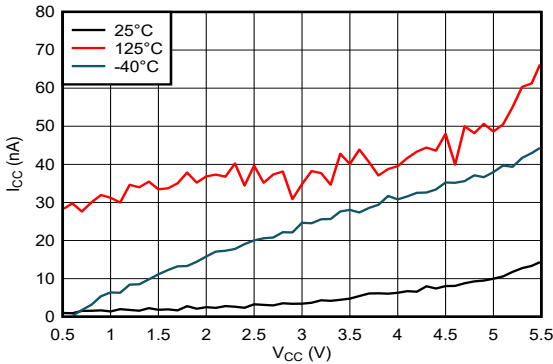


Figure 6-3. Supply Current Across Supply Voltage

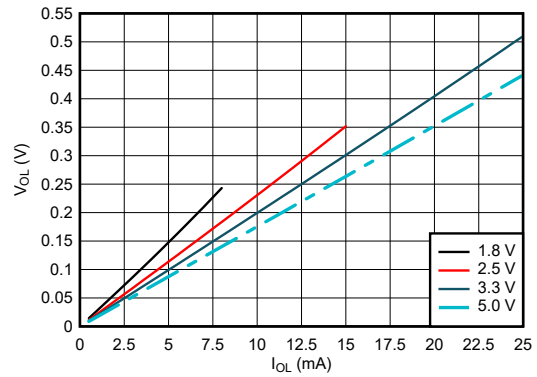


Figure 6-4. Output Voltage vs Current in LOW State

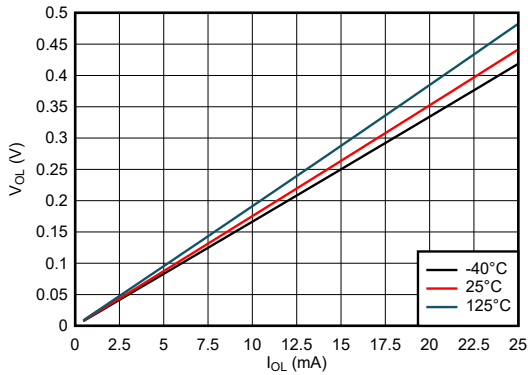


Figure 6-5. Output Voltage vs Current in LOW State; 5-V Supply

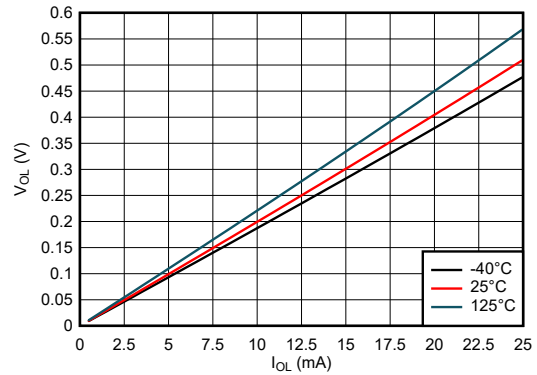


Figure 6-6. Output Voltage vs Current in LOW State; 3.3-V Supply

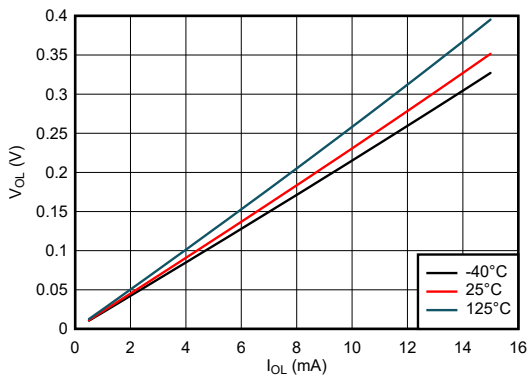


Figure 6-7. Output Voltage vs Current in LOW State; 2.5-V Supply

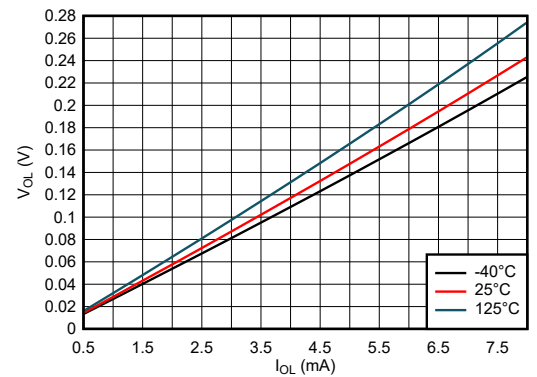


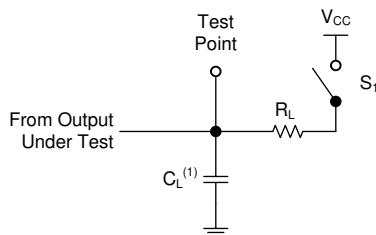
Figure 6-8. Output Voltage vs Current in LOW State; 1.8-V Supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

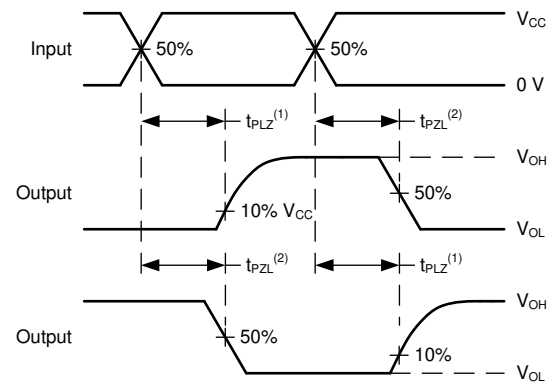
The outputs are measured individually with one input transition per measurement.

TEST	S1	R _L	C _L	ΔV	V _{CC}
t _{PLZ} , t _{PZL}	CLOSED	1 kΩ	15 pF, 50 pF	0.15 V	≤ 2.5 V
t _{PLZ} , t _{PZL}	CLOSED	1 kΩ	15 pF, 50 pF	0.3 V	> 2.5 V



(1) C_L includes probe and test-fixture capacitance.

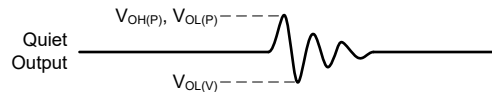
Figure 7-1. Load Circuit for Open-Drain Outputs



(1) t_{PLZ} is the same as t_{dis}.

(2) t_{PZL} is the same as t_{en}.

Figure 7-2. Voltage Waveforms Propagation Delays



Noise values measured with all other outputs simultaneously switching.

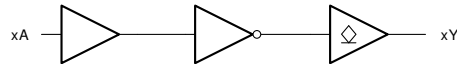
Figure 7-3. Voltage Waveforms, Noise

8 Detailed Description

8.1 Overview

The SN74LV6T06-Q1 device contains six independent inverters with open-drain outputs. Each inverter performs the Boolean function $Y = \bar{A}$ in positive logic.

8.2 Functional Block Diagram



One of six identical channels

8.3 Feature Description

8.3.1 Open-Drain CMOS Outputs

This device includes open-drain CMOS outputs. Open-drain outputs can only drive the output low. When in the high logical state, open-drain outputs will be in a high-impedance state. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10 k Ω resistor can be used to meet these requirements.

Unused open-drain CMOS outputs should be left disconnected.

8.3.2 LVxT Enhanced Input Voltage

The SN74LV6T06-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. For proper functionality, input signals must remain at or above the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. [Figure 8-1](#) shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Input signals must transition between valid logic states quickly, as defined by the input transition rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-k Ω resistor is recommended and will typically meet all requirements.

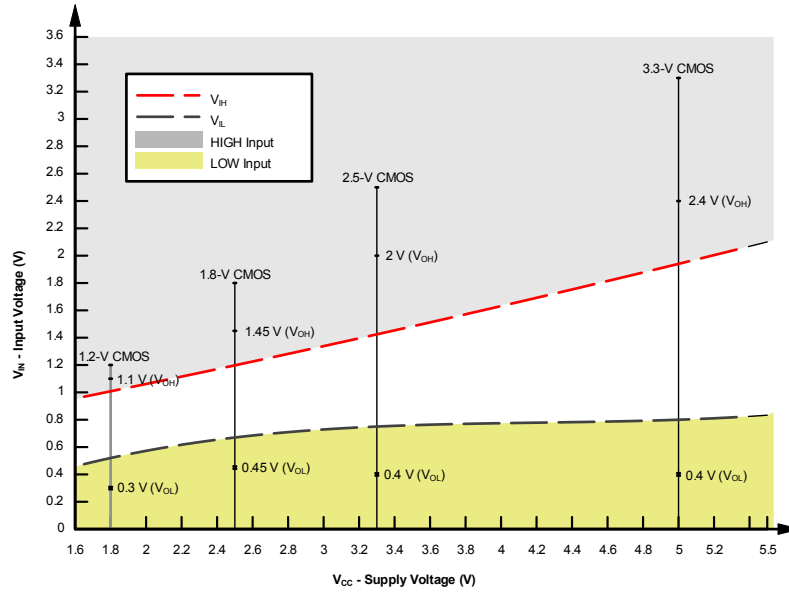


Figure 8-1. LVxT Input Voltage Levels

8.3.3 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

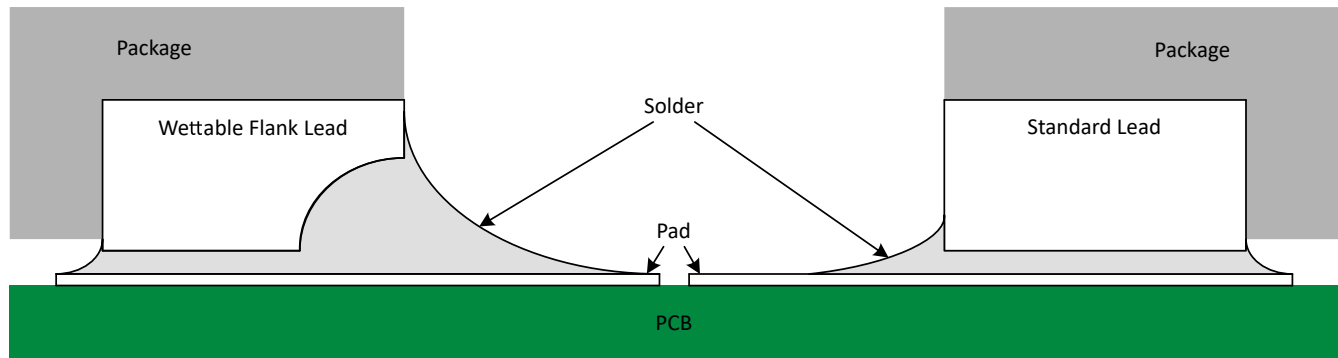


Figure 8-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 8-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

8.3.4 Clamp Diode Structure

Figure 8-3 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

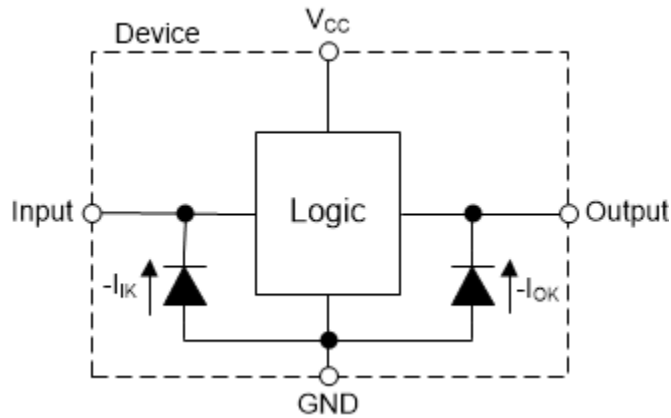


Figure 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74LV6T06-Q1.

Table 8-1. Function Table

INPUT A ⁽¹⁾	OUTPUT Y ⁽²⁾
H	L
L	Z

- (1) H = high voltage level, L = low voltage level, X = do not care
 (2) H = driving high, L = driving low, Z = high impedance

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV6T06-Q1 can be used to drive LEDs with control from very low voltage sources. The supply voltage of the SN74LV6T06-Q1 can be set as low as 1.8 V (± 0.15 V), which allows for controlling an LED powered by up to 5 V with an input voltage as low as 1.2 V. As an example, with a 1.8 V SN74LV6T06-Q1 supply voltage, the output of the SN74LV6T06-Q1 is expected to have an equivalent low-state resistance of 30 Ω ($R_{OL} = V_{OL} / I_{OL} = 0.15$ V / 5 mA, from the *Typical Characteristics*). Therefore the calculation of the current limiting resistor is:

$$R_1 = \frac{V_{PU} - V_F}{I_D} - 30 \quad (1)$$

with V_{PU} shown in Equation 1 as the diode pull-up voltage (separate from the device supply voltage, V_{CC}), V_F as the diode forward voltage, and I_D as the desired diode current.

9.2 Typical Application

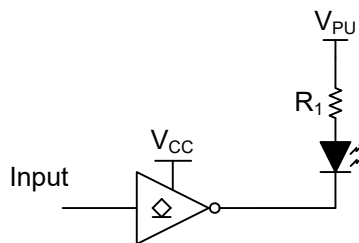


Figure 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV6T06-Q1 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV6T06-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV6T06-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation](#) application note.

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#) application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV6T06-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74LV6T06-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV6T06-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

9.2.3 Application Curves

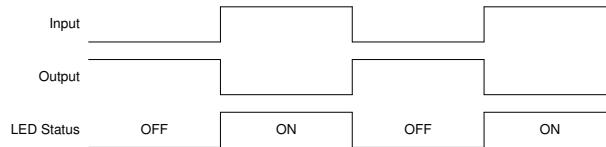


Figure 9-2. Application Timing Diagram

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

9.4.2 Layout Example

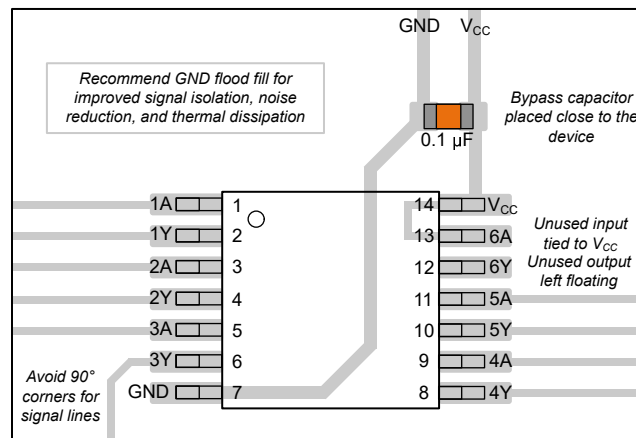


Figure 9-3. Example Layout for the SN74LV6T06-Q1

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV6T06QPWRQ1	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT06Q	Samples
SN74LV6T06QWBQARQ1	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT06Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV6T06-Q1 :

- Catalog : [SN74LV6T06](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV6T06QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV6T06QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV6T06QPWRQ1	TSSOP	PW	14	3000	356.0	356.0	35.0
SN74LV6T06QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

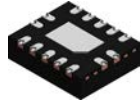
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A

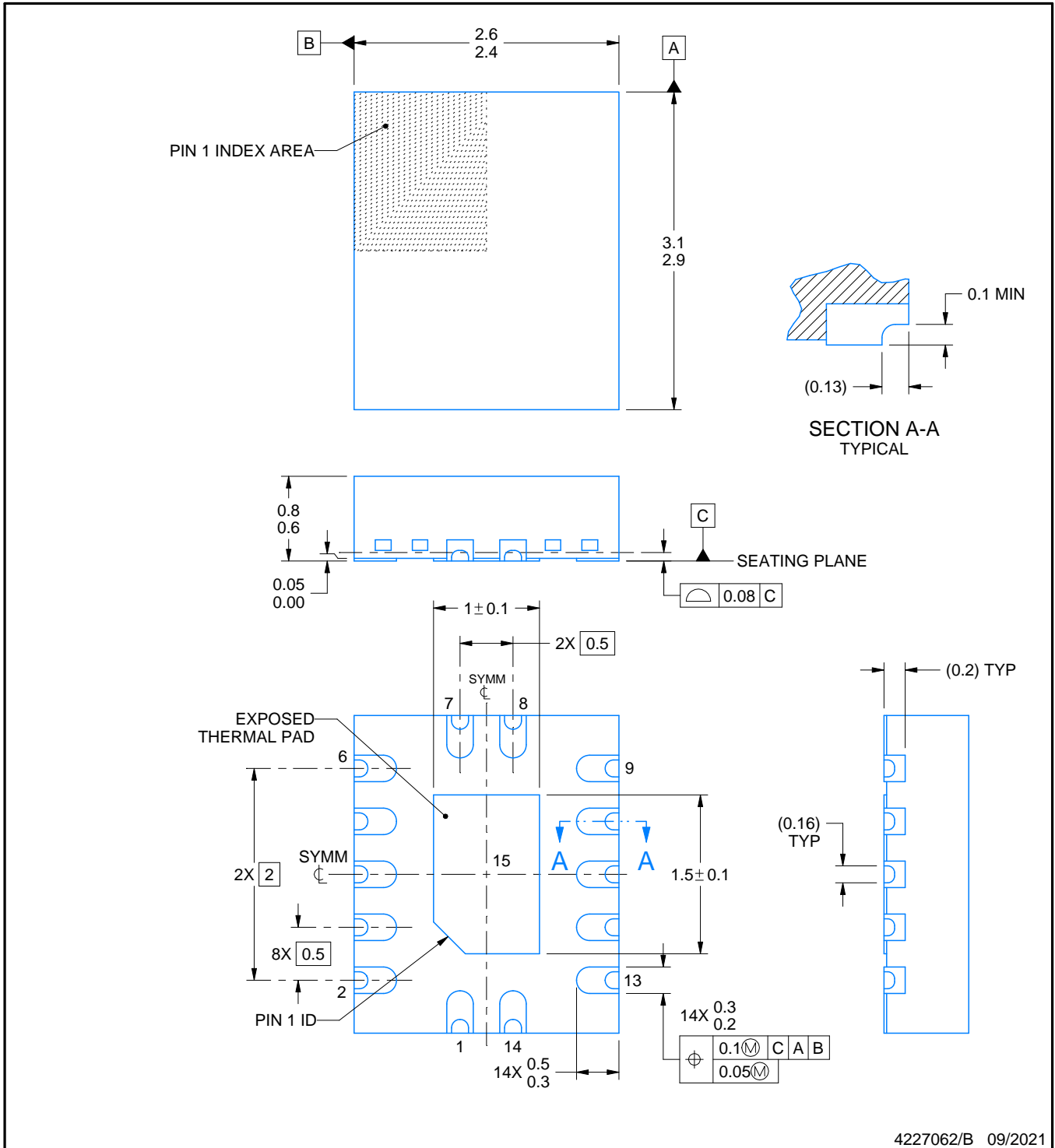
BQA0014B



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4227062/B 09/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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