

SN74LVC258A Quadruple 2-Line To 1-Line Inverting Data Selectors or Multiplexers With 3-State Outputs

1 Features

- Operating range from 1.1V to 3.6V
- Over-voltage tolerant inputs support up to 5.5V independent of V_{CC}
- Supports **partial-power-down** with back drive protection (I_{off})
- High push-pull output drive strength:
 - $\pm 24\text{mA}$ at 3.3V
 - $\pm 8\text{mA}$ at 2.3V
 - $\pm 4\text{mA}$ at 1.65V
- Maximum propagation delay of 6.4ns at 3.3V supply
- Latch-up performance exceeds 100mA per JESD78

2 Applications

- Data selection
- Multiplexing

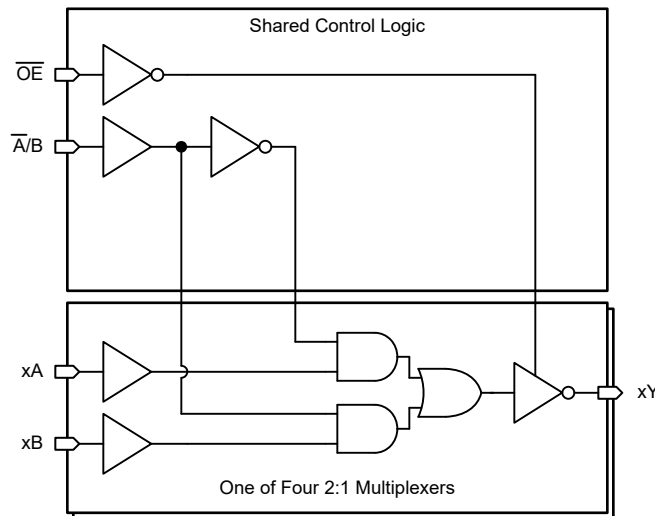
3 Description

The SN74LVC258A contains four 2-to-1 digital multiplexers with inverted outputs. The output enable (\overline{OE}) and select ($\overline{A/B}$) inputs control all channels.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM) ⁽³⁾
SN74LVC258A	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable
- (3) The body size (length × width) is a nominal value and does not include pins.



Functional Diagram



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4 Pin Configuration and Functions

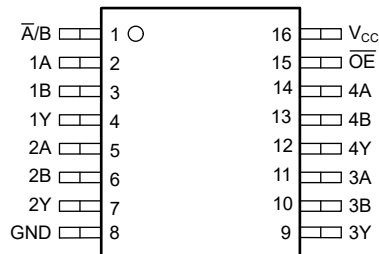


Figure 4-1. D or PW Package, 16-Pin SOIC or TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
\bar{A}/B	1	I	Select data source
1A	2	I	Channel 1, input A
1B	3	I	Channel 1, input B
1Y	4	O	Channel 1, output Y
2A	5	I	Channel 2, input A
2B	6	I	Channel 2, input B
2Y	7	O	Channel 2, output Y
GND	8	G	Ground
3Y	9	O	Channel 3, output Y
3B	10	I	Channel 3, input B
3A	11	I	Channel 3, input A
4Y	12	O	Channel 4, output Y
4B	13	I	Channel 4, input B
4A	14	I	Channel 4, input A
\bar{OE}	15	I	Output enable, active low
V _{CC}	16	P	Positive Supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	-0.5	6.5	V	
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V	
V _O	Output voltage range ⁽²⁾	High or low state	-0.5	V _{CC} + 0.5	V
		High-impedance state	-0.5	6.5	V
I _{IK}	Input clamp current	V _I < 0V	-50	mA	
I _{OK}	Output clamp current	V _O < 0V	-50	mA	
I _O	Continuous output current		±50	mA	
	Continuous current through V _{CC} or GND		±100	mA	
T _J	Junction temperature		150	°C	
T _{stg}	Storage temperature	-65	150	°C	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.1	3.6	V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}
V _O	Output voltage	High-impedance state	0	5.5
V _{IH}	High-level input voltage	V _{CC} = 1.1V	0.75	V
		V _{CC} = 1.2V	0.78	V
		V _{CC} = 1.5V	0.975	V
		V _{CC} = 1.65V	1.0725	V
		V _{CC} = 1.95V	1.2675	V
		V _{CC} = 2.3V	1.7	V
		V _{CC} = 2.7V	1.7	V
		V _{CC} = 3.6V	2	V

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{IL}	Low-Level input voltage	V _{CC} = 1.1V		0.40	V
		V _{CC} = 1.2V		0.42	V
		V _{CC} = 1.5V		0.525	V
		V _{CC} = 1.65V		0.5775	V
		V _{CC} = 1.95V		0.6825	V
		V _{CC} = 2.3V		0.7	V
		V _{CC} = 2.7V		0.7	V
		V _{CC} = 3.6V		0.8	V
I _{OH}	High-level output current	V _{CC} = 1.8V		-4	mA
		V _{CC} = 2.3V		-8	
		V _{CC} = 2.7V		-12	
		V _{CC} = 3V		-24	
I _{OL}	Low-level output current	V _{CC} = 1.8V		4	mA
		V _{CC} = 2.3V		8	
		V _{CC} = 2.7V		12	
		V _{CC} = 3V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
D (SOIC)	16	109.1	70.8	67.3	34.1	67.1	-	°C/W
PW (TSSOP)	16	141.8	74	87.1	22.3	86.6	-	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = -100μA	1.1V to 3.6V	V _{CC} - 0.2	V _{CC} - 0.01		V
V _{OH}	I _{OH} = -4mA	1.65V	1.2			V
V _{OH}	I _{OH} = -8mA	2.3V	1.75			V
V _{OH}	I _{OH} = -12mA	2.7V	2.2			V
V _{OH}		3V	2.4			V
V _{OH}	I _{OH} = -24mA	3V	2.2			V
V _{OL}	I _{OL} = 100μA	1.1V to 3.6V		0.01	0.2	V
V _{OL}	I _{OL} = 4mA	1.65V			0.45	V
V _{OL}	I _{OL} = 8mA	2.3V			0.7	V
V _{OL}	I _{OL} = 12mA	2.7V		0.2	0.4	V
V _{OL}	I _{OL} = 24mA	3V			0.55	V
I _I	V _I = V _{CC} or GND	3.6V			±5	μA

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
I _{off}	V _I or V _O = V _{CC}	0V			±10	μA
I _{OZ}	V _O = V _{CC} or GND	3.6V			±15	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6V			40	μA
ΔI _{CC}	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND	2.7V to 3.6V			5000	μA
C _I	V _I = V _{CC} or GND	3.3V		4.9		pF
C _O	V _O = V _{CC} or GND	3.3V		6.3		pF
C _{PD}	f = 10MHz	1.8V		12		pF
C _{PD}	f = 10MHz	2.5V		15		pF
C _{PD}	f = 10MHz	3.3V		17		pF
C _{PD}	Outputs disabled, f = 10MHz	1.8V		2		pF
		2.5V		3		
		3.3V		4		

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{pd}	A or B	Y	C _L = 15pF	1.2V ± 0.1V	16						13.7	25	ns	
			C _L = 15pF	1.5V ± 0.12V	14						7.7	13.3	ns	
			C _L = 30pF	1.8V ± 0.15V	5.5	13.5	1	13.5	5.5	15.5	ns			
			C _L = 30pF	2.5V ± 0.2V	3.2	7.4	1	7.4	3.7	10	ns			
			C _L = 50pF	2.7V	3.6	5.7	1	5.4	3.7	7.4	ns			
			C _L = 50pF	3.3V ± 0.3V	3	5	1	4.6	3.4	6.4	ns			
	A/B	Y	C _L = 15pF	1.2V ± 0.1V	17						15	26.2	ns	
			C _L = 15pF	1.5V ± 0.12V	16						8.5	14	ns	
			C _L = 30pF	1.8V ± 0.15V	6	15.5	1	15.6	6.3	17.5	ns			
			C _L = 30pF	2.5V ± 0.2V	3.7	9.6	1	9.5	4.4	12.2	ns			
			C _L = 50pF	2.7V	4.1	7.9	1	7.5	4.4	10	ns			
			C _L = 50pF	3.3V ± 0.3V	3.4	6.6	1	6.4	4.1	8.4	ns			

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{en}	\overline{OE}	Y	$C_L = 15\text{pF}$	$1.2\text{V} \pm 0.1\text{V}$	16						13.1	20.6	ns	
			$C_L = 15\text{pF}$	$1.5\text{V} \pm 0.12\text{V}$	15						7.2	10.6	ns	
			$C_L = 30\text{pF}$	$1.8\text{V} \pm 0.15\text{V}$				1	14.6	7.3	8.6	ns		
			$C_L = 30\text{pF}$	$2.5\text{V} \pm 0.2\text{V}$				1	8.7	4.8	5.7	ns		
			$C_L = 50\text{pF}$	2.7V				1	6.7	5.2	6.7	ns		
			$C_L = 50\text{pF}$	$3.3\text{V} \pm 0.3\text{V}$				1	5.6	4.4	5.4	ns		
t_{dis}	\overline{OE}	Y	$C_L = 15\text{pF}$	$1.2\text{V} \pm 0.1\text{V}$	17						12	17	ns	
			$C_L = 15\text{pF}$	$1.5\text{V} \pm 0.12\text{V}$	16						7.5	10.3	ns	
			$C_L = 30\text{pF}$	$1.8\text{V} \pm 0.15\text{V}$				1	15.4	7.9	15.4	ns		
			$C_L = 30\text{pF}$	$2.5\text{V} \pm 0.2\text{V}$				1	6.7	4.7	6.7	ns		
			$C_L = 50\text{pF}$	2.7V	4.8			1	5.2	4.9	5.5	ns		
			$C_L = 50\text{pF}$	$3.3\text{V} \pm 0.3\text{V}$	4.4			1	4.9	4.6	5.1	ns		
$t_{sk(o)}$				$3.3\text{V} \pm 0.3\text{V}$				1			1.5	ns		

5.7 Noise Characteristics

$V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	2.2	3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.0			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

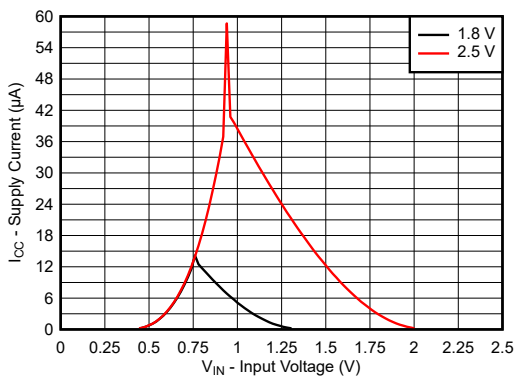


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

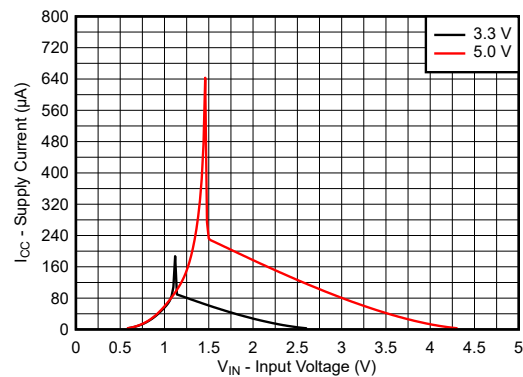


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

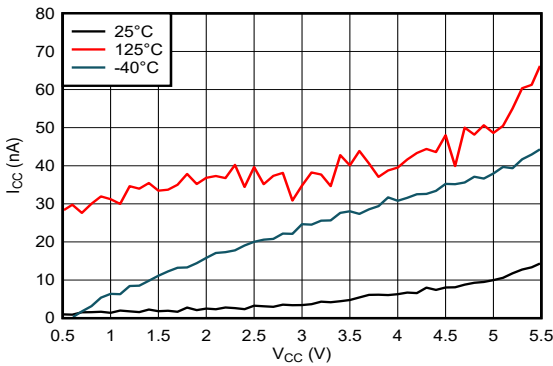


Figure 5-3. Supply Current Across Supply Voltage

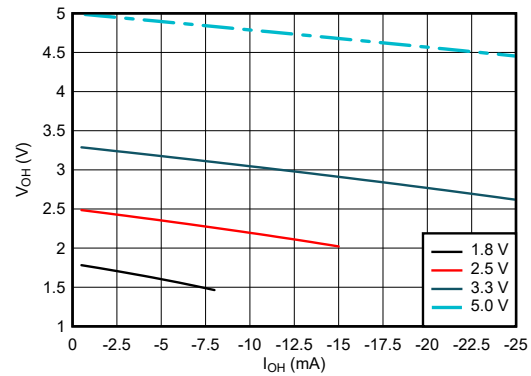


Figure 5-4. Output Voltage vs Current in HIGH State

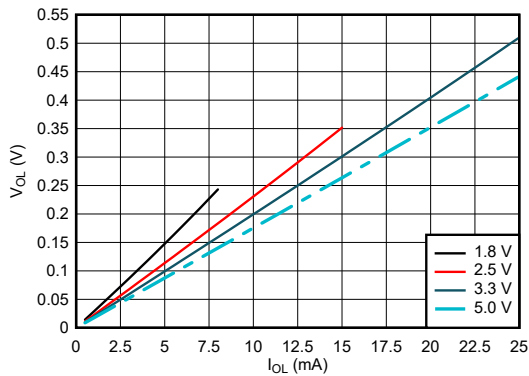


Figure 5-5. Output Voltage vs Current in LOW State

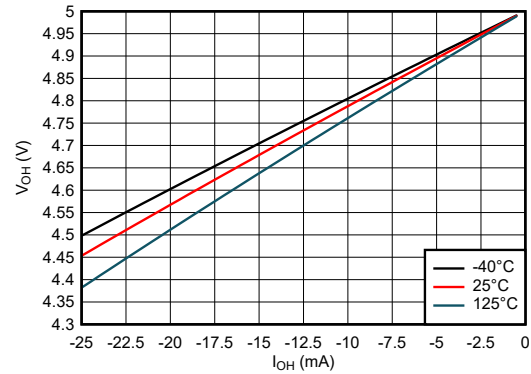


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

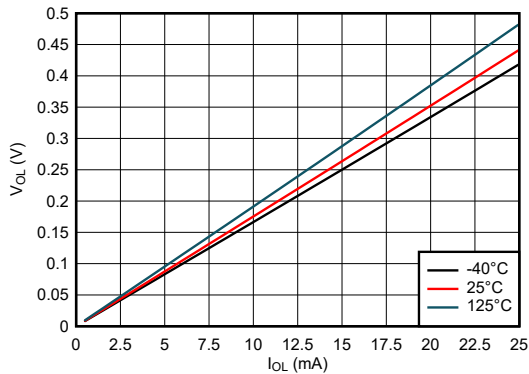


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

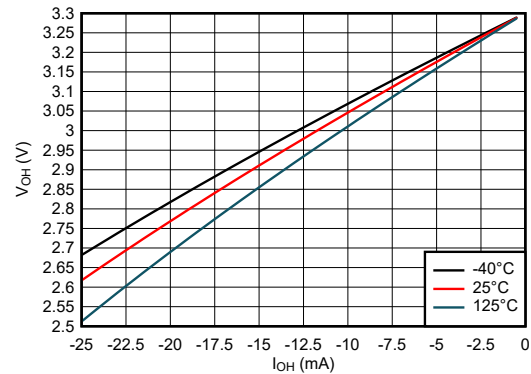


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

5.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

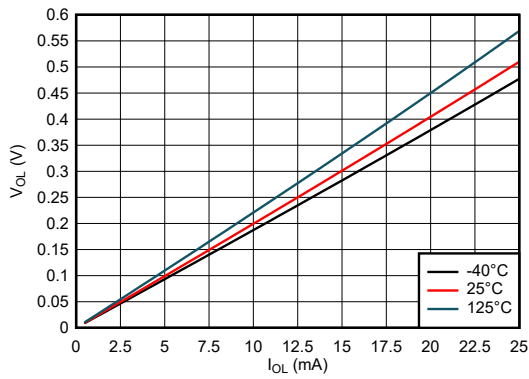


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

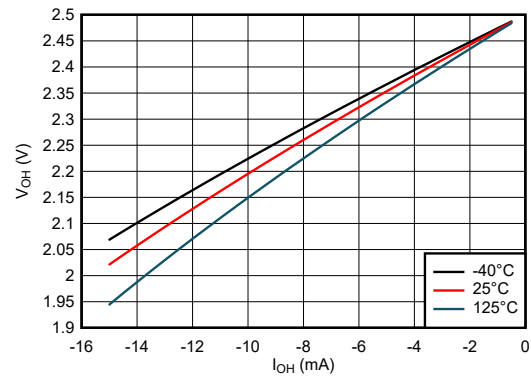


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

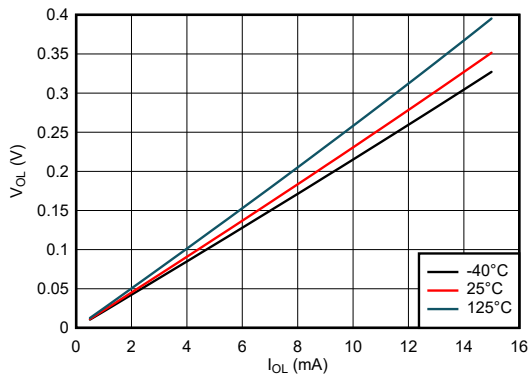


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

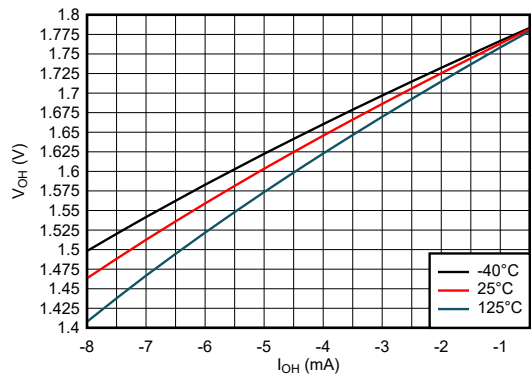


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

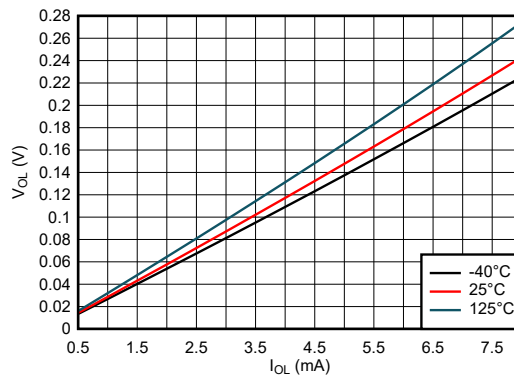


Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

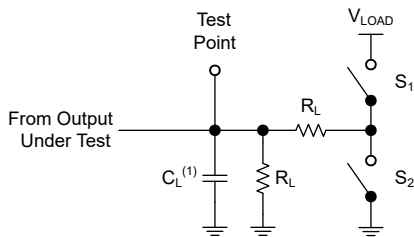
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

The outputs are measured individually with one input transition per measurement.

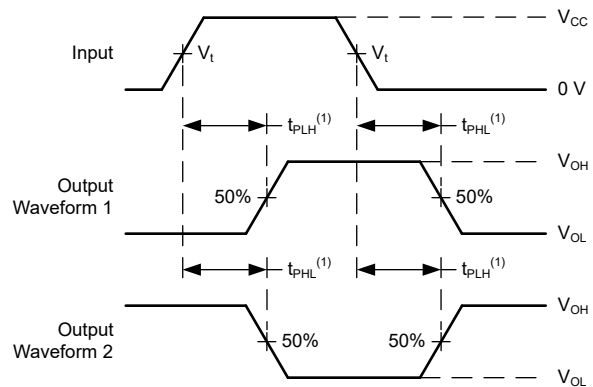
TEST	S1	S2	R _L	C _L	ΔV	V _{LOAD}
t _{PLH} , t _{PHL}	OPEN	OPEN	500Ω	50pF	—	—
t _{PLZ} , t _{PZL}	CLOSED	OPEN	500Ω	50pF	0.3V	2×V _{CC}
t _{PHZ} , t _{PZH}	OPEN	CLOSED	500Ω	50pF	0.3V	—

V _{CC}	V _t	R _L	C _L	ΔV	V _{LOAD}
1.2V ± 0.1V	V _{CC} /2	2kΩ	15pF	0.1V	2×V _{CC}
1.5V ± 0.12V	V _{CC} /2	2kΩ	15pF	0.1V	2×V _{CC}
1.8V ± 0.15V	V _{CC} /2	1kΩ	30pF	0.15V	2×V _{CC}
2.5V ± 0.2V	V _{CC} /2	500Ω	30pF	0.15V	2×V _{CC}
2.7V	1.5V	500Ω	50pF	0.3V	6V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V	6V



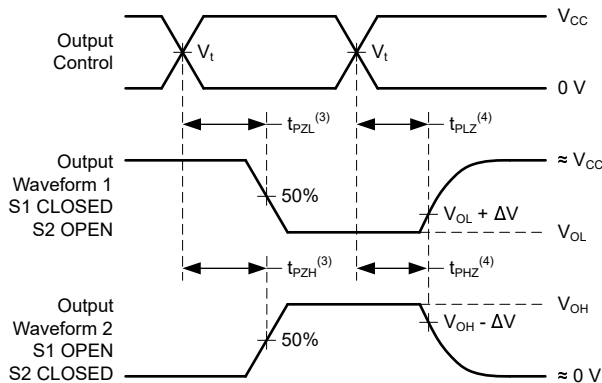
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

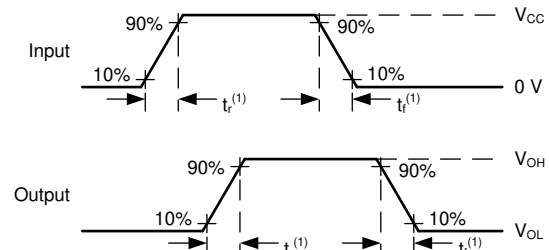
Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

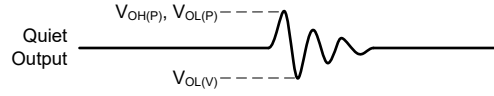
(2) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times



Noise values measured with all other outputs simultaneously switching.

Figure 6-5. Voltage Waveforms, Noise

7 Detailed Description

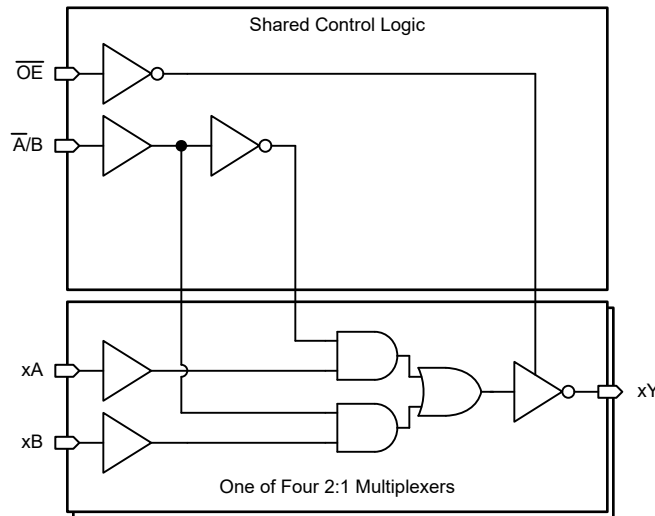
7.1 Overview

The SN74LVC258A is a 4 channel 2-to-1 multiplexer with inverted outputs.

The output enable (\overline{OE}) input enables all outputs when low, and forces all outputs into the high-impedance state when high.

The select ($\overline{A/B}$) input chooses the data source for all channels, with the low state indicating the A data source, and the high state indicating the B data source.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10k Ω resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k Ω resistor, however, is recommended and will typically meet all requirements.

7.3.4 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

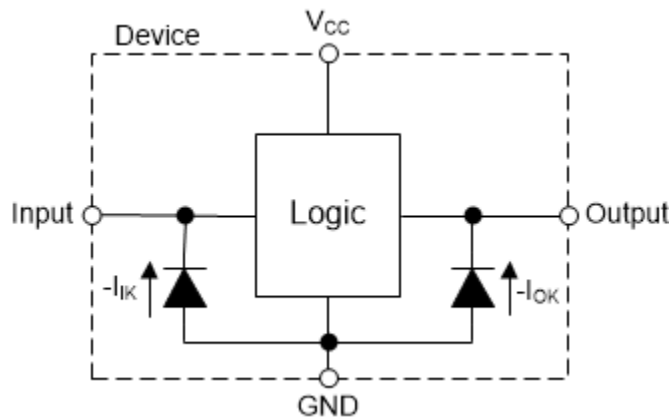


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Function Table lists the functional modes of the SN74LVC258A.

Table 7-1. Function Table

OE	INPUTS ⁽¹⁾			OUTPUT ⁽²⁾
	SELECT	DATA		
	\bar{A}/B	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

(1) H = High voltage level, L = Low voltage level, X = Don't care

(2) H = Driving high, L = Driving low

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC258A is a quadruple 2-to-1 data selector/multiplexer with inverted outputs. The following application shows an example of using the device with all required connections to switch a 4-bit data bus between two source devices.

8.2 Typical Application

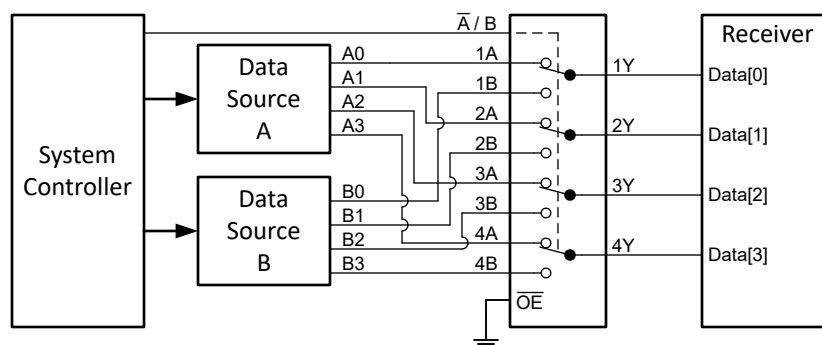


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC258A plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC258A plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC258A can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC258A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC258A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN74LVC258A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC258A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

8.2.3 Application Curve

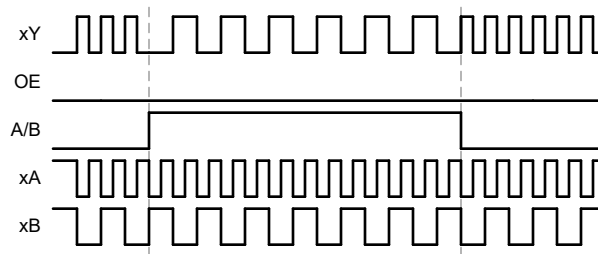


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

During startup, the power supply should ramp within the provided power-up ramp rate range in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For the SN74LVC258A, a $0.1\mu\text{F}$ bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of $0.1\mu\text{F}$ and $1\mu\text{F}$ are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

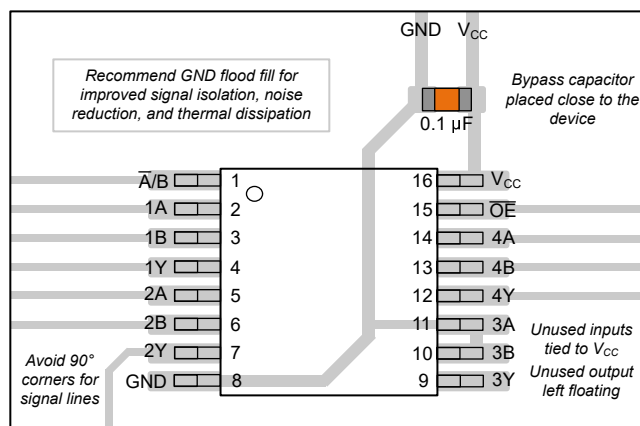


Figure 8-3. Example Layout for the SN74LVC258A

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC258APWR	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LVC258	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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