SN74LVC2G53 Single-Pole Double-Throw (SPDT) Analog Switch 2:1 Analog Multiplexer/Demultiplexer

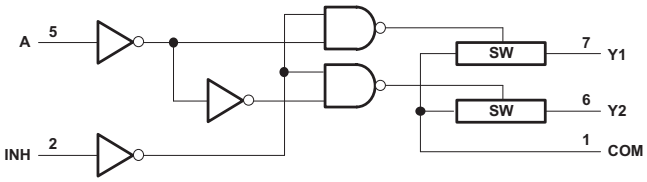
1 Features

- Available in the Texas Instruments NanoFree™ Package
- 1.65-V to 5.5-V V_{CC} Operation
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)
- Low ON-State Resistance, Typically 6.5 Ω (V_{CC} = 4.5 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Wireless Devices
- Audio and Video Signal Routing
- Portable Computing
- Wearable Devices
- Signal Gating, Chopping, Modulation or Demodulation (Modem)
- Signal Multiplexing for Analog-to-Digital and Digital-to-Analog Conversion Systems

Logic Diagram



NOTE: For simplicity, the test conditions shown in Figure 1 through Figure 4 and Figure 6 through Figure 10 are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

3 Description

This single 2:1 analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G53 device can handle both analog and digital signals. This device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

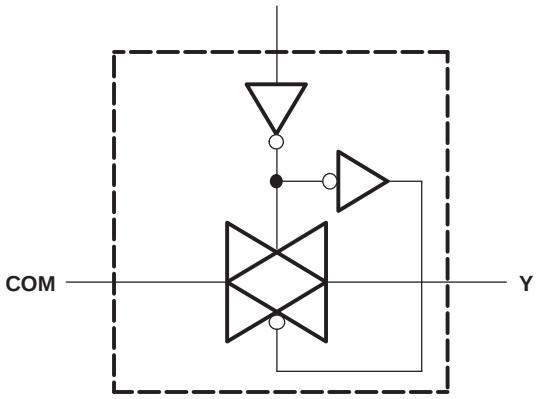
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2G53DCT	SM8 (8)	2.95 mm × 2.80 mm
SN74LVC2G53DCU	VSSOP (8)	2.30 mm × 2.00 mm
SN74LVC2G53YZP	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Switch (SW)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (October 2016) to Revision Q — **Page**

- Changed the *Thermal Information* table ... 5

Changes from Revision O (December 2015) to Revision P — **Page**

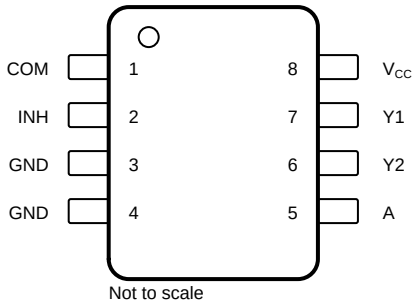
- Added DSBGA package in *Pin Functions* table ... 3
- Added *Receiving Notification of Documentation Updates* section ... 19

Changes from Revision N (January 2014) to Revision O — **Page**

- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Moved T_{stg} to *Absolute Maximum Ratings* table ... 4

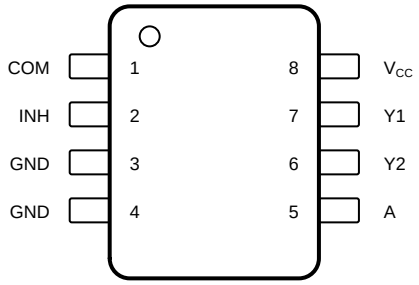
5 Pin Configuration and Functions

DCT Package
8-Pin SM8
Top View



Not to scale

DCU Package
8-Pin VSSOP
Top View



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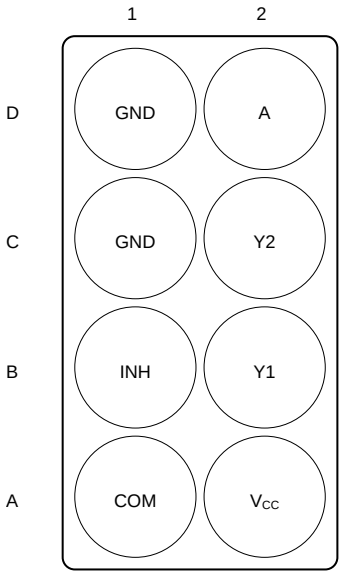
YZP Package
8-Pin DSBGA
Bottom View



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See *Mechanical, Packaging, and Orderable Information* for dimensions.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SM8, VSSOP	DSBGA		
A	5	D2	I	Controls the switch
COM	1	A1	I/O	Bidirectional signal to be switched
GND	3	C1	—	Ground pin
GND	4	D1	—	Ground pin
INH	2	B1	I	Enables or disables the switch
V_{CC}	8	A2	—	Power pin
Y2	6	C2	I/O	Bidirectional signal to be switched
Y1	7	B2	I/O	Bidirectional signal to be switched

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	6.5	V
V_I	Input voltage(2)(3)		–0.5	6.5	V
$V_{I/O}$	Switch I/O voltage(2)(3)(4)		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_I < 0		–50	mA
$I_{I/OK}$	I/O port diode current	$V_{I/O}$ < 0 or $V_{I/O}$ > V_{CC}		±50	mA
I_T	ON-state switch current	$V_{I/O}$ = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See note(1).

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	V_{CC} × 0.65		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		V_{CC} × 0.35	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	V
Δt/Δv	Input transition rise and fall time	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC2G53			UNIT
		DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	185.9	288.9	98.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	116.3	99.6	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.4	207.3	27.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	41.6	22.4	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	97.3	205.7	27.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
r_{on}	ON-state switch resistance		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 2 and Figure 1)	I_S = 4 mA	1.65 V		13	30	Ω
				I_S = 8 mA	2.3 V		10	20	
				I_S = 24 mA	3 V		8.5	17	
				I_S = 32 mA	4.5 V		6.5	13	
$r_{on(p)}$	Peak ON-state resistance		$V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$ (see Figure 2 and Figure 1)	I_S = 4 mA	1.65 V		86.5	120	Ω
				I_S = 8 mA	2.3 V		23	30	
				I_S = 24 mA	3 V		13	20	
				I_S = 32 mA	4.5 V		8	15	
Δr_{on}	Difference of ON-state resistance between switches		$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figure 2 and Figure 1)	I_S = 4 mA	1.65 V			7	Ω
				I_S = 8 mA	2.3 V			5	
				I_S = 24 mA	3 V			3	
				I_S = 32 mA	4.5 V			2	
$I_{S(off)}$	OFF-state switch leakage current		$V_I = V_{CC}$ and V_O = GND or V_I = GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 3)		5.5 V			±1	μA
								±0.1[1]	
$I_{S(on)}$	ON-state switch leakage current		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$, V_O = Open (see Figure 4)		5.5 V			±1	μA
								±0.1[1]	
I_I	Control input current		$V_C = V_{CC}$ or GND		5.5 V			±1	μA
								±0.1[1]	
I_{CC}	Supply current		$V_C = V_{CC}$ or GND		5.5 V			1	μA
ΔI_{CC}	Supply-current change		$V_C = V_{CC}$ – 0.6 V		5.5 V			500	μA
C_{ic}	Control input capacitance				5 V		3.5		pF
$C_{io(off)}$	Switch input/output capacitance	Y			5 V		6.5		pF
		COM					10		
$C_{io(on)}$	Switch input/output capacitance				5 V		19.5		pF

(1) T_A = 25°C

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd} (1)	COM or Y	Y or COM	V_{CC} = 1.8 V ± 0.15 V		2	ns
			V_{CC} = 2.5 V ± 0.2 V		1.2	
			V_{CC} = 3.3 V ± 0.3 V		0.8	
			V_{CC} = 5 V ± 0.5 V		0.6	
t_{en} (2)	INH	COM or Y	V_{CC} = 1.8 V ± 0.15 V	3.3	9	ns
			V_{CC} = 2.5 V ± 0.2 V	2.5	6.1	
			V_{CC} = 3.3 V ± 0.3 V	2.2	5.4	
			V_{CC} = 5 V ± 0.5 V	1.8	4.5	
t_{dis} (3)	INH	COM or Y	V_{CC} = 1.8 V ± 0.15 V	3.2	10.9	ns
			V_{CC} = 2.5 V ± 0.2 V	2.3	8.3	
			V_{CC} = 3.3 V ± 0.3 V	2.3	8.1	
			V_{CC} = 5 V ± 0.5 V	1.6	8	
t_{en} (2)	A	COM or Y	V_{CC} = 1.8 V ± 0.15 V	2.9	10.3	ns
			V_{CC} = 2.5 V ± 0.2 V	2.1	7.2	
			V_{CC} = 3.3 V ± 0.3 V	1.9	5.8	
			V_{CC} = 5 V ± 0.5 V	1.3	5.4	
t_{dis} (3)	A	COM or Y	V_{CC} = 1.8 V ± 0.15 V	2.1	2.1	ns
			V_{CC} = 2.5 V ± 0.2 V	1.4	7.9	
			V_{CC} = 3.3 V ± 0.3 V	1.1	7.2	
			V_{CC} = 5 V ± 0.5 V	1	5	

(1) t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) t_{PZL} and t_{PZH} are the same as t_{en}.
(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

6.7 Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response (switch on)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	35	MHz
				2.3 V	120	
				3 V	190	
				4.5 V	215	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk (1) (between switches)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	–58	dB
				2.3 V	–58	
				3 V	–58	
				4.5 V	–58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	–42	
				2.3 V	–42	
				3 V	–42	
				4.5 V	–42	

(1) Adjust f_{in} voltage to obtain 0 dBm at input.

Analog Switch Characteristics (continued)

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feedthrough attenuation (switch off)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	–60	dB
				2.3 V	–60	
				3 V	–60	
				4.5 V	–60	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	–50	
				2.3 V	–50	
				3 V	–50	
				4.5 V	–50	
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	1.65 V	0.1%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	1.65 V	0.15%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	V_{CC} = 1.8 V	9	pF
			V_{CC} = 2.5 V	10	
			V_{CC} = 3.3 V	10	
			V_{CC} = 5 V	12	

6.9 Typical Characteristics

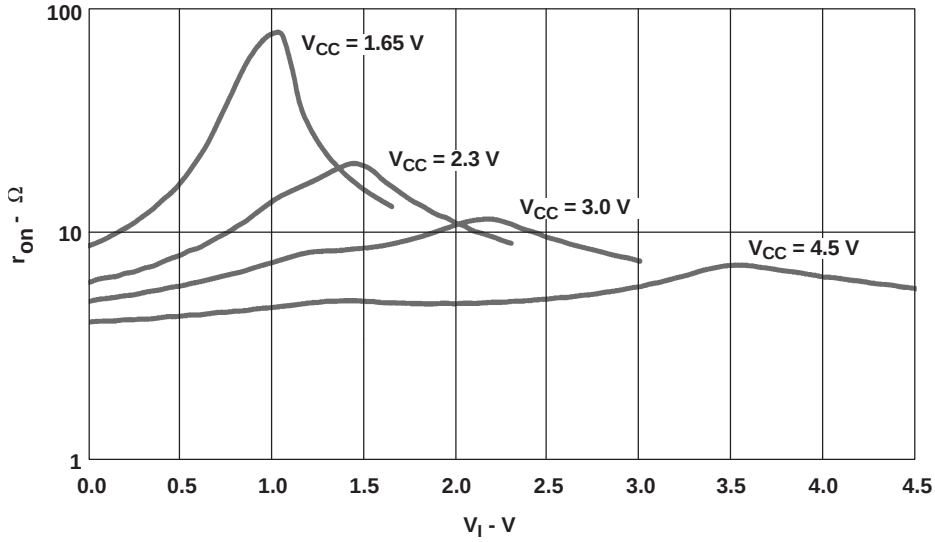


Figure 1. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

7 Parameter Measurement Information

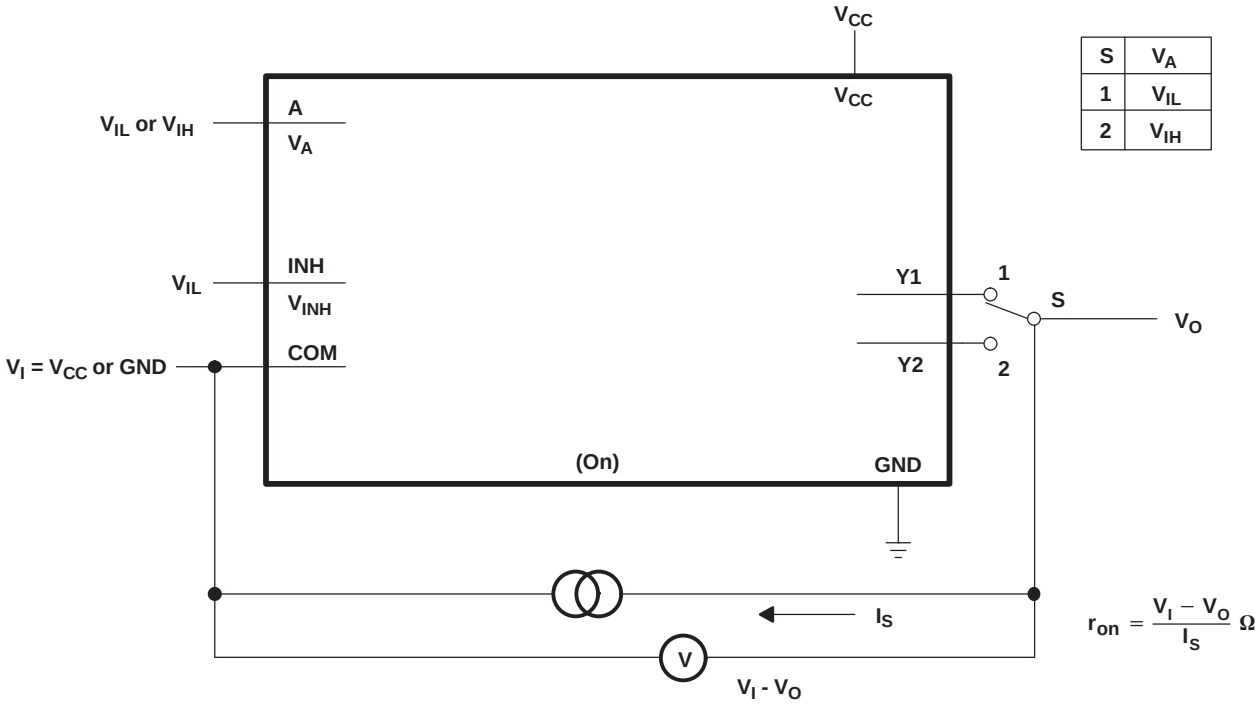
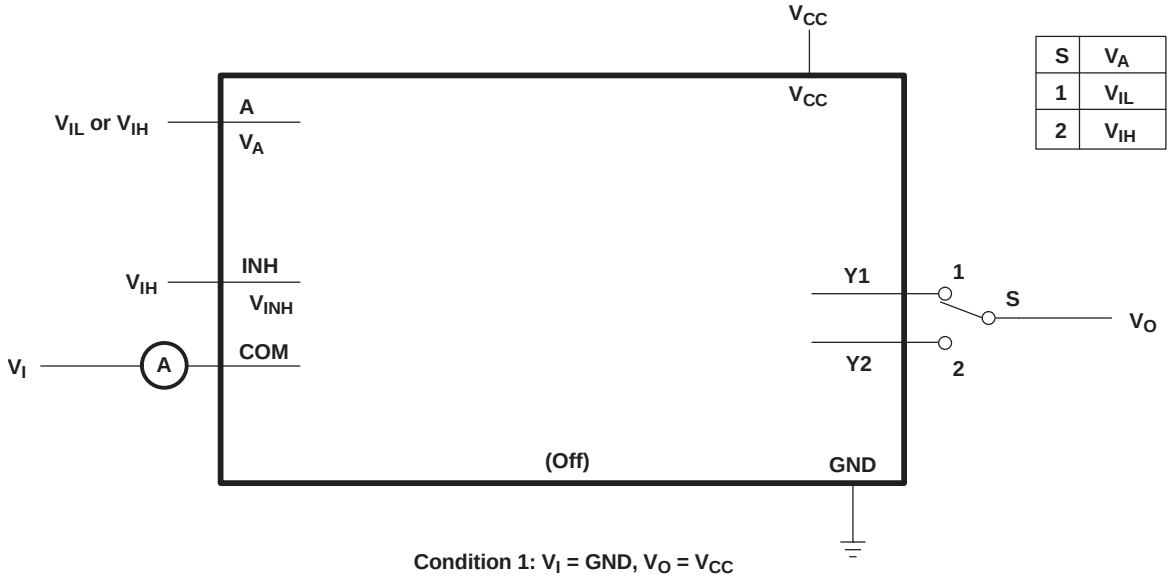


Figure 2. ON-State Resistance Test Circuit



Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. OFF-State Switch Leakage-Current Test Circuit

Parameter Measurement Information (continued)

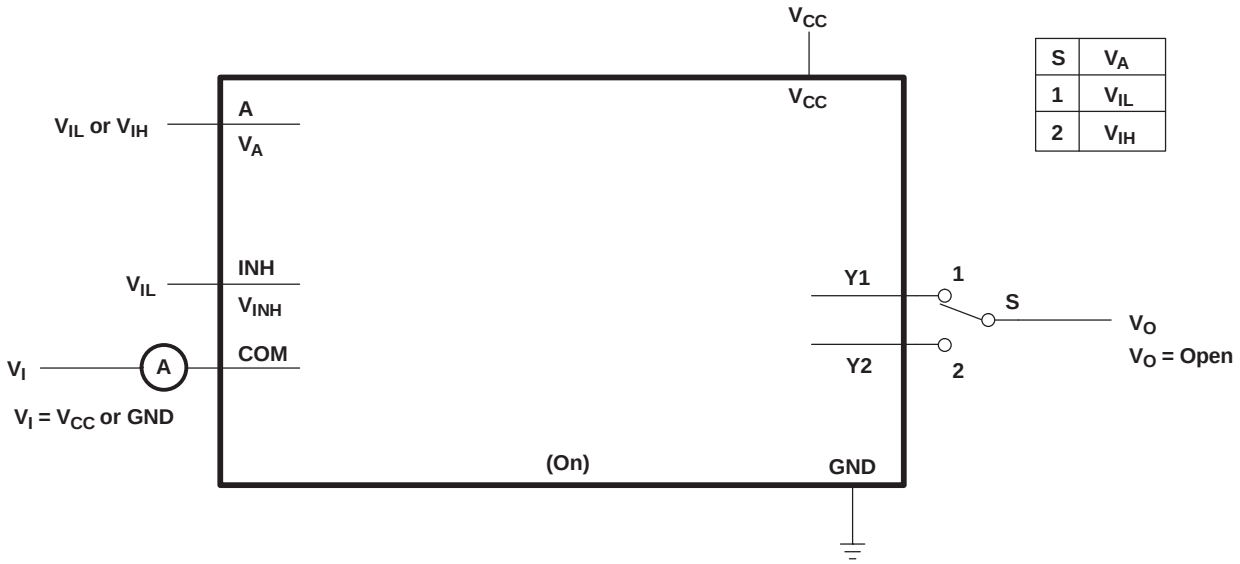
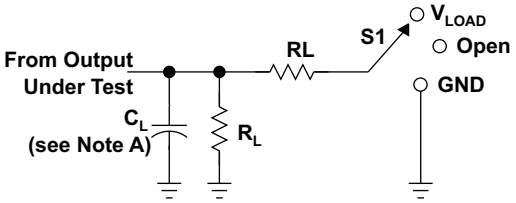


Figure 4. ON-State Switch Leakage-Current Test Circuit

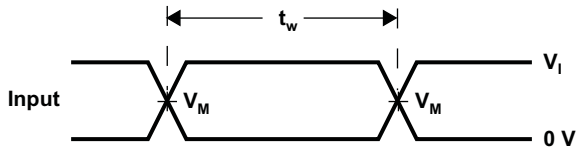
Parameter Measurement Information (continued)



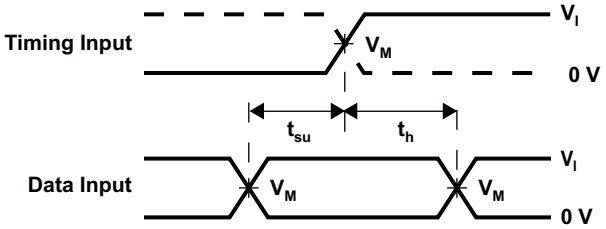
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

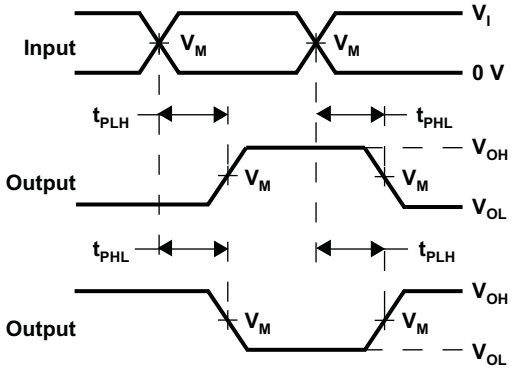
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



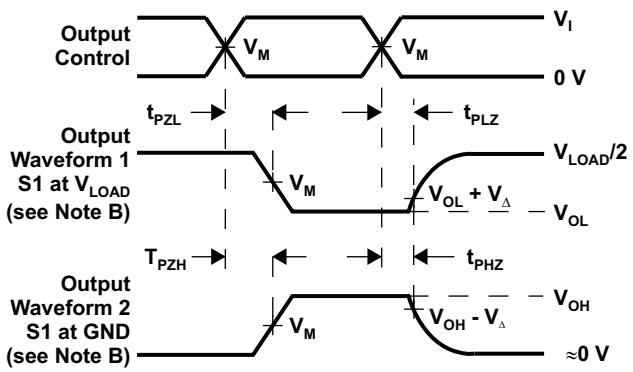
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 Mhz, Z_O = 50 Ω
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

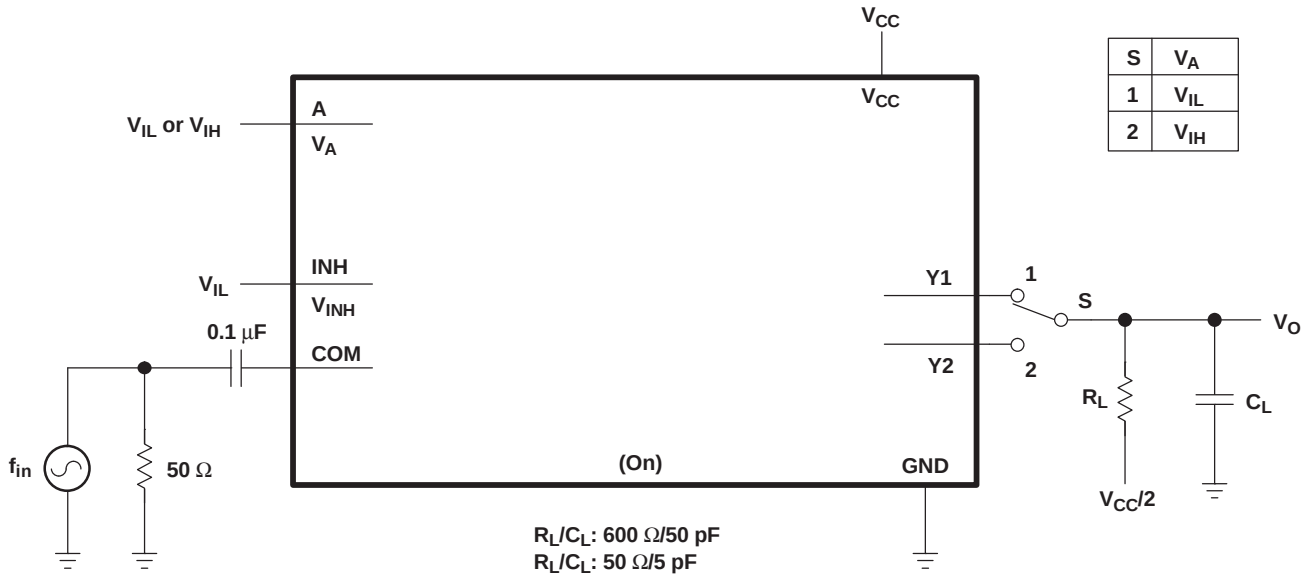


Figure 6. Frequency Response (Switch On)

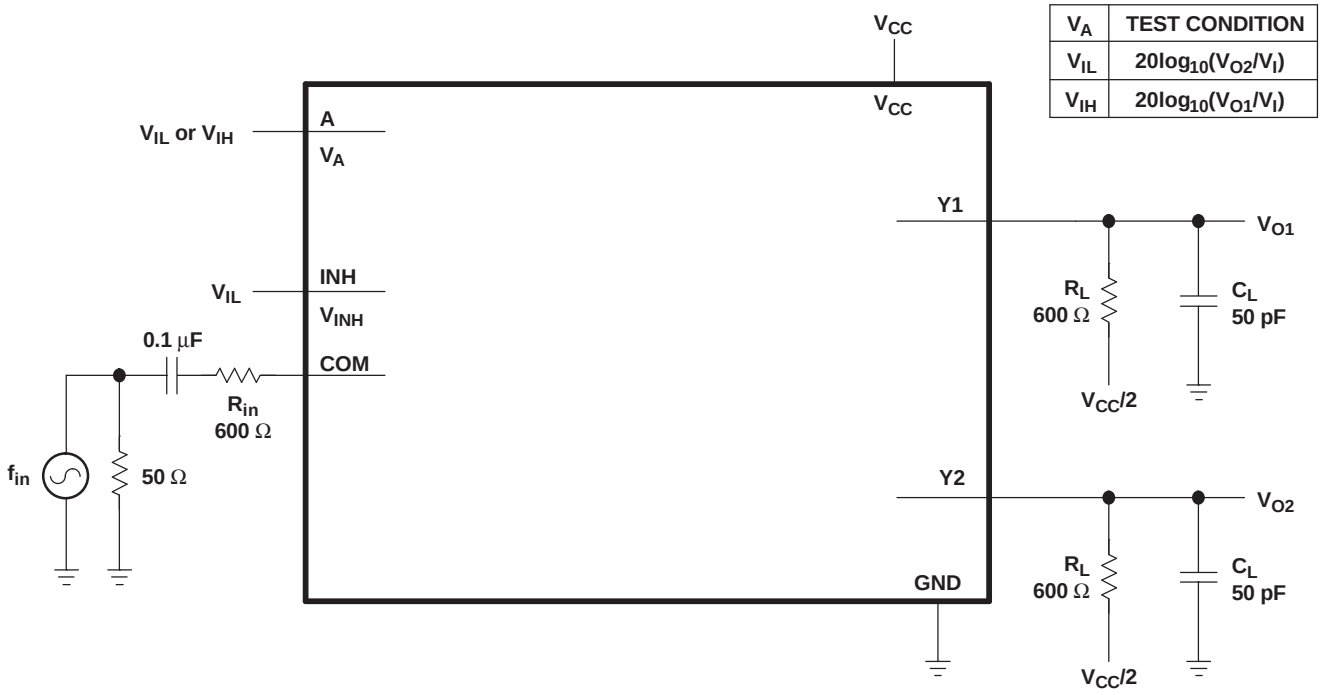


Figure 7. Crosstalk (Between Switches)

Parameter Measurement Information (continued)

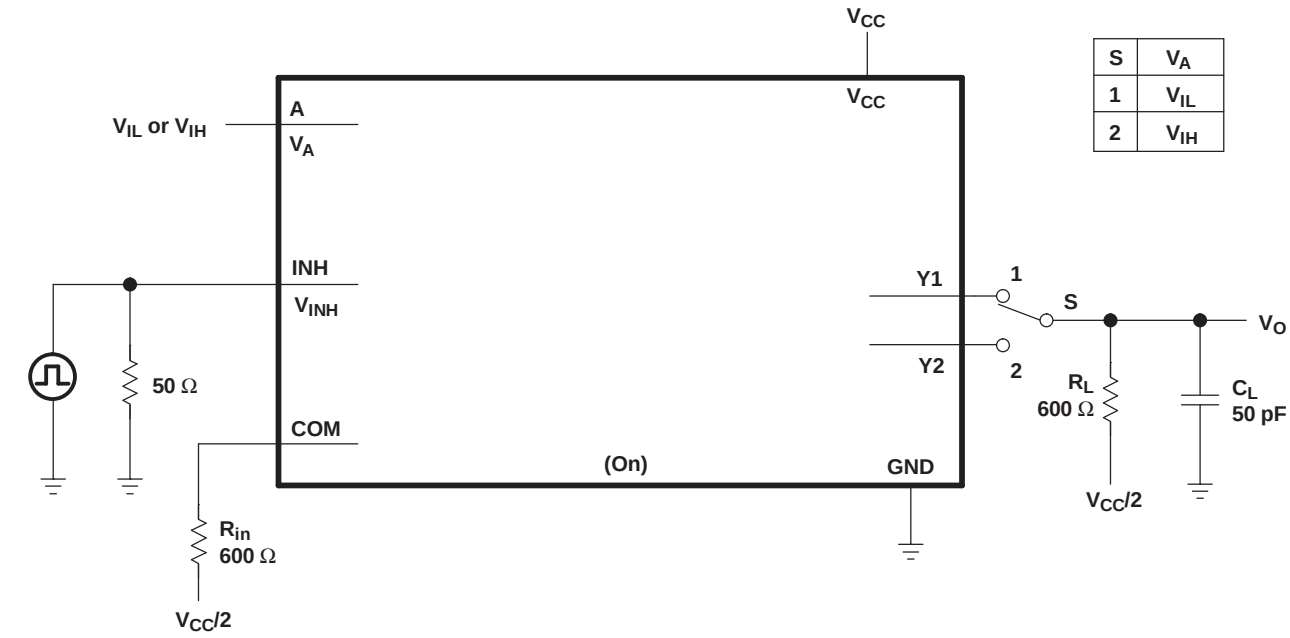


Figure 8. Crosstalk (Control Input, Switch Output)

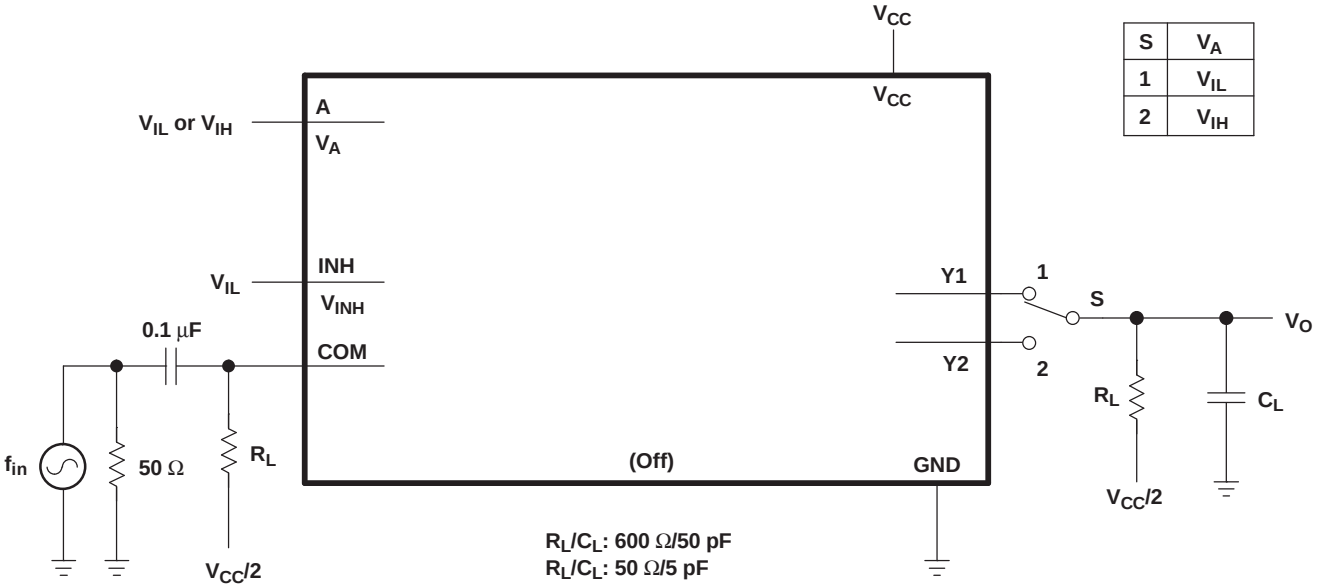


Figure 9. Feedthrough (Switch Off)

Parameter Measurement Information (continued)

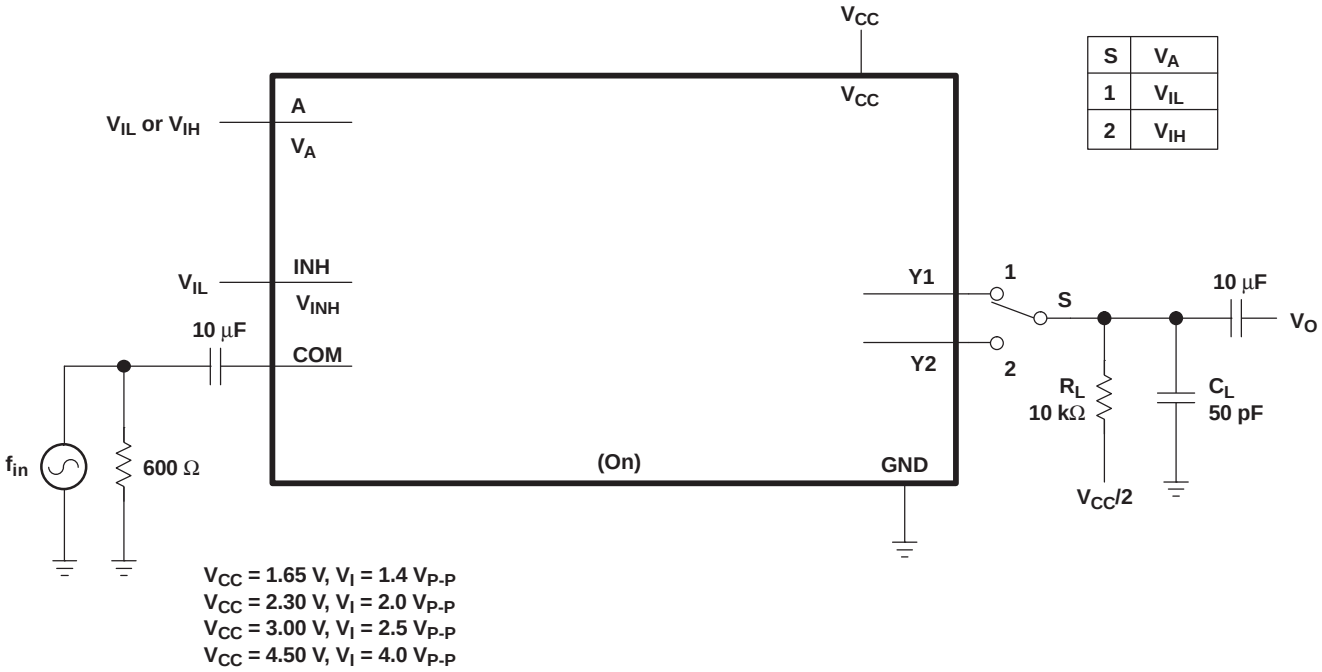


Figure 10. Sine-Wave Distortion

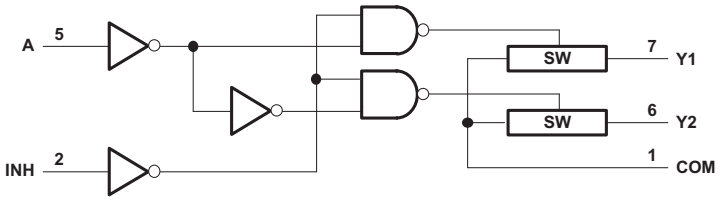
8 Detailed Description

8.1 Overview

This dual analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G53 device can handle both analog and digital signals. This device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

8.2 Functional Block Diagram



NOTE: For simplicity, the test conditions shown in Figure 1 through Figure 4 and Figure 6 through Figure 10 are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

Figure 11. Logic Diagram

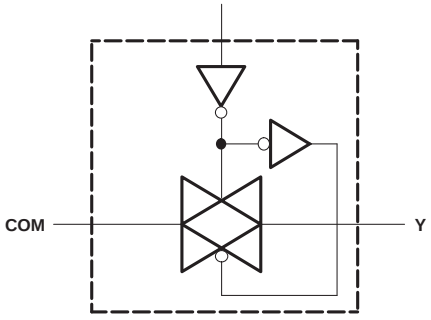


Figure 12. Logic Diagram, Each Switch (SW)

8.3 Feature Description

A high-level voltage applied to INH disables the switches. When INH is low, signals can pass from A to Y or Y to A. Low ON-resistance of 6.5 Ω at 4.5-V V_{CC} is ideal for analog signal conditioning systems. The control signals can accept voltages up to 5.5 V without V_{CC} connected in the system. Combination of lower t_{pd} of 0.8 ns at 3.3 V and low enable and disable time make this part suitable for high-speed signal switching applications.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC2G53.

Table 1. Function Table

CONTROL INPUTS		ON CHANNEL
INH	A	
L	L	Y1
L	H	Y2
H	X	None

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC2G53 can be used in any situation where an SPDT switch is required in an application. This switch helps to select one of two signals of which signals can be either digital or analog.

9.2 Typical Application

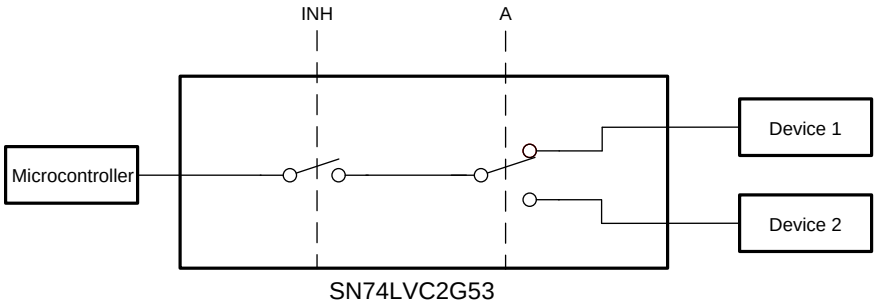


Figure 13. Typical Application Schematic

9.2.1 Design Requirements

The SN74LVC2G53 allows on/off control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and V_{CC} for optimal operation.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents should not exceed ±50 mA.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 150 MHz.
   - Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout*.

Typical Application (continued)

9.2.3 Application Curve

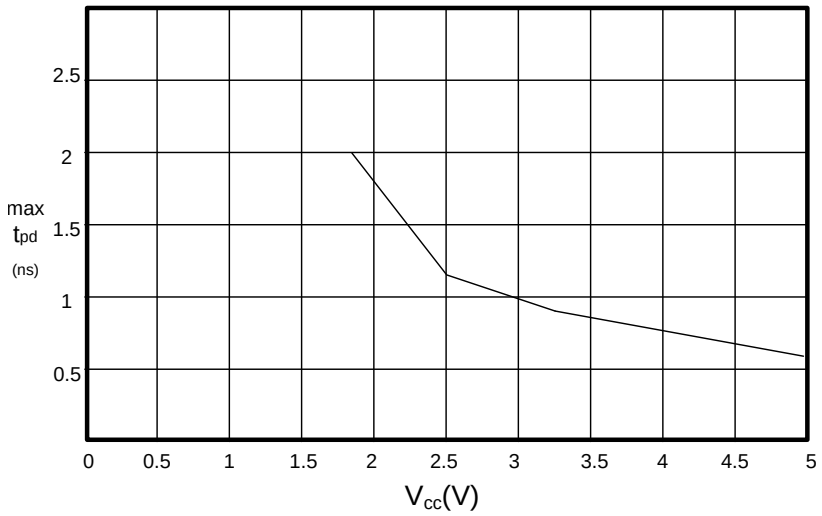


Figure 14. t_{pd} vs V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* .

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection.

NOTE

Not all PCB traces can be straight, and so they will have to turn corners. Figure 15 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

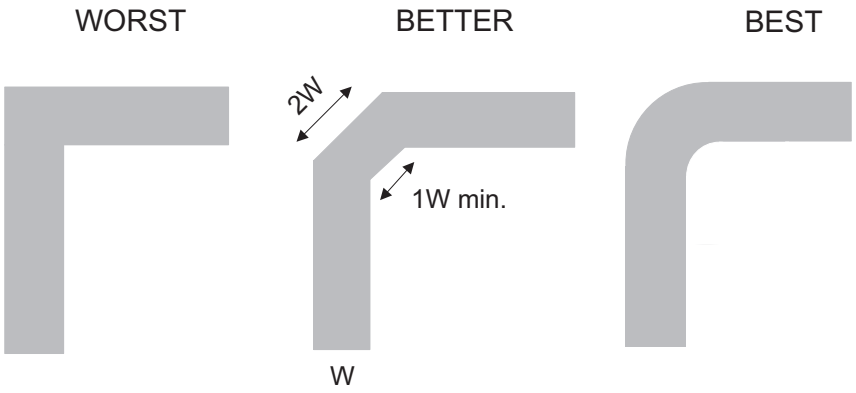


Figure 15. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G53DCT3	OBSOLETE	SSOP	DCT	8		TBD	Call TI	Call TI	-40 to 85	C53 Z	
SN74LVC2G53DCTR	ACTIVE	SSOP	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53 Z	Samples
SN74LVC2G53DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(53, C53Q, C53R) CZ	Samples
SN74LVC2G53DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53R	Samples
SN74LVC2G53DCUT	OBSOLETE	VSSOP	DCU	8		TBD	Call TI	Call TI	-40 to 85	(53, C53Q, C53R) CZ	
SN74LVC2G53DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		C53R	Samples
SN74LVC2G53YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C4N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

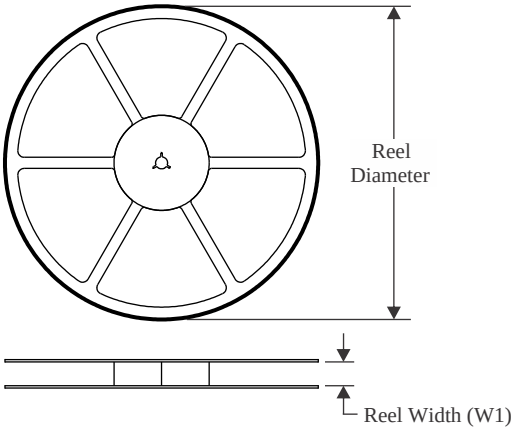
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

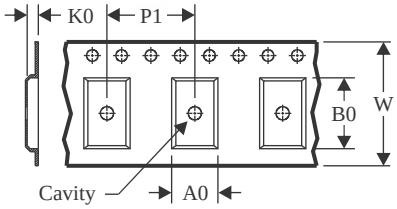
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

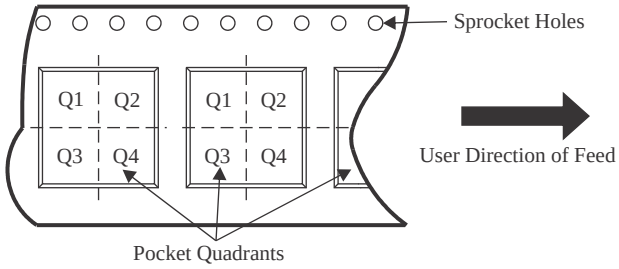


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

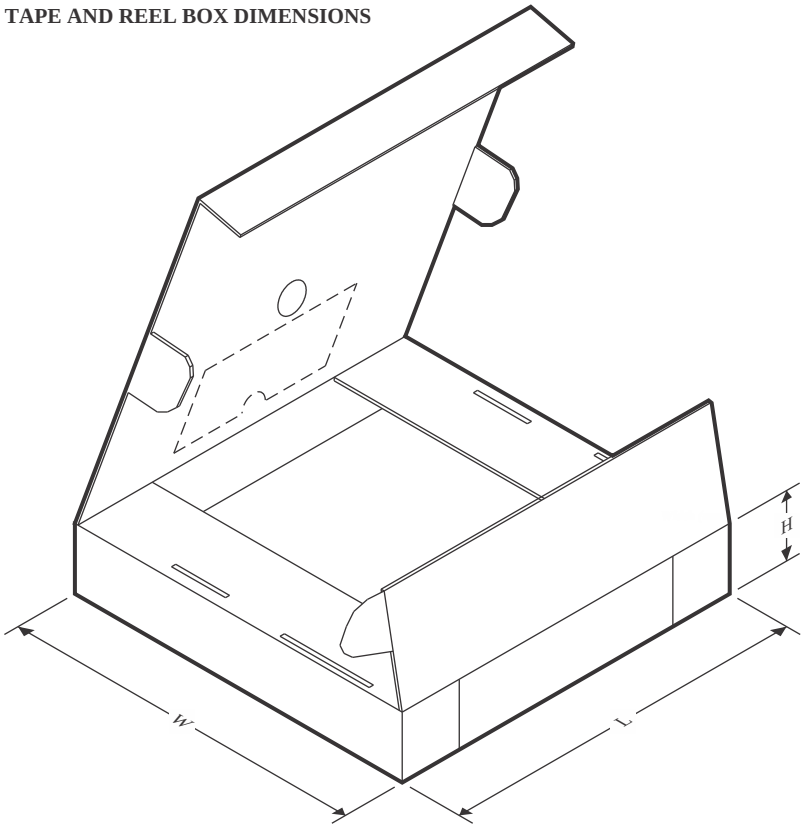
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G53DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G53DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G53DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G53DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G53YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

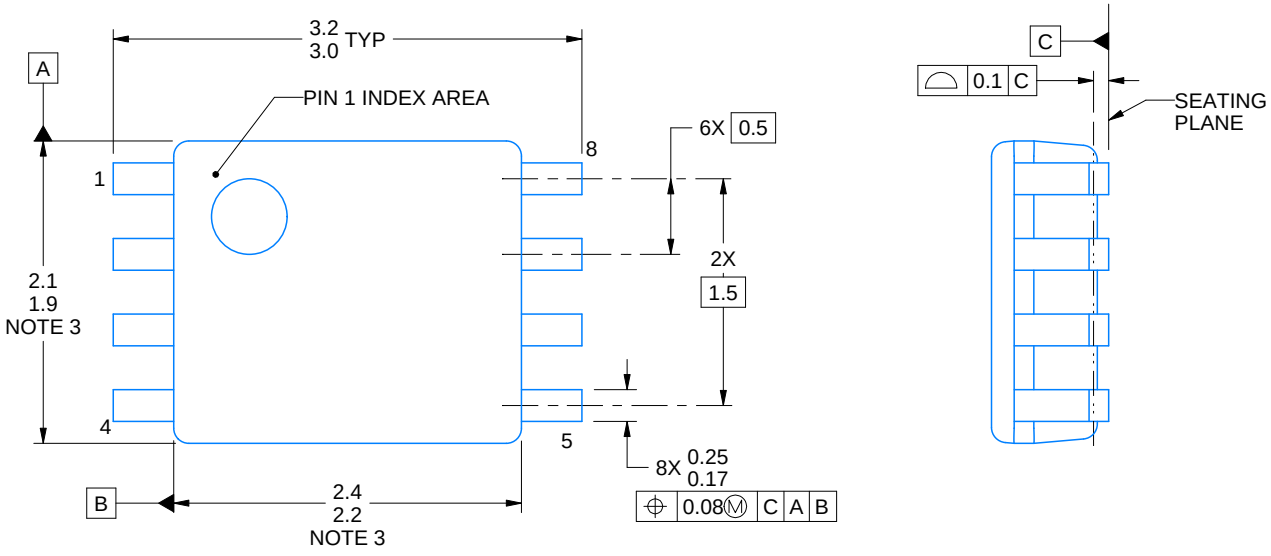
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G53DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G53DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G53DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G53DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G53YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

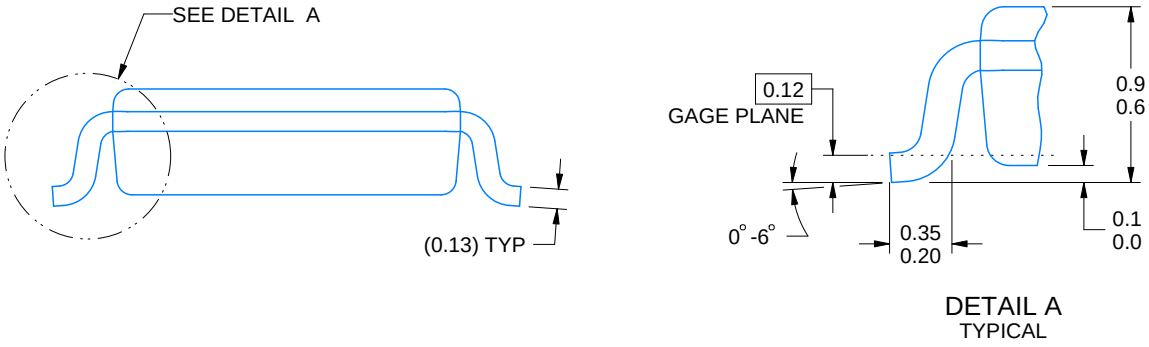
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

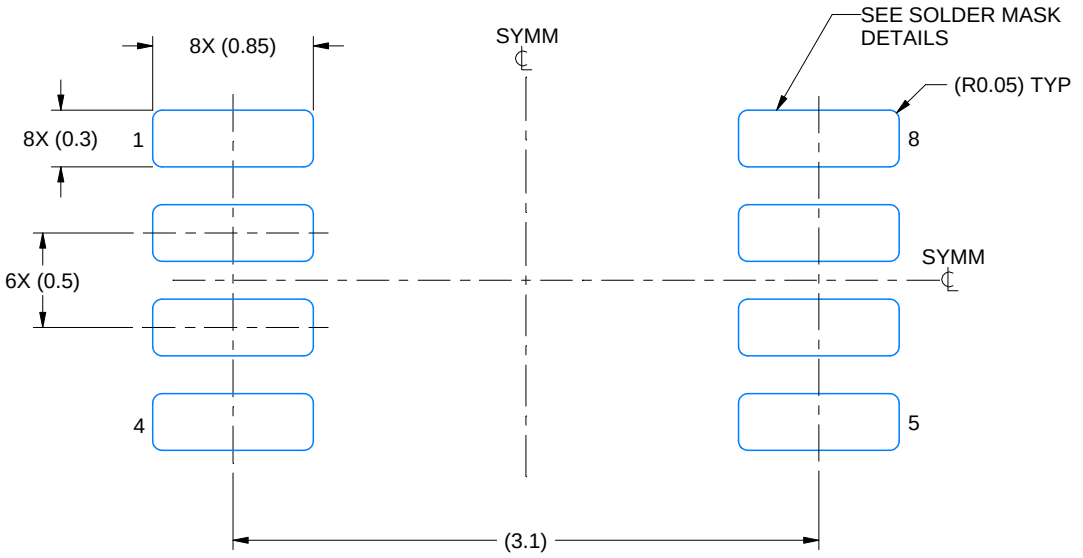




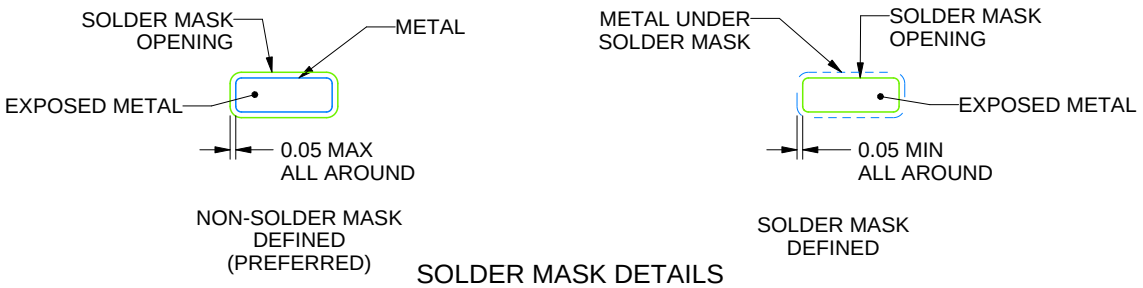
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

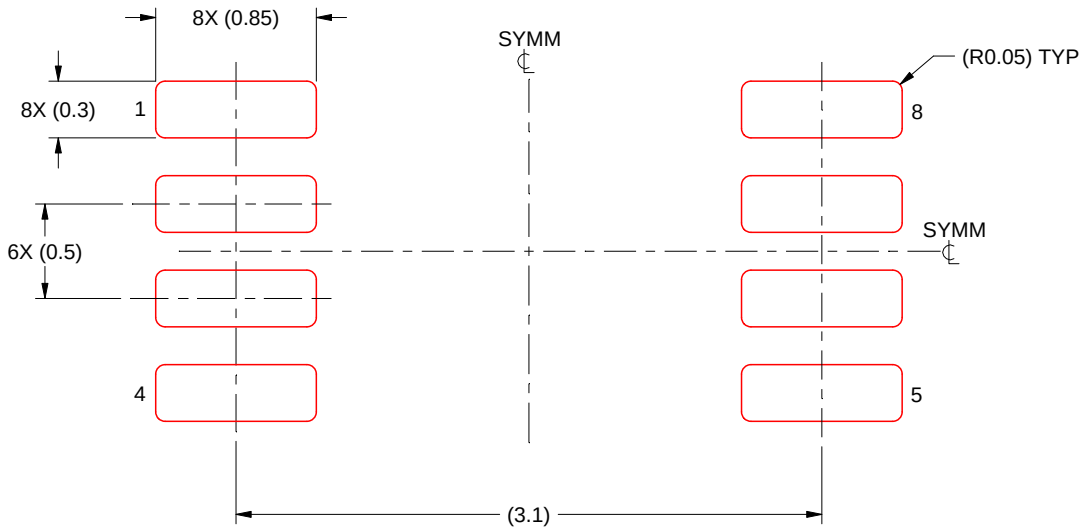


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

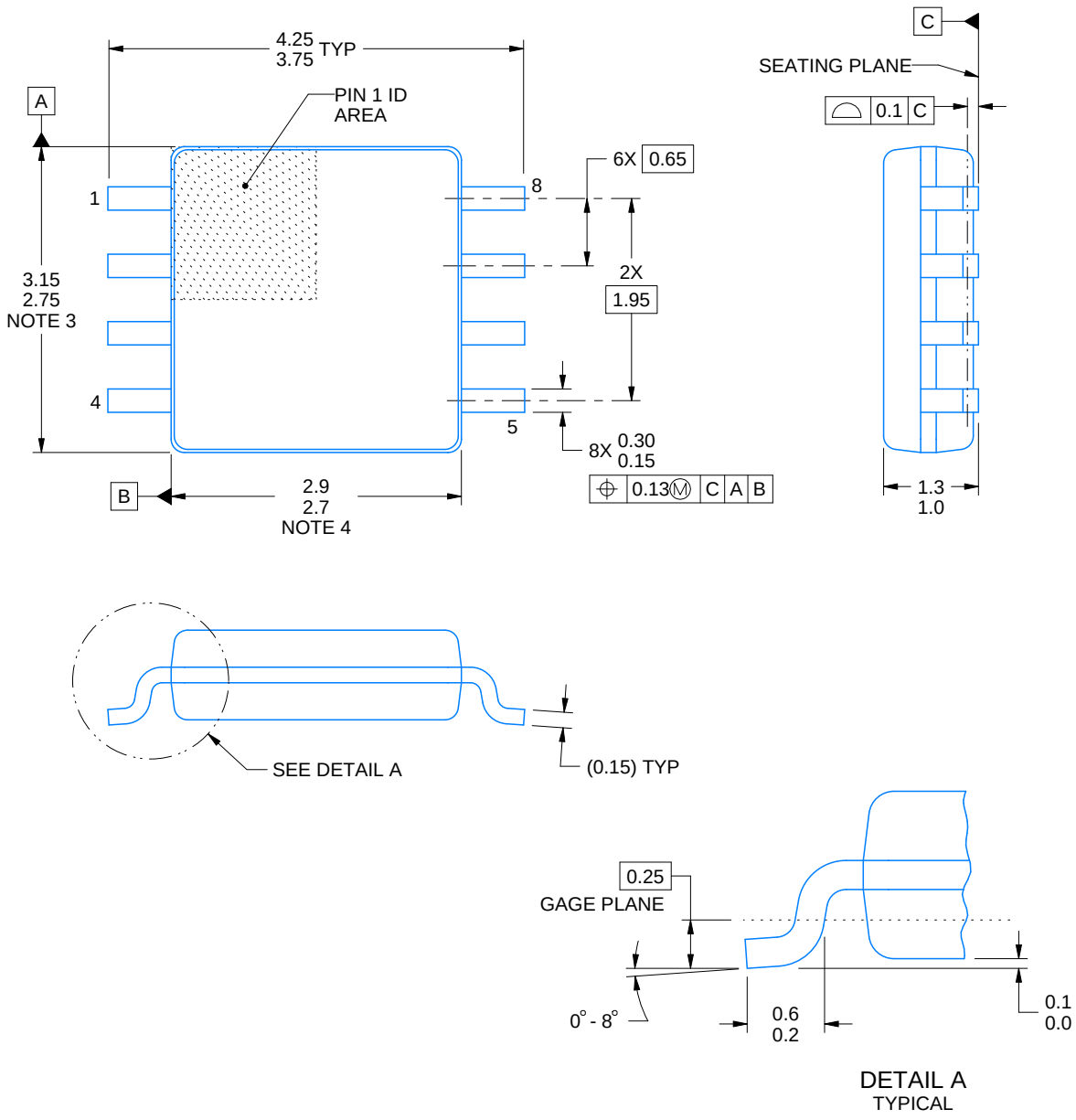
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

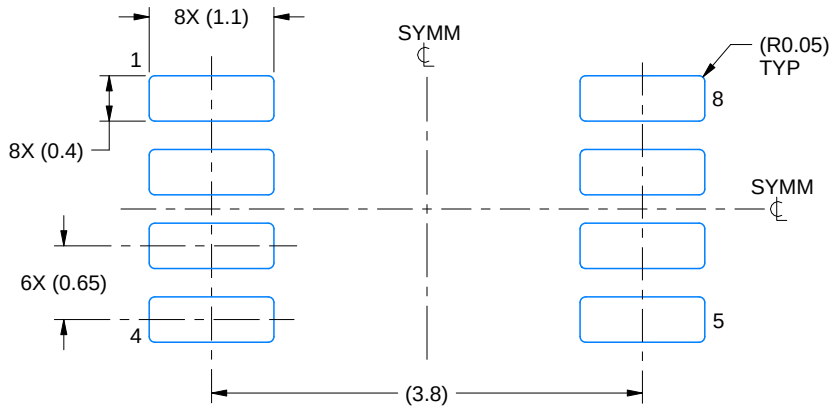
SMALL OUTLINE PACKAGE



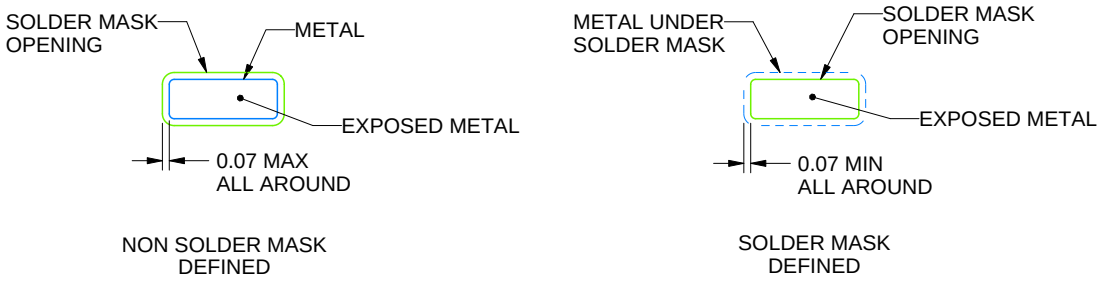
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

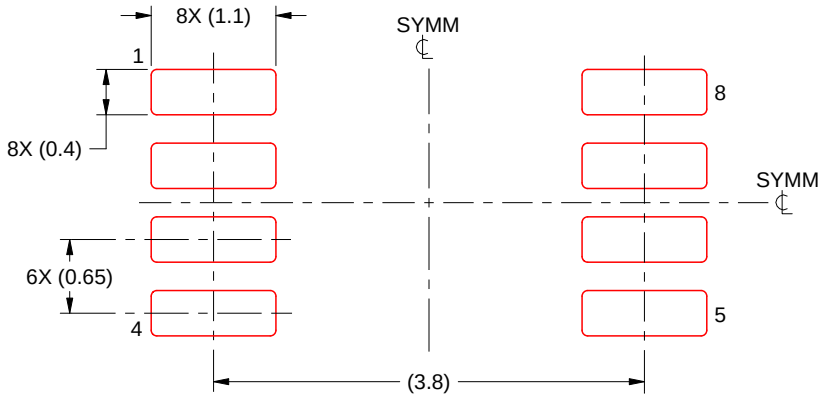


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

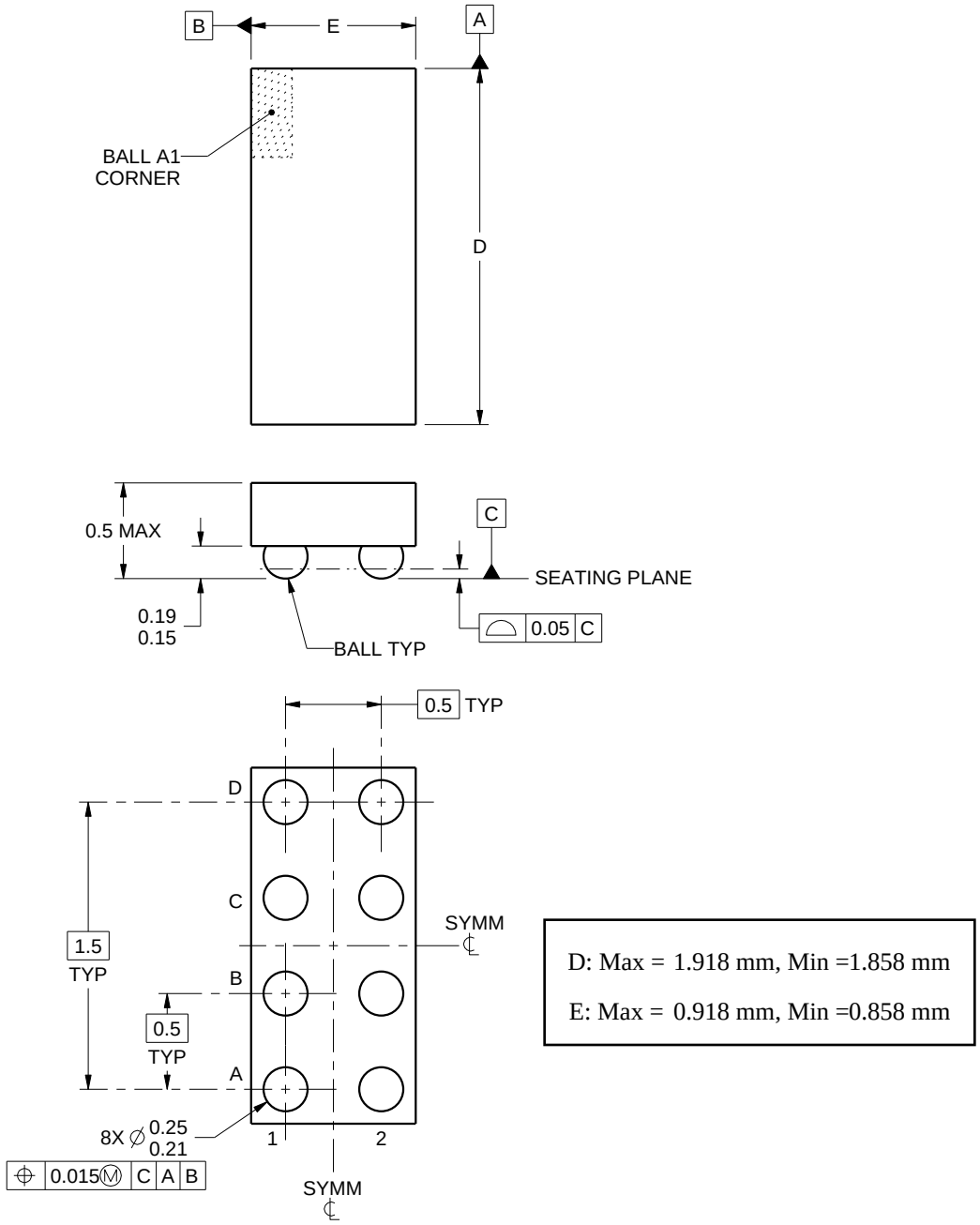
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

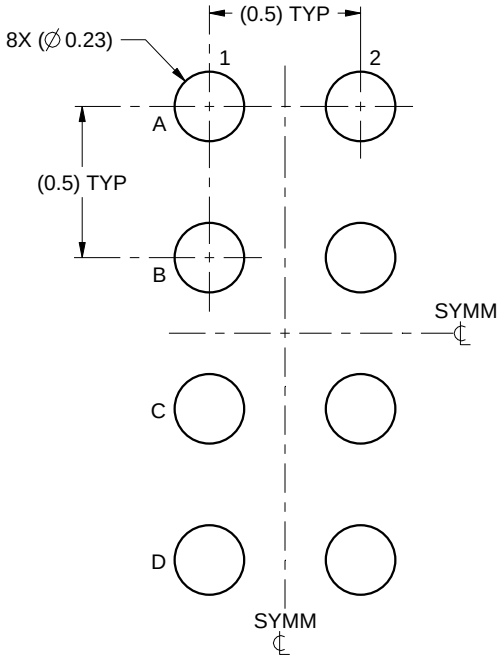
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

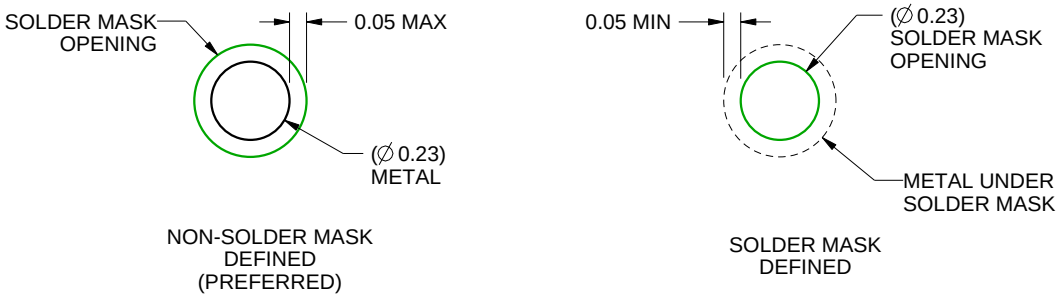


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

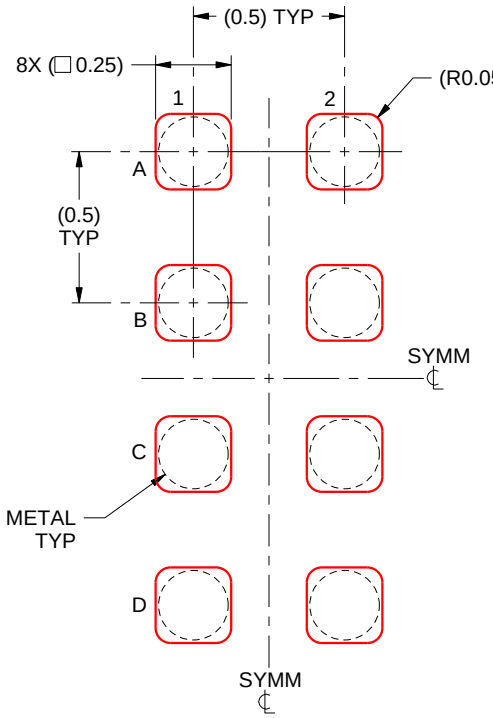


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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