

SN74LVCZ244A Octal Buffer/Driver With 3-State Outputs

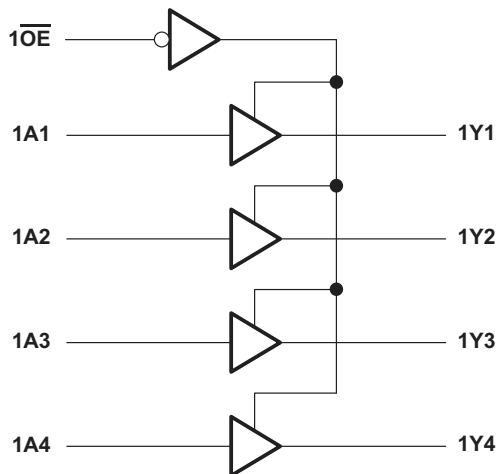
1 Features

- Operates From 2.7 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.9 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Servers
- Databases
- Memory Systems
- Network Switches
- PCs and Notebooks

4 Simplified Schematic



3 Description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCZ244A device is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCZ244A	SSOP (20)	7.50 mm x 5.30 mm
	SOP (20)	12.60 mm x 5.30 mm
	TSSOP (20)	6.50 mm x 4.40 mm
	SOIC (20)	12.80 mm x 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

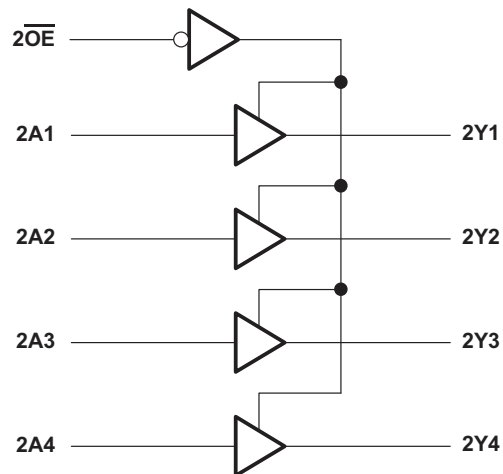


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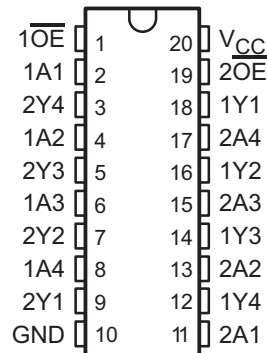
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5 Revision History

Changes from Revision H (August 2003) to Revision I	Page
• Updated document to new TI data sheet standards.	1
• Deleted Ordering Information table.	1
• Changed I_{off} bullet in Features.	1
• Added Applications.	1
• Added Pin Functions table.	3
• Added Handling Ratings table.	4
• Changed Max operating temperature to 125°C in Recommended Operating Conditions table.	4
• Added Thermal Information table.	5
• Added –40°C TO 125°C temperature range to Electrical Characteristics table.	5
• Added Switching Characteristics table for –40°C TO 125°C temperature range.	6
• Added Typical Characteristics section.	6
• Added Detailed Description section.	8
• Added Application and Implementation section.	9
• Added Power Supply Recommendations and Layout sections.	11

6 Pin Configuration and Functions

DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{1OE}$	I	Output Enable 1
2	1A1	I	1A1 Input
3	2Y4	O	2Y4 Output
4	1A2	I	1A2 Input
5	2Y3	O	2Y3 Output
6	1A3	I	1A3 Input
7	2Y2	O	2Y2 Output
8	1A4	I	1A4 Input
9	2Y1	O	2Y1 Output
10	GND	—	Ground
11	2A1	I	2A1 Input
12	1Y4	O	1Y4 Output
13	2A2	I	2A2 Input
14	1Y3	O	1Y3 Output
15	2A3	I	2A3 Input
16	1Y2	O	1Y2 Output
17	2A4	I	2A4 Input
18	1Y1	O	1Y1 Output
19	$\overline{2OE}$	I	Output Enable 2
20	V _{CC}	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-50	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 Handling Ratings

		MIN	MAX	UNIT	
T _{stg}	Storage temperature range	-65	150	°C	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	4000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	2.7	3.6	V	
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V	
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V	
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2.7 V	-12	mA	
		V _{CC} = 3 V	-24		
I _{OL}	Low-level output current	V _{CC} = 2.7 V	12	mA	
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate		6	ns/V	
Δt/ΔV _{CC}	Power-up ramp rate	150		μs/V	
T _A	Operating free-air temperature	-40	125	°C	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVCZ244A				UNIT
		DB	DW	NS	PW	
		20 PINS				
R _{θJA}	Junction-to-ambient thermal resistance	97.7	78.7	77.9	103.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	59.4	45.0	44.5	37.9	
R _{θJB}	Junction-to-board thermal resistance	52.9	46.2	45.5	54.5	
ψ _{JT}	Junction-to-top characterization parameter	21.4	18.3	18.3	3.3	
ψ _{JB}	Junction-to-board characterization parameter	52.5	45.8	45.1	53.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	–40°C TO 85°C			–40°C TO 125°C			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –100 μA	2.7 V to 3.6 V	V _{CC} – 0.2			V _{CC} – 0.2			V
	I _{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I _{OH} = –24 mA	3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA	2.7 V to 3.6 V	0.2			0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
		3 V	0.55			0.55			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V	3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V	0	±5			±5			μA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V	±5			±5			μA
I _{OZPU}	V _O = 0.5 to 2.5 V, \overline{OE} = don't care	0 to 1.5 V	±5			±5			μA
I _{OZPD}	V _O = 0.5 to 2.5 V, \overline{OE} = don't care	1.5 V to 0	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND	3.6 V	100			100			μA
	3.6 V ≤ V _I ≤ 5.5 V ⁽²⁾		100			100			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	100			100			μA
C _i	V _I = V _{CC} or GND	3.3 V	3.5			—			pF
C _o	V _O = V _{CC} or GND	3.3 V	5.5			—			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

7.6 Switching Characteristics, –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	6.9		1.5	5.9	ns
t _{en}	\overline{OE}	A or B	8.6		1.5	7.6	ns
t _{dis}	\overline{OE}	A or B	6.8		1.5	6.5	ns

7.7 Switching Characteristics, –40°C to 125°C

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

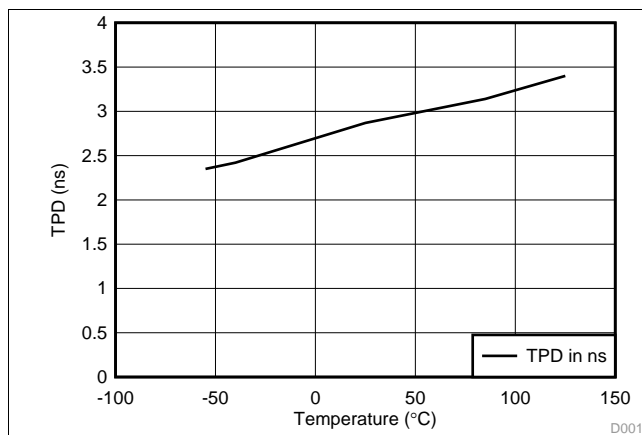
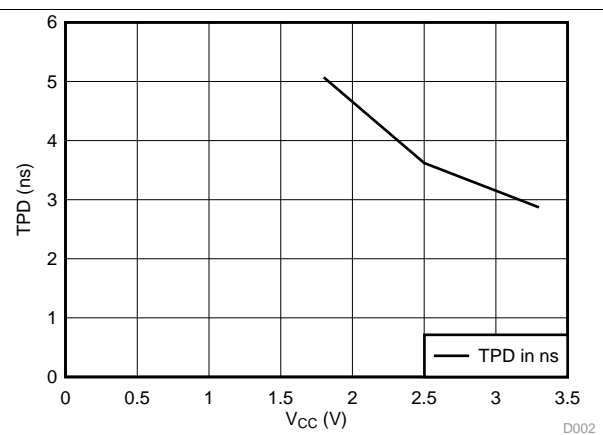
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A		7.4	1.5	6.4	ns
t_{en}	\overline{OE}	A or B		9.1	1.5	8.1	ns
t_{dis}	\overline{OE}	A or B		7.3	1.5	7.1	ns

7.8 Operating Characteristics

 $T_A = 25^\circ\text{C}$

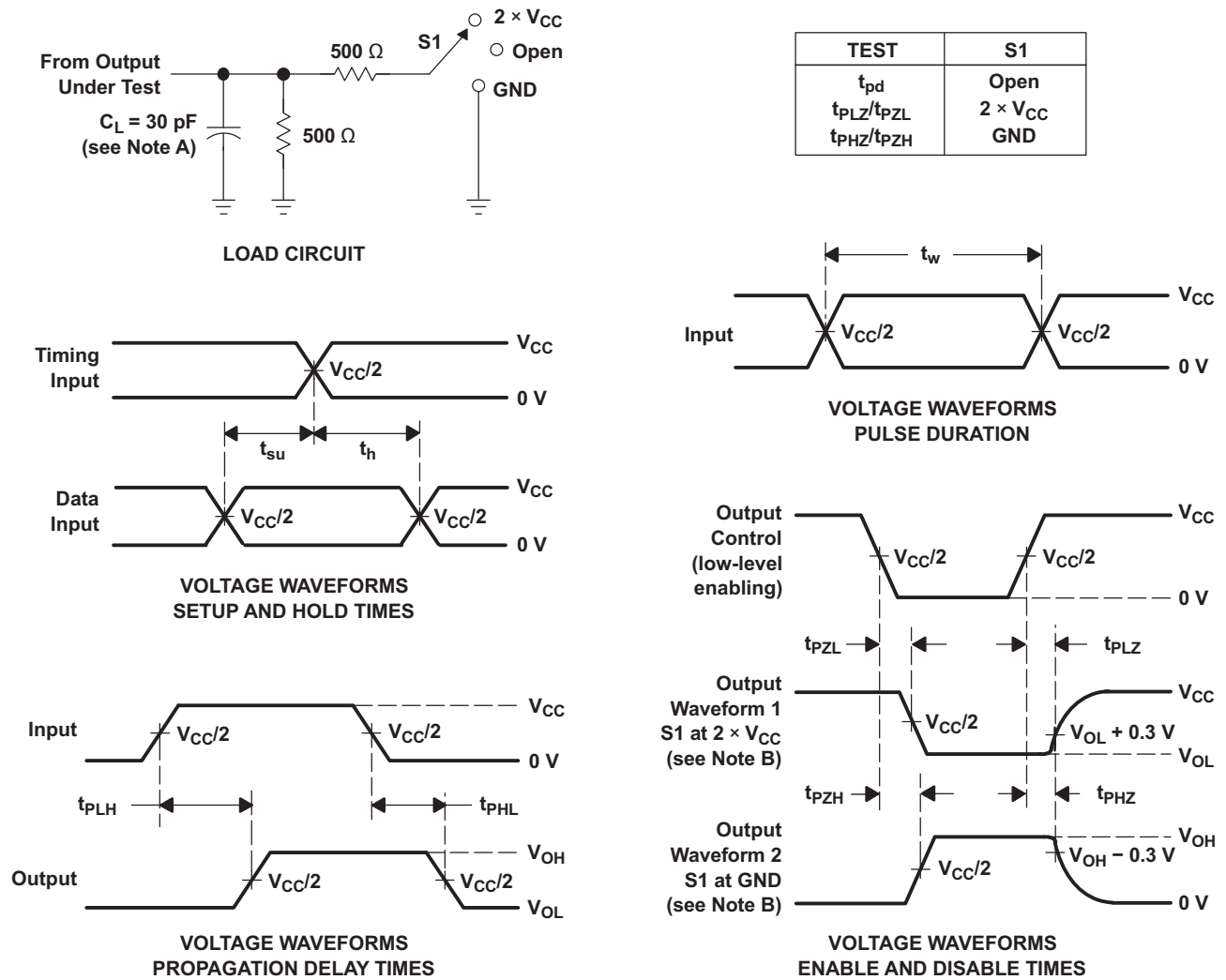
PARAMETER		TEST CONDITIONS	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	40	pF
		Outputs disabled	3	

7.9 Typical Characteristics


Figure 1. TPD Across Temperature at 3.3 V

Figure 2. TPD Across V_{CC} at 25°C

8 Parameter Measurement Information

8.1 $V_{CC} = 2.7\text{ V}$ and $3.3\text{ V} \pm 0.3\text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

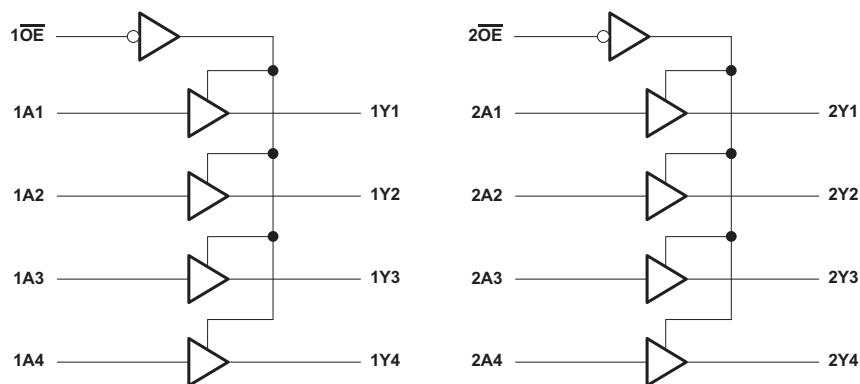
The SN74LVCZ244A device is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

9.2 Functional Block Diagram



9.3 Feature Description

- Wide operating voltage range
 - Operates from 2.7 V to 3.6 V
- Allows down-voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V
- Power-up 3-state feature
 - Keeps the outputs in high impedance during power up and allows for hot insertion

9.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUTS
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	High-Z

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

The SN74LVCZ244A device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

10.2 Typical Application

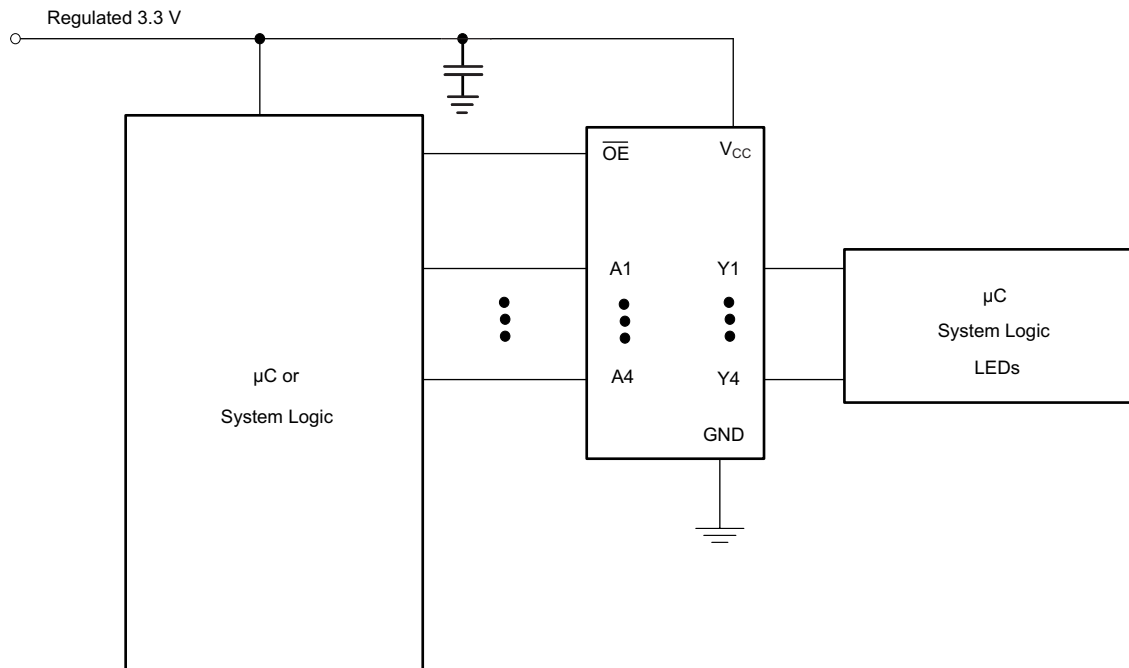


Figure 4. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention, because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

Typical Application (continued)

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:

- For rise time and fall time specifications, see $\Delta t/\Delta V$ in the *Recommended Operating Conditions* table.
- For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
- Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .

2. Recommend Output Conditions:

- Load currents should not exceed 50 mA per output and 100 mA total for the part.
- Outputs should not be pulled above V_{CC} .

10.2.3 Application Curves

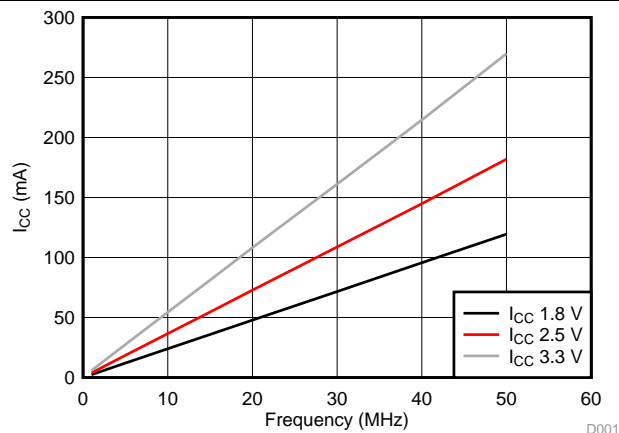


Figure 5. I_{CC} vs Frequency

D001

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF bypass capacitor is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

12.2 Layout Example

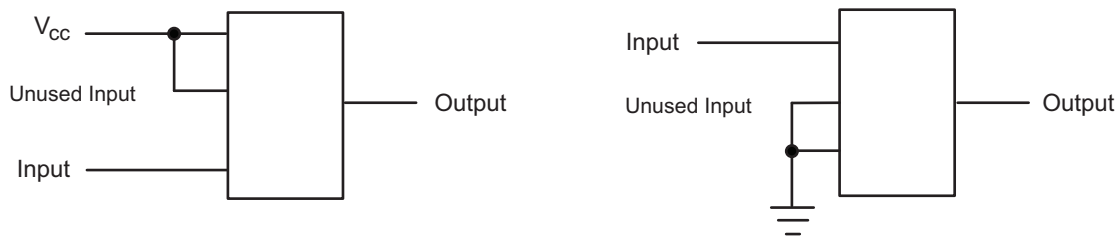


Figure 6. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCZ244ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A	Samples
SN74LVCZ244ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCZ244A	Samples
SN74LVCZ244ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCZ244A	Samples
SN74LVCZ244APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A	Samples
SN74LVCZ244APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A	Samples
SN74LVCZ244APWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV244A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCZ244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCZ244ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVCZ244ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVCZ244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCZ244APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCZ244ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LVCZ244ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVCZ244ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVCZ244APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LVCZ244APWT	TSSOP	PW	20	250	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVCZ244APW	PW	TSSOP	20	70	530	10.2	3600	3.5

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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