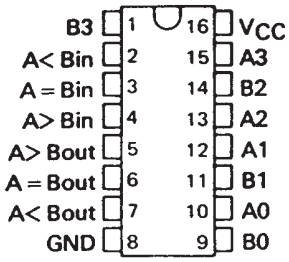
| TYPE | TYPICAL POWER DISSIPATION | TYPICAL DELAY (4-BIT WORDS) |
|---|---|---|
| '85 | 275 mW | 23 ns |
| 'LS85 | 52 mW | 24 ns |
| 'S85 | 365 mW | 11 ns |

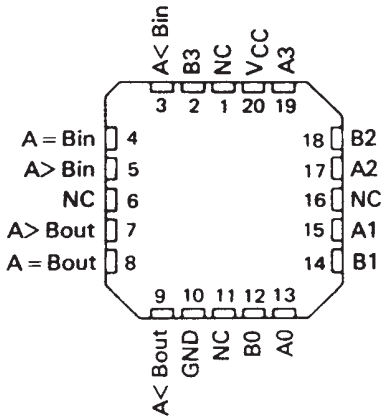
## description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

**SN5485, SN54LS85, SN54S85 . . . J OR W PACKAGE**
**SN7485 . . . N PACKAGE**
**SN74LS85, SN74S85 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54LS85, SN54S85 . . . FK PACKAGE**
**(TOP VIEW)**

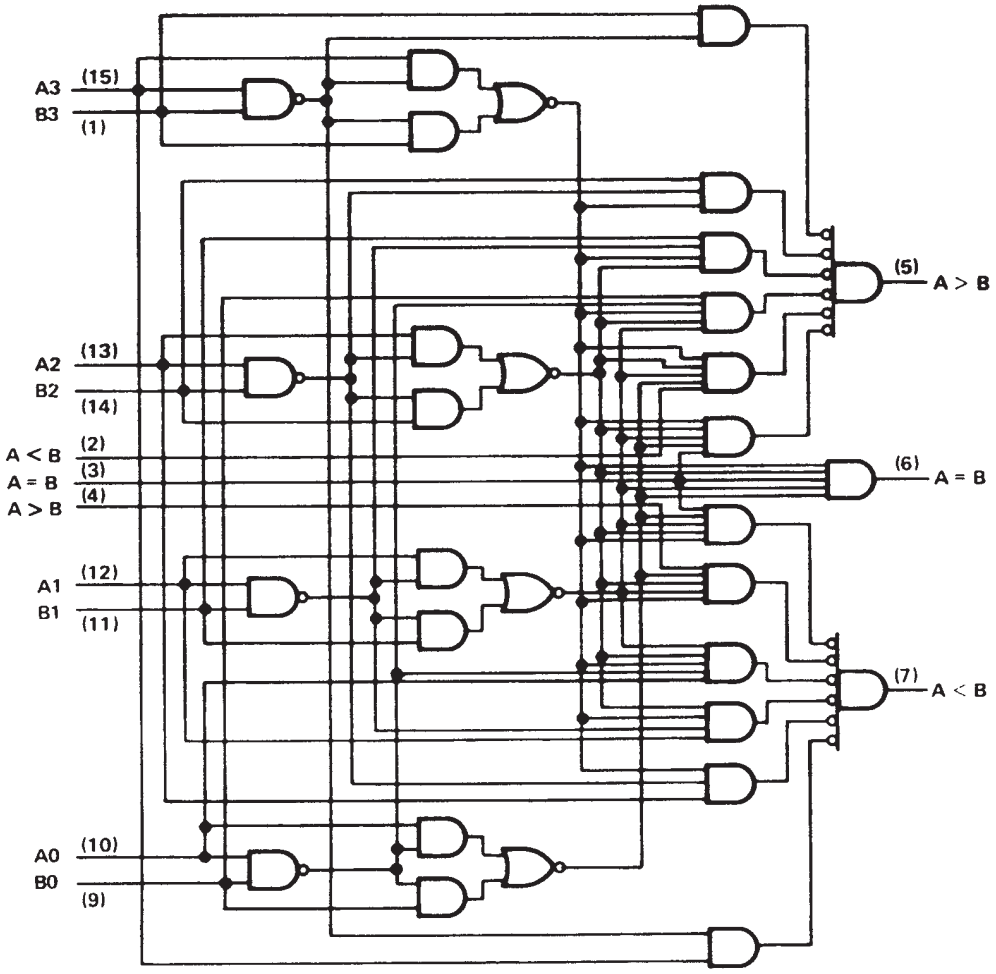



NC - No internal connection

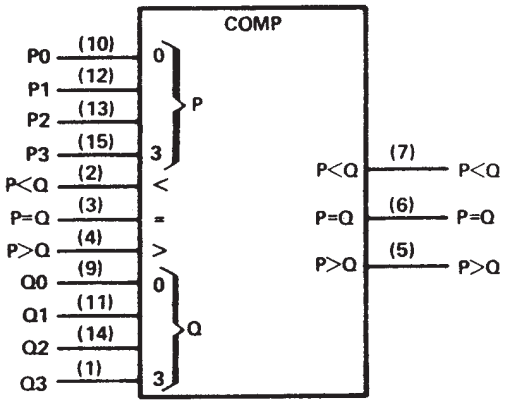
**FUNCTION TABLE**

| COMPARING INPUTS | | | | CASCADING INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A > B | A < B | A = B | A > B | A < B | A = B |
| A3 > B3 | X | X | X | X | X | X | H | L | L |
| A3 < B3 | X | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 > B2 | X | X | X | X | X | H | L | L |
| A3 = B3 | A2 < B2 | X | X | X | X | X | L | H | L |
| A3 = B2 | A2 = B2 | A1 > B1 | X | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | L | H | L |
| A2 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | L | L | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | H | L | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | X | X | H | L | L | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | H | L | L | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | L | H | H | L |

**logic diagrams (positive logic)**

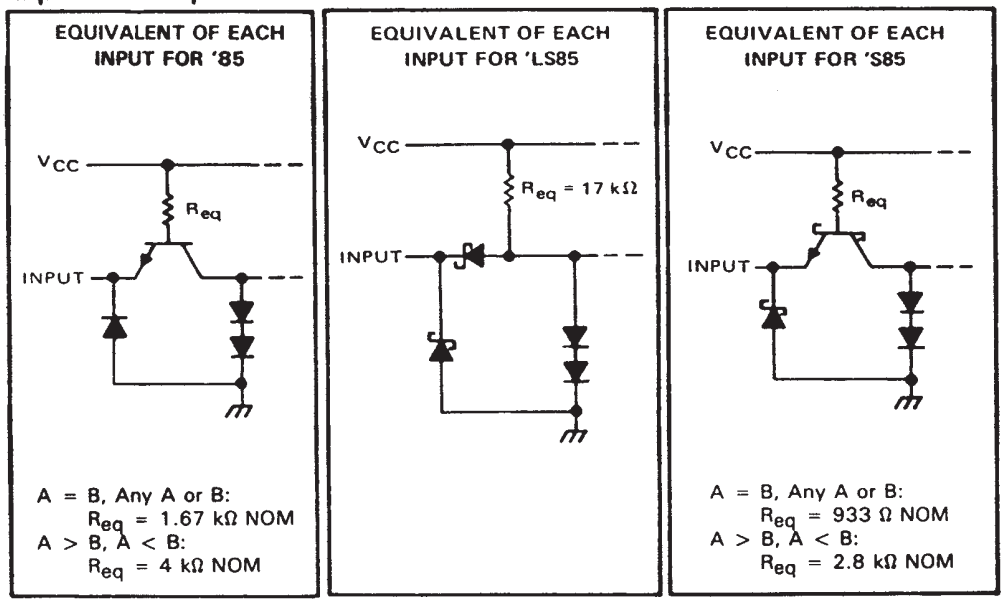


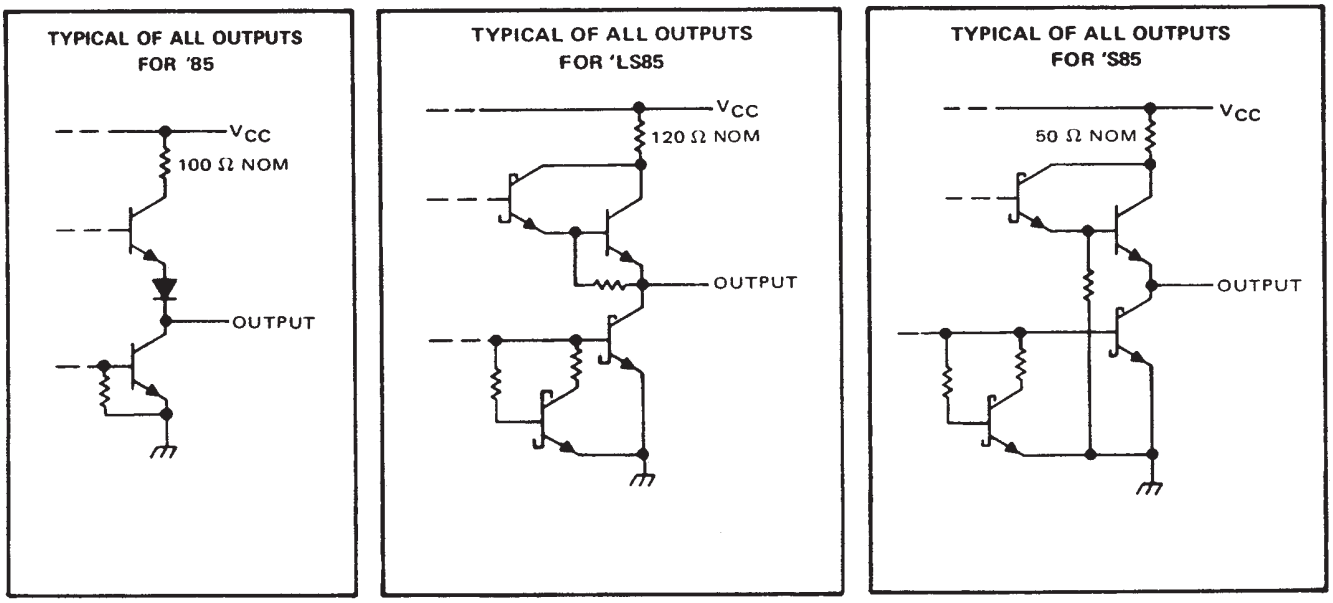

**logic symbol†**




†This symbol is in accordancae with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | SN54' SN54S' | SN54LS' | SN74' SN74S' | SN74LS' | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | 7 | 7 | 7 | 7 | V |
| Input voltage | 5.5 | 7 | 5.5 | 7 | V |
| Interemitter voltage (see Note 2) | 5.5 | | 5.5 | | V |
| Operating free-air temperature range | −55 to 125 | | −0 to 70 | | °C |
| Storage temperature range | −65 to 150 | | −65 to 150 | | °C |

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A input in conjunction with its respective B input of the '85 and 'S85.

## recommended operating conditions

| | SN5485 | | | SN7485 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | 16 | | | 16 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $I_{OH}$ = −400 μA | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | A < B, A > B inputs | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | | 40 | μA |
| | | all other inputs | | | | | | 120 | |
| $I_{IL}$ | Low-level input current | A < B, A > B inputs | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −1.6 | mA |
| | | all other inputs | | | | | | −4.8 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX, | $V_O$ = 0 | SN5485 | −20 | | −55 | mA |
| | | | | | SN7485 | −18 | | −55 | |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, | See Note 4 | | | 55 | 88 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
NOTE 4: $I_{CC}$ is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM INPUT | TO OUTPUT | NUMBER OF GATE LEVELS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Any A or B data input | A < B, A > B | 1 | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 5 | | 7 | | ns |
| | | | 2 | | | 12 | | |
| | | | 3 | | | 17 | 26 | |
| | | A = B | 4 | | | 23 | 35 | |
| $t_{PHL}$ | Any A or B data input | A < B, A > B | 1 | | | 11 | | ns |
| | | | 2 | | | 15 | | |
| | | | 3 | | | 20 | 30 | |
| | | A = B | 4 | | | 20 | 30 | |
| $t_{PLH}$ | A < B or A = B | A > B | 1 | | | 7 | 11 | ns |
| $t_{PHL}$ | A < B or A = B | A > B | 1 | | | 11 | 17 | ns |
| $t_{PLH}$ | A = B | A = B | 2 | | | 13 | 20 | ns |
| $t_{PHL}$ | A = B | A = B | 2 | | | 11 | 17 | ns |
| $t_{PLH}$ | A > B or A = B | A < B | 1 | | | 7 | 11 | ns |
| $t_{PHL}$ | A > B or A = B | A < B | 1 | | | 11 | 17 | ns |

¶$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | SN54LS85 | | | SN74LS85 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | 4 | | | 8 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | SN54LS85 | | | SN74LS85 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.7 | | | 0.7 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $I_{OH}$ = −400 μA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | A < B, A > B inputs | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| | | all other inputs | | | | | 0.3 | | | 0.3 | |
| $I_{IH}$ | High-level input current | A < B, A > B inputs | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| | | all other inputs | | | | | 60 | | | 60 | |
| $I_{IL}$ | Low-level input current | A < B, A > B inputs | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | −0.4 | | | −0.4 | mA |
| | | all other inputs | | | | | −1.2 | | | −1.2 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, | See Note 4 | | 10.4 | 20 | | 10.4 | 20 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 4: $I_{CC}$ is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM INPUT | TO OUTPUT | NUMBER OF GATE LEVELS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Any A or B data input | A < B, A > B | 1 | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 5 | | 14 | | ns |
| | | | 2 | | | 19 | | |
| | | | 3 | | | 24 | 36 | |
| | | A = B | 4 | | | 27 | 45 | |
| $t_{PHL}$ | Any A or B data input | A < B, A > B | 1 | | | 11 | | ns |
| | | | 2 | | | 15 | | |
| | | | 3 | | | 20 | 30 | |
| | | A = B | 4 | | | 23 | 45 | |
| $t_{PLH}$ | A < B or A = B | A > B | 1 | | | 14 | 22 | ns |
| $t_{PHL}$ | A < B or A = B | A > B | 1 | | | 11 | 17 | ns |
| $t_{PLH}$ | A = B | A = B | 2 | | | 13 | 20 | ns |
| $t_{PHL}$ | A = B | A = B | 2 | | | 13 | 26 | ns |
| $t_{PLH}$ | A > B or A = B | A < B | 1 | | | 14 | 22 | ns |
| $t_{PHL}$ | A > B or A = B | A < B | 1 | | | 11 | 17 | ns |

¶$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | SN54S85 | | | SN74S85 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −1 | | | −1 | mA |
| Low-level output current, $I_{OL}$ | | | 20 | | | 20 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.2 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | SN54S85 | 2.5 | 3.4 | | V |
| | | | | SN74S85 | 2.7 | 3.4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 20 mA | | | | 0.5 | V |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | A < B, A > B inputs | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 50 | μA |
| | | all other inputs | | | | | 150 | |
| $I_{IL}$ | Low-level input current | A < B, A > B inputs | $V_{CC}$ = MAX, $V_I$ = 0.5 V | | | | −2 | mA |
| | | all other inputs | | | | | −6 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | | −40 | | −100 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, See Note 4 | | | 73 | 115 | mA |
| | | | $V_{CC}$ = MAX, $T_A$ = 125°C, See Note 4 | SN54S85W | | | 110 | |

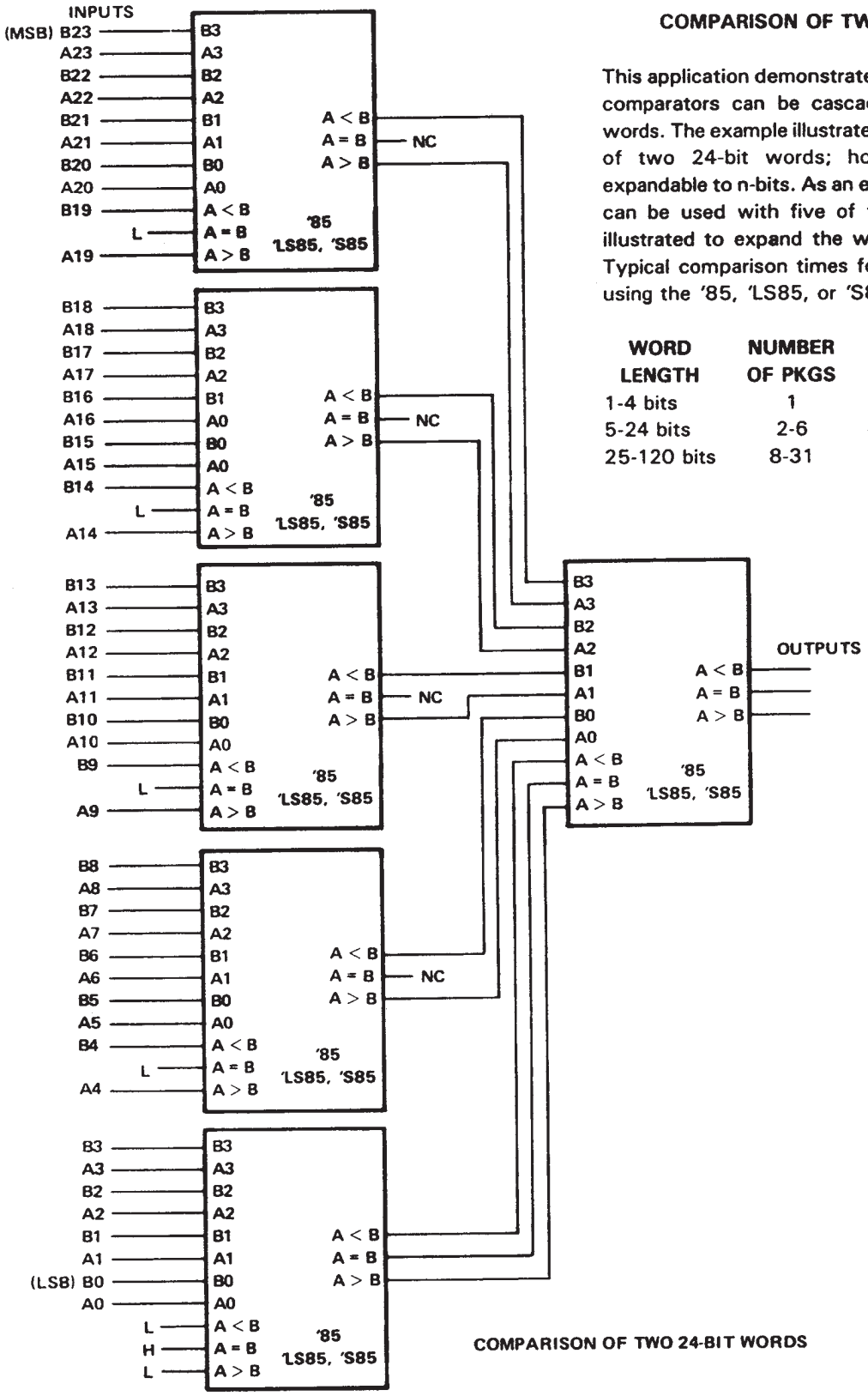
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 4: $I_{CC}$ is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM INPUT | TO OUTPUT | NUMBER OF GATE LEVELS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Any A or B data input | A < B, A > B | 1 | $C_L$ = 15 pF, $R_L$ = 280 Ω, See Note 5 | | 5 | | ns |
| | | | 2 | | | 7.5 | | |
| | | | 3 | | | 10.5 | 16 | |
| | | A = B | 4 | | | 12 | 18 | |
| $t_{PHL}$ | Any A or B data input | A < B, A > B | 1 | | | 5.5 | | ns |
| | | | 2 | | | 7 | | |
| | | | 3 | | | 11 | 16.5 | |
| | | A = B | 4 | | | 11 | 16.5 | |
| $t_{PLH}$ | A < B or A = B | A > B | 1 | | | 5 | 7.5 | ns |
| $t_{PHL}$ | A < B or A = B | A > B | 1 | | | 5.5 | 8.5 | ns |
| $t_{PLH}$ | A = B | A = B | 2 | | | 7 | 10.5 | ns |
| $t_{PHL}$ | A = B | A = B | 2 | | | 5 | 7.5 | ns |
| $t_{PLH}$ | A > B or A = B | A < B | 1 | | | 5 | 7.5 | ns |
| $t_{PHL}$ | A > B or A = B | A < B | 1 | | | 5.5 | 8.5 | ns |

¶$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

## TYPICAL APPLICATION DATA




### COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the '85, 'LS85, or 'S85 are:

| WORD LENGTH | NUMBER OF PKGS | '85 | 'LS85 | 'S85 |
|---|---|---|---|---|
| 1-4 bits | 1 | 23 ns | 24 ns | 11 ns |
| 5-24 bits | 2-6 | 46 ns | 48 ns | 22 ns |
| 25-120 bits | 8-31 | 69 ns | 72 ns | 33 ns |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9754701Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9754701Q2A SNJ54LS 85FK | Samples |
| 5962-9754701QEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9754701QE A SNJ54LS85J | Samples |
| 5962-9754701QFA | ACTIVE | CFP | W | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9754701QF A SNJ54LS85W | Samples |
| JM38510/08201BEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 08201BEA | Samples |
| JM38510/31101B2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31101B2A | Samples |
| JM38510/31101BEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31101BEA | Samples |
| JM38510/31101BFA | ACTIVE | CFP | W | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31101BFA | Samples |
| M38510/08201BEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 08201BEA | Samples |
| M38510/31101B2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31101B2A | Samples |
| M38510/31101BEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31101BEA | Samples |
| M38510/31101BFA | ACTIVE | CFP | W | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 31101BFA | Samples |
| SN54LS85J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS85J | Samples |
| SN54S85J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54S85J | Samples |
| SN74LS85D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | 0 to 70 | LS85 | |
| SN74LS85DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS85 | Samples |
| SN74LS85N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS85N | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS85NSR | ACTIVE | SOP | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS85 | Samples |
| SN74S85D | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S85 | Samples |
| SN74S85N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S85N | Samples |
| SNJ54LS85FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9754701Q2A SNJ54LS 85FK | Samples |
| SNJ54LS85J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9754701QE A SNJ54LS85J | Samples |
| SNJ54LS85W | ACTIVE | CFP | W | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9754701QF A SNJ54LS85W | Samples |
| SNJ54S85FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S 85FK | Samples |
| SNJ54S85J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S85J | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN54LS85, SN54S85, SN74LS85, SN74S85 :**

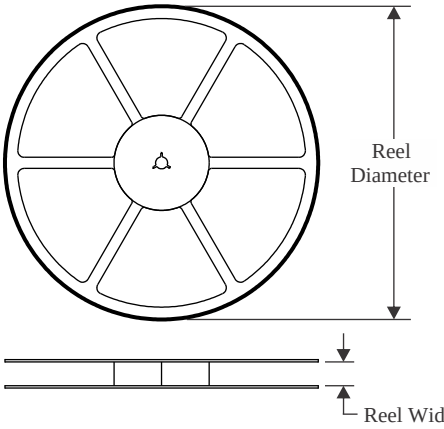
- Catalog : SN74LS85, SN74S85
- Military : SN54LS85, SN54S85

NOTE: Qualified Version Definitions:

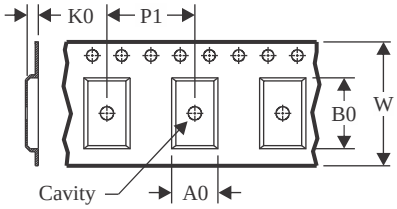
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

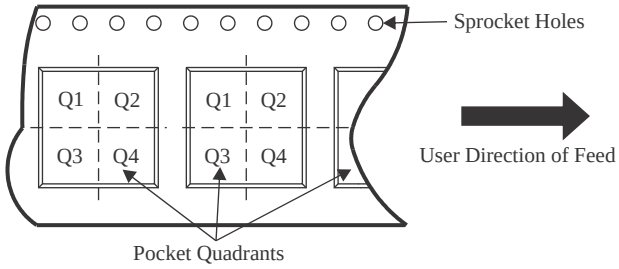



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

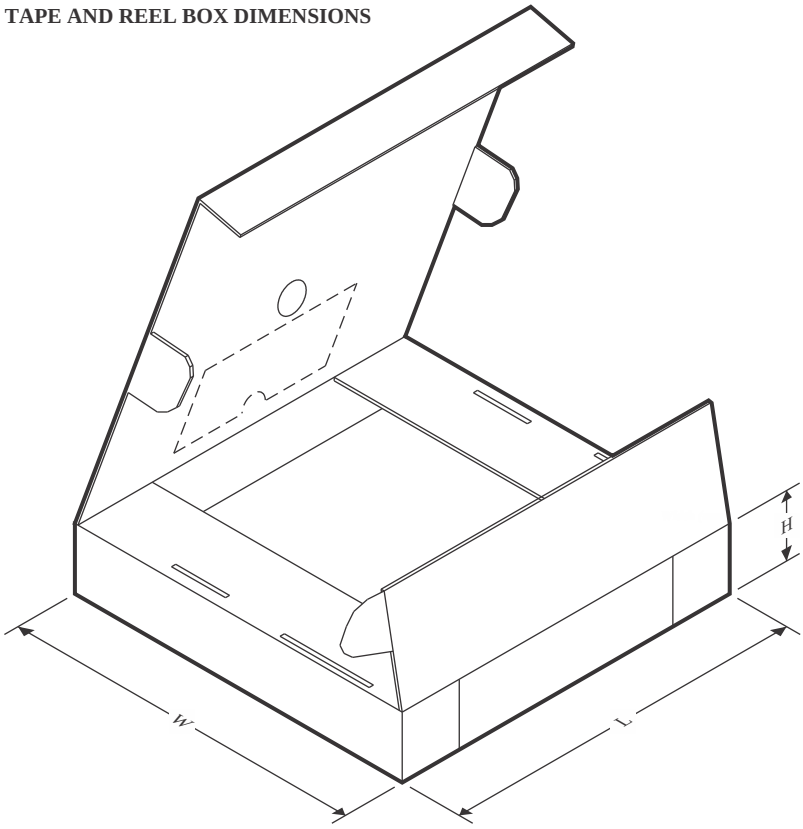
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS85DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS85NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

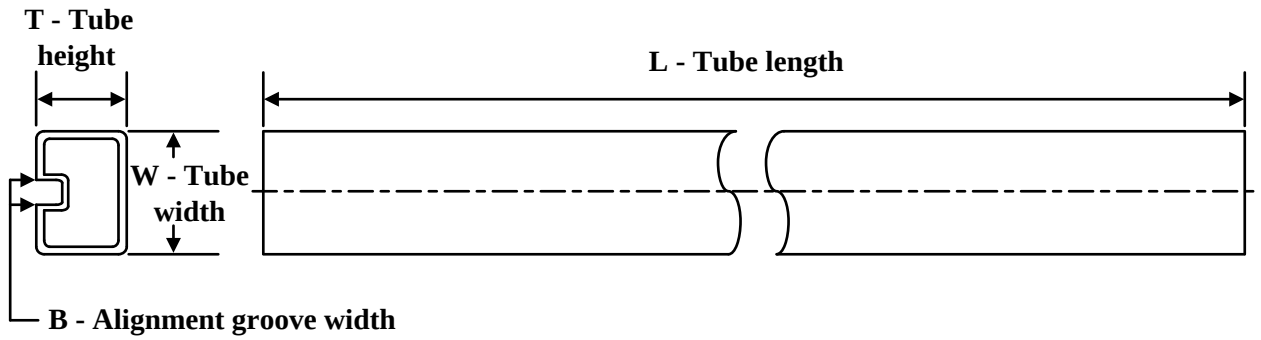
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

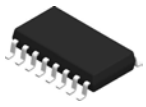
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS85DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LS85NSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9754701Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9754701QFA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/31101B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/31101BFA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| M38510/31101B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| M38510/31101BFA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74LS85N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS85N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74S85D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74S85N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74S85N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54LS85FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LS85W | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54S85FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

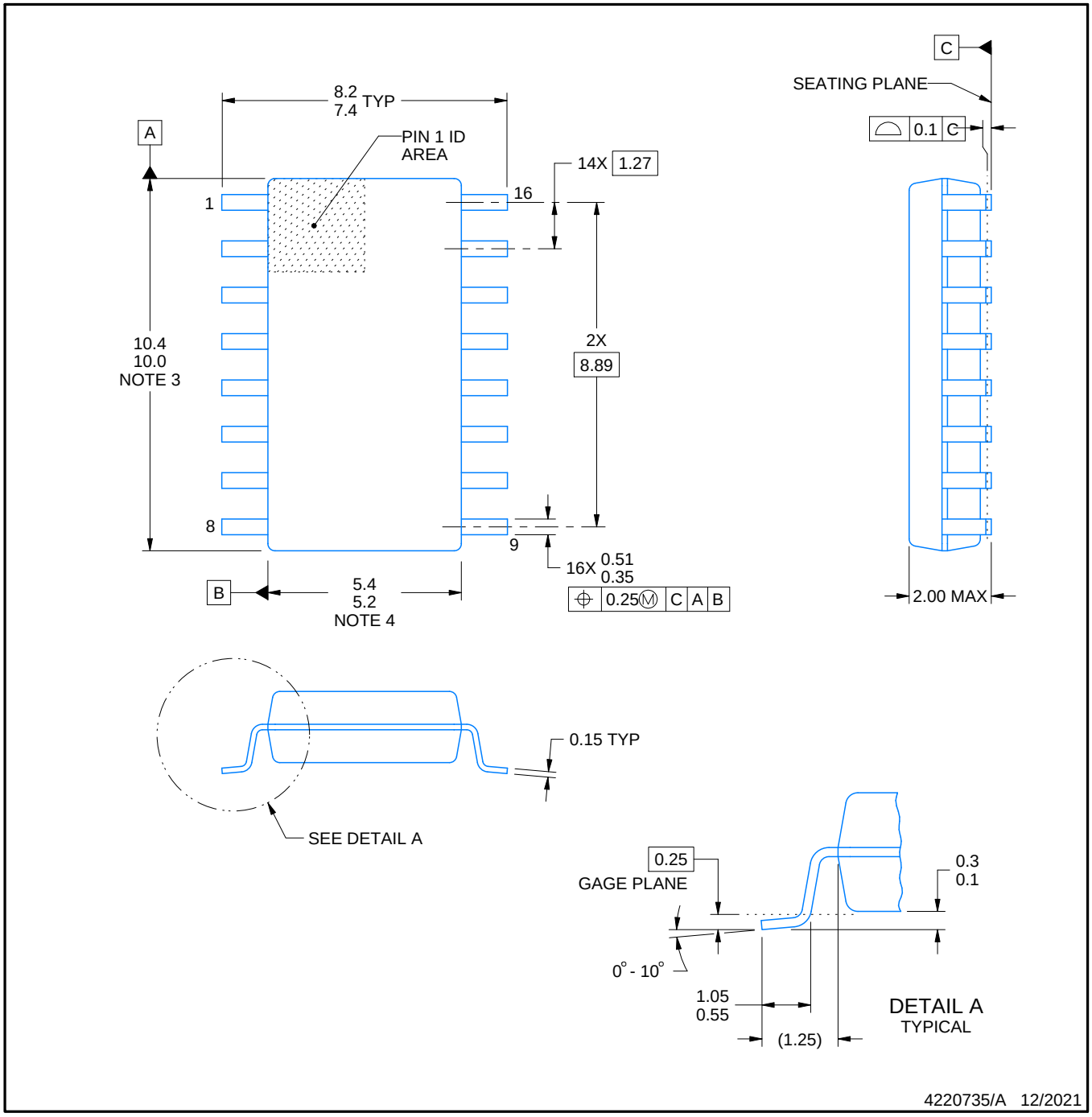


# PACKAGE OUTLINE

## NS0016A

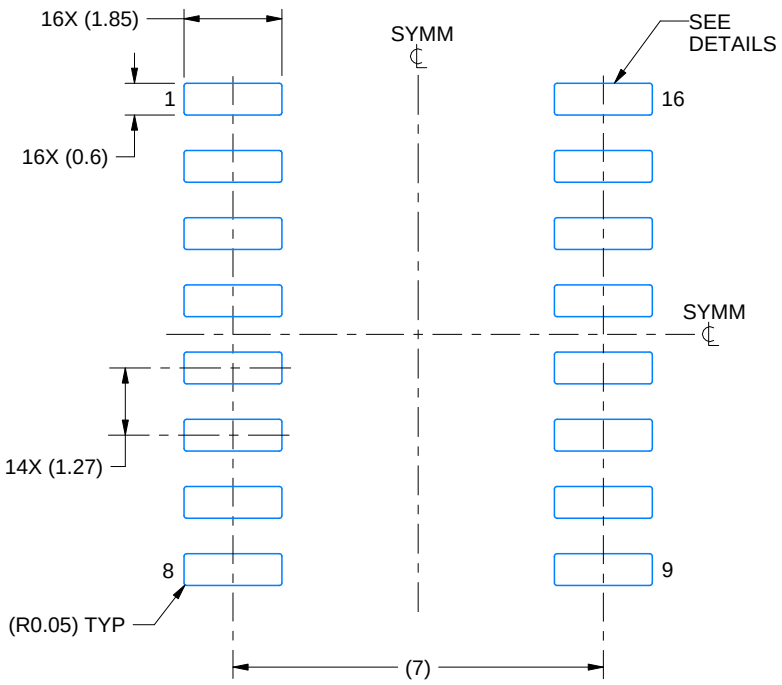
## SOP - 2.00 mm max height

SOP

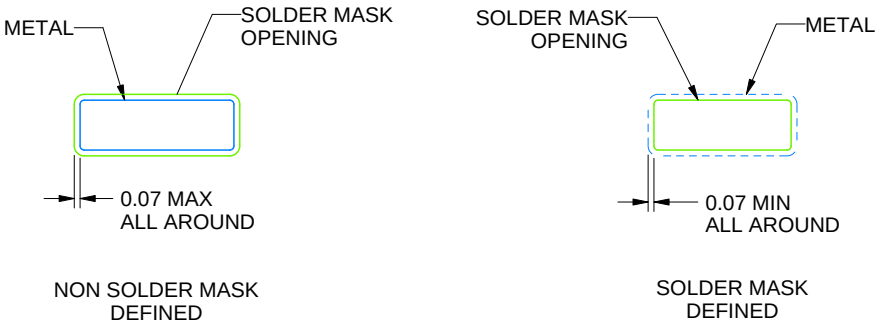



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

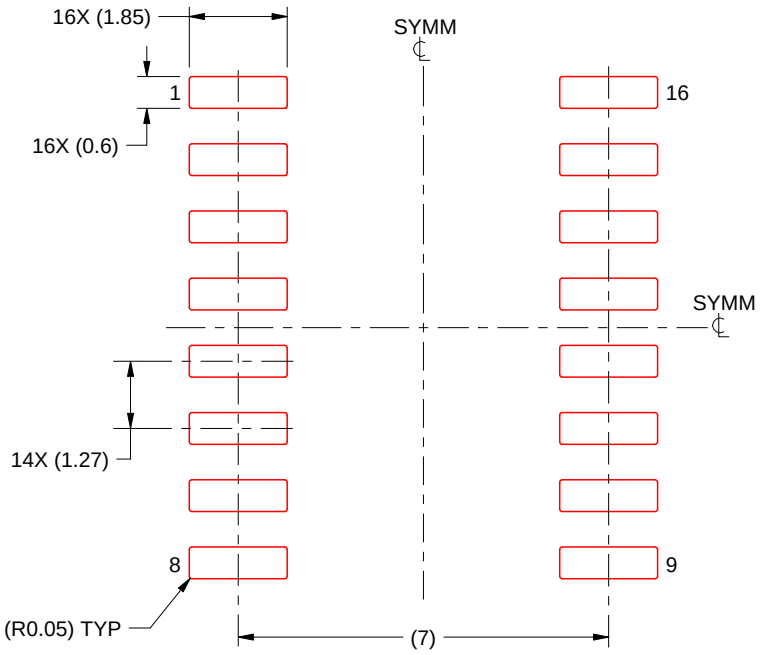
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



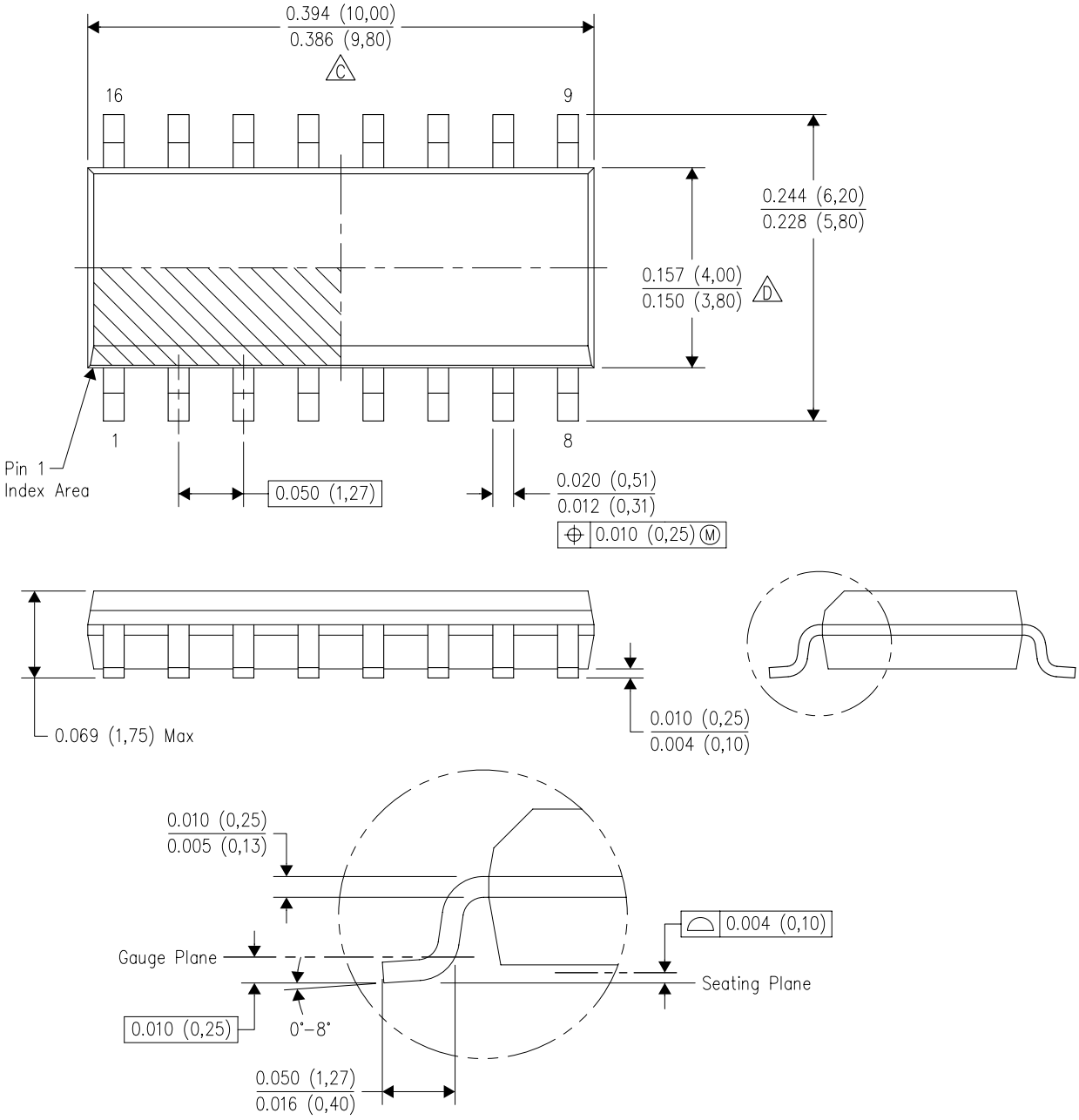

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

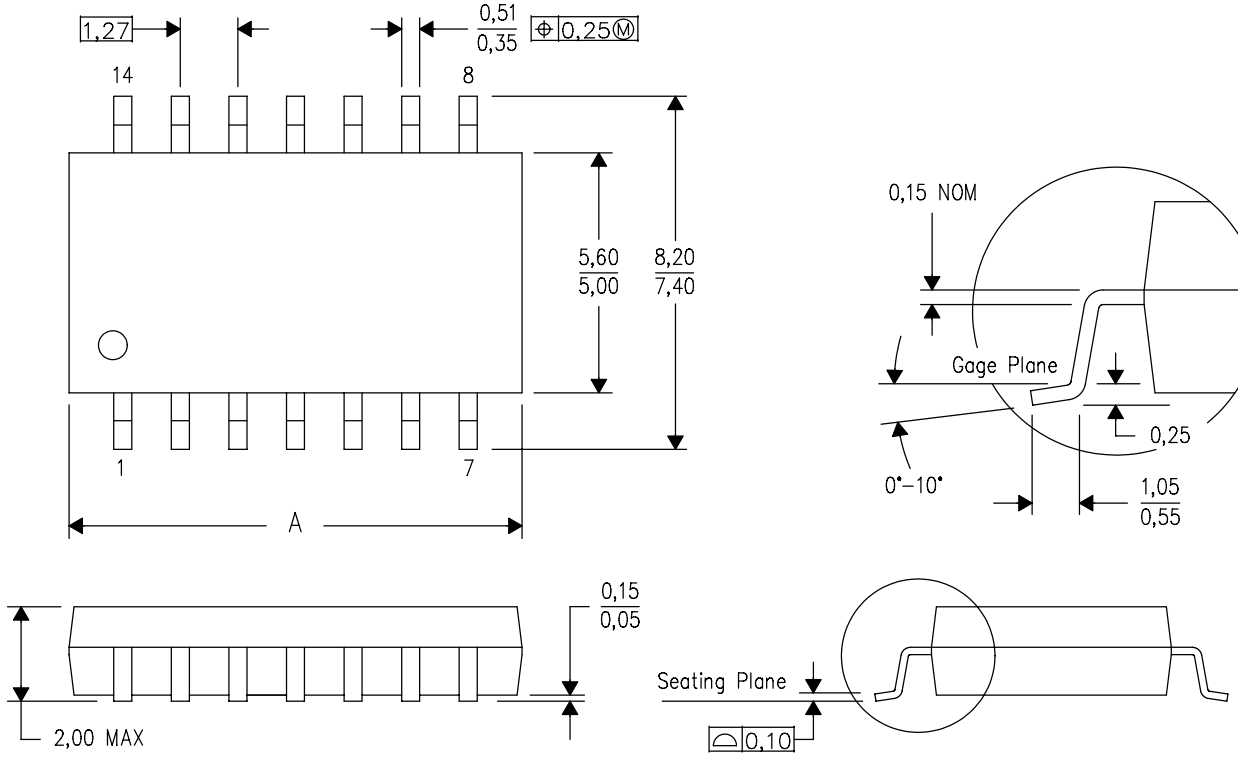



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

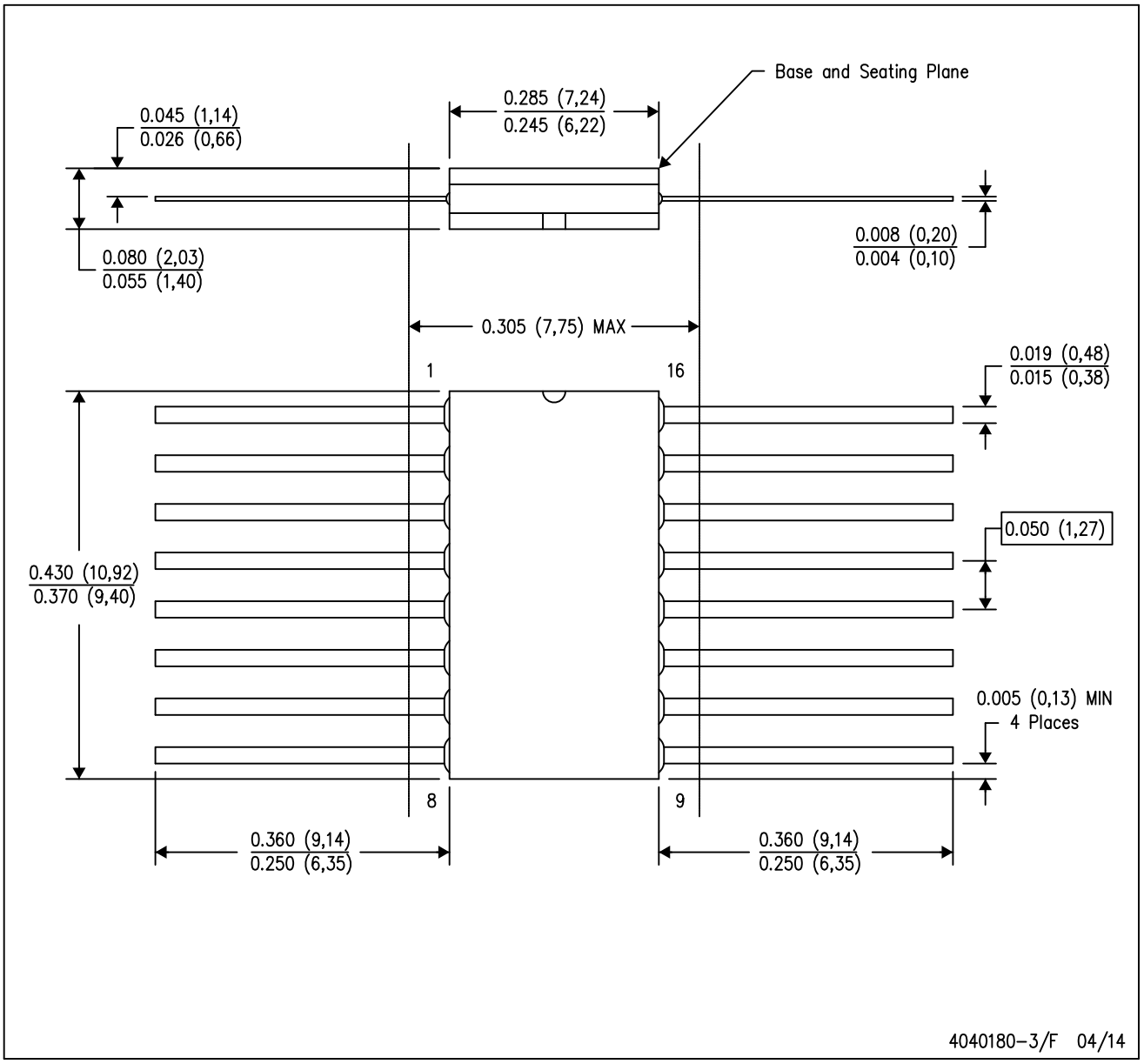



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

# GENERIC PACKAGE VIEW

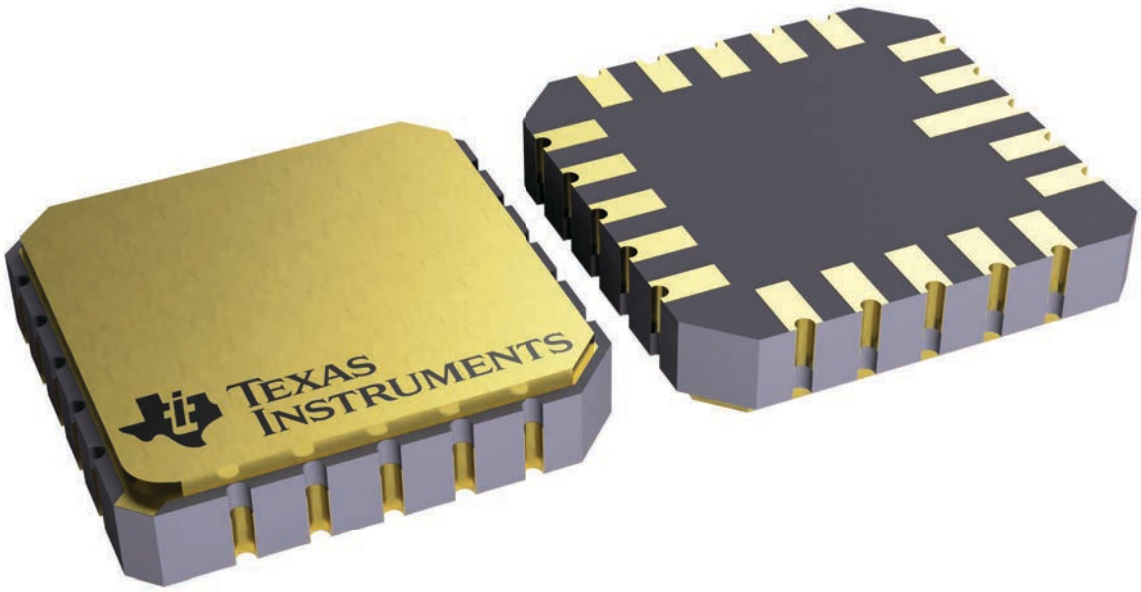
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

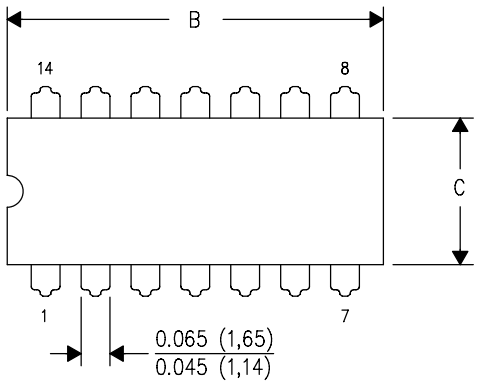



4229370VA\

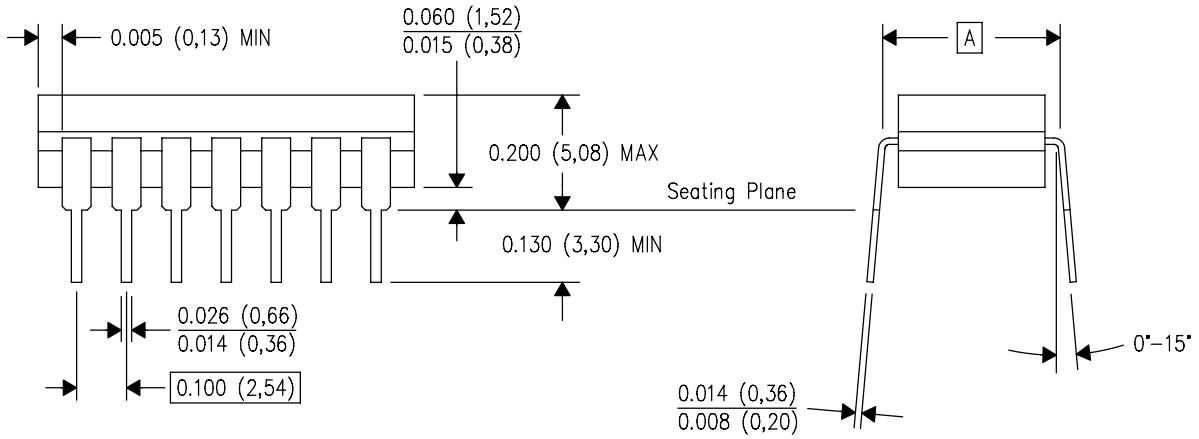
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



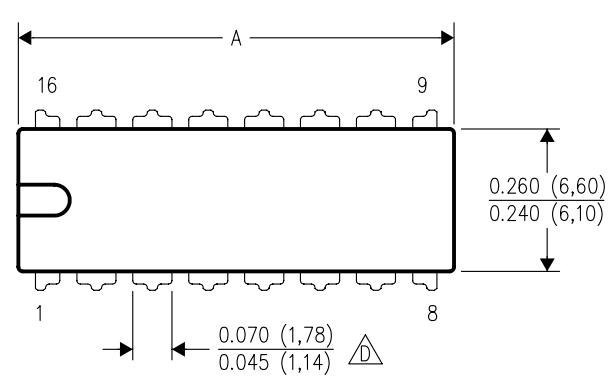

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

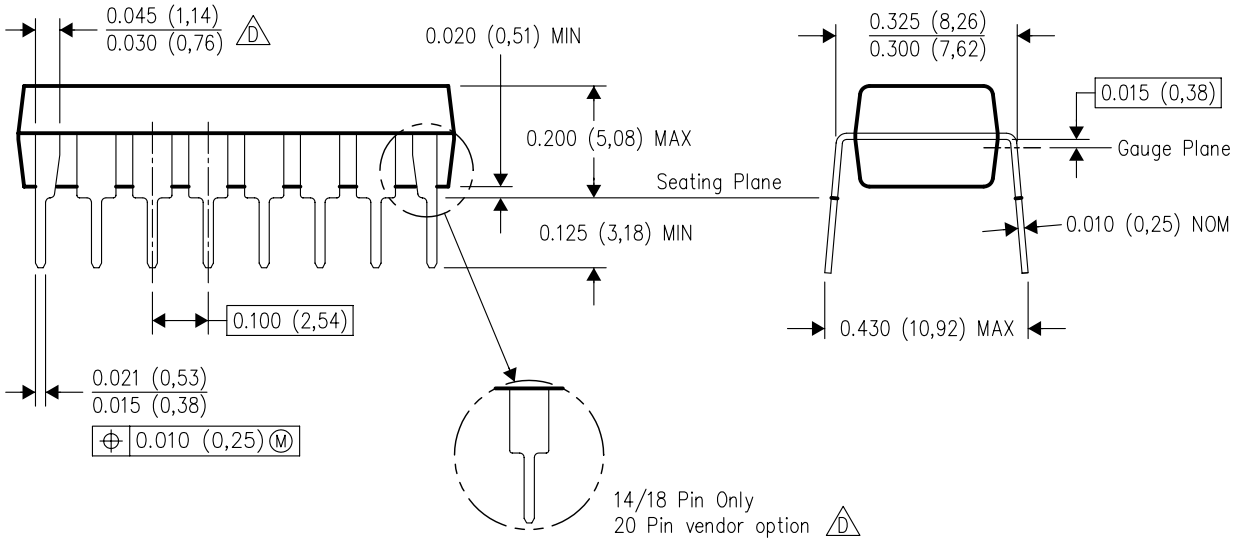
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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