- Operate With 3-V to 5.5-V V_{CC} Supply
- Operate Up To 1 Mbit/s
- Low Standby Current . . . 1 μA Typ
- External Capacitors . . . $4 \times 0.1\ \mu$F
- Accept 5-V Logic Input With 3.3-V Supply
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)
- Applications
  - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

DB, DW, OR PW PACKAGE
(TOP VIEW)

$\overline{\text{EN}}$	1	20	$\overline{\text{FORCEOFF}}$
C1+	2	19	V_{CC}
V+	3	18	GND
C1−	4	17	DOUT1
C2+	5	16	RIN1
C2−	6	15	ROUT1
V−	7	14	FORCEON
DOUT2	8	13	DIN1
RIN2	9	12	DIN2
ROUT2	10	11	$\overline{\text{INVALID}}$
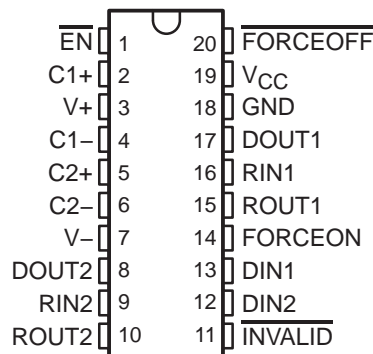
description/ordering information

The SN65C3223 and SN75C3223 consist of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/μs to 150 V/μs

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low and $\overline{\text{EN}}$ is high, both drivers and receivers are shut off, and the supply current is reduced to 1 μA. Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 μs. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between –0.3 V and 0.3 V for more than 30 μs. Refer to Figure 4 for receiver input levels.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 25	SN75C3223DW	75C3223
		Reel of 2000	SN75C3223DWR	
	SSOP – DB	Reel of 2000	SN75C3223DBR	CA3223
	TSSOP – PW	Tube of 70	SN75C3223PW	CA3223
		Reel of 2000	SN75C3223PWR	
−40°C to 85°C	SOIC – DW	Tube of 25	SN65C3223DW	65C3223
		Reel of 2000	SN65C3223DWR	
	SSOP – DB	Reel of 2000	SN65C3223DBR	CB3223
	TSSOP – PW	Tube of 70	SN65C3223PW	CB3223
		Reel of 2000	SN65C3223PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

Function Tables

EACH DRIVER

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	Normal operation with auto-powerdown disabled
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	Normal operation with auto-powerdown enabled
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	Powered off by auto-powerdown feature

H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

INPUTS			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), Open = input
disconnected or connected driver off

logic diagram (positive logic)
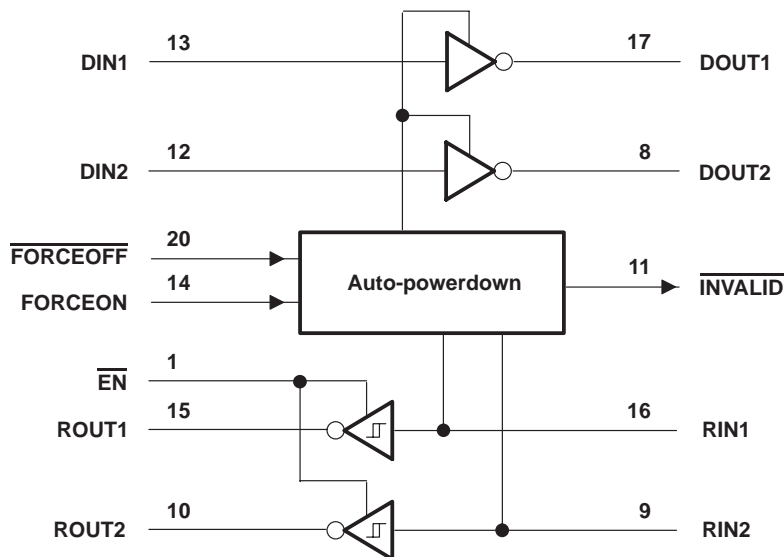
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, V+ (see Note 1)	–0.3 V to 7 V
Negative output supply voltage range, V– (see Note 1)	0.3 V to –7 V
Supply voltage difference, V+ – V– (see Note 1)	13 V
Input voltage range, V_I: Driver, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$	–0.3 V to 6 V
Receiver	–25 V to 25 V
Output voltage range, V_O: Driver	–13.2 V to 13.2 V
Receiver, $\overline{INVALID}$	–0.3 V to V_{CC} + 0.3 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package	70°C/W
DW package	58°C/W
PW package	83°C/W
Operating virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 6)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{EN}$, $\overline{FORCEOFF}$, FORCEON	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{EN}$, $\overline{FORCEOFF}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{EN}$, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
	Receiver input voltage			–25		25	
T_A	Operating free-air temperature		SN65C3223	–40		85	°C
			SN65C3223	0		70	

NOTE 4: Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

	PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_I	Input leakage current	$\overline{EN}$, $\overline{FORCEOFF}$, FORCEON			±0.01	±1	µA
I_{CC}	Supply current	Auto-powerdown disabled	No load, $\overline{FORCEOFF}$, FORCEON at V_{CC}		0.3	1	mA
		Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10	µA
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

‡ All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
NOTE 4: Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND		5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND		–5	–5.4		V
I_{IH}	High-level input current	$V_I = V_{CC}$			±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	µA
I_{OS}	Short-circuit output current‡	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V		±35	±90	
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	$V_O = \pm2$ V	300	10M		Ω
I_{off}	Output leakage current	$\overline{\text{FORCEOFF}}$ = GND	$V_O = \pm12$ V, V_{CC} = 3 V to 3.6 V			±25	µA
			$V_O = \pm10$ V, V_{CC} = 4.5 V to 5.5 V			±25	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
NOTE 4:   Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Maximum data rate (see Figure 1)	R_L = 3 kΩ, One DOUT switching	C_L = 1000 pF	250			kbit/s
			C_L = 250 pF, V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF, V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew§	C_L = 150 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ, See Figure 2			300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 1000 pF	18		150	V/µs

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
§ Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.
NOTE 4:   Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V
V_{OL}	Low-level output voltage	$I_{OL} = 1.6$ mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	$V_{CC} = 3.3$ V		1.6	2.4	V
		$V_{CC} = 5$ V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	$V_{CC} = 3.3$ V	0.6	1.1		V
		$V_{CC} = 5$ V	0.8	1.4		
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.5		V
I_{off}	Output leakage current	$\overline{EN} = V_{CC}$		±0.05	±10	µA
r_i	Input resistance	$V_I = \pm3$ V to ±25 V	3	5	7	kΩ

† All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25°C$.
NOTE 4: Test conditions are C1–C4 = 0.1 µF at $V_{CC} = 3.3$ V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at $V_{CC} = 5$ V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 150$ pF,	See Figure 3		150		ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 150$ pF,	See Figure 3		150		ns
t_{en}	Output enable time	$C_L = 150$ pF, See Figure 4	$R_L = 3$ kΩ,		200		ns
t_{dis}	Output disable time	$C_L = 150$ pF, See Figure 4	$R_L = 3$ kΩ,		200		ns
$t_{sk(p)}$	Pulse skew‡	See Figure 3			50		ns

† All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25°C$.
‡ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1–C4 = 0.1 µF at $V_{CC} = 3.3$ V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at $V_{CC} = 5$ V ± 0.5 V.

TEXAS INSTRUMENTS

AUTO-POWERDOWN SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND,	FORCEOFF = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND,	FORCEOFF = V_{CC}	−2.7		V
$V_{T(invalid)}$	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND,	FORCEOFF = V_{CC}	−0.3	0.3	V
V_{OH}	INVALID high-level output voltage	I_{OH} = −1 mA, FORCEOFF = V_{CC}	FORCEON = GND,	V_{CC} − 0.6		V
V_{OL}	INVALID low-level output voltage	I_{OL} = 1.6 mA, FORCEOFF = V_{CC}	FORCEON = GND,		0.4	V

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TYP†	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	µs
t_{en}	Supply enable time	100	µs

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION
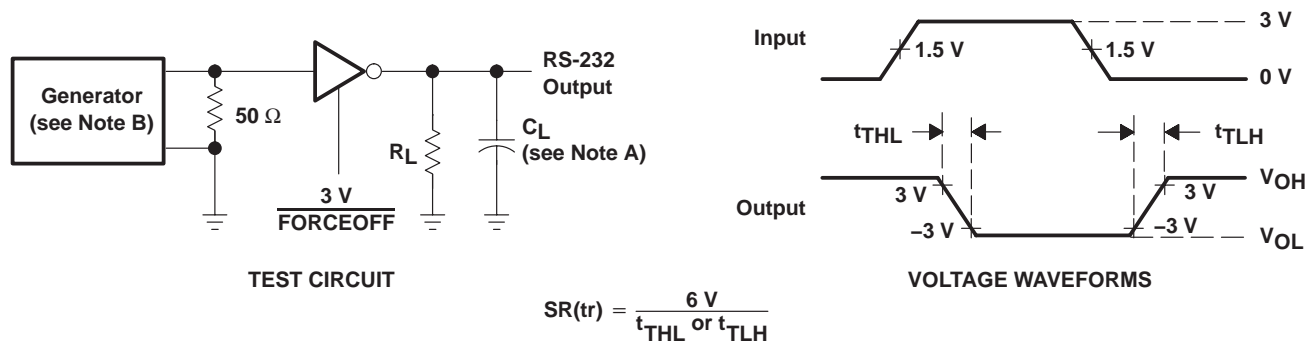
$$SR(tr) = \frac{6\ V}{t_{THL}\ \text{or}\ t_{TLH}}$$
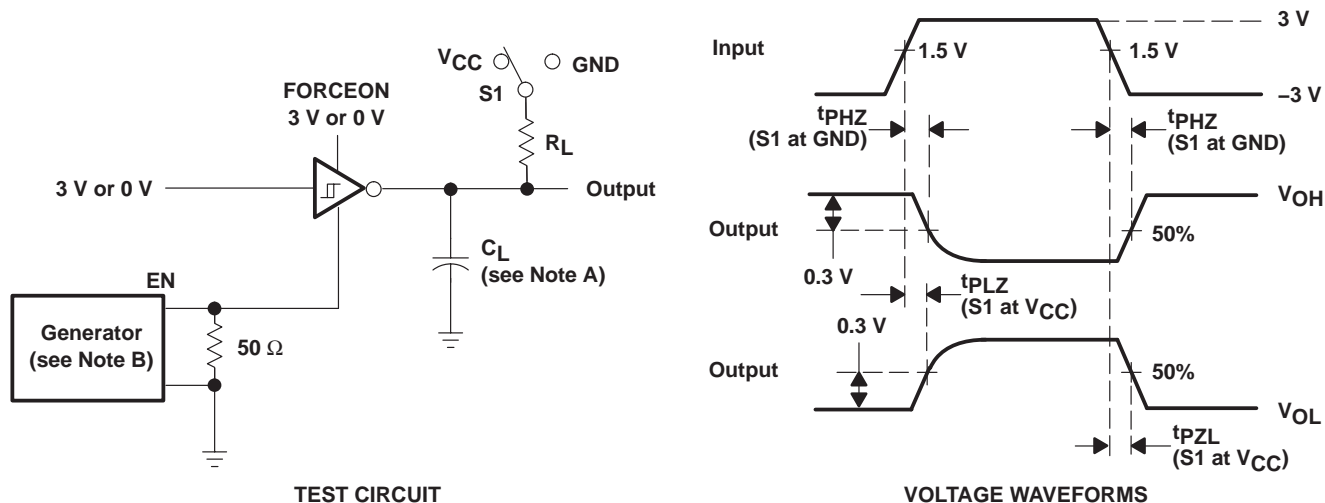
TEST CIRCUIT

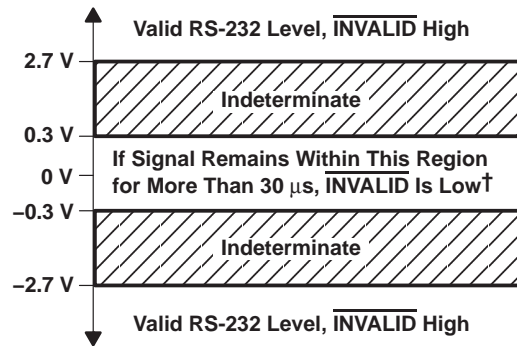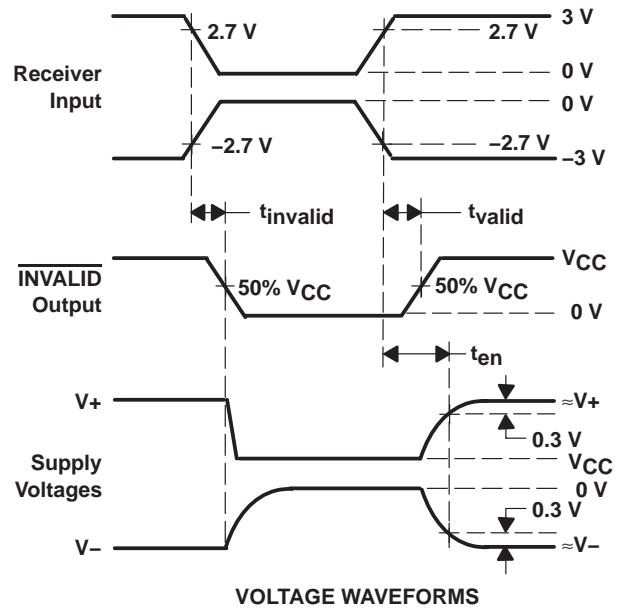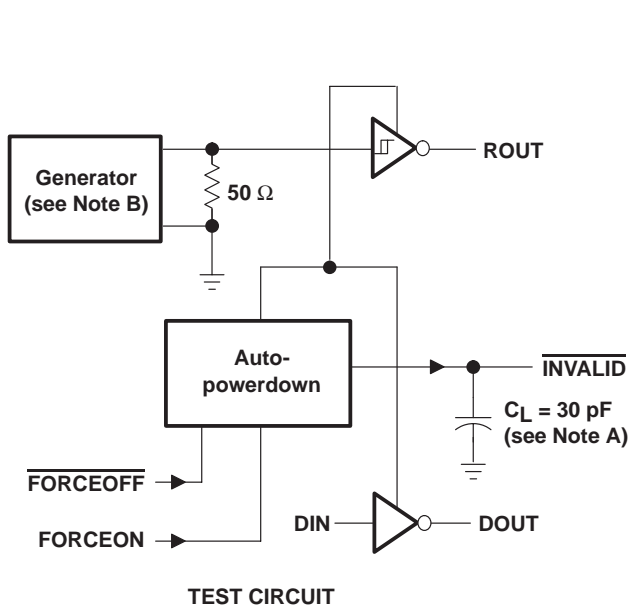**VOLTAGE WAVEFORMS**

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 1. Driver Slew Rate

TEXAS INSTRUMENTS

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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS
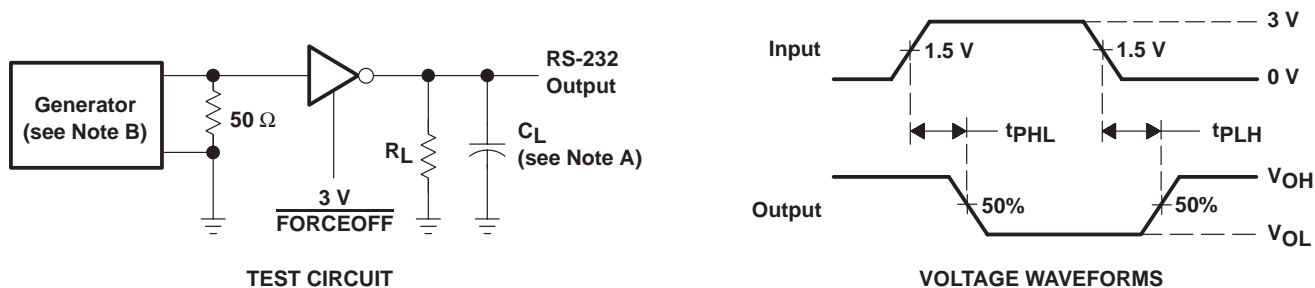
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew
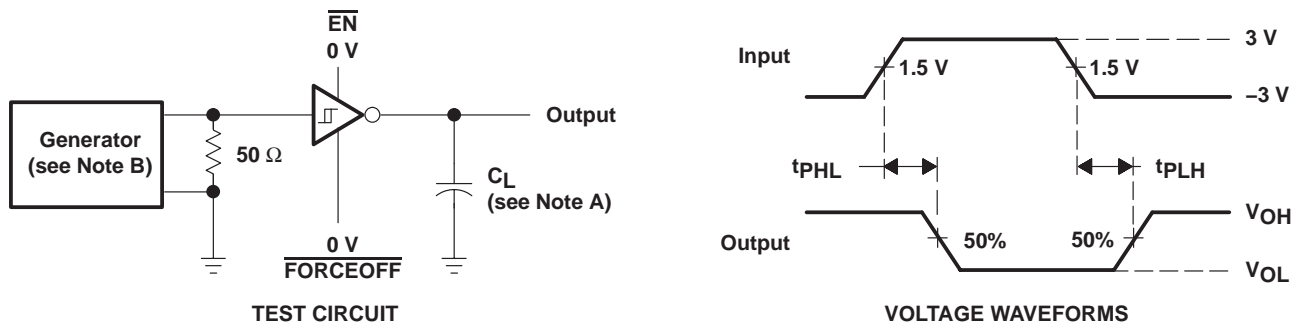
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Receiver Propagation Delay Times

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 4. Receiver Enable and Disable Times

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

Valid RS-232 Level, $\overline{\text{INVALID}}$ High

Indeterminate

If Signal Remains Within This Region
for More Than 30 μs, $\overline{\text{INVALID}}$ Is Low[†]

Indeterminate

Valid RS-232 Level, $\overline{\text{INVALID}}$ High

[†] Auto-powerdown disables drivers and reduces supply current to 1 μA.

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

APPLICATION INFORMATION
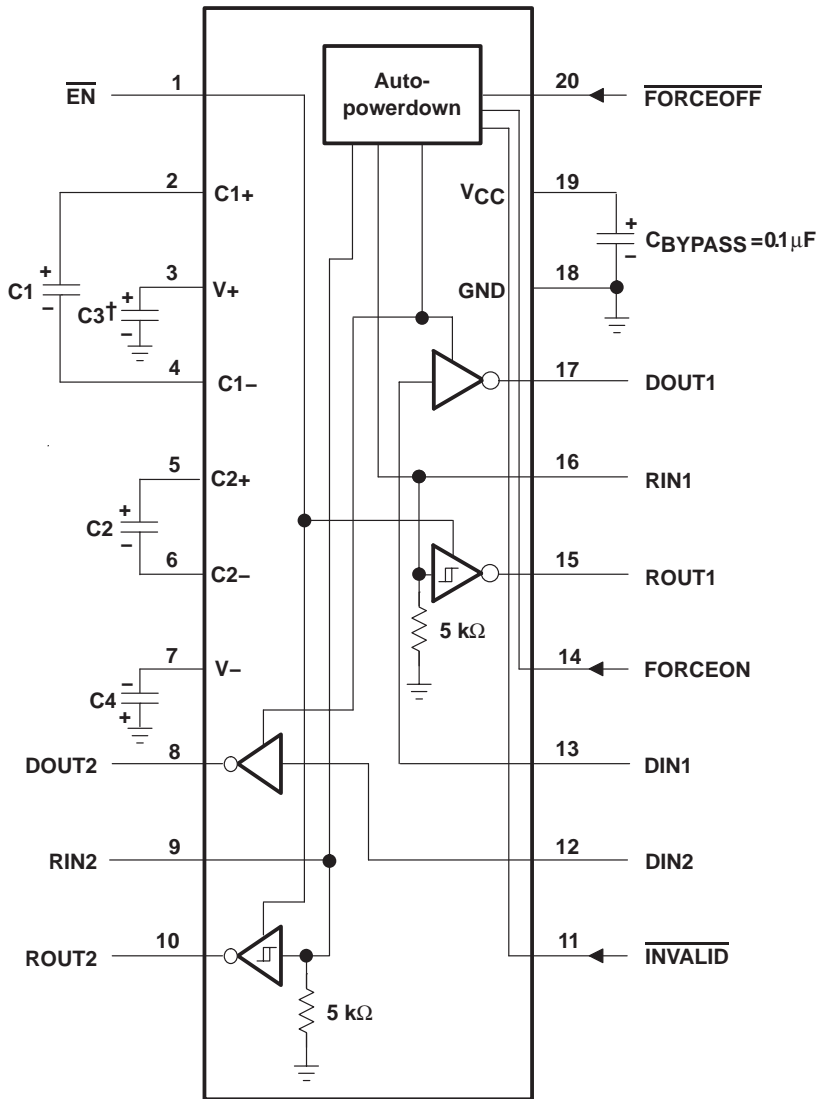
† C3 can be connected to V_{CC} or GND.
NOTE A: Resistor values shown are nominal.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, C4
3.3 V $\pm$ 0.3 V	0.1 μF	0.1 μF
5 V $\pm$ 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C3223DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3223	Samples
SN65C3223DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3223	Samples
SN65C3223PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	CB3223	
SN75C3223DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3223	Samples
SN75C3223DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3223	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
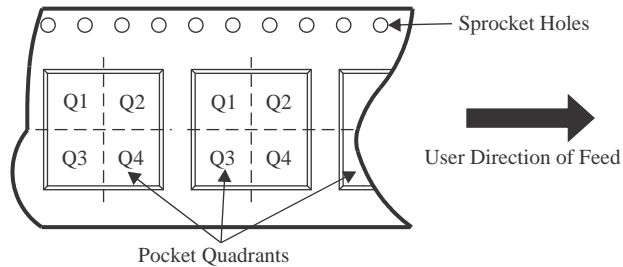
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3223DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75C3223DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75C3223DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3223DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN75C3223DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN75C3223DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE
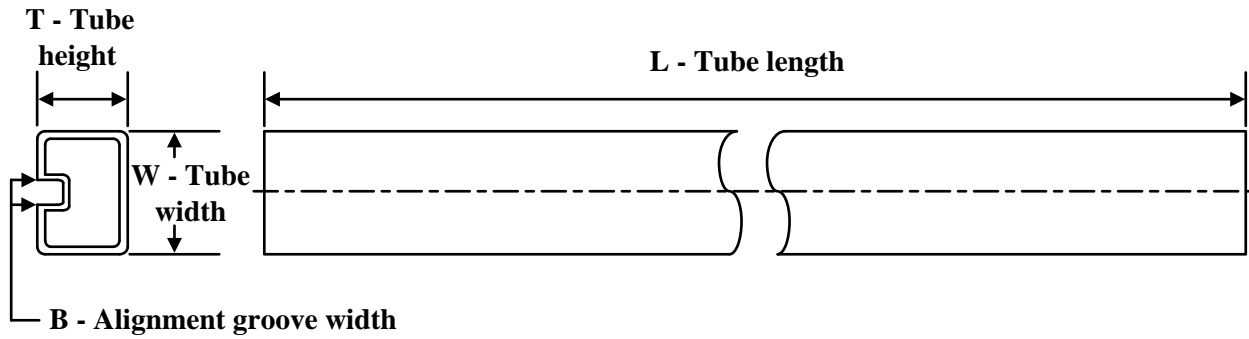
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65C3223DW	DW	SOIC	20	25	507	12.83	5080	6.6

6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

6.6
6.4
NOTE 3

2X
5.85

10

11

B

4.5
4.3
NOTE 4

20X 0.30
0.19

⊕ 0.1 Ⓜ C A B

C

SEATING PLANE

◯ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50

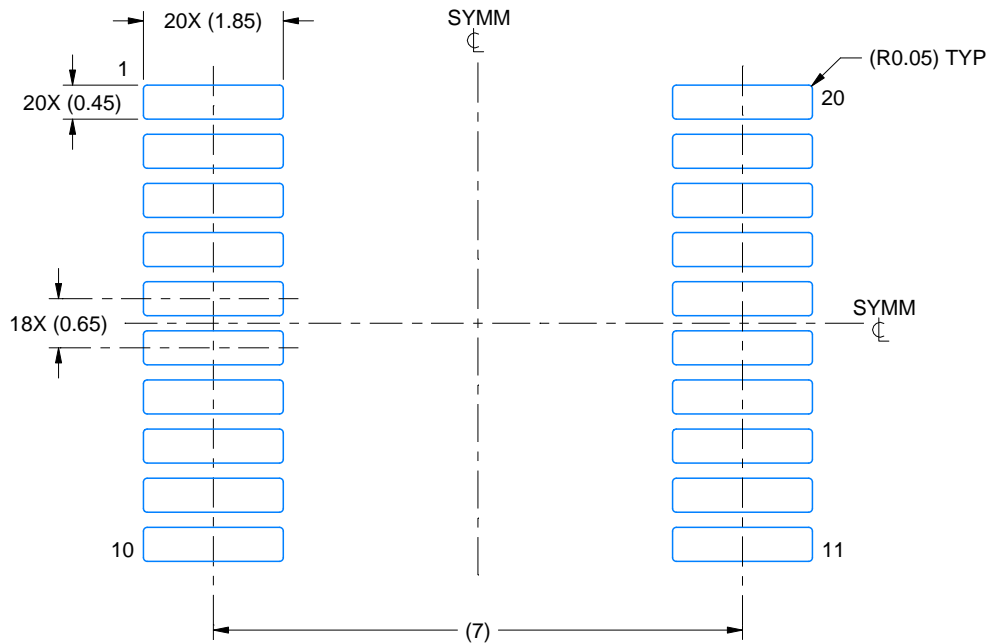DETAIL A
TYPICAL

4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

20X (1.5)

SYMM

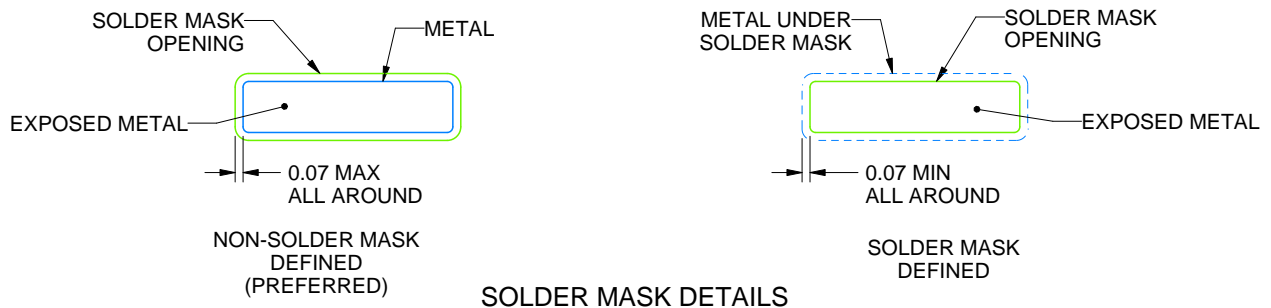(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS
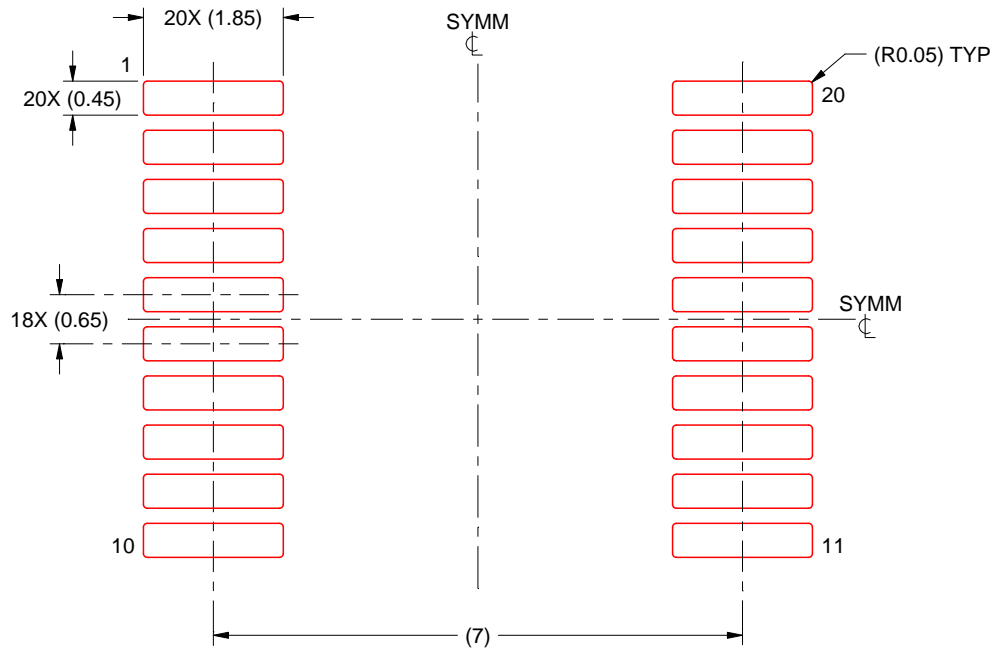
SOLDER MASK
DEFINED

4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

(R0.05) TYP

1

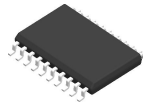20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
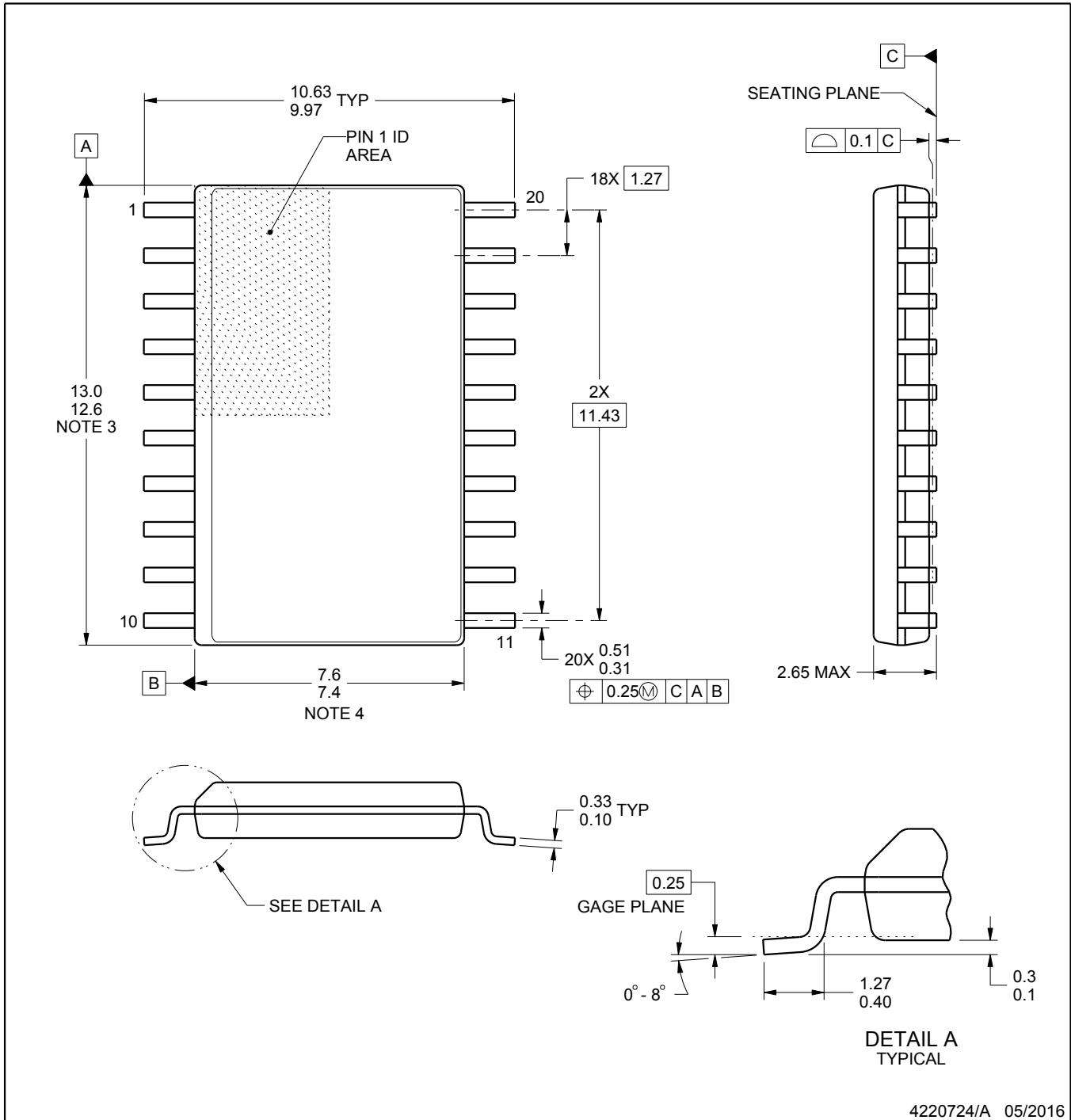
8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

7.5 / 6.9 NOTE 3

2X 5.85

10

11

20X 0.38 / 0.22

⊕ 0.1 Ⓜ C A B

B

5.6 / 5.0 NOTE 4

C

◁ 0.1 C

SEATING PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95 / 0.55

2 MAX

0.05 MIN

DETAIL A
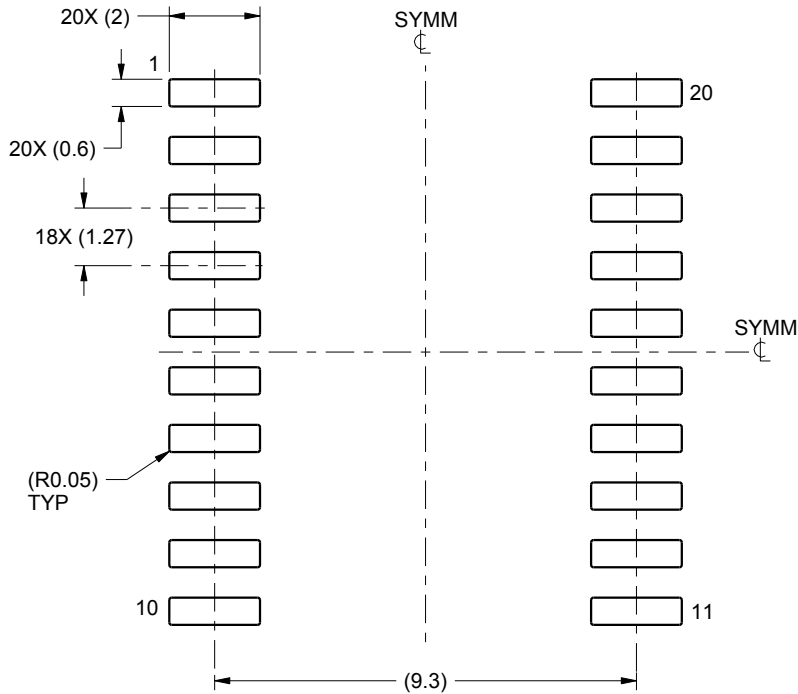TYPICAL
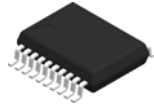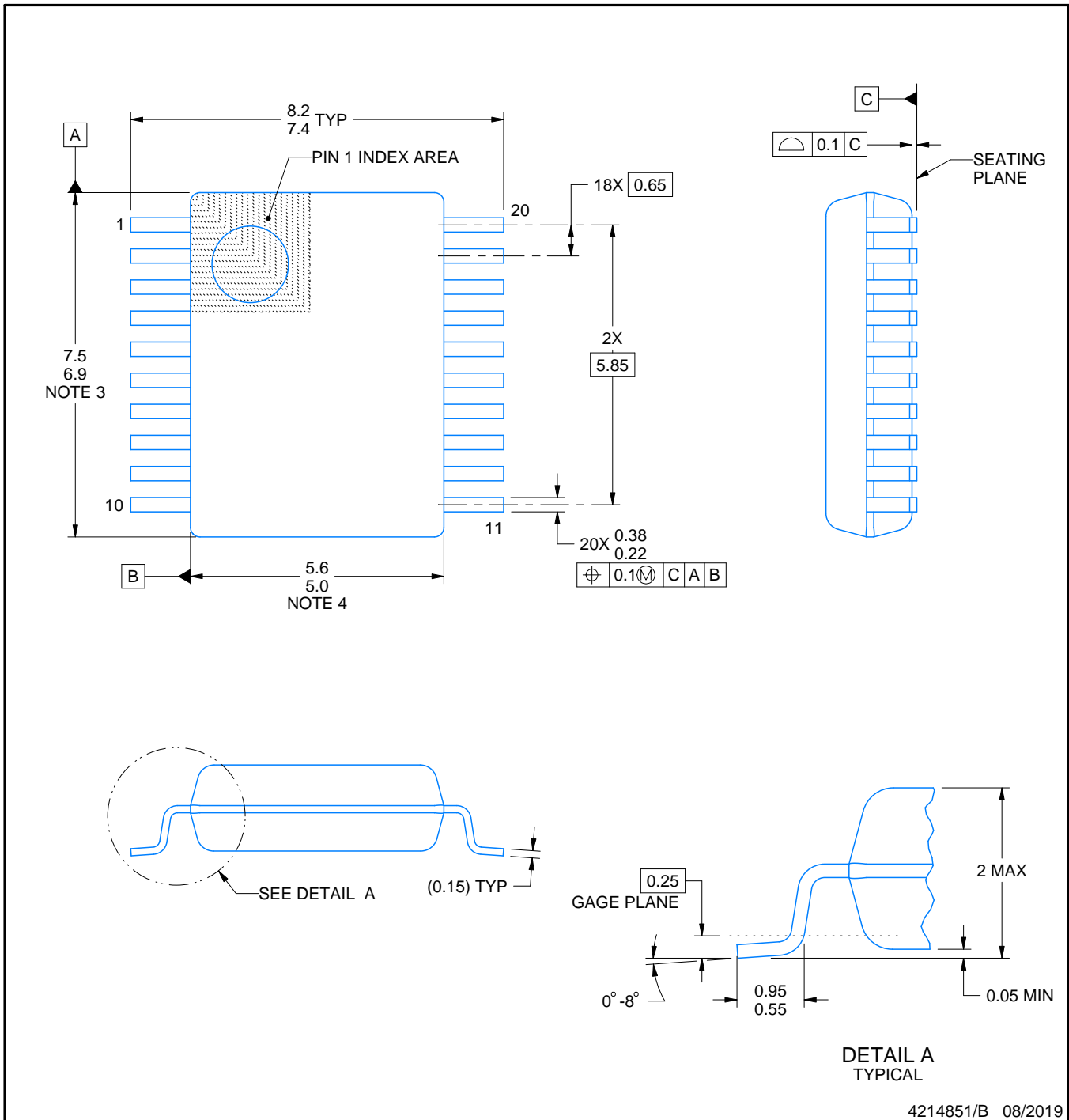
4214851/B   08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

20X (1.85)

1

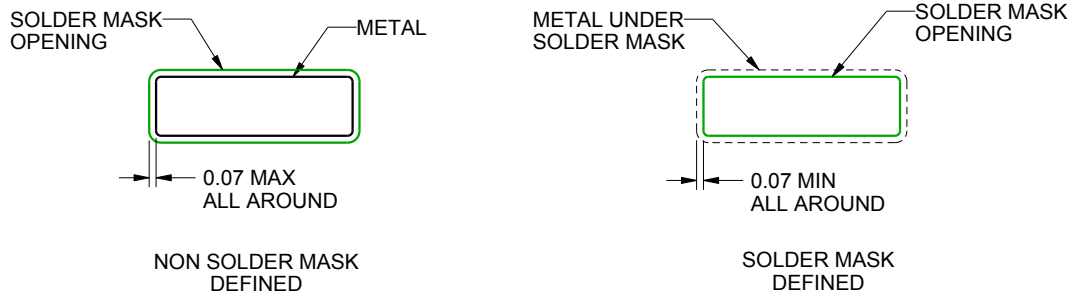20X (0.45)

18X (0.65)

SYMM

(R0.05) TYP

20

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.85)

SYMM

(R0.05) TYP

1

20

20X (0.45)

SYMM

18X (0.65)

10

11

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

20   18X 1.27

13.0 / 12.6 NOTE 3

10

11

2X 11.43

20X 0.51 / 0.31

B   7.6 / 7.4 NOTE 4

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.65 MAX

0.33 / 0.10 TYP

SEE DETAIL A

0.25 GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM
₵

1

20X (0.6)

20

18X (1.27)

SYMM
₵

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10   11

(9.3)
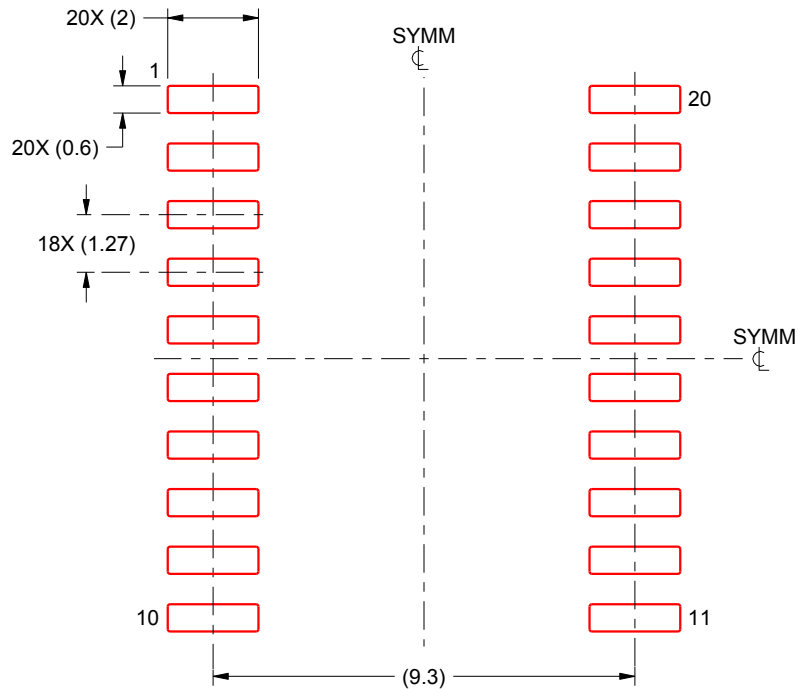
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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