Two Channel SATA 3-Gbps Redriver

FEATURES

- **Data Rates up to 3 Gbps**
- **SATA Gen 2.6, eSATA Compliant**
- **SATA Hot-Plug Capable**
- **Supports Common-Mode Biasing for OOB Signaling with Fast Turn-On**
- **Channel Selectable Pre-Emphasis**
- **Fixed Receiver Equalization**
- **Integrated Termination**
- **Low Power**
  - **<200 mW Typ**
  - **<5 mW in Sleep Mode**
  - **15% Typ Lower Power in Auto Low Power Mode**
- **Excellent Jitter and Loss Compensation Capability to Over 20 Inch FR4 Trace**
- **High Protection Against ESD Transient**
  - **HBM: 8000V**
  - **CDM: 1500V**
  - **MM: 200V**
- **20-Pin SSOP Package**
- **Pin Compatible with PI2EQX3211A and PI2EQX3211B**

APPLICATIONS

- **Notebooks, Desktops, Docking Stations, Servers, and Workstations**

DESCRIPTION

The SN75LVCP422 is a dual channel, single lane SATA redriver and signal conditioner supporting data rates up to 3 Gbps. The device complies with SATA specification revision 2.6 and eSATA requirements.

The SN75LVCP422 operates from a single 3.3-V supply. Integrated 100-Ω line termination and self-biasing make the device suitable for AC coupling. The inputs incorporate an OOB detector, which automatically turns the differential outputs off while maintaining a stable output common-mode voltage compliant to SATA link. The device is also designed to handle SSC transmission per SATA spec.

The SN75LVCP422 handles interconnect losses at both its input and output. The built-in transmitter pre-emphasis feature is capable of applying 0 dB or 2.5 dB of relative amplification at higher frequencies to counter the expected interconnect loss. On the receive side the device applies a fixed equalization of 7 dB to boost input frequencies near 1.5 GHz. Collectively, the input equalization and output pre-emphasis features of the device work to fully restore SATA signal integrity over extended cable and backplane pathways.

The device is hot-plug capable(1) preventing device damage under device *hot*-insertion such as async signal plug/removal, unpowered plug/removal, powered plug/removal, or surprise plug/removal.

(1) *Requires use of AC coupling capacitors at differential inputs and outputs.*

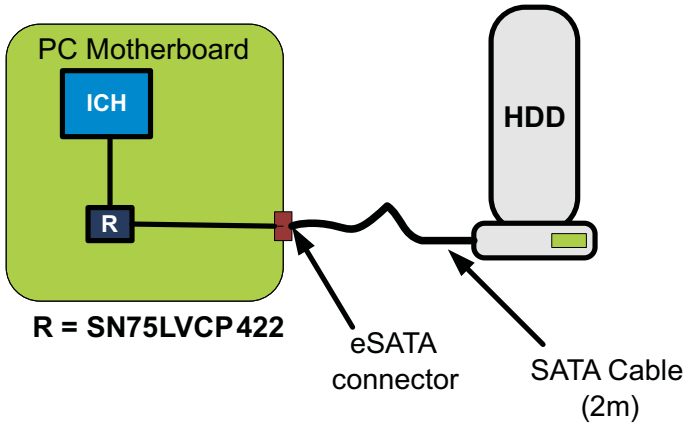
ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75LVCP422DB	LVCP422	20-Pin SSOP Tube
SN75LVCP422DBR	LVCP422	20-Pin SSOP Reel (large)

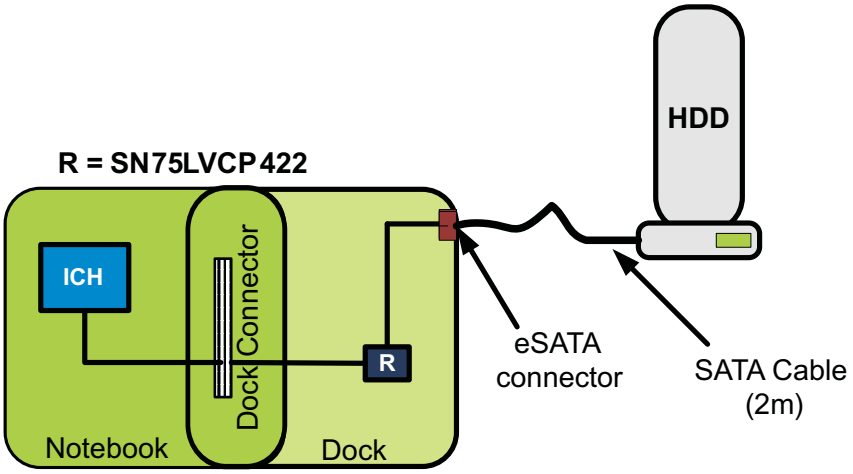
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION



In Notebook and Desktop Motherboard



In Notebook Dock

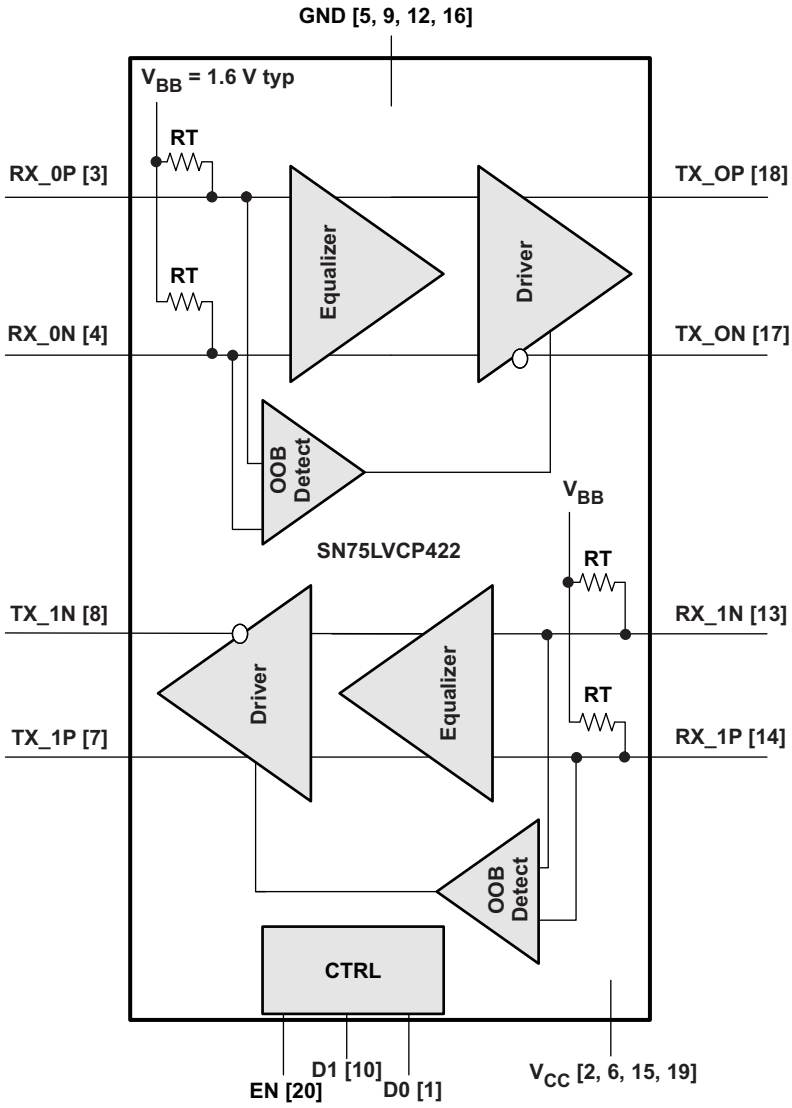


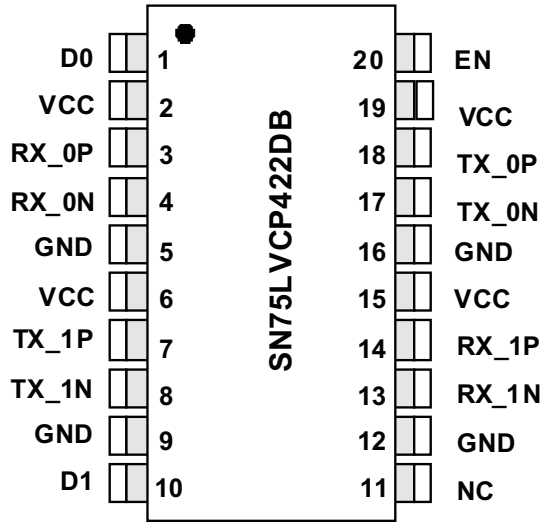
Figure 1. Data Flow Block Diagram

Table 1. Control Logic

EN	D0	D1	FUNCTION
0	X	X	Low power mode
1	**0**	**0**	**Normal SATA output (default state); CH 0 and CH 1 → 0 dB**
1	1	0	CH 0 → 2.5 dB pre-emphasis; CH 1 → 0 dB
1	0	1	CH 1→ 2.5 dB pre-emphasis; CH 0 → 0 dB
1	1	1	CH 0 and CH 1 → 2.5 dB pre-emphasis

PIN ASSIGNMENT

DB PACKAGE
TOP VIEW

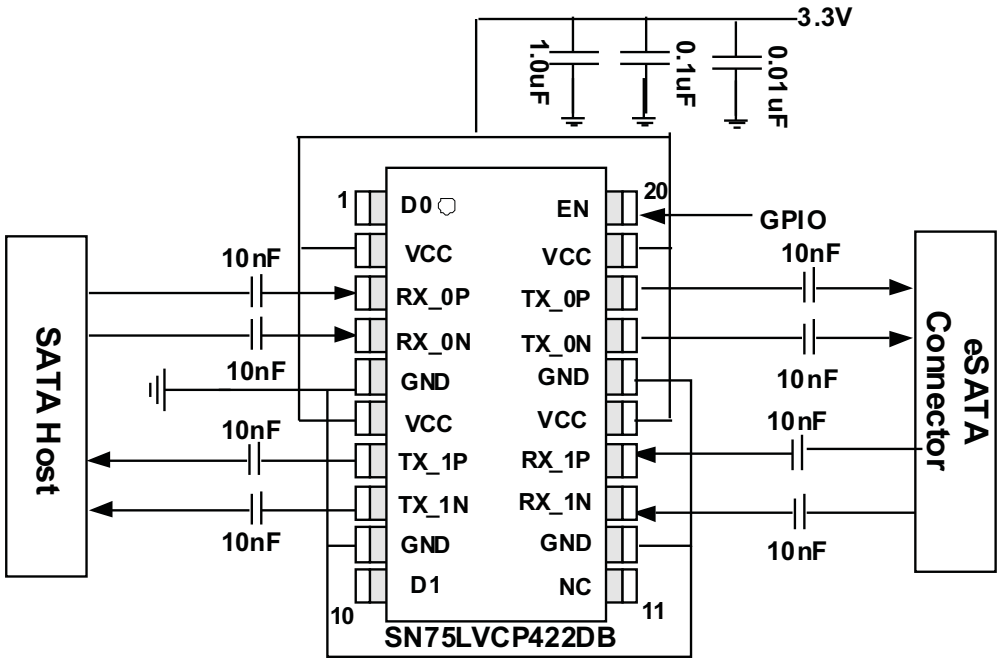


TERMINAL FUNCTIONS

PIN	NAME	DESCRIPTION		PIN	NAME	DESCRIPTION
1	D0(1)	Pre-emphasis _0		11	NC	No connect
2	VCC	Power		12	GND	Ground
3	RX_0P	Input 0, non-inverting		13	RX_1N	Input 1, non-inverting
4	RX_0N	Input 0, inverting		14	RX_1P	Input 1, inverting
5	GND	Ground		15	VCC	Power
6	VCC	Power		16	GND	Ground
7	TX_1P	Output 1, inverting		17	TX_0N	Output 0, inverting
8	TX_1N	Output 1, non-inverting		18	TX_0P	Output 0, non-inverting
9	GND	Ground		19	VCC	Power
10	D1(1)	Pre-emphasis_1		20	EN(2)	Enable

(1) D0 and D1 are tied to VCC via an internal PU resistor.
(2) EN tied to VCC via an internal PU resistor.

TYPICAL DEVICE IMPLEMENTATION



Note:
1) Place supply caps close to device pin
2) EN can be left open or tied to supply when no external control is implemented
3) Output pre-emphasis (D1, D0) is shown enabled. Setting will depend on device placement relative to eSATA connector

DETAILED DESCRIPTION

INPUT EQUALIZATION

Each differential input of the SN75LVCP422 has 7 dB of fixed equalization in its front stage. The equalization amplifies high frequency signals to correct for loss from the transmission channel. The input equalizer is designed to recover signal even when no eye is present at the receiver and affectively supports FR4 trace at the input anywhere from <4 inches to 20 inches or <10 cm to >50 cm.

OUTPUT PRE-EMPHASIS

The SN75LVCP422 provides single step pre-emphasis from 0 dB to 2.5 dB at each of its differential outputs. Pre-emphasis is controlled independently for each channel and is set by the control pins D0 and D1 as shown in Table 1. The pre-emphasis duration is 0.5 UI or 133 ps (typ) at SATA 3-Gbps speed.

LOW POWER MODE

Two low power modes are supported by the SN75LVCP422:

- Sleep Mode (triggered by EN pin, EN = 0 V)
  - Low power mode is controlled by the enable (EN) pin. In its default state this pin is internally pulled high. Pulling this pin low puts the device in sleep mode within 2 us (max). In this mode all active components of the device are driven to their quiescent level and differential outputs are driven to Hi-Z (open). Maximum power dissipation in this mode is 5 mW. Exiting from this mode to normal operation requires a maximum latency of 20 µs.
- Auto Low Power Mode (triggered when a given channel is in electrical idle state, EN = V_{CC})

– The device enters and exits low power mode by actively monitoring the input signal (V_{IDp-p}) level on each of its channels independently. When the input signal on either or both channels is in the electrical idle state, i.e. V_{IDp-p} <50 mV, and stays in this state for > 3 μs, the associated channel(s) enters the low power state. In this state, the output of the associated channel(s) is driven to V_{CM}, and the device selectively shuts off some circuitry to lower power by up to 20% of its normal operating power. Exit time from auto low power mode is less than 50 ns.
– As an example, if under normal operating conditions the device is consuming typical power of 200 mW, when the device enters this mode, i.e. the condition for auto-low power mode is met, power consumption can drop down to 160 mW. The device enters normal operation within 50 ns of signal activity detection.

OUT-OF-BAND (OOB) SUPPORT

The squelch detector circuit within the device enables full detection of OOB signaling as specified in SATA specification 2.6. Differential signal amplitude at the receiver input of 50 mV_{p-p} or less is not detected as an activity and hence is not passed to the output. Differential signal amplitude of 150 mV_{p-p} or more is detected as an activity and therefore passed to the output indicating activity. Squelch circuit on/off time is 5 ns maximum. While in squelch mode outputs are held to V_{CM}.

DEVICE POWER

The SN75LVCL412 is designed to operate from a single 3.3-V supply. Always practice proper power supply sequencing procedures. Apply V_{CC} first before any input signals are applied to the device. The power down sequence is in reverse order.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range(2)	V_{CC}	–0.5 to 6	V
Voltage range	Differential I/O	–0.5 to 4	V
	Control I/O	–0.5 to V_{CC} + 0.5	V
Electrostatic discharge	Human body model(3)	±8000	V
	Charged-device model(4)	±1500	V
	Machine model(5)	±200	V
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
20-pin SSOP (DB)	Low-K	952 mW	9.52 mW/°C	381 mW
	High-K	1149 mW	11.49 mW/°C	460 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			58		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			65		°C/W
P_D	Device power dissipation	D0, D1, EN = 3.3 V, K28.5 pattern at 3 Gbps, V_{ID} = 700 mV_{p-p}, V_{CC} = 3.6 V			300	mW
P_{SD}	Device power dissipation, under low power	EN = 0 V, K28.5 pattern at 3 Gbps, V_{ID} = 700 mV_{p-p}, V_{CC} = 3.6 V			5	mW

(1) The maximum rating is simulated under 3.6-V V_{CC}.

RECOMMENDED OPERATING CONDITIONS

with typical values measured at V_{CC} = 3.3 V, T_A = 25°C; all temperature limits are assured by design

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	Coupling capacitor			12		nF
T_A	Operating free-air temperature		0		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I_{CC}	Supply current, active mode	EN, D0, D1 in default state, K28.5 pattern at 3 Gbps, V_{ID} = 700 mV_{p-p}, V_{CC} = 3.3 V		55	77	mA
I_{CCSDWN}	Shutdown current	EN = 0 V			1	mA
I_{CC-LP}	Supply current in auto low power mode	Low power mode activated		50		mA
	Maximum data rate				3.0	Gbps
t_{PDelay}	Propagation delay	Measured using K28.5 pattern, See Figure 4		300	500	ps
t_{ENB}	Device enable time	ENB = L → H			20	µs
t_{DIS}	Device disable time	ENB = H → L			2	µs
$AutoLP_{ENTRY}$	Auto low power entry time	Electrical idle at input, see Figure 7		6		µs
$AutoLP_{EXIT}$	Auto low power exit time	After first signal activity, see Figure 7		45		ns
V_{OOB}	Input OOB threshold	See Figure 5	50	100	150	mV_{p-p}
t_{OOB1}	OOB mode enter	See Figure 5			5	ns
t_{OOB2}	OOB mode exit	See Figure 5			5	ns
CONTROL LOGIC						
V_{IH}	High-level input voltage		1.4			V
V_{IL}	Low-level input voltage				0.5	V
V_{INHYS}	Input hysteresis			100		mV
I_{IH}	High-level input current				10	µA
I_{IL}	Low-level input current				10	µA
RECEIVER AC/DC						
Z_{DiffRX}	Differential input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.6		V

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

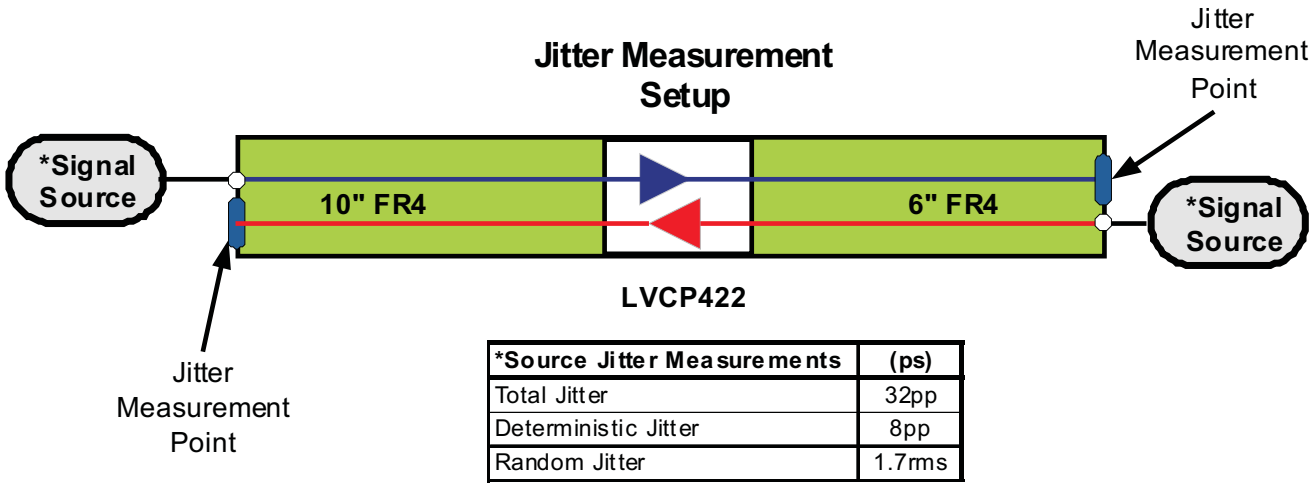
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
RL_{DiffRX}	Differential mode return loss	f = 150 MHz – 300 MHz	18			dB
		f = 300 MHz – 600 MHz	14			
		f = 600 MHz – 1.2 GHz	10			
		f = 1.2 GHz – 2.4 GHz	8			
		f = 2.4 GHz – 3.0 GHz	3			
RL_{CMRX}	Common-mode return loss	f = 150 MHz – 300 MHz	5			dB
		f = 300 MHz – 600 MHz	5			
		f = 600 MHz – 1.2 GHz	2			
		f = 1.2 GHz – 2.4 GHz	1			
		f = 2.4 GHz – 3.0 GHz	1			
V_{DiffRX}	Differential input voltage PP	f = 150 MHz – 300 MHz	200		2000	mV/ppd
IB_{RX}	Impedance balance	f = 150 MHz – 300 MHz	30			dB
		f = 300 MHz – 600 MHz	30			
		f = 600 MHz – 1.2 GHz	20			
		f = 1.2 GHz – 2.4 GHz	10			
		f = 2.4 GHz – 3.0 GHz	4			
$T_{20\text{-}80RX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal	67		136	ps
T_{skewRX}	Differential skew	Difference between the single-ended mid-point of the RX+ signal rising/falling edge and the single-ended mid-point of the RX– signal falling/rising edge			50	ps
TRANSMITTER AC/DC						
Z_{DiffTX}	Pair differential Impedance		85		115	Ω
Z_{SETX}	Single-ended input impedance		40			Ω
RL_{DiffTX}	Differential mode return loss	f = 150 MHz – 300 MHz	14			dB
		f = 300 MHz – 600 MHz	8			
		f = 600 MHz – 1.2 GHz	6			
		f = 1.2 GHz – 2.4 GHz	6			
		f = 2.4 GHz – 3.0 GHz	3			
RL_{CMTX}	Common-mode return loss	f = 150 MHz – 300 MHz	5			dB
		f = 300 MHz – 600 MHz	5			
		f = 600 MHz – 1.2 GHz	2			
		f = 1.2 GHz – 2.4 GHz	1			
		f = 2.4 GHz – 3.0 GHz	1			
IB_{TX}	Impedance balance	f = 150 MHz – 300 MHz	30			dB
		f = 300 MHz – 600 MHz	20			
		f = 600 MHz – 1.2 GHz	10			
		f = 1.2 GHz – 2.4 GHz	10			
		f = 2.4 GHz – 3.0 GHz	4			
$Diff_{VppTX}$	Differential output voltage PP	f = 1.5 GHz, D0/D1 = 0, Refer to Figure 2 for test setup	400	585	700	mVpp
$Diff_{VppTX\_PE}$	Differential output voltage PP	f = 1.5 GHz, D0/D1 = 1, Refer to Figure 2 for test setup	600	790	965	mVpp
	Output pre-emphasis	At 1.5 GHz (when enabled)		2.5		dB
V_{CMTX}	Common-mode voltage			1.97		V
V_{CMTX_AC}	AC CM voltage	Maximum amount of AC CM signal at TX		20	50	mVpp
$T_{20\text{-}80TX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal, D1/D0 = 0 V	67	83	136	ps

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
T_{skewTX}	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising/falling edge and the single-ended mid-point of the TX– signal falling/rising edge		7	20	ps
JITTER (with pre-emphasis disabled; measured at device pin + 2" loadboard trace)						
TJ_{TX}	Total jitter(1)	UI = 333 ps, +K28.5 control character; D1/D0 = 0 V		30	67	ps-pp
DJ_{TX}	Deterministic jitter(1)	UI = 333 ps, +K28.5 control character; D1/D0 = 0 V		10	33	ps-pp
RJ_{TX}	Random jitter(1)	UI = 333 ps, +K28.7 control character; D1/D0 = 0 V		1.7	2.0	ps-rms
JITTER (with pre-emphasis enabled; measured as shown in Figure 2)						
TJ_{TX}	Total jitter(1)	UI = 333 ps, +K28.5 control character; D1/D0 = VCC		60	100	ps-pp
DJ_{TX}	Deterministic jitter(1)	UI = 333 ps, +K28.5 control character; D1/D0 = VCC		33	67	ps-pp
RJ_{TX}	Random jitter(1)	UI = 333 ps, +K28.7 control character; D1/D0 = VCC		1.7	2.0	ps-rms

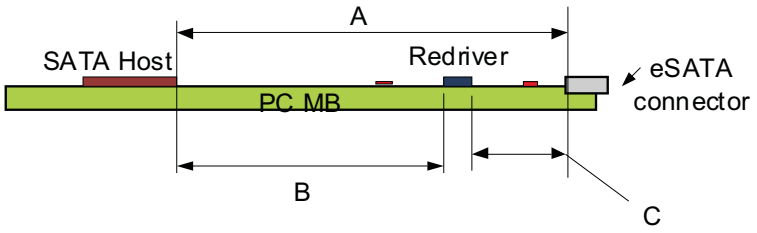
(1) $T_J = (14.1 \times RJ_{SD} + DJ)$ where RJ_{SD} is one standard deviation value of RJ Gaussian distribution. T_J measurement is at the SATA connector and includes jitter generated at the package connection on the printed circuit board and at the board interconnect.



*Source Jitter Measurements	(ps)
Total Jitter	32pp
Deterministic Jitter	8pp
Random Jitter	1.7rms

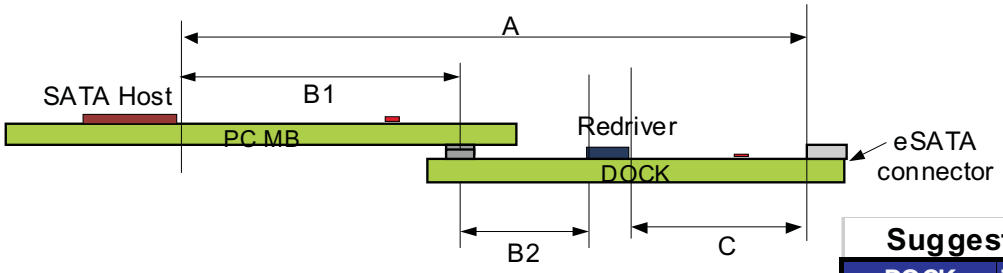
Figure 2. Output Jitter Measurement Test Setup

Suggested Trace Length Using LVCP422 in PC MB and PC Dock



Redriver on PC Motherboard

Suggested Trace Lengths		
PC MB	TYP* (inch)	MAX* (inch)
B	4 to 16	18
C	2 to 4	6
A	6 to 20	24



Redriver on Dock Board

Suggested Trace Lengths		
DOCK	TYP* (inch)	MAX* (inch)
B = (B1+B2)	8 to 14	16
C	2 to 4	6
A	10 to 18	22

Note*:
Trace lengths are suggested values based on TI lab measurements (taken with output pre-emphasis enabled on both channels) to meet SATA loss and jitter spec.

Actual trace length supported by LVCP422 may be more or less than suggested values and will depend on board layout, number of connectors used in the SATA signal path, and SATA host and esata connector design.

Figure 3.

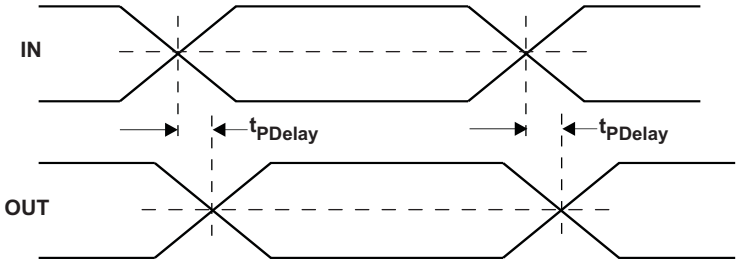


Figure 4. Propagation Delay Timing Diagram

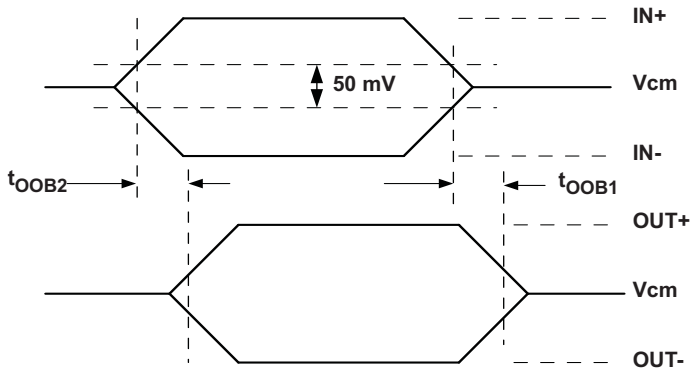


Figure 5. OOB Enter and Exit Timing

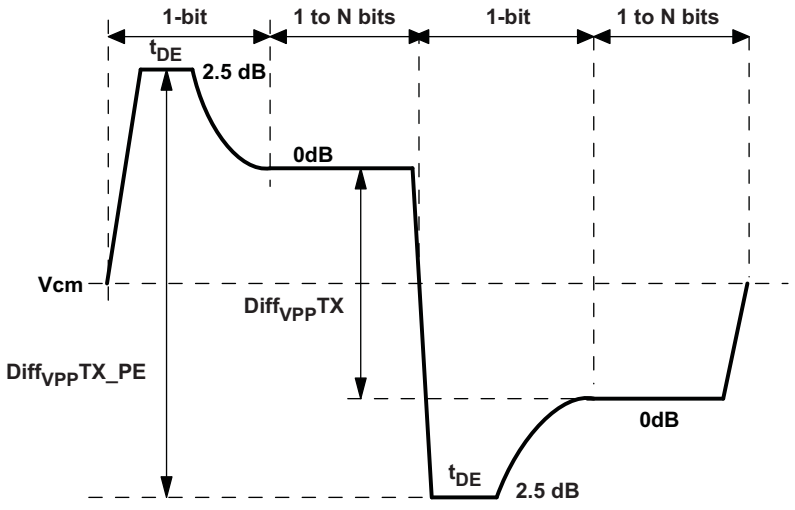


Figure 6. TX Differential Output with 2.5 dB Pre-Emphasis Step

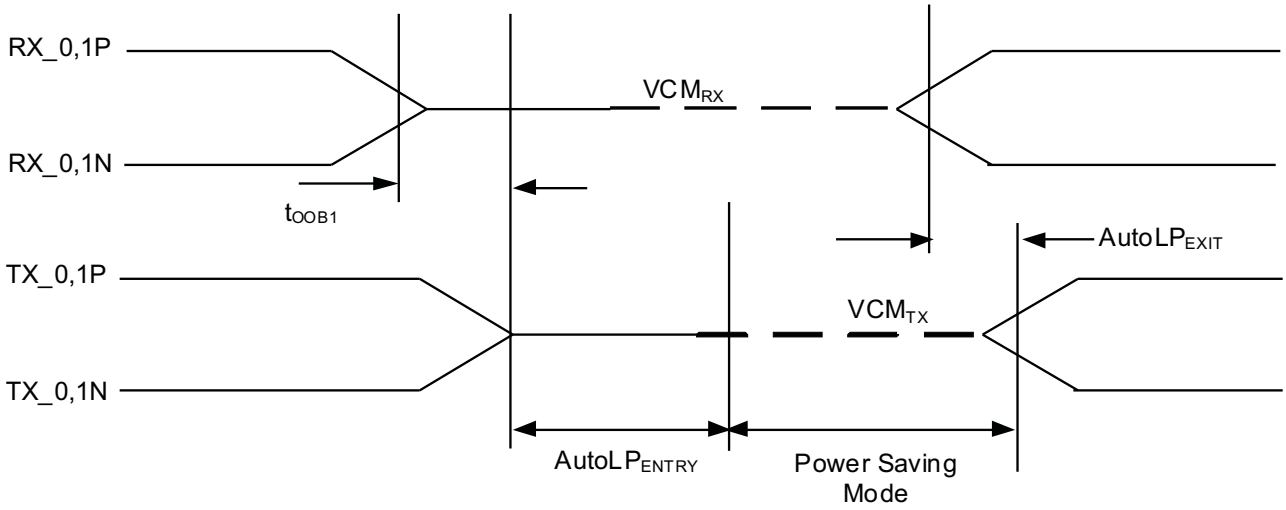


Figure 7. Auto Low Power Mode Timing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVCP422DB	ACTIVE	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 85	LVCP422	Samples
SN75LVCP422DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 85	LVCP422	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

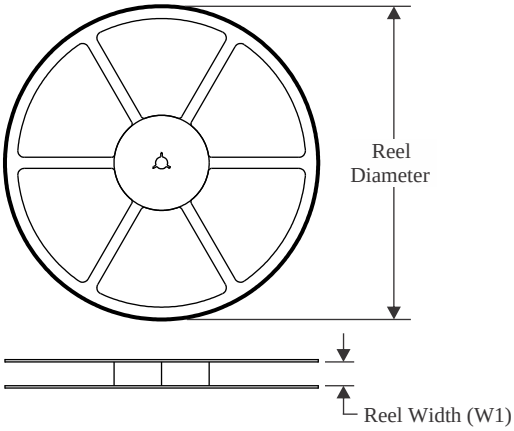
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

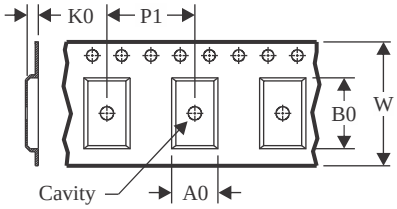
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

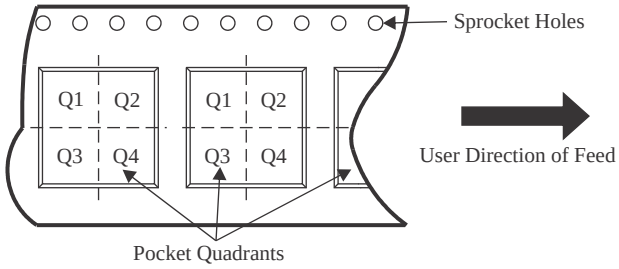


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

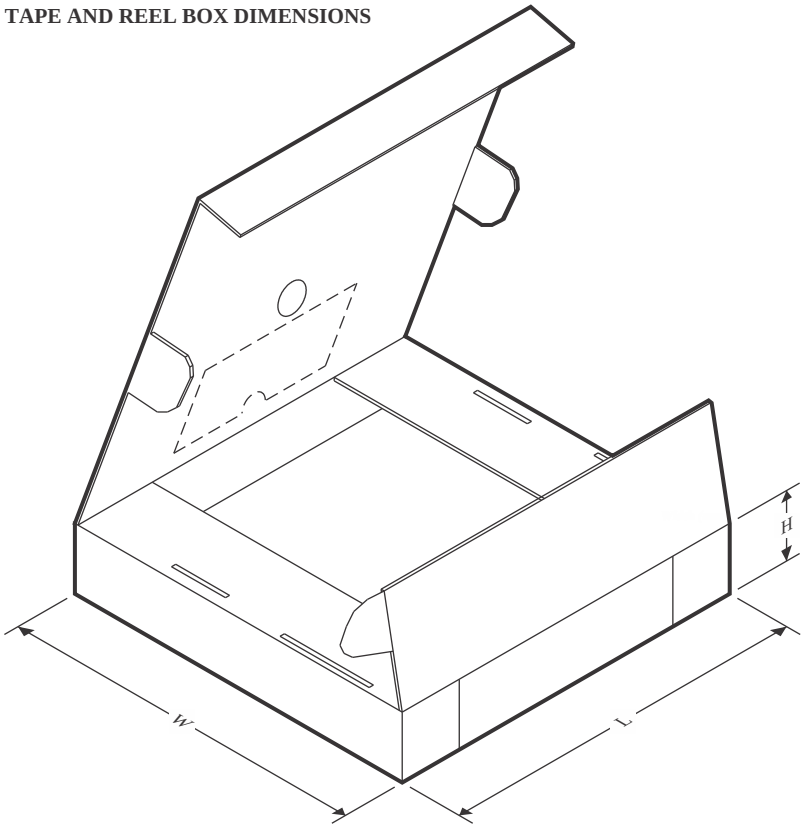
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVCP422DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

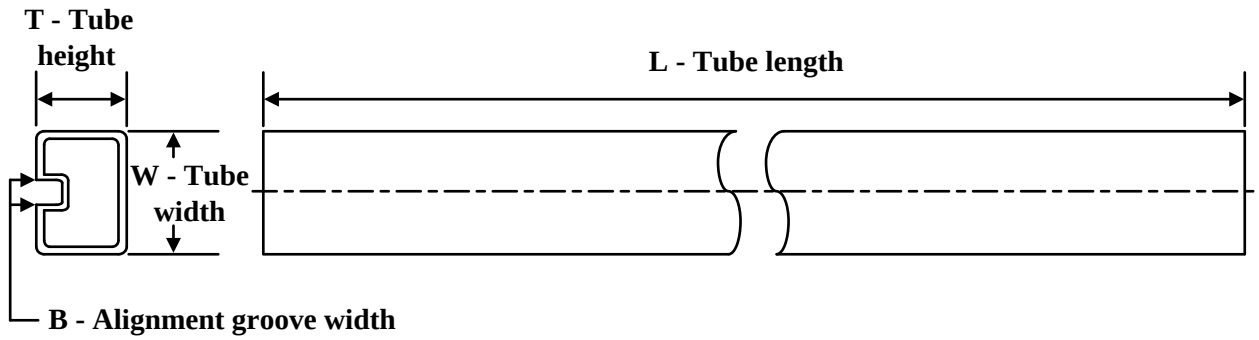
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVCP422DBR	SSOP	DB	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

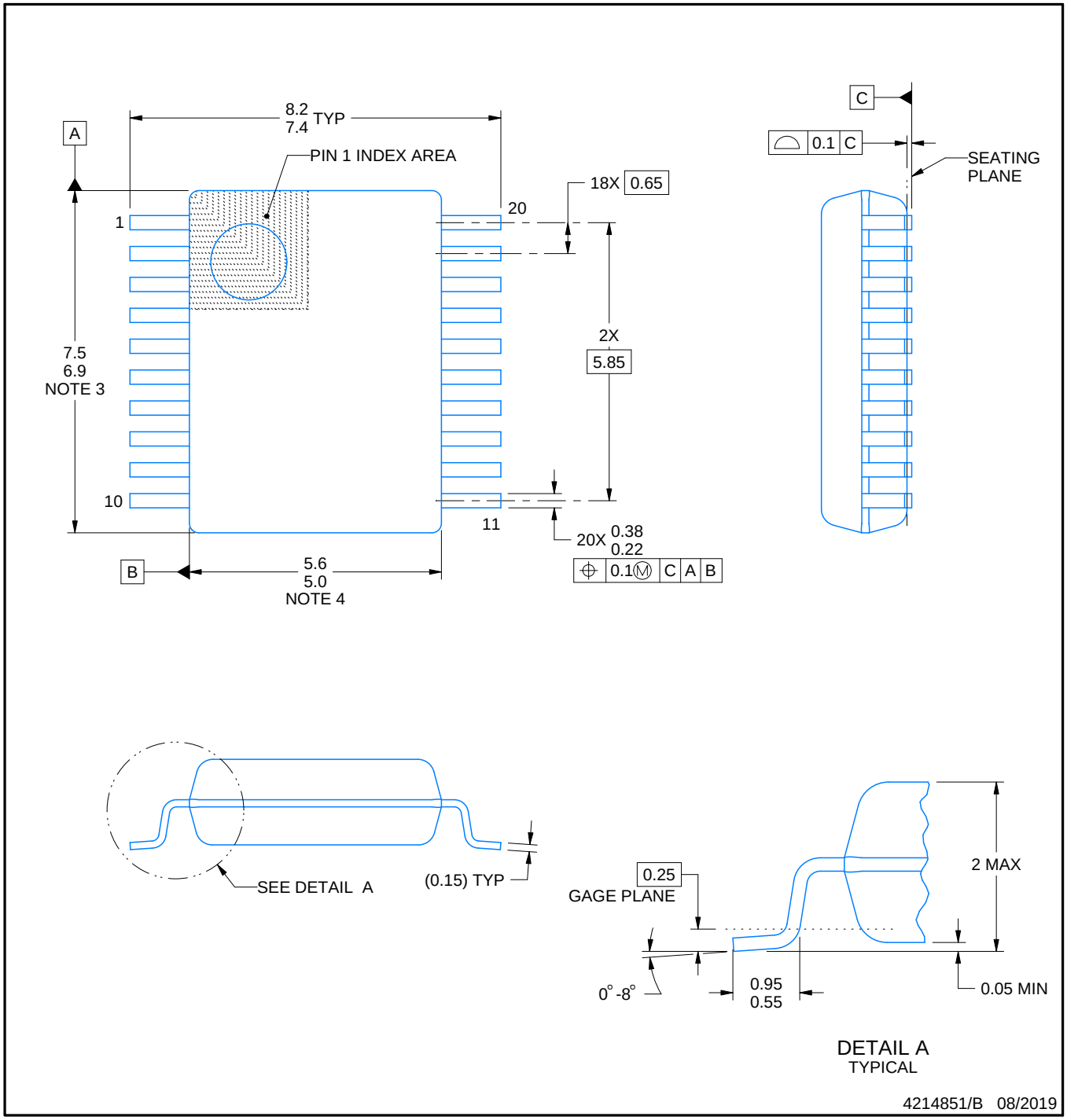
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75LVCP422DB	DB	SSOP	20	70	530	10.5	4000	4.1

PACKAGE OUTLINE

DB0020A

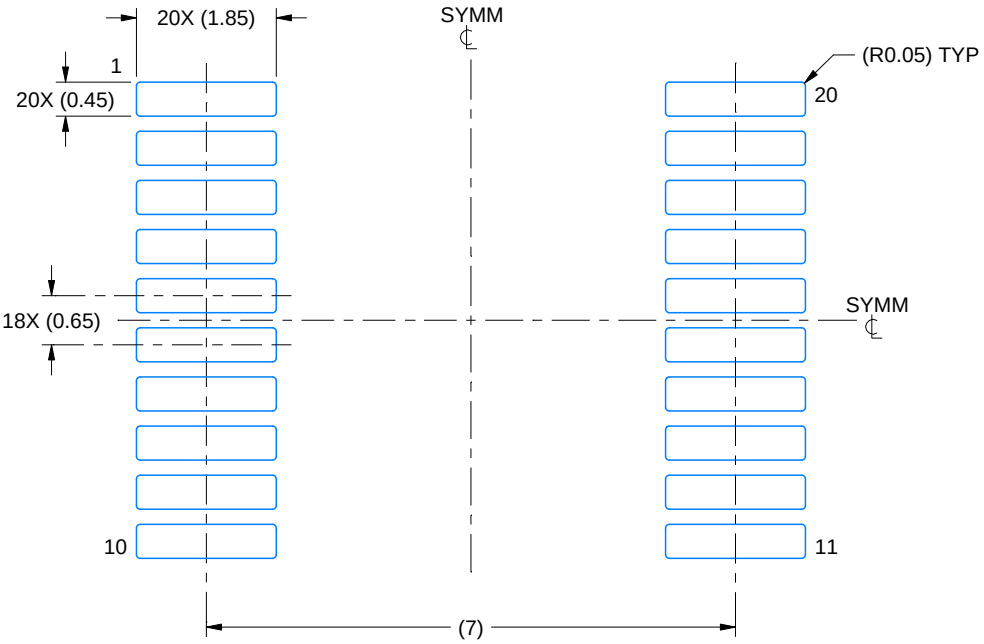
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

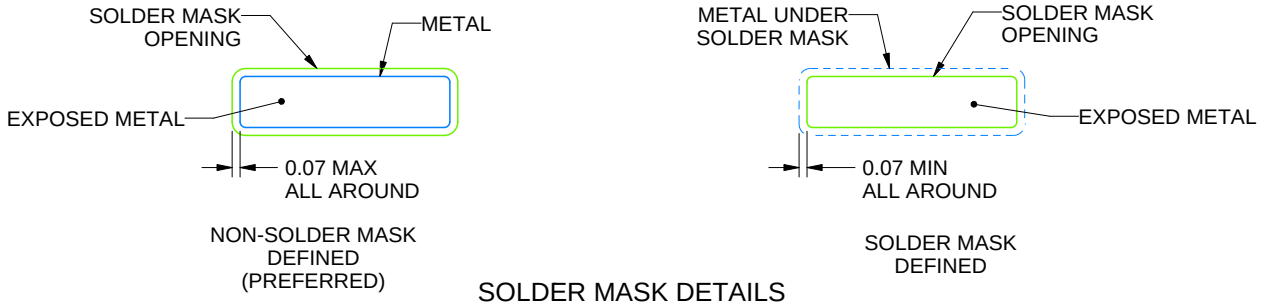


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

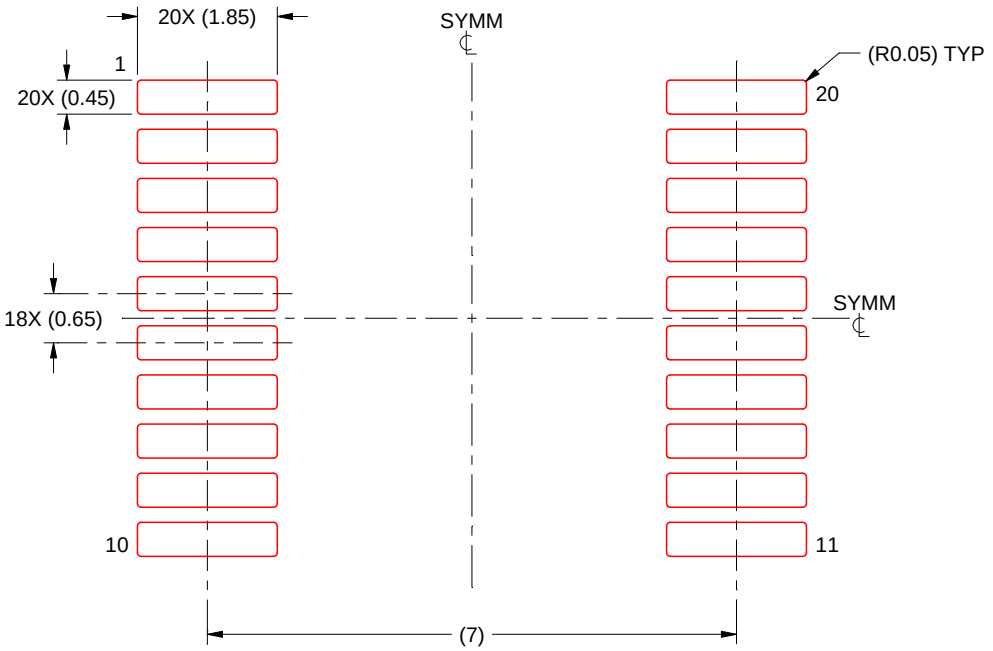
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265