TAC5142 Low-power pin controlled stereo audio codec with 100dB dynamic range ADC and 106dB dynamic range DAC

1 Features

- ADC Channel
  - Performance:
    - Line differential input dynamic range: 100 dB
    - Mic differential input dynamic range: 100 dB
    - THD+N: –95 dB
  - Input voltage:
    - Differential, 2-V_{RMS} full-scale inputs
    - Single-ended, 1-V_{RMS} full-scale inputs
  - Configurable Digital HPF:
    - 1 Hz(48KSPS Sample Rate)
    - 12 Hz(48KSPS Sample Rate)
  - Sample rate (f_S) = 8 kHz to 192 kHz
  - Low noise microphone bias
- – DAC Channel
    - DAC performance:
      - DAC to Line Out Dynamic Range: 106 dB
      - DAC to HP Out Dynamic Range: 106 dB
      - THD+N: –80 dB
    - Head Phone/Line Out output voltage:
      - Differential, 2-V_{RMS} full-scale
      - Pseudo-differential, 1-V_{RMS} full-scale
      - Single-ended, 1-V_{RMS} full-scale
    - DAC sample Rates (f_s) = 8KHz to 192KHz
  - Common Features
    - Pin Control
    - Audio Serial Interface
      - Format: TDM, LJ or I^2S
      - Configurable TDM Slot
      - Bus Controller and Target Modes
      - Word Length: Selectable 16, 24 or 32 Bits
    - Linear Phase Filter
    - Auto Clock Detection and Configuration
    - Low Power Modes
    - Interrupt output
    - Single Supply Operation AVDD: 1.8V or 3.3V
    - I/O Supply Operation: 1.2V or 1.8V or 3.3V
    - Temperature grade 1: –40°C ≤ T_A ≤ +125°C

2 Applications

- Land Mobile Radio
- IP Network Camera
- IP Telephone
- Video Conference System
- Professional audio mixer/control surface

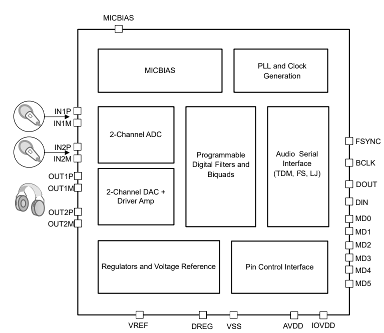
3 Description

The TAC5142 is a Stereo Codec with 2V_{RMS} differential Input, 100dB ADC and 2V_{RMS} 106dB Stereo DAC. The TAC5142 supports both differential and Single Ended input and output. Device supports both Microphone and Line In input on ADC Channel. DAC Output can be configured for either Line Out or Head Phone Load. The device integrates a phase-locked loop (PLL), a DC removal high-pass filter (HPF) and supports sample rates up to 192kHz. TAC5142 can drive upto 62 mW into a Headphone Load. The TAC5142 supports time-division multiplexing (TDM), left-justified (LJ), or I^2S audio formats in controller and target mode, and is pin controlled. These integrated high-performance features, pin control along with a single supply operation, make TAC5142 an excellent choice for space-constrained audio applications.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TAC5142	WQFN (28)	4mm x 4mm with 0.5mm Pitch

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

ADVANCE INFORMATION

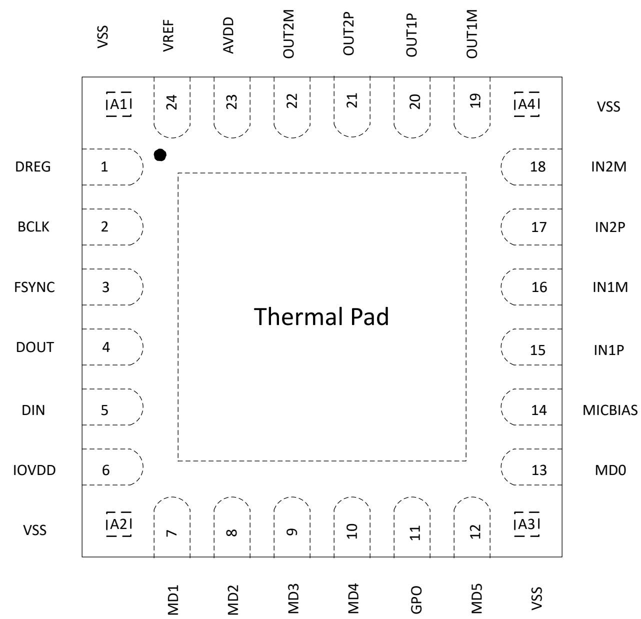
Table of Contents

1 Features 1
2 Applications 1
3 Description 1
4 Device Comparison Table 3
5 Pin Configuration and Functions 4
6 Specifications 6
6.1 Absolute Maximum Ratings 6
6.2 ESD Ratings 6
6.3 Recommended Operating Conditions 6
6.4 Thermal Information 7
6.5 Electrical Characteristics 7
6.6 Timing Requirements: TDM, I^2S or LJ Interface 11
6.7 Switching Characteristics: TDM, I^2S or LJ Interface 11
7 Parameter Measurement Information 13
8 Detailed Description 14
8.1 Overview 14
8.2 Functional Block Diagram 14
8.3 Feature Description 15
8.4 Device Functional Modes 31
9 Application and Implementation 32
9.1 Application Information 32
9.2 Typical Application 32
10 Power Supply Recommendations 34
11 Device and Documentation Support 35
11.1 Documentation Support 35
11.2 Receiving Notification of Documentation Updates 35
11.3 Support Resources 35
11.4 Trademarks 35
11.5 Electrostatic Discharge Caution 35
11.6 Glossary 35
12 Revision History 35
13 Mechanical, Packaging, and Orderable Information 35
13.1 Tape and Reel Information 39

4 Device Comparison Table

FEATURE	TAC5242	TAC5142	TAC5212	TAC5112	TAC5211	TAC5111
Control interface	Pin control		I^2C or SPI			
Digital audio serial interface	TDM or I^2S		TDM or I^2S or left-justified (LJ)			
Audio ADC channel	2		2		1	
Digital microphone channel	Not available (N/A)		4		2	
Programmable MICBIAS voltage	Yes (Fixed Voltage)		Yes			
ADC Dynamic range	118 dB	100 dB	118 dB	100 dB	118 dB	100 dB
Audio DAC Channel	2		2		1	
DAC Dynamic Range	119 dB	106 dB	119 dB	106dB	119 dB	106 dB
Compatibility	Pin-to-pin, package, drop-in replacements of each other		Pin-to-pin, package, and control registers compatible; drop-in replacements of each other		Pin-to-pin, package, and control registers compatible; drop-in replacements of each other	
Package	QFN , 24-pin, 4.00 mm × 4.00 mm (0.5-mm pitch)					

5 Pin Configuration and Functions



Notes:-
Not to Scale
Pinout is subject to changes

Figure 5-1. TAC5142 Pinout

Table 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
VSS	A1	Ground	Short directly to board Ground Plane.
DREG	1	Digital Supply	Digital on-chip regulator output voltage for digital supply (1.5 V, nominal)
BCLK	2	Digital I/O	Audio serial data interface bus bit clock
FSYNC	3	Digital I/O	Audio serial data interface bus frame synchronization signal
DOUT	4	Digital Output	Audio serial data interface bus output
DIN	5	Digital Input	Audio serial data interface bus input
IOVDD	6	Digital Supply	Digital I/O power supply (1.8 V or 3.3 V, nominal)
VSS	A2	Ground	Short directly to board Ground Plane.
MD1	7	Digital Input	Controller Mode: Frame Rate and BCLK frequency selection
			Target Mode: AVDD Supply and Word Length selection
MD2	8	Digital Input	Controller Mode: Frame Rate and BCLK frequency selection
			Target Mode: AVDD Supply and Word Length selection
MD3	9	Digital Input	Controller Mode: Controller Clock Input
			Target Mode: Digital HPF and Data Slot selection
MD4	10	Digital Input	ADC/DAC mode selection
GPO	11	Digital Output	Interrupt Output

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
MD5	12	Digital Input	ADC/DAC mode selection
VSS	A3	Ground	Short directly to board Ground Plane.
MD0	13	Analog Input	Multi-Level Analog input for Controller/Target and I^2S/TDM/LJ selection
MICBIAS	14	Analog	MICBIAS Output (Porgrammable output upto 11V)
IN1P	15	Analog Input	Analog Input 1P Pin
IN1M	16	Analog Input	Analog Input 1M Pin
IN2P	17	Analog Input	Analog Input 2P Pin
IN2M	18	Analog Input	Analo Input 2M Pin
VSS	A4	Ground	Short directly to board Ground Plane.
OUT1M	19	Analog Output	Analog Output 1M Pin
OUT1P	20	Analog Output	Analog Output 1P Pin
OUT2P	21	Analog Output	Analog Output 2P Pin
OUT2M	22	Analog Output	Analog Output 2M Pin
AVDD	23	Analog Supply	Analog power (3.3 V, nominal)
VREF	24	Analog	Analog reference voltage filter output

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AVSS	–0.3	3.9	V
Supply voltage	IOVDD to VSS (thermal pad)	–0.3	3.9	V
Ground voltage differences	AVSS to VSS (thermal pad)	–0.3	0.3	V
Analog input voltage	Analog input pins voltage to AVSS	–0.3	AVDD+0.3	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Functional ambient, T_A	-55	125	°C
	Operating ambient, T_A	–40	125	
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD(1)	Analog supply voltage to AVSS AVDD-3.3V Operation	3.0	3.3	3.6	V
AVDD(1)	Analog supply voltage to AVSS - AVDD 1.8V operation	1.65	1.8	1.95	V
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3-V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8-V operation	1.65	1.8	1.95	
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 1.2-V operation	1.08	1.2	1.32	V
INPUTS					
INxx	Analog input pins voltage to AVSS for line-in recording	0		AVDD	V
INxx	Analog input pins voltage to AVSS for microphone recording	0.1		MICBIAS – 0.1	V
IO	Digital input pins(except MD0) voltage to VSS (thermal pad)	0		IOVDD	V
MD0	MD0 pin w.r.t AVSS	0		AVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C

		MIN	NOM	MAX	UNIT
OTHERS					
	MD3 clock frequency (in controller mode)			36.864(2)	MHz
C_L	Digital output load capacitance		20	50	pF

(1) AVSS and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2 V.
(2) MCLK input rise time (V_{IL} to V_{IH}) and fall time (V_{IH} to V_{IL}) must be less than 5 ns. For better audio noise performance, MCLK input must be used with low jitter.

6.4 Thermal Information

THERMAL METRIC(1)		TAC5142 RGE (WQFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.8	°C/W

(1) For more information about traditional and new thermal metrics, see the spra953 application report.

6.5 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 [char_not_recognized] f_S, TDM target mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC PERFORMANCE FOR INPUT RECORDING						
	Differential input full-scale AC signal voltage	AC-coupled input		2		V_{RMS}
	Single-ended input full-scale AC signal voltage	AC-coupled input		1		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain (MD4/MD5=2'b00)		100		dB
SNR	Signal-to-noise ratio, A-weighted(1) (2)	IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain, Device in Hign Common Mode Tolerance Mode (MD4/MD5=2'b01)		98		
SNR	Signal-to-noise ratio, A-weighted(1) (2)	1.8V AVDD Operation:IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain (MD4/MD5=2'b00)		99		dB
		1.8V AVDD Operation:IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain (MD4/MD5=2'b01)		93		
SNR	Signal-to-noise ratio, A-weighted(1) (2)	IN1 single-ended AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain (MD4/MD5=2'b10 or 2'b11)		96		dB
SNR	Signal-to-noise ratio, A-weighted(1) (2)	1.8V AVDD Operation:IN1 single-ended AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain (MD4/MD5=2'b10 or 2'b11)		92		dB

ADVANCE INFORMATION

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 [char_not_recognized] f_S, TDM target mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DR	Dynamic range, A-weighted(2)	IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		100		dB
		IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		98		
DR	Dynamic range, A-weighted(2)	1.8V AVDD Operation: IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		99		dB
		1.8V AVDD Operation: IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		93		
DR	Dynamic range, A-weighted(2)	IN1 single-ended AC-coupled input selected and -60-dB full-scale AC signal input, 0-dB channel gain (MD4/MD5=2'b10 or 2'b11)		96		dB
DR	Dynamic range, A-weighted(2)	1.8V AVDD Operation: IN1 single-ended DC-coupled input selected and -60-dB full-scale AC signal input, 0-dB channel gain (MD4/MD5=2'b10 or 2'b11)		92		dB
THD+N	Total harmonic distortion(2)	IN1 differential AC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain		–80	TBD	dB
		IN1 differential DC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain		–80		
ADC OTHER PARAMETERS						
	Input impedance	Differential input, between INxP and INxM / Differential input, between INxP and INxM, 5kΩ Mode		40		kΩ
	Offset	Shorted Input.		TBD		mV
	Output data sample word length	Based on MD1/MD2 Configuration	16		32	Bits
	Digital high-pass filter cutoff frequency	First-order IIR filter with programmable coefficients, –3-dB point (default setting)		1		Hz
	Interchannel isolation	–1-dB full-scale AC signal line-in input to non measurement channel		–134		dB
	Interchannel gain mismatch	–6-dB full-scale AC signal line-in input, 0-dB channel gain		0.1		dB
	Interchannel phase mismatch	1-kHz sinusoidal signal		0.01		Degrees
PSRR	Power-supply rejection ratio	100-mV_{PP}, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain		92		dB
MICROPHONE BIAS						
	MICBIAS noise	BW = 20 Hz to 20 kHz, A-weighted, 1-µF capacitor between MICBIAS and AVSS		2		µV_{RMS}
	MICBIAS voltage	AVDD=1.8V		1.375		V
	MICBIAS voltage	AVDD=3.3V		2.75		V

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 [char_not_recognized] f_S, TDM target mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DAC Performance for Line Output/Head Phone Playback						
	Full Scale Output Voltage	Differential output between OUTxP and OUTxM, AVDD=3.3V		2		V_{RMS}
		Differential Output between OUTxP and OUTxM, AVDD=1.8V		1		
		Single-ended Output, AVDD=3.3V		1		
		Single-ended Output, AVDD=1.8V		0.5		
		Pseudo Differential Output between OUTxP and OUTxM, AVDD=3.3V		1		
		Pseudo Differential Output between OUTxP and OUTxM, AVDD=1.8V		0.5		
SNR	Signal-to-noise ratio, A-weighted(1) (2)	Differential Output, 0dBFS Signal, AVDD=3.3V		106		dB
		Single Ended Output, 0dBFS Signal, AVDD=3.3V		97		
		Pseudo Differential Output, 0dBFS Signal, AVDD=3.3V		96		
		Differential Output, 0dBFS Signal, AVDD=1.8V		100		
		Single Ended Output, 0dBFS Signal, AVDD=1.8V		91		
		Pseudo Differential Output, 0dBFS Signal, AVDD=1.8V		90		
DR	Dynamic range, A-weighted(2)	Differential Output, -60dBFS Signal, AVDD=3.3V		106		dB
		Single Ended Output, -60dBFS Signal, AVDD=3.3V		97		
		Pseudo Differential Output, -60dBFS Signal, AVDD=3.3V		96		
		Differential Output, -60dBFS Signal, AVDD=1.8V		100		
		Single Ended Output, -60dBFS Signal, AVDD=1.8V		91		
		Pseudo Differential Output, -60dBFS Signal, AVDD=1.8V		90		
THD+N	Total harmonic distortion(2)			–95		dB
	Head Phone Load Range			16		Ω
	Head Phone/LO Cap Load		0	100	550	pF
	Line Out Load Range		600			Ω
DAC Channel OTHER PARAMETERS						
	Output Offset	0 Input, Fully Differential Output		0.2		mV
	Output Offset	0 Input, Pseudo Differential Output		0.4		mV
	Output Common Mode	Common Mode Level for OUTxP and OUTxM AVDD=1.8V		0.9		V
	Output Common Mode	Common Mode Level for OUTxP and OUTxM AVDD=3.3V		1.66		V
	Common Mode Error	DC Error in Common Mode Voltage		±10		mV
	Output Signal Bandwidth			20		kHz
	Input data sample word length	Programmable	16		32	Bits

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 [char_not_recognized] f_S, TDM target mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Digital high-pass filter cutoff frequency	First-order IIR filter with programmable coefficients, –3-dB point (default setting)		2		Hz
	Interchannel isolation			–134		dB
	Interchannel gain mismatch			0.1		dB
	Interchannel phase mismatch	1-kHz sinusoidal signal		0.01		Degrees
PSRR	Power-supply rejection ratio	100-mV_{PP}, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain		100		dB
	Mute Attenuation			–130		dB
P_{out}	Output Power Delivery	Single ended/Pseudo Differential R_L=16 Ohms, THD+N<1%		62.5		mW
DIGITAL I/O						
V_{IL}	Low-level digital input logic voltage threshold	All digital pins, IOVDD 1.8-V operation	–0.3		0.35 x IOVDD	V
		All digital pins, IOVDD 3.3-V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins, IOVDD 1.8-V operation	0.65 x IOVDD		IOVDD + 0.3	V
		All digital pins, IOVDD 3.3-V operation	2		IOVDD + 0.3	
V_{OL}	Low-level digital output voltage	All digital pins, I_{OL} = –2 mA, IOVDD 1.8-V operation			0.45	V
		All digital pins, I_{OL} = –2 mA, IOVDD 3.3-V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins, I_{OH} = 2 mA, IOVDD 1.8-V operation	IOVDD – 0.45			V
		All digital pins, I_{OH} = 2 mA, IOVDD 3.3-V operation	2.4			
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, input = 0 V	–5	0.1	5	µA
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, input = IOVDD	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in sleep mode (software shutdown mode)	All device external clocks stopped		TBD		µA
I_{IOVDD}				1		
I_{AVDD}	Current consumption with ADC 2-channel operation at f_S 48-kHz, MICBIAS on, PLL off, BCLK = 512 * f_S			TBD		mA
I_{IOVDD}				0.1		
I_{AVDD}	Current consumption with DAC to HP 2-channel operation at f_S 16-kHz, BCLK = 512 * f_S			TBD		mA
I_{IOVDD}				0.2		

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 [char_not_recognized] f_S, TDM target mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{AVDD}	Current consumption with DAC to HP 2-channel operation at f_S 48-kHz, BCLK = 512 * f_S			TBD		mA
I_{IOVDD}				TBD		

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter can result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

6.6 Timing Requirements: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period		40			ns
$t_{H(BCLK)}$	BCLK high pulse duration (1)		18			ns
$t_{L(BCLK)}$	BCLK low pulse duration (1)		18			ns
$t_{SU(FSYNC)}$	FSYNC setup time		8			ns
$t_{HLD(FSYNC)}$	FSYNC hold time		8			ns
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time			10	ns
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time			10	ns

(1) The BCLK minimum high or low pulse duration must be higher than 25 ns (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

6.7 Switching Characteristics: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDOUT-BCLK)}$	BCLK to SDOUT delay	50% of BCLK to 50% of SDOUT, IOVDD = 1.8 V			18	ns
		50% of BCLK to 50% of SDOUT, IOVDD = 3.3 V			14	
$t_{d(SDOUT-FSYNC)}$	FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0)	50% of FSYNC to 50% of SDOUT, IOVDD = 1.8 V			18	ns
		50% of FSYNC to 50% of SDOUT, IOVDD = 3.3 V			14	
$f_{(BCLK)}$	BCLK output clock frequency; master mode (1)				24.576	MHz
$t_{H(BCLK)}$	BCLK high pulse duration; master mode	IOVDD = 1.8 V	14			ns
		IOVDD = 3.3 V	14			
$t_{L(BCLK)}$	BCLK low pulse duration; master mode	IOVDD = 1.8 V	14			ns
		IOVDD = 3.3 V	14			
$t_{d(FSYNC)}$	BCLK to FSYNC delay; master mode	50% of BCLK to 50% of FSYNC, IOVDD = 1.8 V			18	ns
		50% of BCLK to 50% of FSYNC, IOVDD = 3.3 V			14	
$t_{r(BCLK)}$	BCLK rise time; master mode	10% - 90% rise time, IOVDD = 1.8 V			10	ns
		10% - 90% rise time, IOVDD = 3.3 V			10	

ADVANCE INFORMATION

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{f(BCLK)}$	BCLK fall time; master mode	90% - 10% fall time, IOVDD = 1.8 V			8	ns
		90% - 10% fall time, IOVDD = 3.3 V			8	

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

ADVANCE INFORMATION

7 Parameter Measurement Information

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TAC5142 is from a scalable family of devices. As part of the extended family of devices, the TAC5142 consists of a high-performance, low-power, flexible, mono/stereo, audio analog-to-digital converter (ADC) and audio digital-to-analog converter (DAC) with extensive feature integration. This device is intended for broad market applications such as ruggedized communication equipment, IP network camera, Professional Audio and multimedia applications. The high dynamic range of this device enables far-field audio recording with high fidelity. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained system designs. Package, performance, and compatible configuration across extended family make this device well suited for scalable system designs.

The TAC5142 consists of the following blocks:

- 2-channel, multibit, high-performance delta-sigma (ΔΣ) ADCs
- Configurable single-ended or differential audio inputs with 2Vrms differential signal swing
- Low-noise programmable microphone bias output
- 2-channel, multibit, high-performance delta-sigma (ΔΣ) DACs
- Configurable single-ended, differential or pseudo-differential audio outputs
- Protection for MICBIAS and analog outputs
- Linear-phase digital decimation and interpolation filters
- Volume ramp up/down for each channel
- Configurable digital high-pass filter (HPF)
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

8.2 Functional Block Diagram

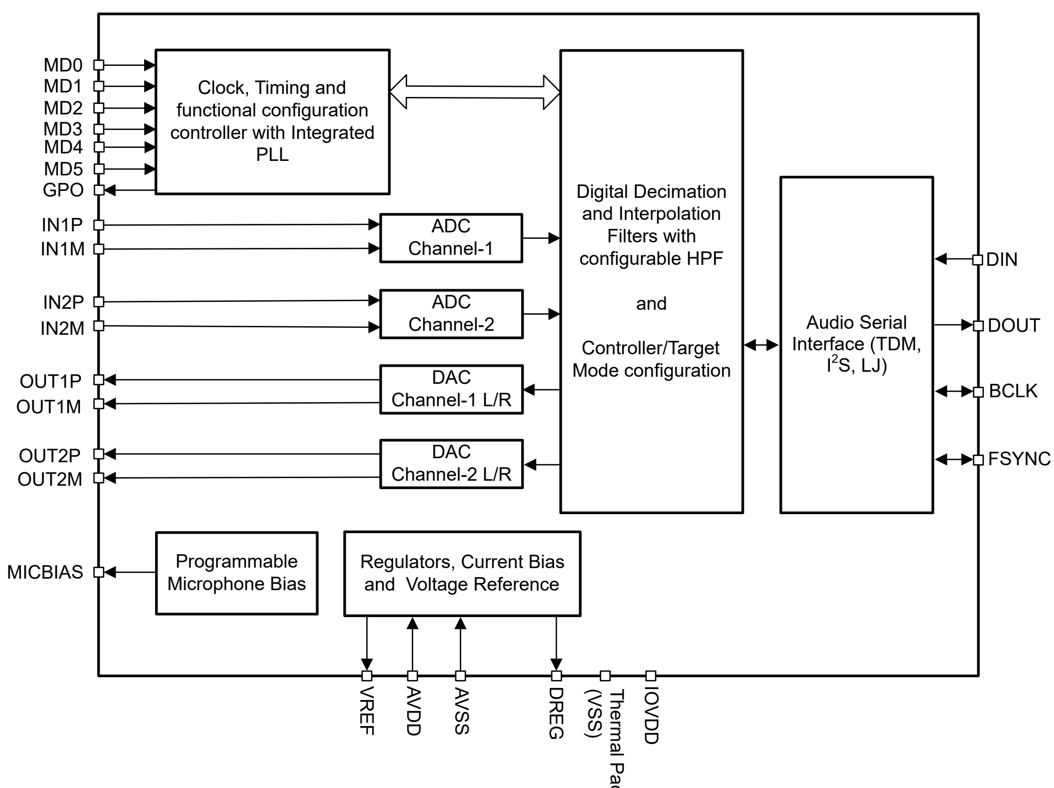


Figure 8-1.

8.3 Feature Description

8.3.1 Hardware Control

The device supports simple hardware-pin-controlled options to select a specific mode of operation and audio interface for a given system. The MD0 to MD5 pins allow the device to be controlled by either pullup or pulldown resistors.

8.3.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAC5142 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for the I^2S and LJF, and the pin-selectable controller-target configurability for bus clock lines.

The device supports an audio bus controller or target mode of operation using the hardware pin MD0. In target mode, FSYNC and BCLK work as input pins whereas in controller mode, FSYNC and BCLK work as output pins generated by the device. Table 8-1 shows the master and slave mode selection using the MD0 pin.

Table 8-1. Controller and Target Mode Selection

MD0	CONTROLLER AND TARGET SELECTION
Short to Ground	Target I2S Mode
Short to Ground with 4.7K Ohms	Target TDM Mode
Short to AVDD	Controller I2S Mode
Short to AVDD with 4.7K Ohms	Controller TDM Mode
Short to AVDD with 22K Ohms	Target LJ Mode

The word length for audio serial interface (ASI) in TAC5142 can be selected through MD1 and MD2 Pins in target mode of operation. In controller mode, fixed word length of 32 bits is supported. The TAC5142 also supports 1.8V AVDD operation in target mode with 32 bit word length. Table 8-2 shows the configuration table for setting word length and AVDD supply voltage

Table 8-2. Word Length and Supply Mode Selection

MD1	MD2	CONTROLLER AND TARGET SELECTION
Low	Low	Word Length=32 AVDD=3.3V
Low	High	Word Length=32 AVDD=1.8V
High	Low	Word Length=24 AVDD=3.3V
High	High	Word Length=16 AVDD=3.3V

The TAC5142 offers slot configuration for target TDM mode of operation. This can be selected through MD3 pin when MD0 is configured in target TDM mode. For options on MD3 in other modes of operation, refer to Digital High-Pass Filter. Table 8-3 shows the slots selected in Target TDM mode of operation based on MD3 pin.

Table 8-3. TDM Slot Selection for Target Mode

MD3	ADC SLOTS	DAC SLOTS
Low	ADC Data on Slot 0 and 1	DAC Data on Slot 0 and 1
High	ADC Data on Slot 2 and 3	DAC Data on Slot 2 and 3

ADVANCE INFORMATION

8.3.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. Figure 8-2 and Figure 8-3 show the protocol timing for TDM operation with various configurations.

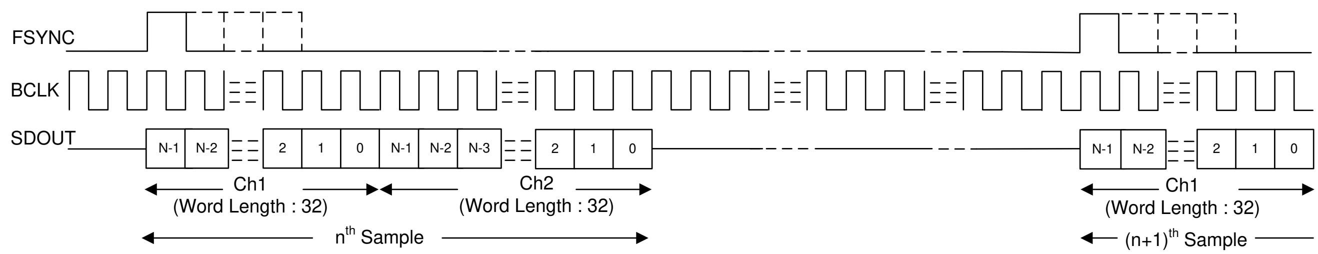


Figure 8-2. TDM Mode Protocol Timing (MD0 shorted to ground with 4.7K Ohms) In Target Mode

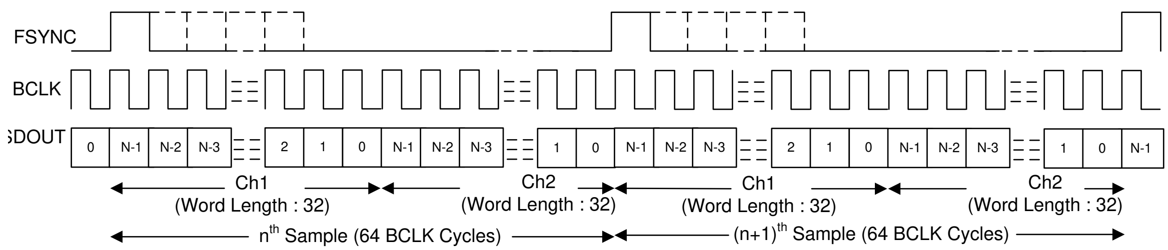


Figure 8-3. TDM Mode Protocol Timing (MD0 shorted to AVDD with 4.7K Ohms) In Controller Mode

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the 32-bits word length of the output channel data. The device transmits a zero data value on SDOUT for the extra unused bit clock cycles. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well.

8.3.2.2 Inter IC Sound (I²S) Interface

The standard I²S protocol is defined for only two channels: left and right. In I²S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. In master mode, FSYNC is transmitted on the rising edge of BCLK. Figure 8-4 and Figure 8-5 show the protocol timing for I²S operation in slave and master mode of operation.

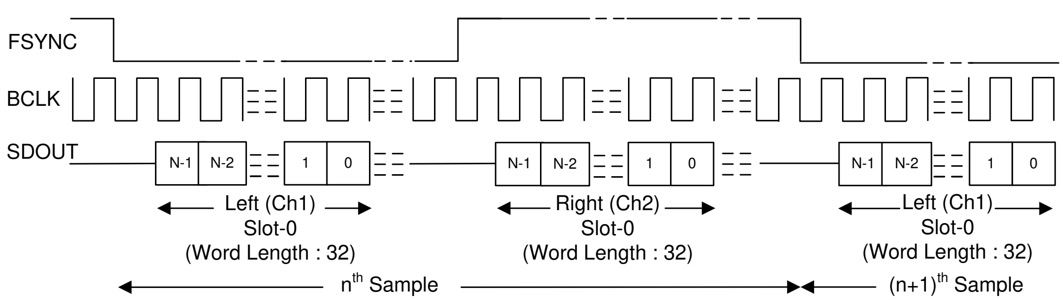


Figure 8-4. I²S Mode Protocol Timing (MD0 shorted to ground) in Target Mode

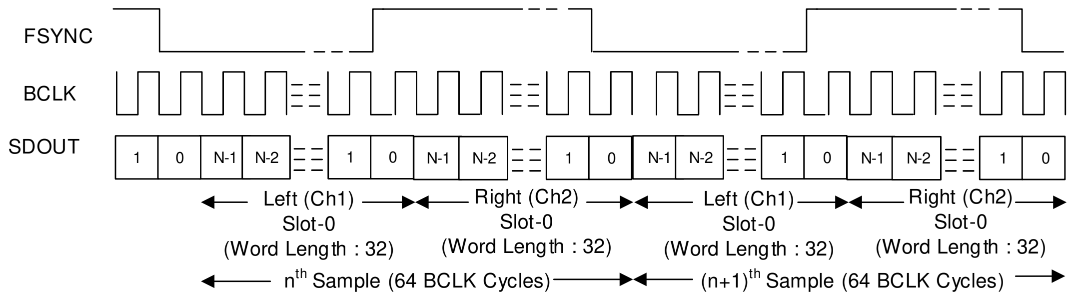


Figure 8-5. I²S Protocol Timing (MD0 shorted to AVDD) In Controller Mode

For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the 32-bits word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the 32-bits data word length. Similarly, the FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the 32-bits data word length. The device transmit zero data value on SDOUT for the extra unused bit clock cycles.

ADVANCE INFORMATION

8.3.3 Phase-Locked Loop (PLL) and Clock Generation

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC and DAC modulators and digital filter engine, as well as other control blocks.

In target mode of operation, the device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. Table 8-4 and Table 8-5 list the supported FSYNC and BCLK frequencies.

Table 8-4. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**

Table 8-5. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**

In the controller mode of operation, the device uses the MD3 pin (as the system clock, CCLK) as the reference input clock source. The device provides flexibility in FSYNC selection with a supported system clock frequency option of either 256 × f_S or 128 × f_S or a fixed 48/44.1KSPS or 96/88.2KSPS as configured using the MD1 and MD2 pins. Table 8-6 shows the FSYNC and BCLK selection for the controller mode using the MD1 and MD2 pins.

ADVANCE INFORMATION

Table 8-6. System Clock Selection for the Controller Mode

MD1	MD2	SYSTEM CLOCK SELECTION (Valid for Master Mode Only)
LOW	LOW	FSYNC = CCLK/256 **I2S Mode**: BCLK = 64*f_S **TDM Mode**: For FSYNC<=96KSPS, BCLK = 128*f_S For FSYNC>96KSPS, BCLK = 64*f_S
LOW	HIGH	FSYNC = CCLK/128 **I2S Mode**: BCLK = 64*f_S **TDM Mode**: For FSYNC<=96KSPS, BCLK = 128*f_S For FSYNC>96KSPS, BCLK = 64*f_S
HIGH	LOW	FSYNC = 96/88.2KSPS; **I2S Mode**: BCLK = 64*f_S **TDM Mode**: BCLK = 128*f_S
HIGH	HIGH	FSYNC = 48/44.1KSPS; **I2S Mode**: BCLK = 64*f_S **TDM Mode**: BCLK = 128*f_S

See Table 8-2 for the MD1, MD2 and MD3 pin function in the target mode of operation.

8.3.4 Analog Input Output Configurations

The device supports simultaneous recording of up to two channels using the high-performance stereo ADC. The device consists of two pairs of analog input pins (INxP and INxM) which can be configured in single-ended or differential input mode by setting MD4 and MD5 pins. The input source for the analog pins can be from electret condenser analog microphones, micro electrical-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board.

The voice or audio signal inputs can be capacitively coupled (AC-coupled) or DC-coupled to the device. For best distortion performance, use of low-voltage coefficient capacitors for AC-coupling is recommended. The typical input impedance for the TAC5142 is 40 kΩ for the INxP or INxM pins. The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power-up. To enable quick charging, the device has a quick charge scheme to speed up the charging of the coupling capacitor at power-up. Quick-charge time for the device is configured using MD3 pin along with digital HPF. Refer to Table 8-8 for quick charge time based on MD3 pin configuration.

The device supports playback of two channels using the high-performance stereo DAC. The device consists of two pairs of analog output pins (OUTxP and OUTxM) which can be configured in single-ended or differential input mode by setting MD4 and MD5 pins. The input source for these channels is from TDM/I2S.

Table 8-7 shows the analog input output configuration modes available with MD4 and MD5 configuration

Table 8-7. Analog Input Output Configurations

MD4	MD5	ANALOG INPUT CONFIGURATION	ANALOG OUTPUT CONFIGURATION
Low	Low	Differential input; AC-Coupled only	Differential Output; Lineout load only

Table 8-7. Analog Input Output Configurations (continued)

MD4	MD5	ANALOG INPUT CONFIGURATION	ANALOG OUTPUT CONFIGURATION
Low	High	Differential input; AC or DC-Coupled	Differential Output; Receiver or Lineout load
High	Low	Single Ended Input on INxP	Single ended output; Lineout only
High	High	Single Ended Input on INxP	Pseudo differential output; Headphone or Lineout load

8.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The TAC5142 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1-µF capacitor connected from the VREF pin to analog ground (AVSS). The value of this reference voltage, VREF, is set to 2.75 V, which in turn supports a 2-V_{RMS} differential full-scale input and 2-V_{RMS} differential full-scale output to the device. The required minimum AVDD voltage for this VREF voltage is 3 V. Do not connect any external load to a VREF pin.

8.3.6 ADC Signal-Chain

The TAC5142 ADC signal chain is comprised of very-low-noise, high-performance, and low-power analog blocks and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with an integrated low noise stereo DAC and compact package makes the TAC5142 optimized for a variety of end-equipments and applications that require low noise multichannel audio record and playback. Figure 8-6 shows a conceptual block diagram for the TAC5142 that highlights the various building blocks used in the signal chain, and how the blocks interact in the signal chain.

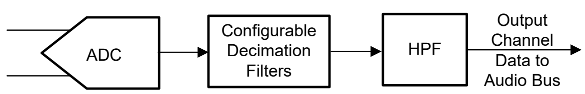


Figure 8-6. ADC Signal-Chain Processing Flowchart

The ADC front-end in the TAC5142 is very low noise, with a 118-dB dynamic range performance. This enables the TAC5142 to record a far-field audio signal with very high fidelity, both in quiet and loud environments. Moreover, the ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multistage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation. The TAC5142 supports sample rates of up to 192KSPS in both controller and target mode of operation.

8.3.6.1 Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a configurable high-pass filter (HPF) with –3-dB cut-off frequency of 0.000021 × f_S or 0.00025 × f_S. The HPF is not a channel-independent filter but is globally applicable for all the ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. This configuration is only available in I2S or LJF Target mode of operation. In Target TDM Mode of operation, MD3 is used to set slot for input and output data streams. Refer to section for more details on Daisy chain features. In Controller Mode, MD3 is used as CCLK input and HPF is by default set to 0.000021 × f_S. Additionally, As lower frequency filter in digital requires higher value capacitor as well for low droop at cutoff frequency, the device also adjusts the quick charge time along with HPF cutoff with this configuration. Table 8-8 shows the MD3 configuration and –3-dB cutoff frequency value and quick charge time.

Table 8-8. HPF Cutoff Frequency Value

MD3	–3-dB CUTOFF FREQUENCY VALUE	QUICK CHARGE TIME	-3-dB CUTTOFF FREQUENCY AT 48 kHz SAMPLE RATE
Low	0.000021 × f_S	50 ms	1 Hz
High	0.00025 × f_S	12.5 ms	12 Hz

ADVANCE INFORMATION

8.3.6.2 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled data from the multibit delta-sigma (ΔΣ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. The decimation filters in the device have Linear Phase response making them suitable for a wide variety of Audio applications.

8.3.6.2.1 Linear Phase Filters

The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

8.3.6.2.1.1 Sampling Rate: 16 kHz or 14.7 kHz

Figure 8-7 and Figure 8-8 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 16 kHz or 14.7 kHz. Table 8-9 lists the specifications for a decimation filter with a 16-kHz or 14.7-kHz sampling rate.

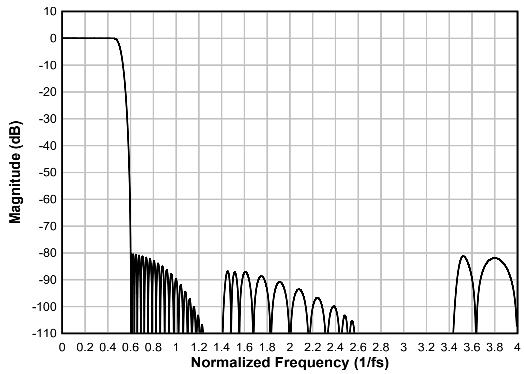


Figure 8-7. Linear Phase Decimation Filter Magnitude Response

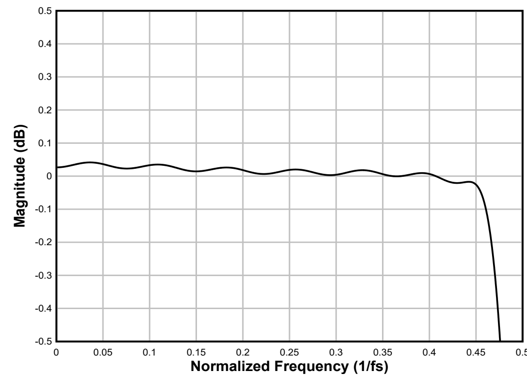


Figure 8-8. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-9. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.2			dB
	Frequency range is 4 × f_S onwards	84.7			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.1		$1/f_S$

8.3.6.2.1.2 Sampling Rate: 24 kHz or 22.05 kHz

Figure 8-9 and Figure 8-10 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 24 kHz or 22.05 kHz. Table 8-10 lists the specifications for a decimation filter with an 24-kHz or 22.05-kHz sampling rate.

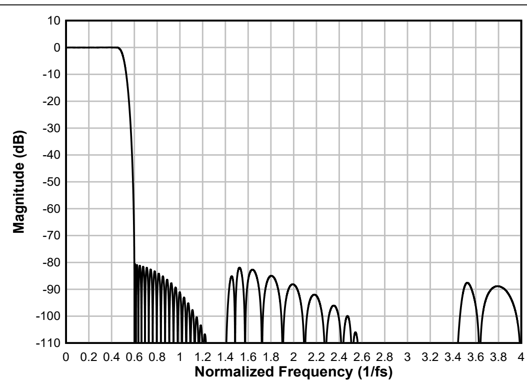


Figure 8-9. Linear Phase Decimation Filter Magnitude Response

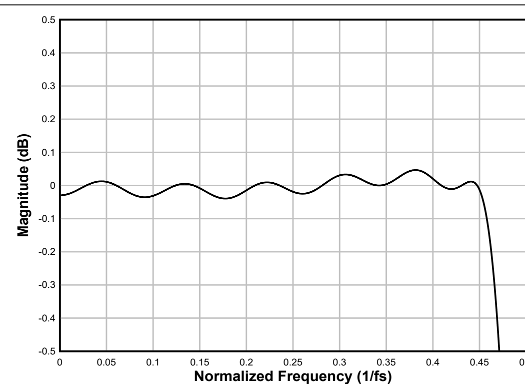


Figure 8-10. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-10. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.6			dB
	Frequency range is 4 × f_S onwards	92.9			

Table 8-10. Linear Phase Decimation Filter Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay or latency	Frequency range is 0 to 0.454 × f_S		14.7		$1/f_S$

8.3.6.2.1.3 Sampling Rate: 32 kHz or 29.4 kHz

Figure 8-11 and Figure 8-12 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 32 kHz or 29.4 kHz. Table 8-11 lists the specifications for a decimation filter with an 32-kHz or 29.4-kHz sampling rate.

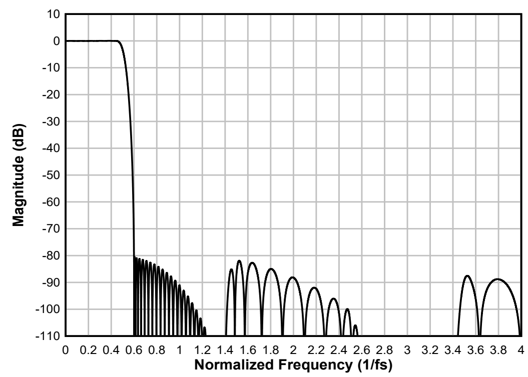


Figure 8-11. Linear Phase Decimation Filter Magnitude Response

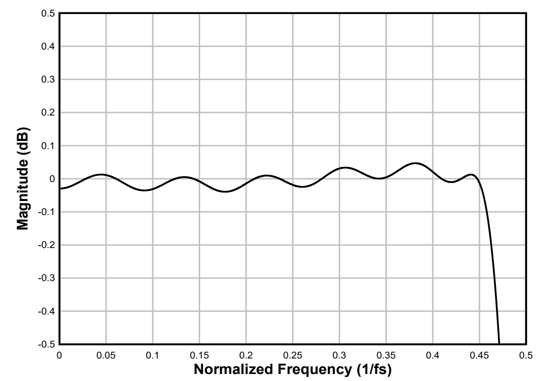


Figure 8-12. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-11. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.6			dB
	Frequency range is 4 × f_S onwards	92.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		14.7		$1/f_S$

8.3.6.2.1.4 Sampling Rate: 48 kHz or 44.1 kHz

Figure 8-13 and Figure 8-14 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 48 kHz or 44.1 kHz. Table 8-12 lists the specifications for a decimation filter with an 48-kHz or 44.1-kHz sampling rate.

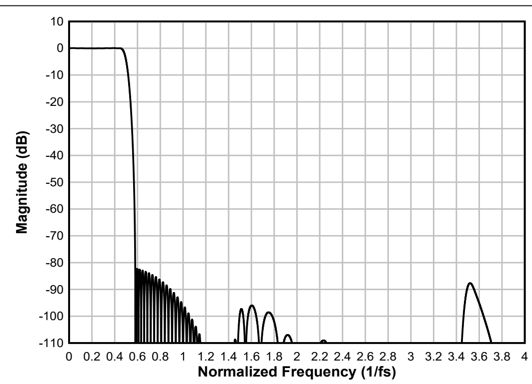


Figure 8-13. Linear Phase Decimation Filter Magnitude Response

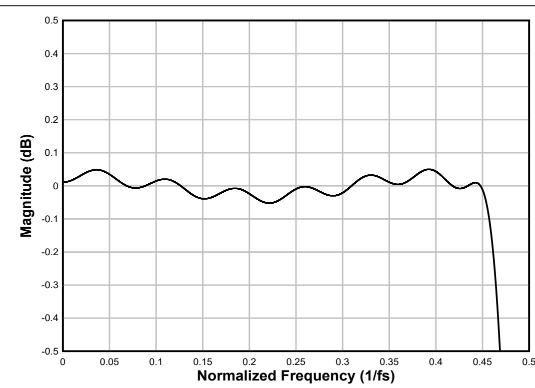


Figure 8-14. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-12. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.052		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82.2			dB
	Frequency range is 4 × f_S onwards	97.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.0		1/f_S

8.3.6.2.1.5 Sampling Rate: 96 kHz or 88.2 kHz

Figure 8-15 and Figure 8-16 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 96 kHz or 88.2 kHz. Table 8-13 lists the specifications for a decimation filter with an 96-kHz or 88.2-kHz sampling rate.

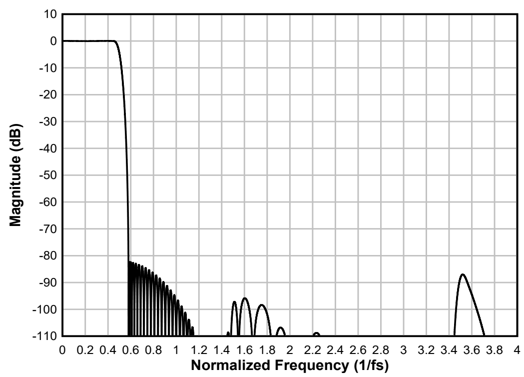


Figure 8-15. Linear Phase Decimation Filter Magnitude Response

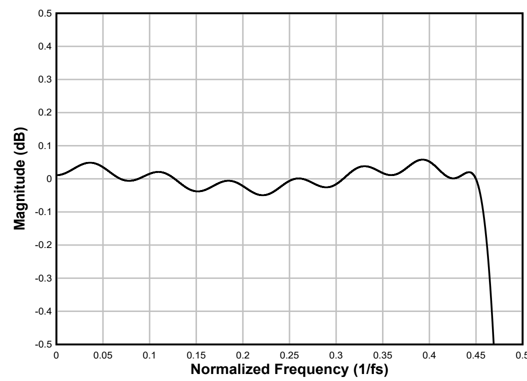


Figure 8-16. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-13. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.058	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82.2			dB
	Frequency range is 4 × f_S onwards	96.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.9		1/f_S

8.3.7 DAC Signal-Chain

Figure 8-17 shows the key components of the playback signal chain.

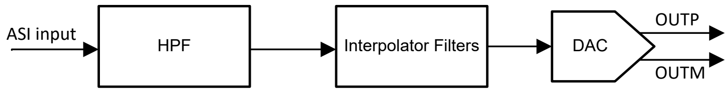


Figure 8-17. DAC Signal-Chain Processing Flowchart

The DAC signal chain offers a highly flexible low-noise playback path for low-noise and high-fidelity audio applications. This low-noise and low-distortion, multibit, delta-sigma DAC enables the TAC5142 to achieve 120 dB dynamic range in very low power. Moreover, the DAC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band. The TAC5142 also integrates, high-performance multistage digital interpolation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

8.3.7.1 Configurable Digital Interpolation Filters

The device playback channel includes a high dynamic range, built-in digital interpolation filter to process the input data stream to generate digital data stream for multibit delta-sigma (ΔΣ) modulator. The interpolation filters in the device are linear phase making them suitable for a wide variety of Audio applications. Following section describes the filter response for different samples rates.

8.3.7.1.1 Linear Phase Filters

The linear phase interpolation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

ADVANCE INFORMATION

8.3.7.1.1.1 Sampling Rate: 16 kHz or 14.7 kHz

Figure 8-18 and Figure 8-19 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 16 kHz or 14.7 kHz. Table 8-14 lists the specifications for a interpolation filter with an 16-kHz or 14.7-kHz sampling rate.

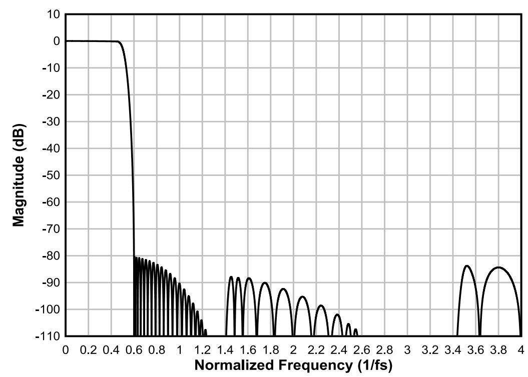


Figure 8-18. Linear Phase Interpolation Filter Magnitude Response

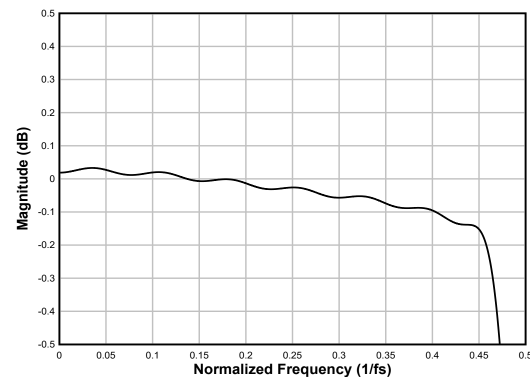


Figure 8-19. Linear Phase Interpolation Filter Pass-Band Ripple

Table 8-14. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.17		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.4			dB
	Frequency range is 4 × f_S to 7.43 × f_S	86.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.0		1/f_S

8.3.7.1.1.2 Sampling Rate: 24 kHz or 22.05 kHz

Figure 8-20 and Figure 8-21 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 24 kHz or 22.05 kHz. Table 8-15 lists the specifications for a interpolation filter with an 24-kHz or 22.05-kHz sampling rate.

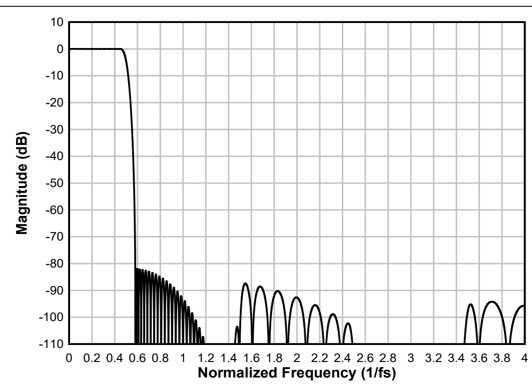


Figure 8-20. Linear Phase Interpolation Filter Magnitude Response

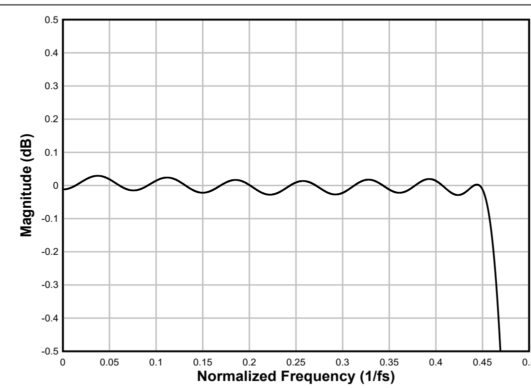


Figure 8-21. Linear Phase Interpolation Filter Pass-Band Ripple

Table 8-15. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.03	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	81.9			dB
	Frequency range is 4 × f_S to 15.42 × f_S	87.6			

Table 8-15. Linear Phase Interpolation Filter Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.6		$1/f_S$

8.3.7.1.1.3 Sampling Rate: 32 kHz or 29.4 kHz

Figure 8-22 and Figure 8-23 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 32 kHz or 29.4 kHz. Table 8-16 lists the specifications for a interpolation filter with an 32-kHz or 29.4-kHz sampling rate.

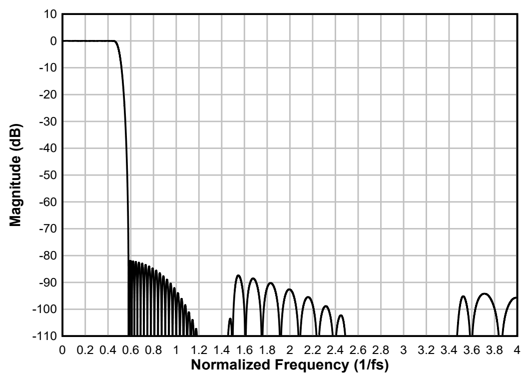


Figure 8-22. Linear Phase Interpolation Filter Magnitude Response

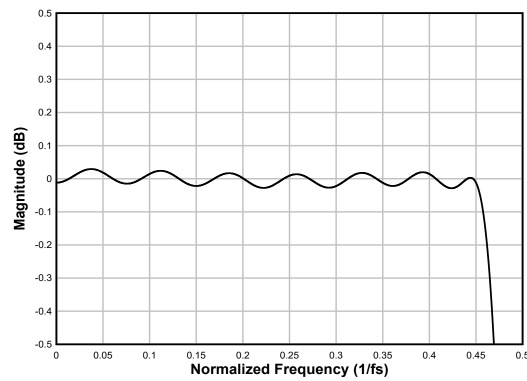


Figure 8-23. Linear Phase Interpolation Filter Pass-Band Ripple

Table 8-16. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.03	dB
Stop-band attenuation	Frequency range is 0.586 × f_S to 4 × f_S	81.9			dB
	Frequency range is 4 × f_S to 15.42 × f_S	87.6			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.6		$1/f_S$

8.3.7.1.1.4 Sampling Rate: 48 kHz or 44.1 kHz

Figure 8-24 and Figure 8-25 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 48 kHz or 44.1 kHz. Table 8-17 lists the specifications for a interpolation filter with an 48-kHz or 44.1-kHz sampling rate.

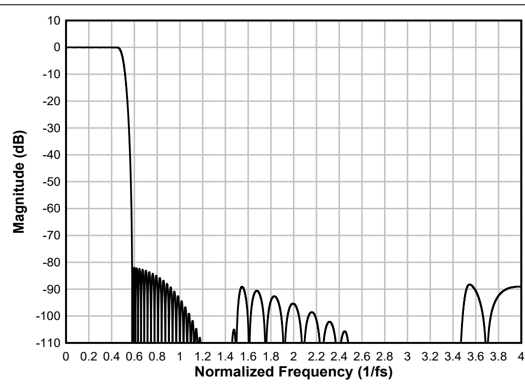


Figure 8-24. Linear Phase Interpolation Filter Magnitude Response

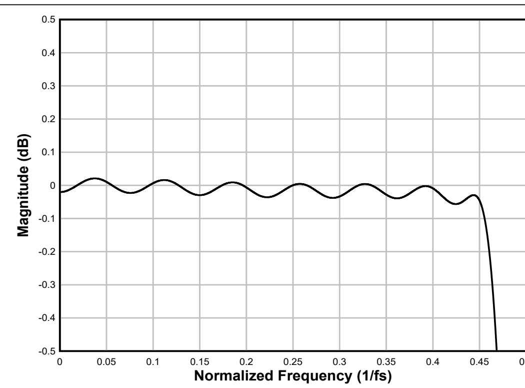


Figure 8-25. Linear Phase Interpolation Filter Pass-Band Ripple

Table 8-17. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.08		0.02	dB
Stop-band attenuation	Frequency range is 0.585 × f_S to 4 × f_S	82.0			dB
	Frequency range is 4 × f_S to 7.42 × f_S onwards	89.0			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.3		1/f_S

8.3.7.1.1.5 Sampling Rate: 96 kHz or 88.2 kHz

Figure 8-26 and Figure 8-27 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 96 kHz or 88.2 kHz. Table 8-18 lists the specifications for a interpolation filter with an 96-kHz or 88.2-kHz sampling rate.

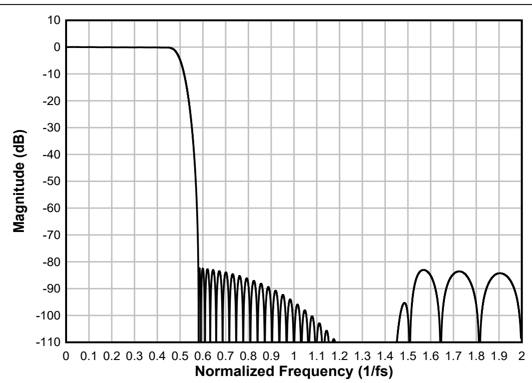


Figure 8-26. Linear Phase Interpolation Filter Magnitude Response

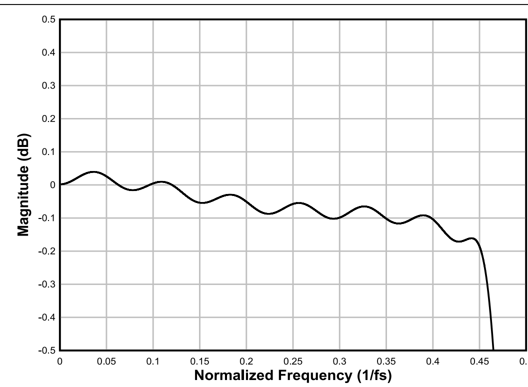


Figure 8-27. Linear Phase Interpolation Filter Pass-Band Ripple

Table 8-18. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.2		0.04	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 3.42 × f_S	82.4			dB
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.7		1/f_S

8.3.7.1.1.6 Sampling Rate: 384 kHz or 352.8 kHz

Figure 8-28 and Figure 8-29 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 384 kHz or 352.8 kHz. Table 8-19 lists the specifications for a interpolation filter with an 384-kHz or 352.8-kHz sampling rate.

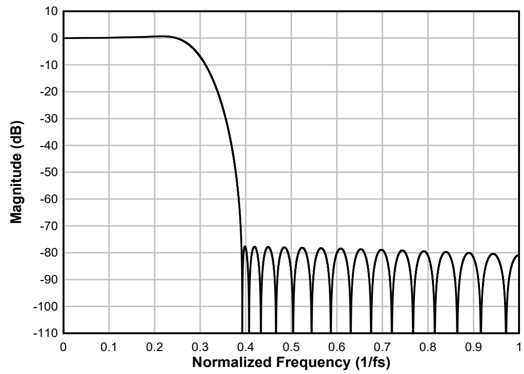


Figure 8-28. Linear Phase Interpolation Filter Magnitude Response

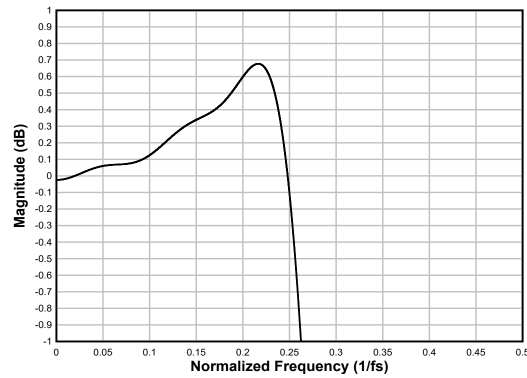


Figure 8-29. Linear Phase Interpolation Filter Pass-Band Ripple

Table 8-19. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.245 × f_S	–0.03		0.67	dB
Stop-band attenuation	Frequency range is 0.391 × f_S to 1.61 × f_S	77.6			dB
Group delay or latency	Frequency range is 0 to 0.212 × f_S		10.7		1/f_S

8.4 Device Functional Modes

8.4.1 Active Mode

The device wakes up in active mode when AVDD and IOVDD are available. Configure all hardware control pins (MD0, MD1, MD2, MD3, MD4 and MD5) for the device desired mode of operation before enabling clocks for the device.

In active mode, when the audio clocks are available, the device automatically powers up all ADC and DAC channels and starts transmitting and playing data over the audio serial interface. If the clocks are stopped, then the device auto powers down the ADC and DAC channels.

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TAC5142 is a stereo, high-performance audio Codec that supports sample rates of up to 192 kHz. The device can be configured by controlling the Pins MD0 to MD5 and can support 1.8/3.3V AVDD along with flexible Digital interfaces of I2S/TDM/LJF. The device supports stereo high dynamic range ADC with differential and single ended input support along with 2 channel differential, single ended or psuedo differential output with options for headphone and lineout drive capabilities.

9.2 Typical Application

9.2.1 Application

Figure 9-1 shows a typical configuration of the TAC5142 for an application using two channel lineout operation in an I^{2}S target audio data target interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

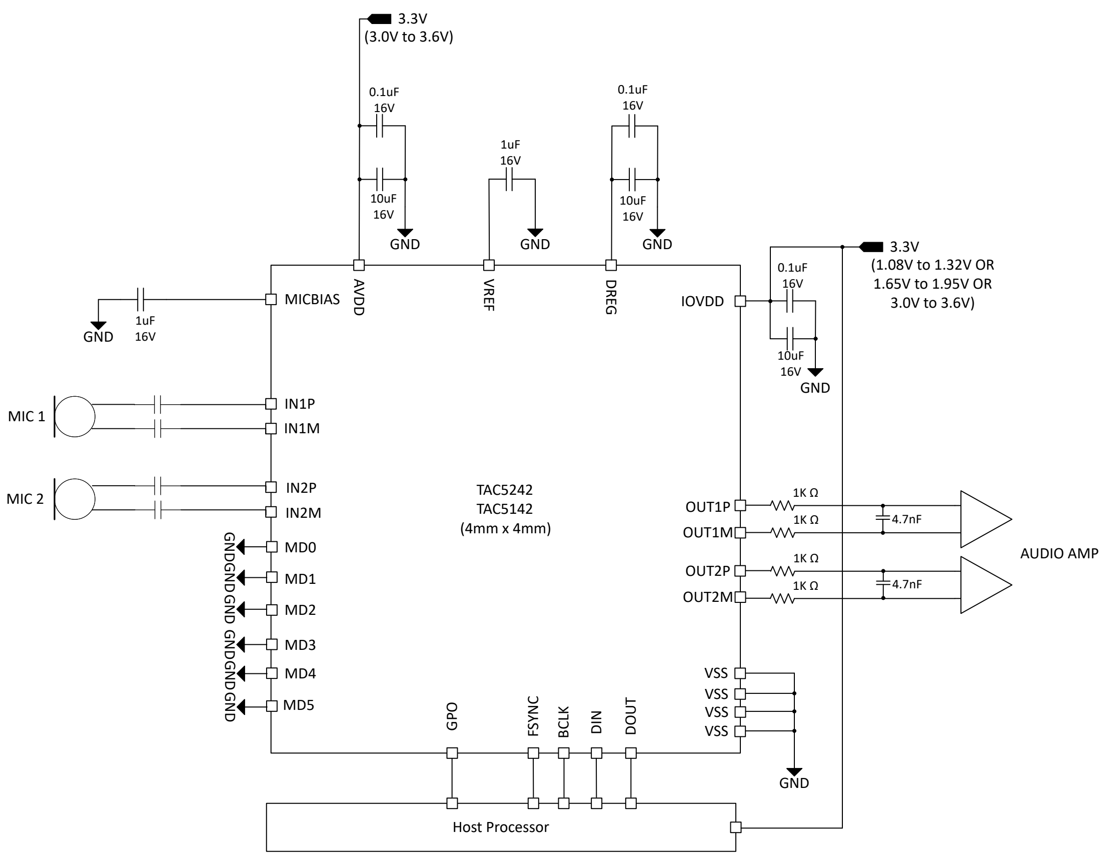


Figure 9-1. Stereo MEMS microphone with Stereo Lineout in Target I2S Mode Block Diagram

9.2.2 Design Requirements

Table 9-1 lists the design parameters for this application.

Table 9-1. Design Parameters

PARAMETER	VALUE
AVDD	3.3 V
IOVDD	1.2 V or 1.8 V or 3.3 V
AVDD supply current consumption	TBD
IOVDD supply current consumption	TBD
Maximum MICBIAS current	5 mA
Load on OUT1M, OUT1P, OUT2M, OUT2P	>600 ohms

9.2.3 Detailed Design Procedure

This section describes the necessary steps to configure the TAC5142 for this specific application.

1. Apply power to the device:
   a. Power up the IOVDD and AVDD power supplies
   b. Wait for at least 1ms to allow the device to initialize the internal registers.
   c. The device now goes into sleep mode (low-power mode < 10 µA)
2. Configure the Mode Pins as per the system requirements:
   a. Select the ASI Mode by pulling up to AVDD or down to VSS; MD0 Pin. MD0 should be grounded for this use case.
   b. Pull Up to IOVDD or Pull down to VSS on MD1 to MD5 Pin as per the reuqired configuration. All the Pins are grounded for this use case.
3. Applying the ASI Clocks will wake up the device (BCLK and FSYNC)
4. To put the device back in sleep mode, Stop the clocks:
   a. Wait at least 100 ms to allow the device to complete the shutdown sequence
   b. Change the Mode configuration by changing MD0 to MD5 as per requirement
5. Repeat step 3 and step 4 as required for mode transitions

ADVANCE INFORMATION

10 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, after all Mode pins are stable, then only initiate the clocks to initialize the device.

For the supply power-up requirement, t_1, t_2 and t_3 must be at least 2 ms to allow the device to initialize the internal registers. See the *Section 8.4* section for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement, t_4, t_5 and t_6 must be at least 10 ms. This timing (as shown in Figure 10-1) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into low power mode.

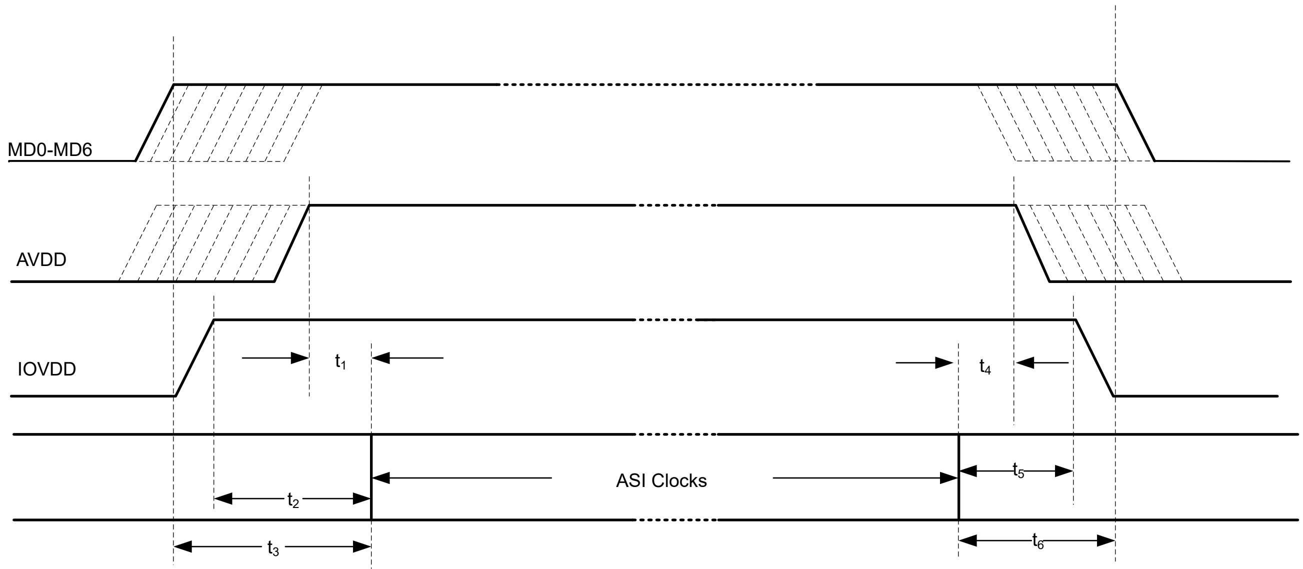


Figure 10-1. Power-Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 0.1V/µs and that the wait time between a power-down and a power-up event is at least 100 ms.

The TAC5142 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2023	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

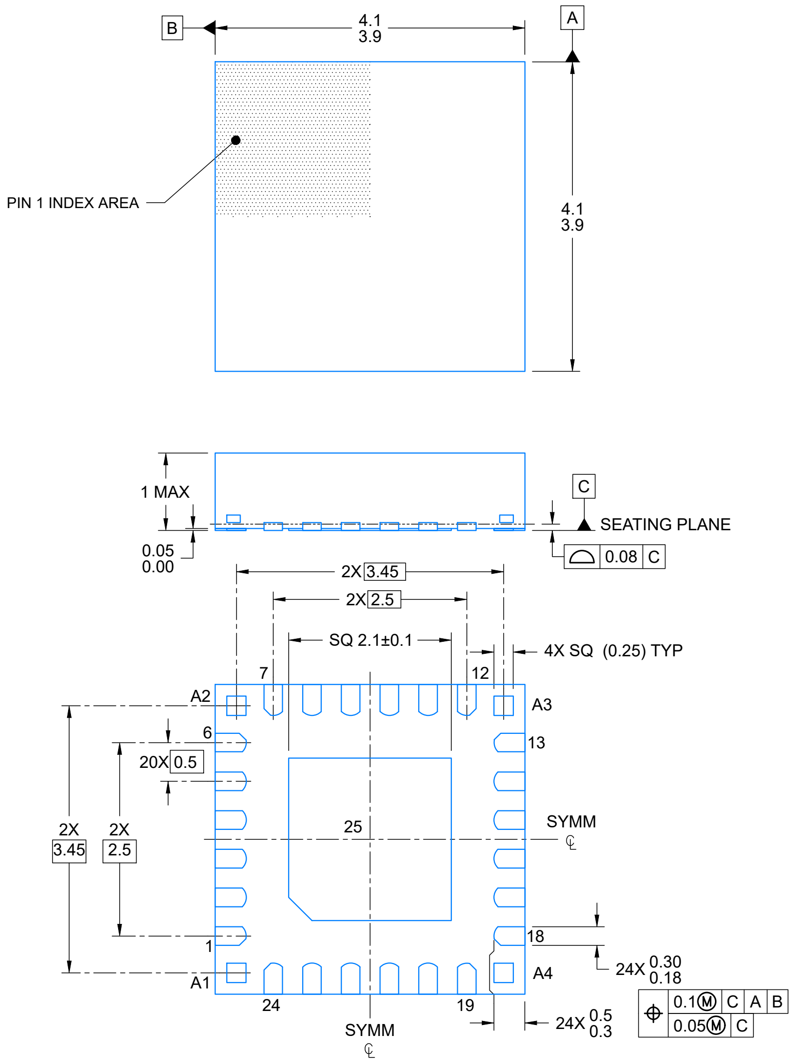
ADVANCE INFORMATION

PACKAGE OUTLINE

RGE0024R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



4225246/A 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

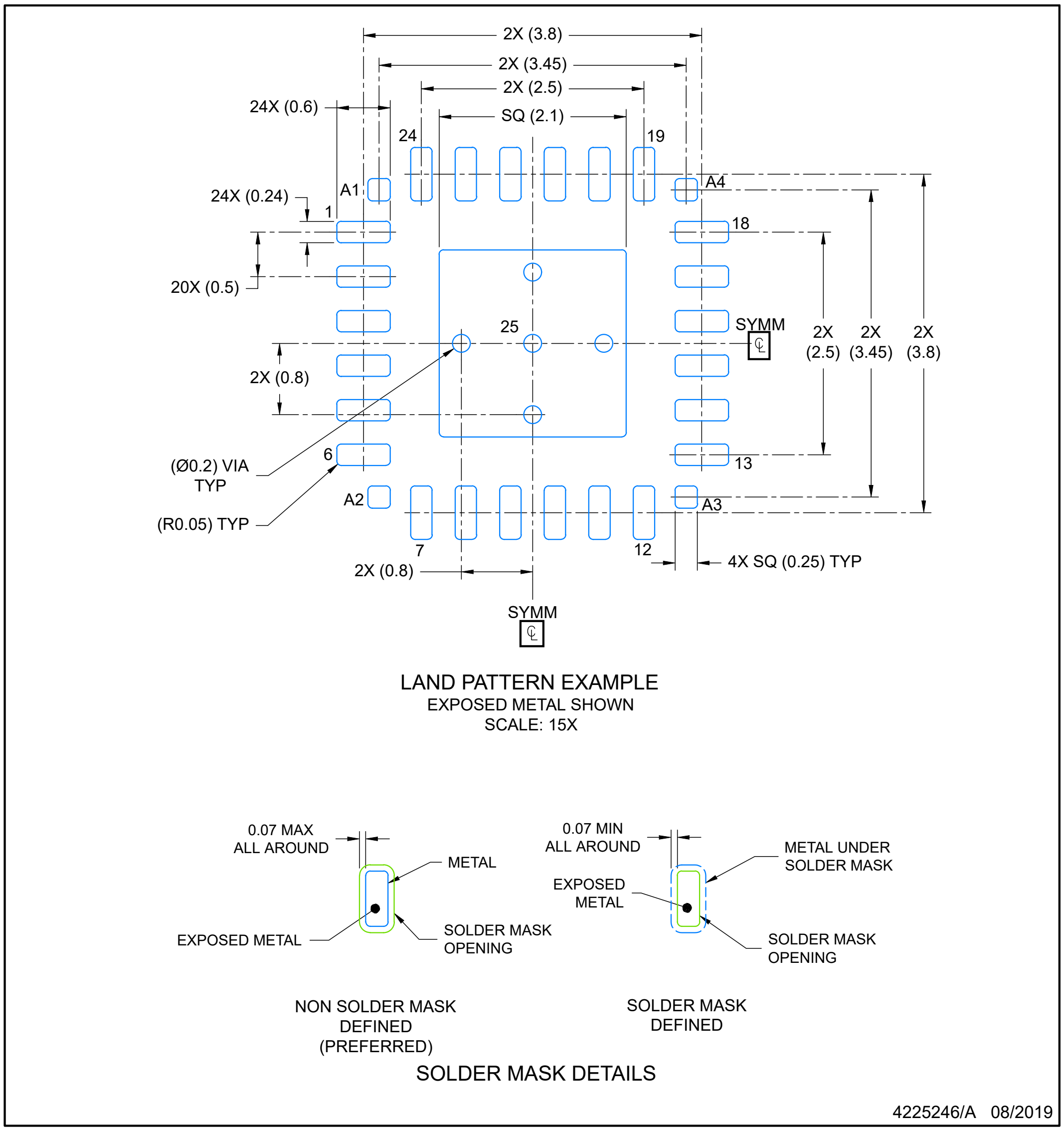
www.ti.com

EXAMPLE BOARD LAYOUT

RGE0024R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

Texas Instruments
www.ti.com

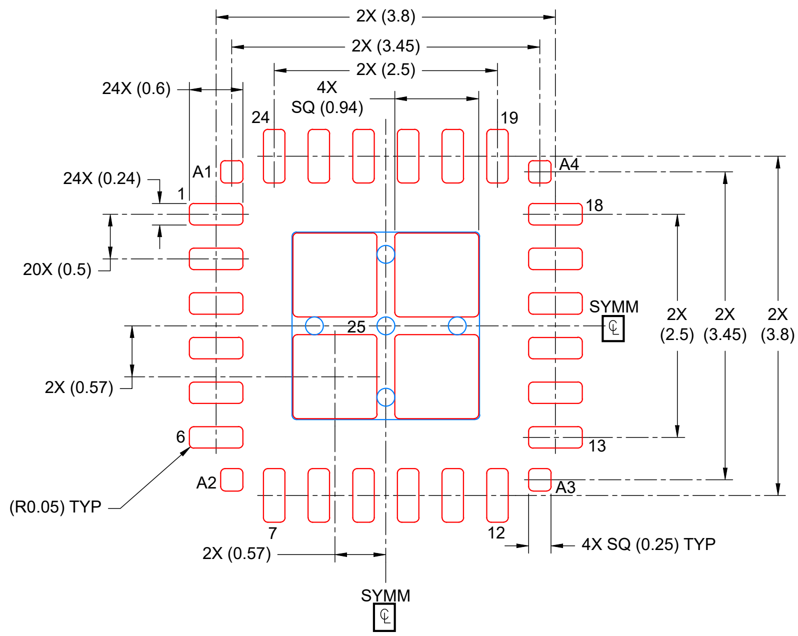
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGE0024R **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

4225246/A 08/2019

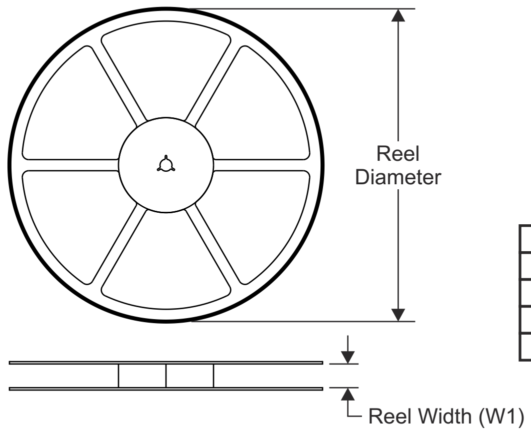
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

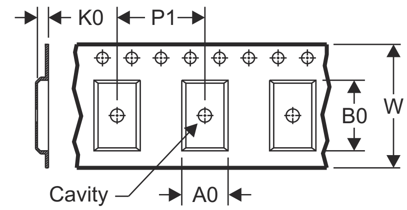
www.ti.com

13.1 Tape and Reel Information

REEL DIMENSIONS

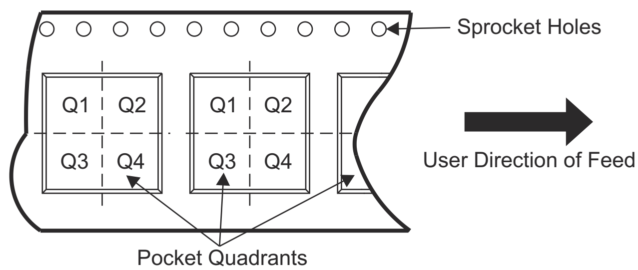


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

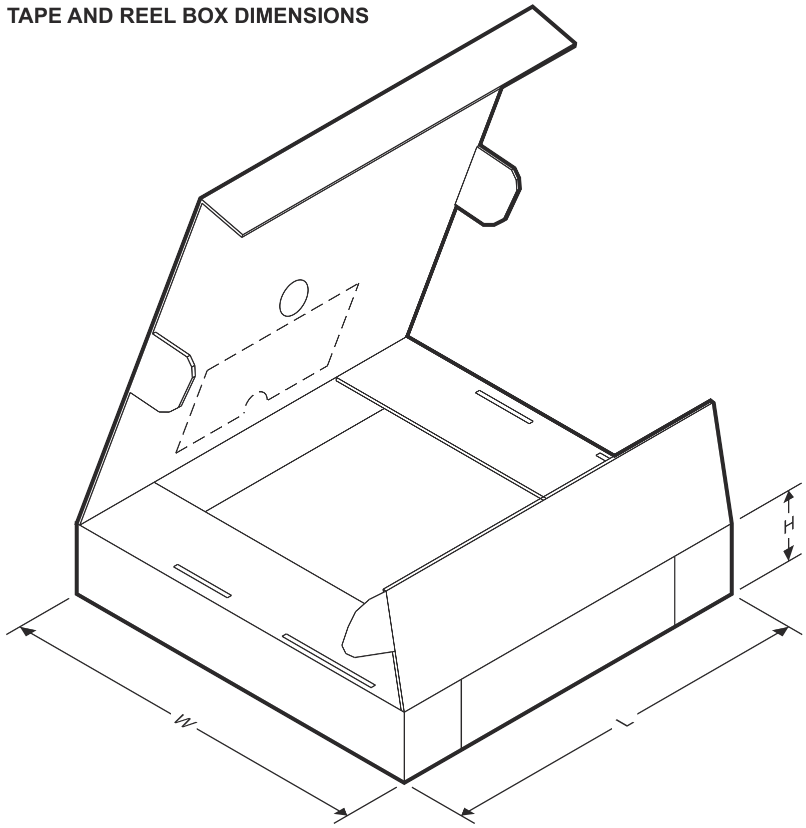
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTAC5142IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTAC5142IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTAC5142IRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

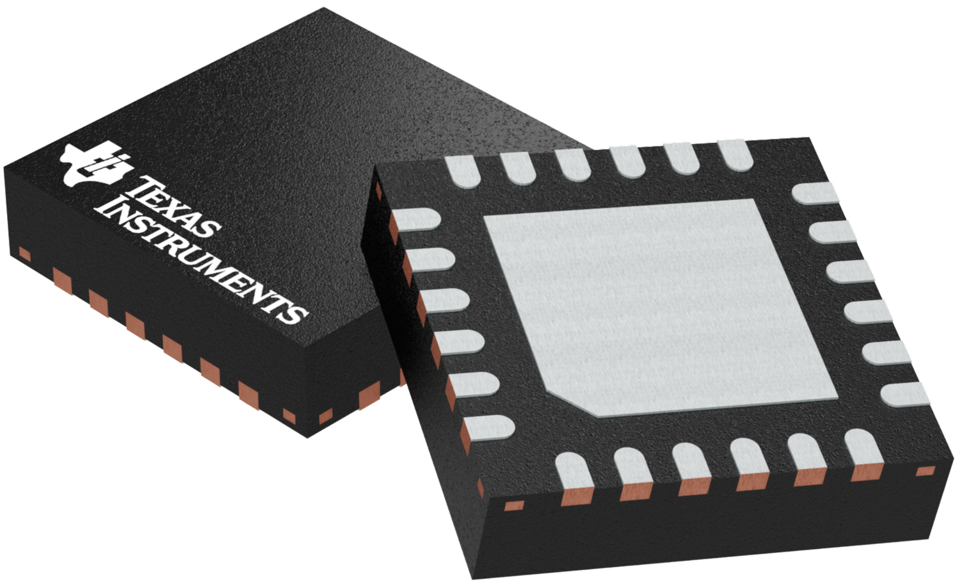
[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265