

# TAS2120 8.2W Mono Digital Input Class-D Speaker Amp with Integrated 14.75V Class-H Boost

## 1 Features

- Powerful Class-D amplifier
  - 8.2W 1% THD+N
  - 14.75V boost with 5.1A max current limit
- Best in class efficiency
  - Upto 90% efficiency at system level for 8Ω load
  - 12.9mW idle channel power, noise gate off
  - 5mW idle channel power, noise gate on
  - Integrated 1.8V Y-bridge
- High performance audio channel
  - 4.2μV A-wt. idle channel noise
  - 114dB Dynamic Range
  - 89dB THD+N
  - Low EMI performance with ERC and SSM
  - < 1μs chip to chip group delay matching
- Advanced integrated features
  - Signal detection high efficiency modes
  - High accuracy voltage monitor & temp sensor
  - Programmable battery current limit at 39mA step size
- Ease of use features
  - Hardware pin control or I<sup>2</sup>C control
  - 1S battery, 2S battery, External PVDD (3S battery) supply
  - Clock based power up/down
  - Auto clock rate detection: 16 to 192kHz
  - MCLK free operation
  - Thermal and over current protection
- Power Supplies and user interface
  - VBAT: 2.5V to 5.5V
  - VDD: 1.65V to 1.95V
  - IOVDD: 1.8V or 3.3V
  - VBAT\_SNS: 2.5V to 10.0V
  - I<sup>2</sup>S/TDM: 8 channels
  - HW pin control or I<sup>2</sup>C based control
- 26-Pin, 0.4mm Pitch, QFN package

## 2 Applications

- [Smart Speakers with Voice Assistance](#)
- [Bluetooth and Wireless speakers](#)
- [Tablets, Wearables](#)
- [Laptop, Desktop Computers](#)

## 3 Description

The TAS2120 is a mono, digital input Class-D audio amplifier with an integrated Boost for higher power delivery in battery-operated systems.

Device is optimized to deliver best battery life for real-use cases of music playback and voice calls. Advanced efficiency optimization features like Y-bridge, and algorithms enable the device to produce best-in-class efficiency across all power regions of operation. The Class-D amplifier is capable of delivering 8.2W output power using integrated Class-H Boost.

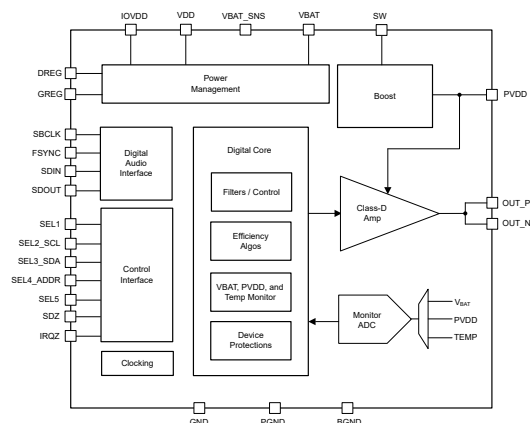
TAS2120 device supports look-ahead algorithm based optimum boost voltage levels to match the output of audio signal. This provides all the power needed for peak output while significantly reducing the average power consumption.

Up to four devices can share a common bus via I<sup>2</sup>S/TDM + I<sup>2</sup>C interfaces. The device also supports five HW Control pins that can configure the device for the desired mode of operation.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TAS2120	QFN	4mm × 3.5mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.



Functional block diagram



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## 4 Pin Configuration and Functions

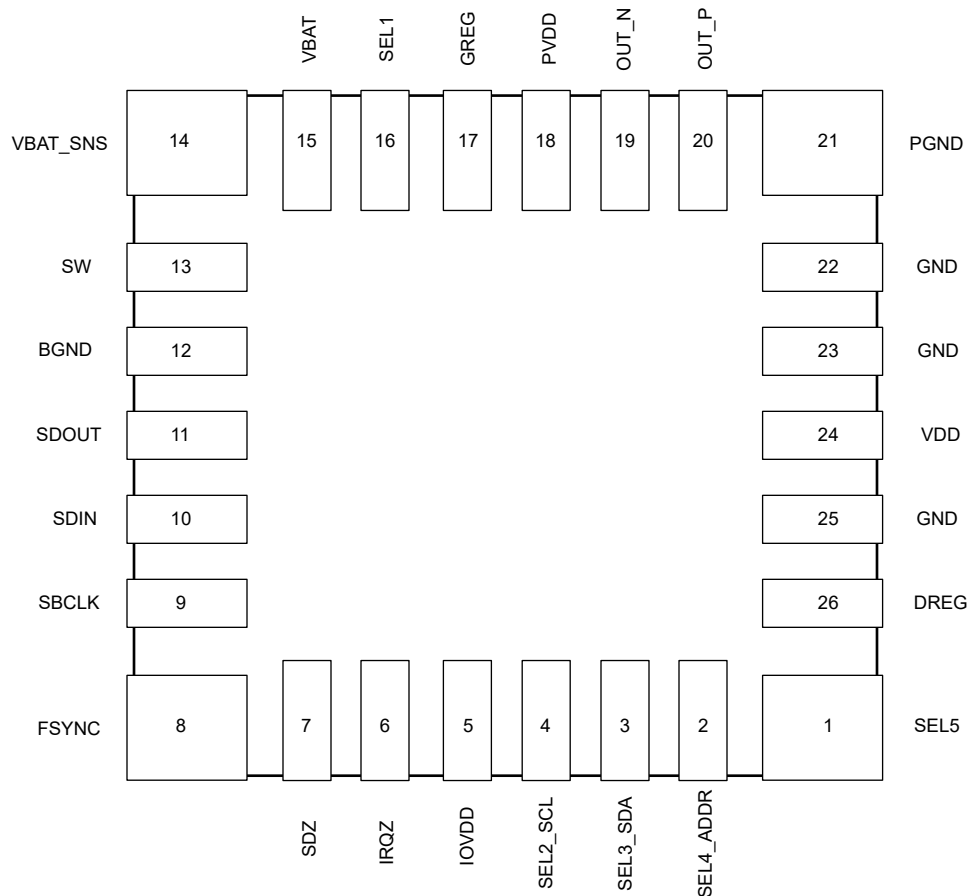


Figure 4-1. QFN Package Bottom View

### Pin Functions

PIN		Type <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
BGND	12	P	Boost ground. Connect to PCB GND plane strongly with multiple vias.
DREG	26	P	Digital core voltage regulator output. Bypass to GND with a capacitor. Do not connect to an external load.
FSYNC	8	I	I <sup>2</sup> S word clock or TDM frame sync.
GREG	17	P	High-side gate CP regulator output. Do not connect to an external load.
GND	22, 23, 25	P	Connect to PCB GND plane. Strong connection to ground plane required through multiple vias.
IOVDD	5	P	1.8V or 3.3V Digital IO supply. Decouple to GND with capacitor.
IRQZ	6	O	Open drain, active low interrupt pin. Pull up to IOVDD with resistor if optional internal pullup is not used.
OUT_N	19	O	Class-D negative output.
OUT_P	20	O	Class-D positive output.
PGND	21	P	Class-D Power stage ground. Connect to PCB GND plane strongly through multiple vias.
PVDD	18	P	Integrated boost output and Class-D power stage supply.
SBCLK	9	I	I <sup>2</sup> S/TDM serial bit clock.
SDIN	10	I	I <sup>2</sup> S or TDM serial data input.
SDOUT	11	I/O	I <sup>2</sup> S or TDM serial data output.
SDZ	7	I	Active low hardware shutdown.
SEL1	16	I	HW Mode: Select 1 Pin. Amplifier gain level selection with volume ramp enable and disable options. I <sup>2</sup> C Mode: Short to GND for I <sup>2</sup> C mode selection.
SEL2_SCL	4	I	HW Mode: Select 2 Pin. I <sup>2</sup> S, TDM, Left justified selection. I <sup>2</sup> C Mode: Clock Pin. Pull up to IOVDD with a resistor.
SEL3_SDA	3	I/O	HW Mode: Select 3 Pin. Data valid rising edge and falling edge selection. I <sup>2</sup> C Mode: Data Pin. Pull up to IOVDD with a resistor.
SEL4_ADDR	2	I	HW Mode: Select 4 Pin. Y-bridge threshold configuration setting. I <sup>2</sup> C Mode: I <sup>2</sup> C address pin.
SEL5	1	I/O	HW Mode: Select5 Pin. Boost 1S, 2S, External PVDD mode selection.
SW	13	P	Boost converter switch input.
VBAT	15	P	Battery power supply input. Connect to a 2.5 to 5.5V supply and decouple with a capacitor.
VBAT_SNS	14	I	Battery sense terminal. Connect to 1S or 2S battery supply for remote battery sensing. Ground the pin if remote sensing is not used.
VDD	24	P	Connect to 1.8V supply and decouple to GND with capacitor.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage	PVDD	-0.3	19	V
Supply Voltage	VBAT	-0.3	6	V
Supply Voltage Sense	VBAT_SNS	-0.3	12	V
Supply Voltage	VDD	-0.3	2	V
Supply Voltage	IOVDD	-0.3	6	V
Boost Switching Pin	SW	-0.7	19	V
Class-D Output	OUTP, OUTM	-0.7	19	V
High Side Drive Regulator	GREG	-0.3	PVDD + 6	V
Digital Supply Regulator	DREG	-0.3	1.65	V
Digital IO Pins	Digital pins referenced to IOVDD supply	-0.3	6	V
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2000
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins <sup>(2)</sup>	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>BAT</sub>	Battery Supply (1S Mode of operation - Default )	2.5	3.6	5.5	V
	Battery Supply (2S Mode of operation)	3	3.6	5.5	V
V <sub>BAT_SNS</sub>	Battery Sense pin voltage	2.5		10	V
V <sub>LOW_VBAT</sub>	Battery Voltage in Low volt battery mode of operation (connected to SW pin through inductor)	1.8	3.6	5.5	V
V <sub>BAT2S</sub>	2S Battery Voltage (connected to SW pin through inductor in 2S Mode of operation)	4.7	7.2	10	V
V <sub>PVDD</sub>	Amplifier Supply (External PVDD Mode)	V <sub>BAT</sub>	12	15	V
V <sub>VDD</sub>	Supply Voltage	1.65	1.8	1.95	V
V <sub>IOVDD</sub>	IO Supply Voltage 1.8V	1.62	1.8	1.98	V
V <sub>IOVDD</sub>	IO Supply Voltage 3.3V	3.0	3.3	3.6	V
R <sub>SPK</sub>	Speaker resistance	3.2	8	38.4	Ω
L <sub>SPK</sub>	Speaker inductance	5	33	100	μH
T <sub>A</sub>	Ambient temperature	-40		85	°C
T <sub>J</sub>	Junction temperature	-40		150	°C

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		Standard JEDEC <sup>(2)</sup>		UNIT
		HR-QFN		
		26 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	51.5		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	28.5		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	15.3		°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.9		°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	15.2		°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a		°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.  
(2) JEDEC Standard 4 Layer PCB

## 5.5 Electrical Characteristics

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V ( External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST\_ILIM (1S battery) = 5.1A, BST\_ILIM (2S battery, HW mode)=4.1A, BST\_ILIM (2S battery, I2C mode)=5.1A, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>AMPLIFIER PERFORMANCE - 15V INTERNAL BOOST 1S Mode</b>						
P <sub>OUT</sub>	Maximum Continuous Output Power - 1% THDN	R <sub>L</sub> = 8 Ω + 33 μH		6.6		W
		R <sub>L</sub> = 8 Ω + 33 μH, VBAT = 4.4V		8.2		W
		R <sub>L</sub> = 4 Ω + 33 μH		6.6		W
		R <sub>L</sub> = 4 Ω + 33 μH, VBAT = 4.4V		8.2		W
P <sub>OUT</sub>	Maximum Continuous Output Power - 1% THDN	R <sub>L</sub> = 8 Ω + 33 μH, HW pin control mode		6.6		W
		R <sub>L</sub> = 4 Ω + 33 μH, HW pin control mode		6.6		W
P <sub>OUT</sub>	Maximum Continuous Output Power - 10% THDN	R <sub>L</sub> = 8 Ω + 33 μH, VBAT = 4.4V		9.5		W
		R <sub>L</sub> = 4 Ω + 33 μH, VBAT = 4.4V		9.5		W
η <sub>SYSTEM_0.5W</sub>	System Efficiency at P <sub>OUT</sub> = 0.5W	R <sub>L</sub> = 8 Ω + 33 μH		84.8		%
		R <sub>L</sub> = 8 Ω + 33 μH, VBAT = 4.4V		88		%
η <sub>SYSTEM_1W</sub>	System Efficiency at P <sub>OUT</sub> = 1.0W	R <sub>L</sub> = 8 Ω + 33 μH		86.8		%
		R <sub>L</sub> = 8 Ω + 33 μH, VBAT = 4.4V		87		%
η <sub>SYSTEM_1W</sub>	System Efficiency at P <sub>OUT</sub> = 1.0W	R <sub>L</sub> = 8 Ω + 33 μH, HW pin control mode		86.8		%
		R <sub>L</sub> = 4 Ω + 33 μH, HW pin control mode		86.8		%
η <sub>SYSTEM_MAX_POUT</sub>	System Efficiency at 1% THD+N power Level	R <sub>L</sub> = 8 Ω + 33 μH		81.2		%
η <sub>SYSTEM_MAX_POUT</sub>	System Efficiency at 1% THD+N power Level	R <sub>L</sub> = 8 Ω + 33 μH, HW pin control mode		73		%
		R <sub>L</sub> = 4 Ω + 33 μH, HW pin control mode		77.4		%
V <sub>N</sub>	Idle channel Noise	A-Weighted, Gain = 6dBV (Receiver Mode), DAC-Running		4.2		μV
		A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.4		μV
DNR	Dynamic Range	A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 μH, Gain = 6dBV (Receiver Mode)		113.7		dB
		A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 μH, Gain = 21dBV (Speaker Mode)		117.2		dB

## 5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V ( External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST\_ILIM (1S battery) = 5.1A, BST\_ILIM (2S battery, HW mode)=4.1A, BST\_ILIM (2S battery, I2C mode)=5.1A, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD+N	Total Harmonic distortion + Noise	P <sub>OUT</sub> = 1 W, R <sub>L</sub> = 8 Ω + 33 μH		0.01		%
		P <sub>OUT</sub> = 1 W, R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 6.6kHz		0.01		%
		P <sub>OUT</sub> = 1 W, R <sub>L</sub> = 4 Ω + 33 μH		0.01		%
		P <sub>OUT</sub> = 0.25 W, R <sub>L</sub> = 8 Ω + 33 μH, Gain = 6dBV (Receiver Mode)		0.01		%
K <sub>CP</sub>	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes in/out of mute, power up and power down, noise gate mode entry and exit. Measured as peak A-weighted voltage. RL = 8 Ω + 33 μH, Input = digital silence		-67		dBV
BW	Amplifier input signal Bandwidth	f <sub>s</sub> ≥ 96ksps, Gain error < Pass-Band Ripple		40		kHz
V <sub>FS</sub>	Full scale equivalent Voltage	Measured at -6dBFS Input		11.22		V <sub>RMS</sub>
		Measured at -6dBFS Input, Gain = 6dBV (Receiver Mode)		2.00		V <sub>RMS</sub>
A <sub>GAIN</sub>	Audio channel Gain programmability range	Gain programmability in steps of 0.5dB	0		21	dBV
A <sub>GAIN_ER</sub>	Amplifier Gain error	P <sub>OUT</sub> = 1W		±0.1		dB
		P <sub>OUT</sub> = 0.25W, Gain = 6dBV (Receiver Mode)		±0.1		dB
V <sub>OS</sub>	Output Offset Voltage	Idle channel	-1		1	mV
		Idle channel, Gain = 6dBV (Receiver Mode)	-1		1	mV
F <sub>PWM</sub>	Class-D PWM switching Frequency	Average clock frequency		384		kHz
PSRR <sub>VB</sub> AT	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 217 Hz		115		dB
		VBAT = 3.6 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 1 kHz		115		dB
		VBAT = 3.6 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 20 kHz		85		dB
PSRR <sub>VD</sub> D	VDD power-supply rejection ratio	VDD = 1.8 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 217 Hz		110		dB
		VDD = 1.8 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 1 kHz		110		dB
		VDD = 1.8 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 20 kHz		85		dB
MUTE <sub>ATTN</sub>	Mute Attenuation	Device is MUTE mode. DAC modulator running		110		dB
<b>AMPLIFIER PERFORMANCE - INTERNAL BOOST 2S Mode</b>						
P <sub>OUT_BO</sub> OST_2S	Maximum Continuous Output Power - 10% THDN	R <sub>L</sub> = 8 Ω + 33 μH		9.8		W
P <sub>OUT_BO</sub> OST_2S	Maximum Continuous Output Power - 10% THDN	R <sub>L</sub> = 8 Ω + 33 μH, VBAT2S = 8.4V		10.5		W
η <sub>SYSTEM</sub> 0.5W_2S	System Efficiency at P <sub>OUT</sub> = 0.5W	R <sub>L</sub> = 8 Ω + 33 μH		87.0		%
		R <sub>L</sub> = 8 Ω + 33 μH, VBAT2S= 8.4V		86.2		%
		R <sub>L</sub> = 4 Ω + 33 μH		83.5		%
		R <sub>L</sub> = 4 Ω + 33 μH, VBAT2S = 8.4V		82.7		%

## 5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V ( External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST\_ILIM (1S battery) = 5.1A, BST\_ILIM (2S battery, HW mode)=4.1A, BST\_ILIM (2S battery, I2C mode)=5.1A, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
η <sub>SYSTEM_1W_2S</sub>	System Efficiency at P <sub>OUT</sub> = 1.0W	R <sub>L</sub> = 8 Ω + 33 μH		89.9		%
		R <sub>L</sub> = 8 Ω + 33 μH, VBAT2S = 8.4V		89.5		%
		R <sub>L</sub> = 4 Ω + 33 μH		86.2		%
		R <sub>L</sub> = 4 Ω + 33 μH, VBAT2S = 8.4V		85.8		%
η <sub>SYSTEM_1W_2S</sub>	System Efficiency at P <sub>OUT</sub> = 1.0W	R <sub>L</sub> = 8 Ω + 33 μH, HW pin control mode		89.9		%
		R <sub>L</sub> = 4 Ω + 33 μH, HW pin control mode		89.9		%
η <sub>SYSTEM_MAX_POUT_2S</sub>	System Efficiency at 1% THD+N power Level	R <sub>L</sub> = 8 Ω + 33 μH		85		%
		R <sub>L</sub> = 8 Ω + 33 μH, VBAT2S= 8.4V		86.5		%
		R <sub>L</sub> = 4 Ω + 33 μH		77.4		%
		R <sub>L</sub> = 4 Ω + 33 μH, VBAT2S = 8.4V		78.0		%
η <sub>SYSTEM_MAX_POUT_2S</sub>	System Efficiency at 1% THD+N power Level	R <sub>L</sub> = 8 Ω + 33 μH, HW pin control mode		85		%
		R <sub>L</sub> = 4 Ω + 33 μH, HW pin control mode		78.5		%
V <sub>N_2S</sub>	Idle channel Noise	A-Weighted, Gain = 6dBV (Receiver Mode), DAC-Running		7.0		μV
		A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.4		μV
DNR_2S	Dynamic Range	A-Weighted, -60 dBFS Method, Gain = 6dBV (Receiver Mode)		108.9		dB
		A-Weighted, -60 dBFS Method, Gain = 21dBV (Speaker Mode)		114.4		dB
THD+N_2S	Total Harmonic distortion + Noise	P <sub>OUT</sub> = 1 W, R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz		0.003		%
		P <sub>OUT</sub> = 1 W, R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz		0.003		%
		P <sub>OUT</sub> = 0.25 W, RL = 8 Ω + 33 μH, fin = 1 kHz, Gain = 6dBV (Receiver Mode)		0.005		%
K <sub>CP_2S</sub>	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes In/Out of Mute, Power Up and power Down, Noise Gate mode entry and Exit. Measured at Peak A-weighted Voltage. RL = 8 Ω + 33 μH, Input = Digital silence.		-68		dBV
PSRR <sub>VB_AT2S</sub>	VBAT2S power-supply rejection ratio	VBAT2S = 7.2 V + 200 mVpp, fripple = 217 Hz		115		dB
		VBAT2S = 7.2 V + 200 mVpp, fripple = 1 kHz		115		dB
		VBAT2S = 7.2 V + 200 mVpp, fripple = 20 kHz		90		dB
PSRR <sub>VB_AT_2S</sub>	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mVpp, f <sub>ripple</sub> = 217 Hz		115		dB
		VBAT = 3.6 V + 200 mVpp, f <sub>ripple</sub> = 1 kHz		115		dB
		VBAT = 3.6 V + 200 mVpp, f <sub>ripple</sub> = 20 kHz		90		dB
PSRR <sub>VD_D_2S</sub>	VDD power-supply rejection ratio	VDD = 1.8 V + 200 mVpp, f <sub>ripple</sub> = 217 Hz		110		dB
		VDD = 1.8 V + 200 mVpp, f <sub>ripple</sub> = 1 kHz		110		dB
		VDD = 1.8 V + 200 mVpp, f <sub>ripple</sub> = 20 kHz		90		dB
<b>AMPLIFIER PERFORMANCE - EXTERNAL PVDD Mode</b>						
P <sub>OUT_EXT_PVDD</sub>	Maximum Continuous Output Power - 1% THDN	R <sub>L</sub> = 8 Ω + 33 μH		8.3		W
		R <sub>L</sub> = 4 Ω + 33 μH		14.9		W



## 5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V ( External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST\_ILIM (1S battery) = 5.1A, BST\_ILIM (2S battery, HW mode)=4.1A, BST\_ILIM (2S battery, I2C mode)=5.1A, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>OUT_EXT_PVDD</sub>	Maximum Continuous Output Power - 1% THDN	R <sub>L</sub> = 8 Ω + 33 μH, HW pin control mode		8.3		W
P <sub>OUT_EXT_PVDD</sub>	Maximum Continuous Output Power - 10% THDN	R <sub>L</sub> = 8 Ω + 33 μH		10.3		W
		R <sub>L</sub> = 4 Ω + 33 μH		18.4		W
		R <sub>L</sub> = 4 Ω + 33 μH, PVDD=14V		24.5		W
η <sub>SYSTEM_EXT_0.5W</sub>	System Efficiency at P <sub>OUT</sub> = 0.5W	R <sub>L</sub> = 8 Ω + 33 μH		83.9		%
		R <sub>L</sub> = 4 Ω + 33 μH		80.0		%
η <sub>SYSTEM_EXT_1W</sub>	System Efficiency at P <sub>OUT</sub> = 1.0W	R <sub>L</sub> = 8 Ω + 33 μH		88.1		%
		R <sub>L</sub> = 4 Ω + 33 μH		84.2		%
η <sub>SYSTEM_EXT_1W</sub>	System Efficiency at P <sub>OUT</sub> = 1.0W	R <sub>L</sub> = 8 Ω + 33 μH, HW pin control mode		88.1		%
η <sub>SYSTEM_EXT_MAX_POUT</sub>	System Efficiency at 1% THD+N power Level	R <sub>L</sub> = 8 Ω + 33 μH		93.2		%
		R <sub>L</sub> = 4 Ω + 33 μH		88.5		%
η <sub>SYSTEM_EXT_MAX_POUT</sub>	System Efficiency at 1% THD+N power Level	R <sub>L</sub> = 8 Ω + 33 μH, HW pin control mode		93.2		%
V <sub>N_EXT</sub>	Idle channel Noise	A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.4		μV
DNR <sub>EXT</sub>	Dynamic Range	A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 μH		114.4		dB
THD+N <sub>EXT</sub>	Total Harmonic distortion + Noise	P <sub>OUT</sub> = 1 W, R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz		0.003		%
		P <sub>OUT</sub> = 1 W, R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz		0.004		%
K <sub>CP_EXT</sub>	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes In/Out of Mute, Power Up and power Down, Noise Gate mode entry and Exit. Measured at Peak A-weighted Voltage. RL = 8 Ω + 33 μH, Input = Digital Silence		-68		dBV
V <sub>OS_EXT</sub>	Output Offset Voltage	Idle channel	-1		1	mV
PSRR <sub>PVDD_EXT</sub>	PVDD power-supply rejection ratio	PVDD = 12 V + 200 mV <sub>pp</sub> , fripple = 217 Hz		115		dB
		PVDD = 12 V + 200 mV <sub>pp</sub> , fripple = 1 kHz		115		dB
		PVDD = 12 V + 200 mV <sub>pp</sub> , fripple = 20 kHz		95		dB
PSRR <sub>VBAT_EXT</sub>	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 217 Hz		115		dB
		VBAT = 3.6 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 1 kHz		115		dB
		VBAT = 3.6 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 20 kHz		90		dB
PSRR <sub>VDD_EXT</sub>	VDD power-supply rejection ratio	VDD = 1.8 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 217 Hz		110		dB
		VDD = 1.8 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 1 kHz		110		dB
		VDD = 1.8 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 20 kHz		90		dB
<b>Boost Converter</b>						
V <sub>BOOST_RANGE</sub>	Max Output Voltage programmability Range	Programmable in steps of 66mV	5.5		14.75	V
V <sub>BOOST_STEP</sub>	Class-H Output Voltage Step Size			33		mV



## 5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V ( External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST\_ILIM (1S battery) = 5.1A, BST\_ILIM (2S battery, HW mode)=4.1A, BST\_ILIM (2S battery, I2C mode)=5.1A, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>BOOST</sub>	Output Boost Voltage	I <sub>O</sub> = 0.1A. Average output value. VBOOST_MAX_CTRL = max value		14.9		V
I <sub>BOOST_CL</sub>	Peak Input Current Limit	BST_ILIM = Max Setting		5.1		A
I <sub>BOOST_CL</sub>	Peak Input Current Limit	BST_ILIM = Min Setting		1.5		A
	Peak Input Current Limit Programmable step size			39.1		mA
<b>Boost Converter 2S Mode of operation</b>						
V <sub>BOOST_RANGE</sub>	Output Voltage Range	Programmable in steps of 66mV	10		14.75	V
V <sub>BOOST_STEP</sub>	Class-H Output Voltage Step Size			33		mV
I <sub>BOOST_CL</sub>	Peak Input Current Limit	Max Setting		5.1		A
I <sub>BOOST_CL</sub>	Peak Input Current Limit	Min Setting		1.5		A
<b>TDM Serial Port</b>						
	PCM Sample Rates and FSYNC Input Frequency		16		192	kHz
	SBCLK Input Frequency	I <sup>2</sup> S/TDM Operation	0.512		24.57	MHz
	SBCLK Maximum Input Jitter	RMS Jitter below 40 kHz that can be tolerated without performance degradation			0.5	ns
		RMS Jitter above 40 kHz that can be tolerated without performance degradation			5	ns
	SBCLK Cycles per FSYNC in I <sup>2</sup> S and TDM Modes	Values: 64, 96, 128, 192, 256, 384 and 512	64		512	Cycles
<b>PCM Playback Characteristics to fs ≤ 48 kHz</b>						
fs	Sample Rates		16		48	kHz
	Audio Channel Passband LPF Corner	Ripple < pass-band ripple		0.454		fs
	Audio Channel Passband Ripple	20 Hz to LPF cutoff		± 0.1		dB
	Audio Channel Stop Band Attenuation	≥ 0.55 fs		60		dB
		≥ 1 fs		65		dB
	Audio Channel Group Delay	Fin = 1kHz, Class-H mode		31.5		1/fs
		Fin = 1kHz, Class-H bypassed		6.5		1/fs
		DC to 20kHz, HPF bypassed, Class-H bypassed		11.0		1/fs
		DC to 20kHz, HPF bypassed, Class-H mode		37.0		1/fs
<b>PCM Playback Characteristics to fs &gt; 48 kHz</b>						
fs	Sample Rates		88.2		192	kHz
	Audio Channel Passband LPF Corner	fs = 96 kHz		0.469		fs
		fs = 192 kHz		0.234		fs
	Audio Channel Passband Ripple	20 Hz to LPF cutoff		± 0.2		dB

## 5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V ( External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST\_ILIM (1S battery) = 5.1A, BST\_ILIM (2S battery, HW mode)=4.1A, BST\_ILIM (2S battery, I2C mode)=5.1A, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Audio Channel Stop Band Attenuation	fs = 96 kHz, fin ≥ 0.55 fs		60		dB
		fs = 96 kHz, fin ≥ 1 fs		65		dB
		fs = 192 kHz, 0.55 fs ≥ fin ≥ 0.275 fs		60		dB
	Audio Channel Group Delay	fin=1kHz, fs=96 kHz, Class-H mode		56.7		1/fs
		DC to 40kHz, fs=96 kHz, HPF Bypassed, Class-H bypassed		8.6		1/fs
		DC to 40kHz, fs=192 kHz, HPF Bypassed, Class-H Mode		117.8		1/fs
<b>Sense Circuits</b>						
	Temperature Measurement Range		-40		150	°C
	Temperature Measurement Resolution			2		°C
	Temperature Measurement Accuracy	Measured at 25C		±2.5		°C
	VBAT Measurement Range	VBAT pin			6	V
		VBAT_SNS pin			12	V
	VBAT Measurement Resolution	VBAT pin		1.25		mV
		VBAT_SNS pin		2.5		mV
	VBAT Measurement Accuracy	VBAT pin, measured at 3.6V		±25		mV
		VBAT_SNS pin, measured at 7.2V		±50		mV
	PVDD Measurement Range				18	V
	PVDD Measurement Resolution			3.75		mV
	PVDD Measurement Accuracy			±75		mV
<b>Protection Circuits</b>						
	Thermal shutdown temperature			140		°C
	Thermal shutdown retry time			1.5		s
	VBAT undervoltage lockout threshold (UVLO)	UVLO is asserted	1.9			V
		UVLO is released			2.3	V
	VDD undervoltage lockout threshold (UVLO)	UVLO is asserted	1.4			V
		UVLO is released			1.6	V
	PVDD undervoltage lockout threshold (UVLO)	UVLO is asserted, external PVDD mode only	2.6			V
		UVLO is released, external PVDD mode only			2.8	V
	PVDD overvoltage lockout threshold (OVLO)	OVLO is asserted, OVLO protection enabled.		16		V
	Output Short circuit protection	Output to Output, Output to GND, Output to PVDD, Output to VBAT, H-bridge mode		4.1		A
<b>Power up/down Time</b>						
T <sub>STDBY</sub>	Turn ON time from SDZ Asserted to device ready for i2c Command				300	us
T <sub>ACTIVE</sub>	Turn ON time from release of Software Shutdown to Amplifier output Active	Volume ramping disabled		1.6		ms
		Volume ramping enabled		3.9		ms
T <sub>TURNOFF</sub>	Turn OFF time from assertion of Software Shutdown to Amplifier output Hi-Z	Volume ramping disabled		0.2		ms
		Volume ramping enabled		13.9		ms

## 5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V ( External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST\_ILIM (1S battery) = 5.1A, BST\_ILIM (2S battery, HW mode)=4.1A, BST\_ILIM (2S battery, I2C mode)=5.1A, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Current Consumption - Internal Boost Mode</b>						
I <sub>Q_HW_SD</sub>	Current consumption in Hardware Shutdown	VBAT, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA
I <sub>Q_SW_SD</sub>	Current consumption in Software Shutdown	VBAT, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA
I <sub>Q_NG</sub>	Current consumption in Idle channel	VBAT, P <sub>OUT</sub> = 0, Noise Gate enabled		0.19		mA
		VDD, P <sub>OUT</sub> = 0, Noise Gate enabled		2.3		mA
		IOVDD, P <sub>OUT</sub> = 0, Noise Gate enabled		0.1		mA
		Total Power, P <sub>OUT</sub> = 0, Noise Gate enabled		4.8		mW
I <sub>Q_IDLE</sub>	Current consumption in Idle channel	VBAT, P <sub>OUT</sub> = 0, Noise gate disabled		0.62		mA
		VDD, P <sub>OUT</sub> = 0, Noise gate disabled		5.7		mA
		IOVDD, P <sub>OUT</sub> = 0, Noise gate disabled		0.1		mA
		Total Power, P <sub>OUT</sub> = 0, Noise gate disabled		12.5		mW
<b>Current Consumption - Internal Boost Mode 2S Mode</b>						
I <sub>Q_HW_SD</sub>	Current consumption in Hardware Shutdown	VBAT, SDZ=0		0.1		uA
		VBAT2S, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA
I <sub>Q_SW_SD</sub>	Current consumption in Software Shutdown	VBAT, All clocks Stopped		0.1		uA
		VBAT2S, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA
I <sub>Q_NG</sub>	Current consumption in Idle channel	VBAT, P <sub>OUT</sub> = 0, Noise gate enabled		0.2		mA
		VBAT2S, P <sub>OUT</sub> = 0, Noise gate enabled		0.1		mA
		VDD, P <sub>OUT</sub> = 0, Noise gate enabled		2.3		mA
		IOVDD, P <sub>OUT</sub> = 0, Noise gate enabled		0.1		mA
		Total Power, P <sub>OUT</sub> = 0, Noise gate enabled		5.1		mW
I <sub>Q_IDLE</sub>	Current consumption in Idle Channel	VBAT, P <sub>OUT</sub> = 0, Noise gate disabled		0.5		mA
		VBAT2S, P <sub>OUT</sub> = 0, Noise gate disabled		0.35		mA
		VDD, P <sub>OUT</sub> = 0, Noise gate disabled		5.9		mA
		IOVDD, P <sub>OUT</sub> = 0, Noise gate disabled		0.1		mA
		Total Power, P <sub>OUT</sub> = 0, Noise gate disabled		14.9		mW

## 5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V ( External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST\_ILIM (1S battery) = 5.1A, BST\_ILIM (2S battery, HW mode)=4.1A, BST\_ILIM (2S battery, I2C mode)=5.1A, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>Q_IDLE</sub>	Current consumption in Idle Channel, , HW pin control mode	VBAT, P <sub>OUT</sub> = 0, Noise gate disabled				mA
		VBAT2S, P <sub>OUT</sub> = 0, Noise gate disabled				mA
		VDD, P <sub>OUT</sub> = 0, Noise gate disabled				mA
		IOVDD, P <sub>OUT</sub> = 0, Noise gate disabled				mA
		Total Power, P <sub>OUT</sub> = 0, Noise gate disabled				mW
<b>Current Consumption - External PVDD Mode</b>						
I <sub>Q_HW_SD</sub>	Current consumption in Hardware Shutdown	PVDD, SDZ=0		1		uA
		VBAT, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA
I <sub>Q_SW_SD</sub>	Current consumption in Software Shutdown	PVDD, All clocks Stopped		1		uA
		VBAT, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA
I <sub>Q_NG</sub>	Current consumption in Idle channel	PVDD, P <sub>OUT</sub> = 0, Noise gate enabled		0.1		mA
		VBAT, P <sub>OUT</sub> = 0, Noise gate enabled		0.15		mA
		VDD, P <sub>OUT</sub> = 0, Noise gate enabled		2.2		mA
		IOVDD, P <sub>OUT</sub> = 0, Noise gate enabled		0.1		mA
		Total Power, P <sub>OUT</sub> = 0, Noise gate enabled		5.3		mW
I <sub>Q_IDLE</sub>	Current consumption in Idle channel	PVDD, P <sub>OUT</sub> = 0, Noise gate disabled		0.2		mA
		VBAT, P <sub>OUT</sub> = 0, Noise gate disabled		0.5		mA
		VDD, P <sub>OUT</sub> = 0, Noise gate disabled		5.6		mA
		IOVDD, P <sub>OUT</sub> = 0, Noise gate disabled		0.1		mA
		Total Power, P <sub>OUT</sub> = 0, Noise gate disabled		14.0		mW
I <sub>Q_IDLE</sub>	Current consumption in Idle channel, , HW pin control mode	PVDD, P <sub>OUT</sub> = 0, Noise gate disabled				mA
		VBAT, P <sub>OUT</sub> = 0, Noise gate disabled				mA
		VDD, P <sub>OUT</sub> = 0, Noise gate disabled				mA
		IOVDD, P <sub>OUT</sub> = 0, Noise gate disabled				mA
		Total Power, P <sub>OUT</sub> = 0, Noise gate disabled				mW
<b>DIGITAL I/Os</b>						
V <sub>IH</sub>	High-level digital input logic voltage threshold	All digital pins		0.7 x IOVDD		V
V <sub>IL</sub>	Low-level digital input logic voltage threshold	All digital pins			0.3 x IOVDD	V
V <sub>OH</sub>	High-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I <sub>OH</sub> = 100μA		IOVDD - 0.2 V		V
V <sub>OL</sub>	Low-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I <sub>OL</sub> = -100μA			0.2	V
V <sub>OL(I2C)</sub>	Low-level digital output voltage	SDA and SCL; I <sub>OL</sub> = -1mA			0.2 x IOVDD	V

## 5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V ( External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST\_ILIM (1S battery) = 5.1A, BST\_ILIM (2S battery, HW mode)=4.1A, BST\_ILIM (2S battery, I2C mode)=5.1A, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OL(IRQZ)</sub>	Low-level digital output voltage for open drain output	IRQZ pin; I <sub>OL</sub> = -1mA			0.2	V
I <sub>IH</sub>	Input logic-high leakage for digital inputs	All digital pins; Input = IOVDD.	-1		1	μA
I <sub>IL</sub>	Input logic-low leakage for digital inputs	All digital pins; Input = GND	-1		1	μA
C <sub>IN</sub>	Input capacitance for digital inputs	All digital pins		5		pF
R <sub>PD</sub>	Pull down resistance for digital input/IO pins when asserted on	All digital pins. Pull down resistance option enabled		18		kΩ

## 5.6 Timing Requirements

T<sub>A</sub> = 25 °C, VDD = IOVDD = 1.8 V (unless other wise noted)

		MIN	NOM	MAX	UNIT
<b>I2C - Standard-Mode</b>					
f <sub>SCL</sub>	SCL clock frequency	0		100	kHz
t <sub>HD,STA</sub>	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			μs
t <sub>LOW</sub>	LOW period of the SCL clock	4.7			μs
t <sub>HIGH</sub>	HIGH period of the SCL clock	4			μs
t <sub>SU,STA</sub>	Setup time for a repeated START condition	4.7			μs
t <sub>HD,DAT</sub>	Data hold time: For I <sup>2</sup> C bus devices	0		3.45	μs
t <sub>SU,DAT</sub>	Data set-up time	250			ns
t <sub>r</sub>	SDA and SCL rise time			1000	ns
t <sub>f</sub>	SDA and SCL fall time			300	ns
t <sub>SU,STO</sub>	Set-up time for STOP condition	4			μs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	4.7			μs
C <sub>b</sub>	Capacitive load for each bus line			400	pF
<b>I2C - Fast-Mode</b>					
f <sub>SCL</sub>	SCL clock frequency	0		400	kHz
t <sub>HD,STA</sub>	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			μs
t <sub>LOW</sub>	LOW period of the SCL clock	1.3			μs
t <sub>HIGH</sub>	HIGH period of the SCL clock	0.6			μs
t <sub>SU,STA</sub>	Setup time for a repeated START condition	0.6			μs
t <sub>HD,DAT</sub>	Data hold time: For I <sup>2</sup> C bus devices	0		0.9	μs
t <sub>SU,DAT</sub>	Data set-up time	100			ns
t <sub>r</sub>	SDA and SCL rise time	20 + 0.1 × C <sub>b</sub>		300	ns
t <sub>f</sub>	SDA and SCL fall time	20 + 0.1 × C <sub>b</sub>		300	ns
t <sub>SU,STO</sub>	Set-up time for STOP condition	0.6			μs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	1.3			μs
C <sub>b</sub>	Capacitive load for each bus line			400	pF
<b>I2C - Fast-Mode Plus</b>					
<b>TDM Port</b>					

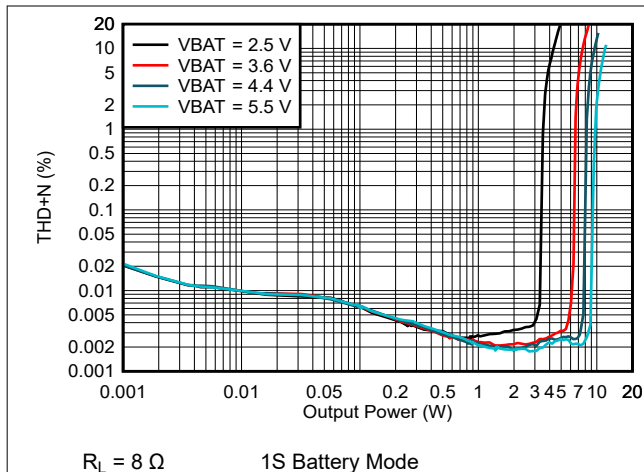
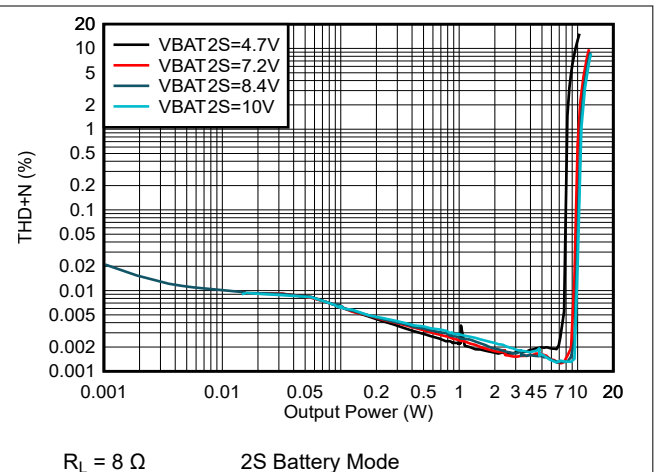
## 5.6 Timing Requirements (continued)

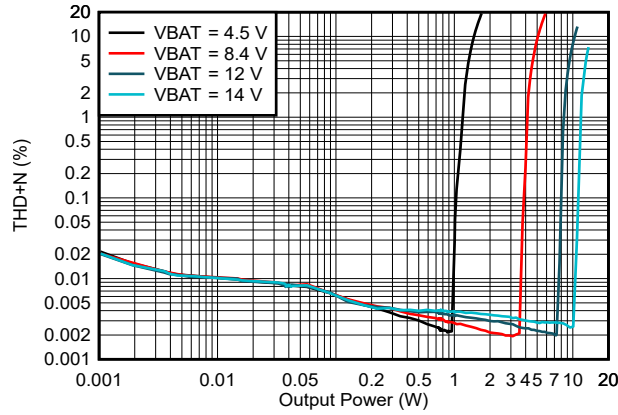
 $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = I_{OVDD} = 1.8\text{ V}$  (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_H$ (SBCLK)	SBCLK high period	20			ns
$t_L$ (SBCLK)	SBCLK low period	20			ns
$t_{SU}$ (FSYNC)	FSYNC setup time	8			ns
$t_{HLD}$ (FSYNC)	FSYNC hold time	8			ns
$t_{SU}$ (SDIN/ICC)	SDIN/ICC setup time	8			ns
$t_{HLD}$ (SDIN/ICC)	SDIN/ICC hold time	8			ns
$t_d$ (SDO/ICC-SBCLK)	SBCLK to SDOOUT/ICC delay : 50% of SBCLK to 50% of SDOOUT IOVDD=1.8V			13	ns
$t_d$ (SDO/ICC-SBCLK)	SBCLK to SDOOUT/ICC delay : 50% of SBCLK to 50% of SDOOUT IOVDD=3.3V			30	ns
$t_r$ (SBCLK)	SBCLK rise time : 10 % - 90 % Rise Time			8	ns
$t_f$ (SBCLK)	SBCLK fall time : 90 % - 10 % Rise Time			8	ns

## 5.7 Typical Characteristics

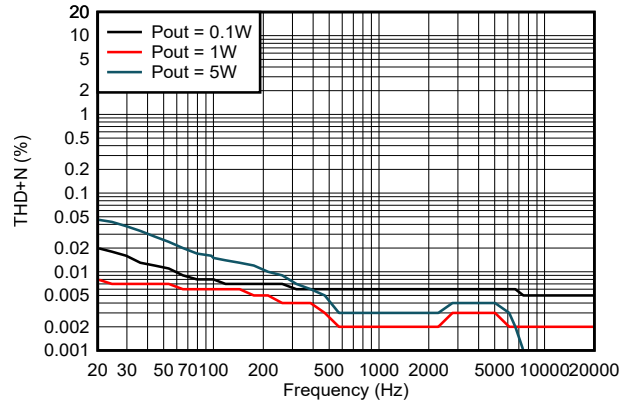
$T_A = 25\text{ }^\circ\text{C}$ ,  $V_{BAT} = 3.6\text{ V}$ ,  $V_{BAT2S} = 7.2\text{ V}$  (2S mode enabled),  $PVDD = 12\text{ V}$  (External PVDD mode enabled),  $V_{DD} = 1.8\text{ V}$ ,  $I_{OVDD} = 1.8\text{ V}$ , Load =  $8\text{ }\Omega + 33\text{ }\mu\text{H}$ , LBOOST =  $1\text{ }\mu\text{H}$ ,  $F_{IN} = 1\text{ kHz}$ ,  $F_s = 48\text{ kHz}$ , Gain = 21dBV, BST\_ILIM (1S Boost mode) = 5.1A, BST\_ILIM (2S Boost mode) = 4.1A, SDZ=1, Noise gate mode disabled, Measured filter free with an Audio Precision with a 22Hz to 20kHz un-weighted bandwidth, unless otherwise noted.


**Figure 5-1. THD+N vs Output Power**

**Figure 5-2. THD+N vs Output Power**



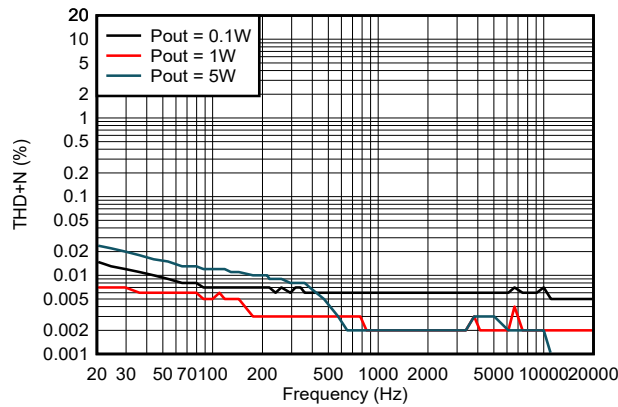
$R_L = 8 \Omega$  External PVDD mode

Figure 5-3. THD+N vs Output Power



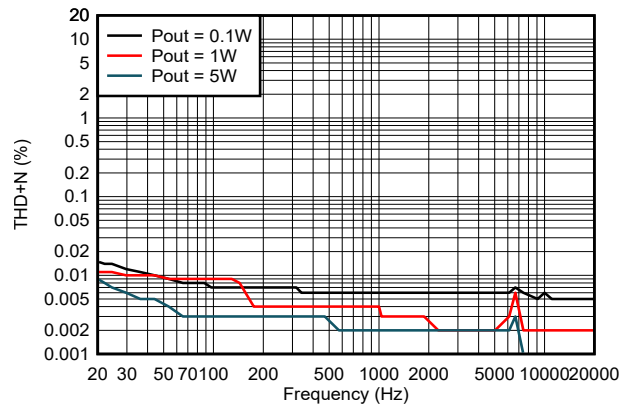
$R_L = 8 \Omega$  VBAT = 3.6 V 1S Battery Mode

Figure 5-4. THD+N vs Frequency



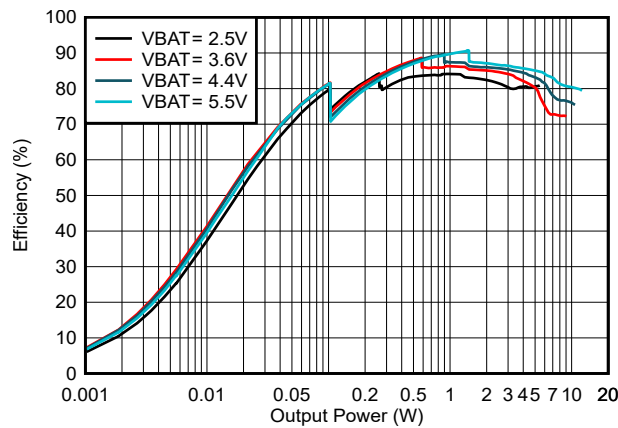
$R_L = 8 \Omega$  VBAT2S = 7.2 V 2S Battery mode

Figure 5-5. THD+N vs Frequency



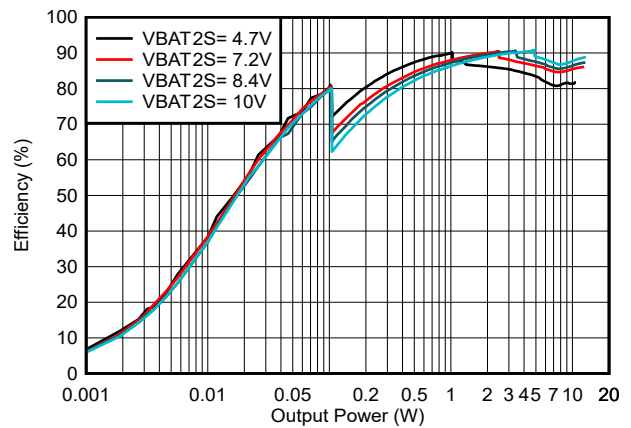
$R_L = 8 \Omega$  PVDD = 12 V External PVDD mode

Figure 5-6. THD+N vs Frequency



$R_L = 8 \Omega$  1S Battery Mode

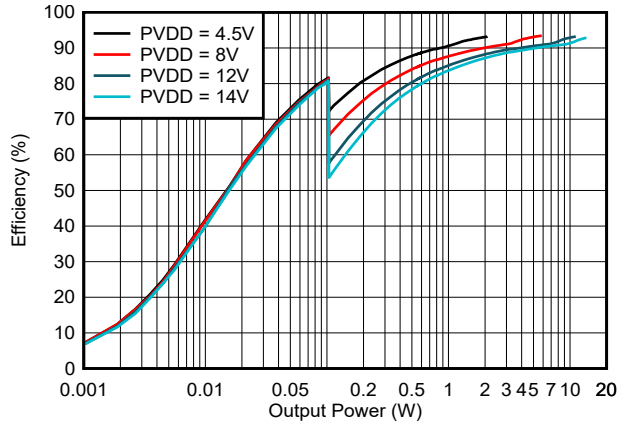
Figure 5-7. Efficiency vs Output Power



$R_L = 8 \Omega$  2S Battery mode

Figure 5-8. Efficiency vs Output power





$R_L = 8 \Omega$

External PVDD mode

Figure 5-9. Efficiency vs Output Power

## 6 Detailed Description

### 6.1 Overview

The TAS2120 is a mono digital input Class-D amplifier optimized for delivering the highest efficiency across all powers for longer battery life operation. It comes with a small solution size for board space-constrained applications. It integrates Class-H Boost with 33mV step size resolution for class-H control, highly accurate speaker voltage and current sensors, and battery/temperature sensors for system-level protection features.

### 6.2 Functional Block Diagram

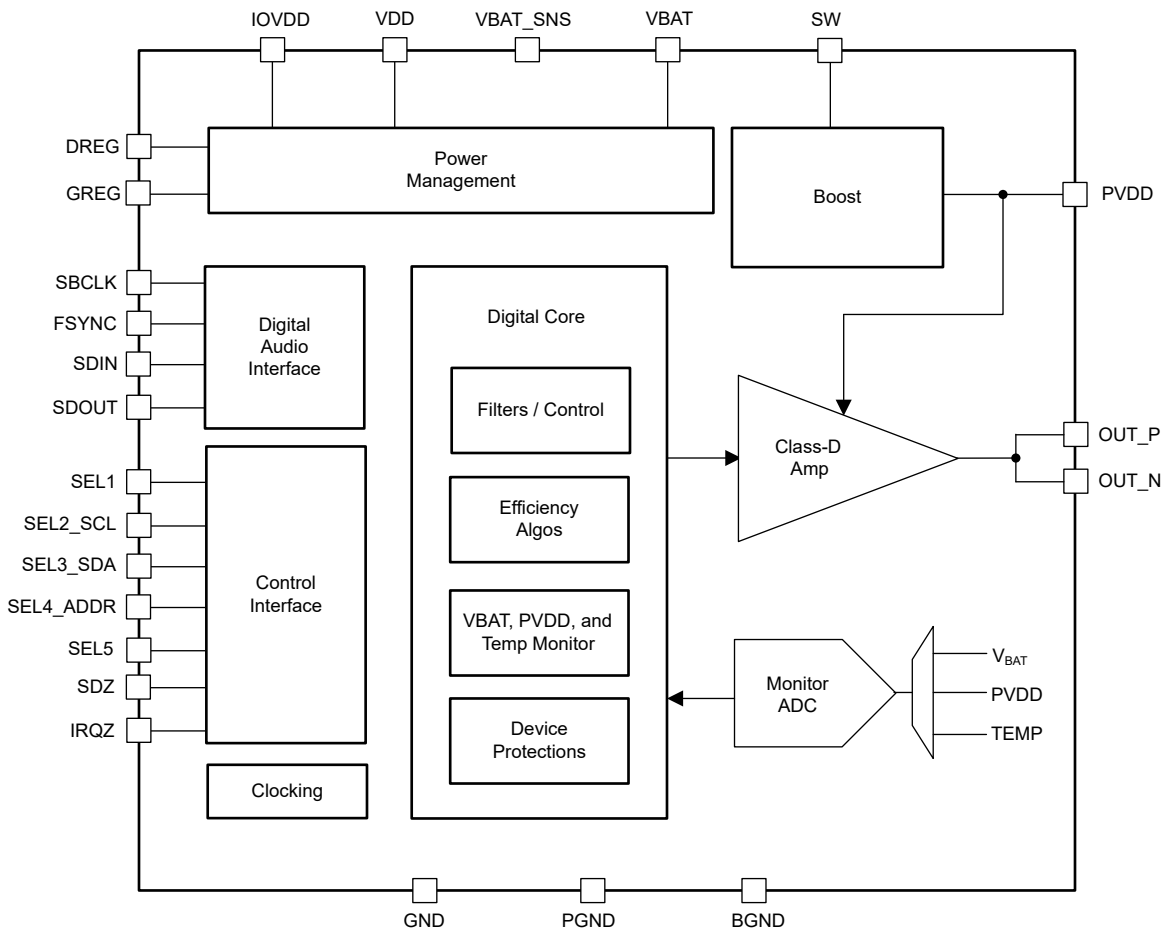


Figure 6-1. Top Level Functional block diagram

### 6.3 Device Functional Modes

#### 6.3.1 Operational Modes

##### 6.3.1.1 Hardware Shutdown

The device can be powered down by asserting SDZ pin low. The shutdown behavior of the device when SDZ pin is pulled low is controlled by SDZ\_MODE register settings.

In Hardware Shutdown mode (SDZ\_MODE[1:0] = 00 or 01) if the SDZ pin is asserted low, the device consumes the minimum quiescent current from VDD and VBAT supplies. All registers lose state in this mode and go back to default settings, and I<sup>2</sup>C communication is disabled.

If configured in SDZ\_MODE[1:0] = 00, when the SDZ pin is asserted low while audio is playing, the device will follow the normal power down sequencing like volume ramp down on the audio (if enabled), stop the Class-D

switching, power down analog and digital blocks to ensure no power down pop and finally put the device into Hardware Shutdown mode. I2C communication is disabled while the SDZ pin is asserted low in this mode.

If configured in SDZ\_MODE[1:0] = 01, when the SDZ pin is asserted low the device will immediately enter the hardware shutdown and will not go through any power-down sequencing routine. It is recommended to ensure that the audio input signal is ramped down to the idle channel before asserting the SDZ pin low in this mode (device software mute mode can be used to realize this). I2C communication is disabled while the SDZ pin is asserted low in this mode.

Finally, the device can be configured to Software shutdown mode by setting SDZ\_MODE[1:0] = 10. In this mode, when the SDZ pin is pulled low, the device will follow normal power-down sequencing and enter software shutdown mode. All the device register configuration programmed is retained as is from the state the device was in before the SDZ pin was pulled low. I2C communication is still available while the SDZ pin is asserted low in this mode.

**Table 6-1. Shutdown Control**

SDZ_MODE[1:0]	Configuration
00 (default)	Hardware shutdown mode with power-down sequencing
01	Hardware shutdown mode - immediate
10	Software shutdown mode (All register values retained)
11	Reserved

When SDZ\_MODE[1:0] is 00 or 10, the device goes through shutdown sequencing and the SDZ pin must be held low for the entire duration of the shutdown time. The shutdown time is specified in the Power up/down Time section of the Electrical Characteristics section. When SDZ is released, the device will sample the AD1 and AD2 pins and enter the software shutdown mode.

### 6.3.1.2 Hardware Config Modes

The device can operate in a pre-configured HW Mode depending on the terminations used for Select pin1 to Select Pin5. HW Mode behavior of the device is designed to simplify device configuration without using any software based configurations through I<sup>2</sup>C communication.

**Table 6-2. SEL1 HW Mode configuration**

SEL1 Connection	Configuration
Direct Short to GND	I <sup>2</sup> C Mode selection
1.2k to GND	6dBV Amp Gain, Volume ramp disabled
1.2k to Supply	12dBV Amp Gain, Volume ramp disabled
5k to GND	18dBV Amp Gain, Volume ramp disabled
330 to Supply	21dBV Amp Gain, Volume ramp disabled
4.7k to Supply	6dBV Amp Gain, Volume ramp enabled
24k to GND	12dBV Amp Gain, Volume ramp enabled
24k to Supply	18dBV Amp Gain, Volume ramp enabled
Direct Short to Supply	21dBV Amp Gain, Volume ramp enabled

**Table 6-3. SEL2 HW Mode configuration**

SEL2_SCL Connection	Configuration
Direct Short to GND	I <sup>2</sup> S L or TDM0
470 to Supply	I <sup>2</sup> S R or TDM1
Direct Short to Supply	I <sup>2</sup> S (L+R)/2 or TDM2
1.2k to GND	Left-Justified L or TDM3
1.2k to Supply	Left-Justified R or TDM4
4.7k to GND	Left-Justified (L+R)/2 or TDM5
4.7k to Supply	I <sup>2</sup> S L+Tx or TDM6
24k to GND	I <sup>2</sup> S R+Tx or TDM7
24k to Supply	Reserved

**Table 6-4. SEL3 HW Mode configuration**

SEL3_SDA Connection	Configuration
Direct Short to GND	Data valid on rising edge
Direct Short to Supply	Data valid on falling edge

**Table 6-5. SEL4 HW Mode configuration**

SEL4_ADDR Connection	Configuration
Direct Short to GND	Y-bridge threshold of 80mW
Direct Short to Supply	Y-bridge threshold of 40mW
24k to Supply	Y-bridge threshold of 1mW

**Table 6-6. SEL5 HW Mode configuration**

SEL5_CLASSH Connection	Configuration
Direct Short to GND	1S Battery Mode, Boost ON
Direct Short to Supply	External PVDD (3S Battery) Mode
24k to Supply	2S Battery Mode, Boost ON

### 6.3.1.3 Software Power Modes Control and Software Reset

The TAS2120 power state can be controlled using the register MODE[1:0]. Change in any of the MODE settings will not cause the device to lose any of the existing device configuration register settings.

**Active state:** When MODE[1:0] is configured as '00', the device enters an active mode of operation with proper power-up sequencing to minimize the click and pop.

**Software shutdown state:** When MODE[1:0] is configured as '10', the device enters software shutdown mode. This mode powers down all analog blocks required to playback audio but does not cause the device to lose register state. If audio is playing when Software Shutdown is asserted, the Class-D will volume ramp down before shutting down. When de-asserted, the Class-D will begin switching and volume ramp back to the programmed digital volume setting.

**Clock based Active and shutdown state:** When MODE[1:0] is configured as '11' the device toggles between Active and Shutdown state based on valid ASI clock signals applied on the ASI input pins, BCLK and FSYNC. When clocks are applied, the device will automatically detect the clock signals and follow proper power-up sequencing to avoid any power-up click and pop. When the audio channels are powered up and the ASI clock is removed, the device will automatically start power-down sequencing and avoid any click and pop. It is recommended to do a volume ramp-down in the input data stream before stopping the clocks for the best pop & click experience (device software mute mode can be used to realize this).

**Table 6-7. Software Mode Control**

MODE[1:0]	Configuration
00	Device in active mode of operation
01	Reserved
10 (default)	Device in software shutdown mode
11	Device in Clock based Active and shutdown mode

TAS2120 can be reset to its default configuration by setting the SW\_RESET register to '1'. If the device is powered up, when the SW\_RESET bit is set high, all the channels are powered down immediately. All the registers are restored to the default state when SW\_RESET is set high. This bit is self-clearing and goes back to '0' once the reset is complete.

The device can also signal to the host once the status of the device reaches Active mode of operation using the INT\_LTCH0[1] bit (Section 6.3.2). This bit is a live device status bit and reflects the device status in real-time. This bit is set high when the device is in Active mode and set low when the device is in shutdown mode.

#### 6.3.1.4 Efficiency and power saving modes

TAS2120 has multiple power-saving modes of operation designed to achieve the highest system level efficiency under all operating conditions. The device transitions from one mode to the next based on the configured mode and the signal condition. The transitions from one mode to another are automatic and designed to ensure high-performance audio levels during the transition of the modes.

EFFICIENCY\_MODE[1:0] register allows for configuration of the Music efficiency and Noise gate modes of operation

##### 6.3.1.4.1 Noise Gate

When the Noise gate feature is enabled, the device automatically detects periods of silence during active playback mode and reduces the idle channel power consumption significantly to extend the battery life. This feature is useful for signals playback having long periods of silence, eg voice calls, movie tracks, etc.

The device monitors the input audio signal level against the programmed Noise gate threshold configured by the NG\_TH\_LVL[2:0] register. When the audio signal falls below the threshold, an internal Hysteresis timer is enabled. If the signal level remains below the configured NG\_TH\_LVL[2:0] for the entire duration of the NG\_HYST\_TIMER[1:0], the device enters into the Noise gate mode and reduces the idle channel power consumption. In the Noise gate mode of operation, the high switching blocks like class-D PWM output are turned OFF and outputs are pulled low. The output impedance of class-D can be controlled when the Noise gate mode is active using the CLASSD\_HIZ\_MODE register. While the Noise gate mode is active, class-D outputs are not switching and the device does not produce any audio output signal. When the device is in Noise gate mode, the NG\_STATUS bit is set as high and when the device comes out of noise gate mode, the status bit is set to low.

When the signal level increases above the NG\_TH\_LVL[1:0], the device automatically wakes up the blocks in low IQ mode and starts playing out the audio input signals. The wake up from Noise gate maintains the signal fidelity by buffering the input signal data during the transition time from noise gate mode to active playback mode. The device does not lose any audio input samples while transitioning from noise gate to active playback.

The transition into noise gate mode and recovery out of noise gate mode is designed to be click and pop-free by following the proper shutdown and power up sequencing.

**Table 6-8. Noise gate threshold**

<i>NG_TH_LVL[2:0]</i>	Configuration
000	-85 dBFs
001	-90 dBFs
010	-95 dBFs
011	-100 dBFs
100 (default)	-105 dBFs
101	-110 dBFs
110	-115 dBFs
111	-120 dBFs

**Table 6-9. Noise gate hysteresis timer**

<i>NG_HYST_TIMER[1:0]</i>	Configuration
00	10 ms
01 (default)	50 ms
10	100 ms
11	1000 ms

#### 6.3.1.4.2 Music Efficiency Mode

When the Music efficiency mode feature is enabled, the device automatically detects low-power signal states during active playback mode and reduces the overall  $I_Q$  power consumption to extend the battery life. This feature is useful for dynamic audio signals with varying signal levels for example music tracks, voice calls movie tracks, and so forth.

The device monitors the input audio signal level against the programmed Music efficiency threshold configured by the *MUSIC\_EFF\_MODE\_THR[23:0]* register. When the audio signal falls below the threshold, an internal hysteresis timer is enabled. If the signal level remains below the configured *MUSIC\_EFF\_MODE\_THR[23:0]* for the entire duration of the *MUSIC\_EFF\_MODE\_TIMER[23:0]*, the device enters into the Music efficiency mode. When the device is in Music efficiency mode, the *MUSIC\_EFF\_STATUS* bit is set as high and when the device comes out of music efficiency mode, the status bit is set low.

When the signal level increases above the *MUSIC\_EFF\_MODE\_THR[23:0]*, the device automatically wakes up the blocks in low  $I_Q$  mode and continues playing out the audio input signals. The transition from Music efficiency mode to normal operation occurs with minimal click and pop. While the device is in Music efficiency mode, the audio channel performance is maintained and doesn't impact the output signal level or noise.

The *MUSIC\_EFF\_MODE\_THR[23:0]* and *MUSIC\_EFF\_MODE\_TIMER[23:0]* registers can be configured using the PPC3 Software [Section 6.4.1](#).

#### 6.3.1.4.3 VDD Y-bridge

TAS2120 uses a Y-bridge output stage for switching the class-D output PWM voltage between the VDD and PVDD supply. When the feature is enabled using *EN\_Y\_BRIDGE\_MODE* set to high, the device will automatically select the output voltage to switch the output PWM at. When the signal level is low, the output will switch at VDD to enable higher system-level efficiency by reducing the class-D output switching voltage. When the signal level is high, the output switches on the PVDD voltage rail set by the integrated Boost, or external PVDD in the external PVDD mode of operation.

The device monitors the input audio signal level against the programmed Y-bridge mode threshold configured by *VDD\_MODE\_THR\_LVL[23:0]* register. When the audio signal falls below the threshold, an internal hysteresis timer is enabled. If the signal level remains below the configured *YBRIDGE\_HYST\_TIMER[1:0]* for the entire duration of the selected time, the device enters into the lower voltage VDD supply-based PWM switching mode.

When the signal level increases above the  $VDD\_MODE\_THR\_LVL[23:0]$  plus  $VDD\_MODE\_HYST[23:0]$ , the device starts switching the output PWM signal on PVDD supply without introducing any signal clipping.

The  $VDD\_MODE\_THR\_LVL[23:0]$  and  $VDD\_MODE\_HYST[23:0]$  registers can be configured using the PPC3 Software [Section 6.4.1](#).

**Table 6-10. VDD Y-bridge hysteresis timer**

$YBRIDGE\_HYST\_TIMER[1:0]$	Configuration
00	100us
01 (default)	500us
10	5ms
11	50ms

**Table 6-11. VDD Y-bridge enable**

$EN\_Y\_BRIDGE\_MODE$	Configuration
0	Y-bridge mode is disabled
1 (default)	Y-bridge mode is enabled

#### 6.3.1.4.4 Class-H Boost

TAS2120 has an advanced class-H algorithm to control the integrated Boost. The class-H algorithm enables Boost supply to closely track audio signal levels and achieve high system level efficiency for extending battery life. Class-H mode is enabled using the  $BST\_MODE[1:0]$  register.

The class-H algorithm buffers the input signal to enable sufficient look-ahead time required to charge the Boost output capacitor and avoid any signal clipping. The algorithm monitors the input signal level and uses system-level parameters configured in PPC3 software like Boost output voltage, Boost output capacitor, channel gain, and so forth, and computes the most optimum class-H tuning parameters. These tuning parameter registers are then calculated in the PPC3 software and configured in the corresponding  $CLASSH\_TUNING\_x[23:0]$  registers.

When the  $BST\_MODE[1:0]$  is configured to use the device in Class-G mode or Boost always-ON mode, the max inrush current from the battery can be controlled by setting the Inrush current parameter in PPC3 software. The software generates the required coefficients in the  $CLASSH\_TUNING\_x[23:0]$  register based on the system level parameters configured like Boost output capacitor, Inrush current required, and so forth.

#### 6.3.1.5 2S Battery Mode

TAS2120 can be configured to function for different battery systems like single series cell (1S) Li-ion battery (2.5 V to 5.5 V) or 2-series cell (2S) series cell battery (4.7 V to 10 V). When the 2S battery is selected for the device, the diagram below shows the conceptual connections in the system to connect the 2S battery. When selected for 2S battery operation, the VBAT pin of the device is used for biasing internal blocks and needs to be supplied from external power source between 3.0 V to 5.5 V.

The internal battery voltage monitor needs to be switched to sense the voltage on the VBAT\_SNS pin instead of the default sensing done on the VBAT pin.  $SEL\_VBAT\_MODE[1:0]$  configures the internal voltage monitor and the device configuration between 1S or 2S battery systems.

When  $SEL\_VBAT\_MODE[1:0]$  is set as '10', ie 2S mode of operation, the device internal bias voltage needs to be configured based on  $VBAT\_BIAS\_SELx$  registers. If the VBAT pin voltage is available from the center tap or half of the 2S battery voltage, the  $VBAT\_BIAS\_SEL1$  needs to be set high. For other VBAT voltage configurations the  $VBAT\_BIAS\_SEL1$  should be set low and appropriate  $VBAT\_BIAS\_SEL2$  configuration should be selected.



**Table 6-12. Battery mode selection**

<i>SEL_VBAT_MODE[1:0]</i>	Configuration
00 (default)	Voltage monitor on VBAT pin. 1S mode of operation
01	Voltage monitor on VBAT_SNS pin. 1S mode of operation
10	Voltage monitor on VBAT_SNS pin. 2S mode of operation
11	Reserved

**Table 6-13. VBAT pin bias voltage selector**

<i>VBAT_BIAS_SEL1</i>	Configuration
0 (default)	VBAT pin biasing based on <i>VBAT_BIAS_SEL2</i> register
1	VBAT pin voltage is half of 2S battery voltage

**Table 6-14. VBAT pin bias voltage selector**

<i>VBAT_BIAS_SEL2[1:0]</i>	Configuration
00	Reserved
01(default)	Minimum VBAT pin voltage > 2.9V
10	Minimum VBAT pin voltage > 3.3V
11	Minimum VBAT pin voltage > 3.7V

### 6.3.1.6 External PVDD Mode

The internal Boost of TAS2120 can be disabled by setting *BST\_EN* register low. When the external PVDD mode is used, the class-D amplifier is directly powered from the voltage source on PVDD pin. The device configurations needs to be updated using PPC3 software to configure the device in required performance configurations for external PVDD mode of operation.

### 6.3.2 Faults and Status

During power-up sequencing, the power-on-reset circuit (POR) monitors the VDD and IOVDD pins and holds device in reset (including all the configuration registers) until the supplies are valid. Any supply voltage dip on VDD or IOVDD below the UVLO voltage thresholds resets the device immediately along with all the register configurations.

During operation modes, the device monitors internal device status and fault conditions and can notify the host of error and status conditions using the IRQZ interrupt pin and internal I<sup>2</sup>C based interrupt registers. The interrupt generation in IRQZ pin can be masked by configuring the corresponding Interrupt mask register bit.

[Table 6-15](#) lists the different faults and interrupts that the device monitors and the corresponding configuration bits to enable/disable the interrupt generation and reading the I2C interrupt status

**Table 6-15. Faults and Interrupts**

Category	Interrupt	Interrupt Mask register bit	Default Mask status	Interrupt Latched status bit
Limiter & Brown out protection <a href="#">Section 6.4.2.4</a>	Brownout detected	<i>INT_MASK0[3]</i>	Not Masked	<i>INT_LTCH0[3]</i>
	BOP Active	<i>INT_MASK0[2]</i>	Not Masked	<i>INT_LTCH0[2]</i>
	BOP infinite hold	<i>INT_MASK0[7]</i>	Not Masked	<i>INT_LTCH0[7]</i>
	Limiter Active	<i>INT_MASK0[4]</i>	Not Masked	<i>INT_LTCH0[4]</i>
	Limiter attenuation	<i>INT_MASK0[6]</i>	Not Masked	<i>INT_LTCH0[6]</i>
	Supply below inflection point	<i>INT_MASK0[5]</i>	Not Masked	<i>INT_LTCH0[5]</i>
Supply Voltage Monitors <a href="#">Section 6.4.5</a>	PVDD Over voltage	<i>INT_MASK3[2]</i>	Not Masked	<i>INT_LTCH3[2]</i>
	PVDD Under voltage	<i>INT_MASK1[7]</i>	Not Masked	<i>INT_LTCH1[7]</i>
	VBAT2S supply under voltage	<i>INT_MASK1[6]</i>	Not Masked	<i>INT_LTCH1[6]</i>
	VBAT supply under voltage	<i>INT_MASK4[7]</i>	Not Masked	<i>INT_LTCH4[7]</i>
Thermal protection <a href="#">Section 6.4.6</a>	Thermal warning at 135C	<i>INT_MASK1[4]</i>	Masked	<i>INT_LTCH1[4]</i>
	Thermal warning at 125C	<i>INT_MASK1[3]</i>	Masked	<i>INT_LTCH1[3]</i>
	Thermal warning at 115C	<i>INT_MASK1[2]</i>	Masked	<i>INT_LTCH1[2]</i>
	Thermal warning at 105C	<i>INT_MASK1[1]</i>	Masked	<i>INT_LTCH1[1]</i>
	Over temperature error	<i>INT_MASK3[7]</i>	Not Masked	<i>INT_LTCH3[7]</i>
Clock protection <a href="#">Section 6.4.7.1</a>	Clock error	<i>INT_MASK2[3]</i>	Not Masked	<i>INT_LTCH2[3]</i>
	Pre-Power-up Clock error	<i>INT_MASK4[2]</i>	Not Masked	<i>INT_LTCH4[2]</i>
	Clock ratio change error	<i>INT_MASK2[2]</i>	Not Masked	<i>INT_LTCH2[2]</i>
	Fs change error	<i>INT_MASK2[1]</i>	Not Masked	<i>INT_LTCH2[1]</i>
	Fs invalid error	<i>INT_MASK2[0]</i>	Not Masked	<i>INT_LTCH2[0]</i>
	Frame out of sync	<i>INT_MASK2[5]</i>	Not Masked	<i>INT_LTCH2[5]</i>
	Internal PLL Clock error	<i>INT_MASK2[4]</i>	Not Masked	<i>INT_LTCH2[4]</i>
	Digital watchdog	<i>INT_MASK2[7]</i>	Not Masked	<i>INT_LTCH2[7]</i>
Other Protections & Status	Class-D Over current error	<i>INT_MASK3[3]</i>	Not Masked	<i>INT_LTCH3[3]</i>
	Device Active	<i>INT_MASK0[1]</i>	Masked	<i>INT_LTCH0[1]</i>

### 6.3.2.1 Interrupt generation and clearing

The IRQZ is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to IOVDD. An internal pull up resistor (18kΩ) is provided in the device and can be assessed by setting the *IRQZ\_PU* register bit.

The interrupt generation on IRQZ pin can be configured using *IRQZ\_PIN\_CFG[1:0]* register. For the interrupts that have auto retry feature, the retry timer can be configured using *RETRY\_WAIT\_TIME* register. The interrupt pin polarity can be changed from the default case of Active Low to Active high by setting the *IRQZ\_POL* register bit high.

Any latched interrupt can be cleared by setting *INT\_CLR\_LTCH* bit high. This is self clearing bit and automatically gets updated to low once the interrupt is cleared. Interrupts can also be cleared by hardware shutdown by pulling the SDZ pin low, or by software reset using *SW\_RESET* bit.

**Table 6-16. IRQZ pin configuration**

<i>IRQZ_PIN_CFG[1:0]</i>	Configuration
00	Reserved
01(default)	Interrupt generated on any unmasked latched interrupt
10	Reserved

**Table 6-16. IRQZ pin configuration (continued)**

<i>IRQZ_PIN_CFG[1:0]</i>	Configuration
11	Interrupt generated for 2 to 4 ms every 4 ms on any unmasked latched interrupt

**Table 6-17. Retry wait timer**

<i>RETRY_WAIT_TIME</i>	Configuration
0 (default)	Retry every 1.5sec
1	Retry every 100ms

## 6.4 Feature Description

### 6.4.1 PurePath™ Console 3 Software

The TAS2120's advanced features and device configuration can be performed using PurePath Console 3 (PPC3) software. The base software PPC3 is downloaded and installed from the TI website. Once installed the TAS2120 application can be downloaded from with-in PPC3. The PCC3 tool calculates necessary register coefficients that are described in the following sections. The device performance is optimized using registers named *TUNING* based on the options for system configuration selected in the GUI. This is the recommended method to configure the device. Once the TAS2120 application calculates and updates the device, the registers values can be read back using the PPC3 tool for final system integration.

### 6.4.2 Playback Signal Path

#### 6.4.2.1 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier's analog gain level ( $A_{AMP}$ ) and digital volume control ( $A_{DVC}$ ). Equation 1 calculates the amplifiers output voltage. Amplifier analog gain setting should be set before powering up the playback channel and shouldn't be changed while the channel is active. The digital volume control can be modified while the channel is active and also allows for soft volume ramp up/down feature to allow for smooth transition of output voltage from one level to another.

$$V_{AMP} = \text{Input} + A_{dvc} + A_{AMP} \text{ dBV} \quad (1)$$

where

- $V_{AMP}$  is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0 dBFS
- $A_{DVC}$  is the digital volume control setting, 6 dB to -110 dB in 0.5 dB steps
- $A_{AMP}$  is the amplifier output level setting, -0.071dBV to 21.0dBV in 0.5017dBV steps.

Amplifier output level settings are presented in dBV (dB relative to 1  $V_{rms}$ ) with a full scale digital audio input (0 dBFS) and the digital volume control set to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used to convey gain only.

Table below shows gain settings that can be programmed via the *AMP\_LVL* register. When *AMP\_LVL* is set to less than 9dBV settings, the playback channel is automatically configured to low noise mode or receiver mode of operation.

**Table 6-18. Amplifier Output Level Settings**

<i>AMP_LVL[5:0]</i>	FULL SCALE OUTPUT	
	dBV	$V_{PEAK}$ (V)
0x00	21.000	15.9
0x01	20.498	15.0
0x02	19.997	14.1
0x03	19.495	13.3

**Table 6-18. Amplifier Output Level Settings  
(continued)**

AMP_LVL[5:0]	FULL SCALE OUTPUT	
	dBV	V <sub>PEAK</sub> (V)
0x04	18.993	12.6
...	...	...
0x27	1.434	1.7
0x28	0.932	1.6
0x29	0.430	1.5
0x2A	-0.071	1.4
0x2B-0x3F	Reserved	Reserved

When a change in digital volume control occurs, the device ramps the volume to the new setting based on the *DVC\_SLEW\_RATE* register bits. If *DVC\_SLEW\_RATE* is set to 0x7FFFFFFF, volume ramp is disabled. This can be used to speed up start up, shutdown and digital volume changes when volume ramp is handled by the system host. When volume ramp is disabled, the input audio data stream should be held at digital silence during shutdown and power up of the device to avoid any clicks and pops.

The device can be put in software based mute by setting *DVC\_LEVEL* to 0x000000 setting.

The digital voltage control registers *DVC\_LEVEL* and *DVC\_SLEW\_RATE* registers can be configured using the PPC3 Software [Section 6.4.1](#).

**Table 6-19. Digital Volume Control**

DVC_LEVEL[23:0]	VOLUME (dB)
0x000000	Software MUTE
0x00000D (MIN)	-110
...	...
0x400000	0 (default)
...	...
0x7FB261 (MAX)	6

**Table 6-20. Digital Volume Ramp Rate**

DVC_SLEW_RATE[23:0]	RAMP RATE @ 48kHz (s)
0x00036A	1000ms
...	...
0x034A51	4ms (default)
...	...
0x7FFFFFFF	0 - Ramp disabled

#### 6.4.2.2 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers. The playback path employs a high-pass filter (HPF) to prevent this from occurring. The HPF is a 1st order filter and can be changed from the default 2 Hz for 48ksps fs using the *AUDIO\_HPF\_N0*, *AUDIO\_HPF\_N1*, *AUDIO\_HPF\_D1* registers. The HPF filter frequency scales with change in the FSYNC clock and can be re-configured to achieve the required cutoff frequency for different FSYNC clock frequencies. The coefficients can also be changed to disable the HPF coefficients appropriately. These coefficients should be calculated and set using PPC3 Software [Section 6.4.1](#).

#### 6.4.2.3 Class-D Amplifier

TAS2120 has integrated high performance class-D amplifier with low idle channel noise, low distortion and high PSRR. The Class-D amplifier switches on a clock frequency derived from the SBCLK frequency and is always synchronized to the input clock source. The *SAMP\_RATE\_CFG* register enables selection between input clock source based out of multiple of 44.1kHz vs 48kHz multiples.

**Table 6-21. Sample rate configuration**

<i>SAMP_RATE_CFG</i>	Configuration
0 (default)	Audio data rate is multiple/sub-multiple of 48ksps
1	Audio data rate is multiple/sub-multiple of 44.1ksps

For improvements in EMI performance the class-D amplifier supports programmable Edge rate control (ERC) and class-D clock spread spectrum modulation (SSM).

The edge rate of class-D can be controlled using *CLASSD\_OUTPUT\_EDGERATE\_CTRL[1:0]* register. By default the class-D output edge rate is configured to fastest setting to enable high efficiency in the system. The class-D output edge rate can be slowed down using other configuration settings to reduce the EMI energy at high frequency with reduction in efficiency. The exact rate of change of output edge rate varies based on output load conditions, and the values mentioned in the tables below are approximate edge rate levels for default loading conditions.

**Table 6-22. Class-D output edge rate control**

<i>CLASSD_OUTPUT_EDGERATE_CTRL[1:0]</i>	Configuration
00	Class-D output edge rate of 0.5 V/ns
01	Class-D output edge rate of 1.0 V/ns
10	Reserved
11(default)	Class-D output edge rate of 2 V/ns

The class-D amplifier has over current protection on each of the output power FETs, including the PVDD High side, VDD high side and the ground power FETs.

The class-D amplifier output impedance can be controlled when the outputs stop switching during Noise gate mode using *CLASSD\_HIZ\_MODE* control register.

**Table 6-23. Class-D high-Z mode control**

<i>CLASSD_HIZ_MODE</i>	Configuration
0 (default)	Output pulled down with 2.5kΩ
1	Output pulled down with >13kΩ

#### 6.4.2.4 Supply Tracking Limiters with Brown Out Prevention

TAS2120 monitors class-D supply voltage (VBAT or PVDD) along with the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions. The limiter and brown out module calculates the signal attenuation required based on the condition of the signal level, channel gain and the selected supply voltage.

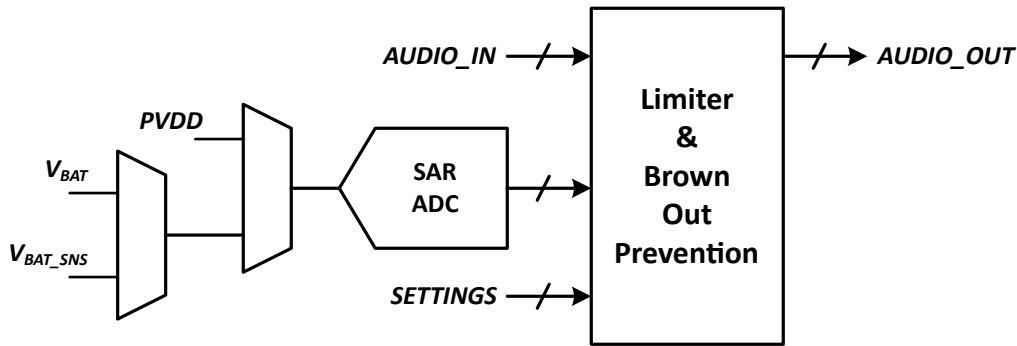


Figure 6-2. Limiter and Brown out protection module

The Brown Out Prevention (BOP) module provides a priority input to provide a fast response to transient dips in the battery supply. The BOP feature can be enabled by configuring the register bit *BOP\_EN* high. The supply voltage that is tracked to determine Brown out conditions can be configured as  $V_{BAT}$ ,  $V_{BAT\_SNS}$  or *PVDD* based on system configuration needs by using *BOP\_SRC* register bit. When the selected supply dips below the brown-out threshold configured by setting register *BOP\_THR\_LVL[23:0]*, the BOP will begin reducing gain. The rate of gain reduction (db/sample) can be configured by setting the *BOP\_ATK\_RATE[23:0]* registers. When the  $V_{BAT}$  supply rises above the brownout threshold, the BOP will begin to release the gain after the programmed hold timer, *BOP\_HLD\_COUNT[23:0]*. The BOP feature uses the *LIM\_RLS\_RATE[23:0]* register setting to release after a brown out event. The release rate is rate of gain increase in db/sample ratio. During a BOP event the limiter updates will be paused. This is to prevent a limiter from releasing during a BOP event.

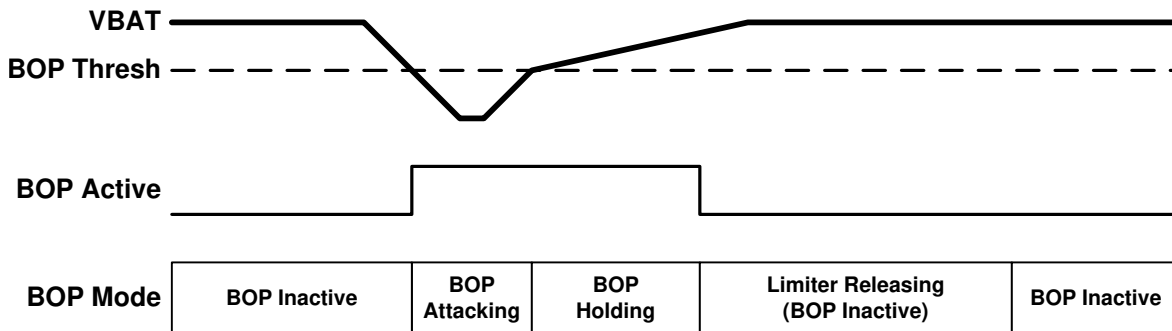


Figure 6-3. Brown Out Prevention Event

The device can be configured to hold the gain attenuation once a BOP event is detected by setting the register bit *BOP\_INF\_HLD* high. When the bit is programmed high, the Limiter and BOP module does not release the gain attenuation and holds the device in the programmed min gain attenuation level until the infinite hold is cleared by setting the register bit *BOP\_HLD\_CLR* high. The hold clearing bit is self clearing and will automatically reset to low state once the hold is cleared.

A hard brownout level can be set to shutdown the device if the BOP gain attenuation cannot mitigate the drop in battery voltage. The brown out based shutdown of the device is enabled when *BOPSD\_EN* bit is set high and shuts down when the battery voltage falls below the voltage threshold set by *BOSD\_THR\_LVL[23:0]* register bits.

A maximum level of attenuation applied by the limiters and brown out prevention feature is configurable via the *LIM\_MAX\_ATN* register. This attenuation limit is shared between the features. For instance, if the maximum attenuation is set to 6 dB and the limiters have reduced gain by 4 dB, the brown out prevention feature will only be able to reduce the gain further by another 2 dB. If the limiter or brown out prevention feature is attacking and it reaches the maximum attenuation, gain will not be reduced any further.

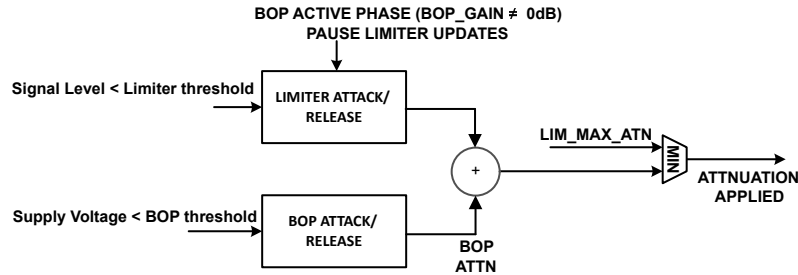


Figure 6-4. Limiter and Brown out gain attenuation

#### 6.4.2.4.1 Voltage Limiter and Clipping protection

The supply tracking limiter can be configured using *LIM\_MODE[1:0]* register. In the VBAT voltage mode, the limiter tracks the VBAT supply voltage for voltage limiter and in PVDD voltage mode, the limiter tracks the PVDD voltage for external PVDD mode of use case.

Table 6-24. Limiter mode selection

<i>LIM_MODE[1:0]</i>	Configuration
00 (default)	Disabled
01	VBAT voltage based limiter
10	PVDD voltage based limiter
11	Reserved

The limiter can be configured to reduce the output signal based on fixed signal threshold level, or it can attenuate signal based on a dynamic threshold which tracks the selected supply voltage. The register bit *SUPPLY\_HEADROOM\_LIM\_MODE* enables the dynamic supply tracking and can be used to limit the clipping distortion when the supply voltage is varying in the system.

Table 6-25. Limiter dynamic supply headroom tracking mode

<i>SUPPLY_HEADROOM_LIM_MODE</i>	Configuration
0 (default)	Disabled
1	Enabled. Limiter threshold is dynamically changed based as a fixed percentage of monitored supply voltage.

When *SUPPLY\_HEADROOM\_LIM\_MODE* is set high, the limiter sets the threshold as a fixed percentage of the monitored supply voltage. The limiter begins reducing gain when the output signal level is greater than the threshold configured. For eg, if voltage limiting is desired to be 10% below the supply voltage, then *LIM\_SLOPE[23:0]* is configured as 0.9 and the threshold is calculated as monitored supply voltage multiplied by 1.1. Similarly if the *LIM\_SLOPE[23:0]* is configured at > 1.0, the limiter threshold is set at higher than the supply voltage, and a small amount of controlled clipping occurs.



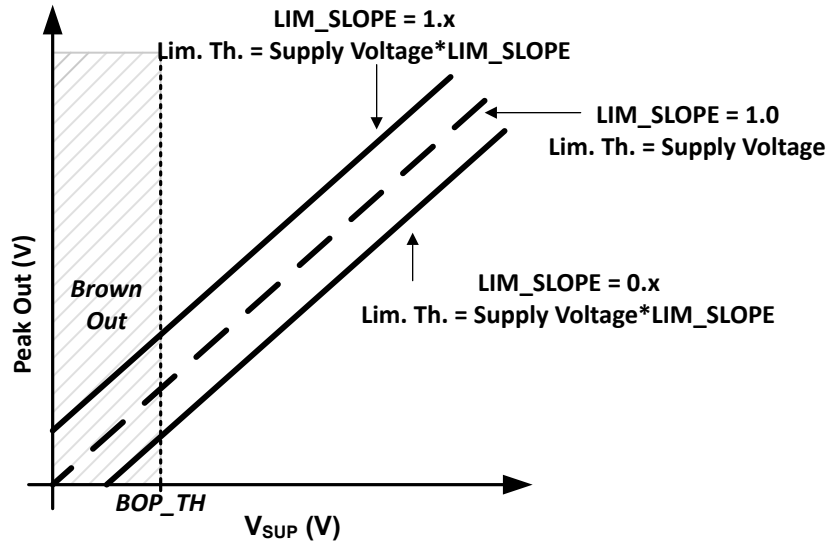


Figure 6-5. Limiter with dynamic supply headroom

When *SUPPLY\_HEADROOM\_LIM\_MODE* is set low, the limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track selected supply below a programmable inflection point with a minimum threshold value. Figure 6-6 below shows the limiter configured to limit to a constant level regardless of the selected supply level. To achieve this behavior, set the limiter maximum threshold to the desired level using *LIM\_TH\_MAX[23:0]*. Set the limiter inflection point using *LIM\_INF\_PT[23:0]* below the minimum allowable supply setting. The limiter minimum threshold register *LIM\_TH\_MIN[23:0]* does not impact limiter behavior in this use case.

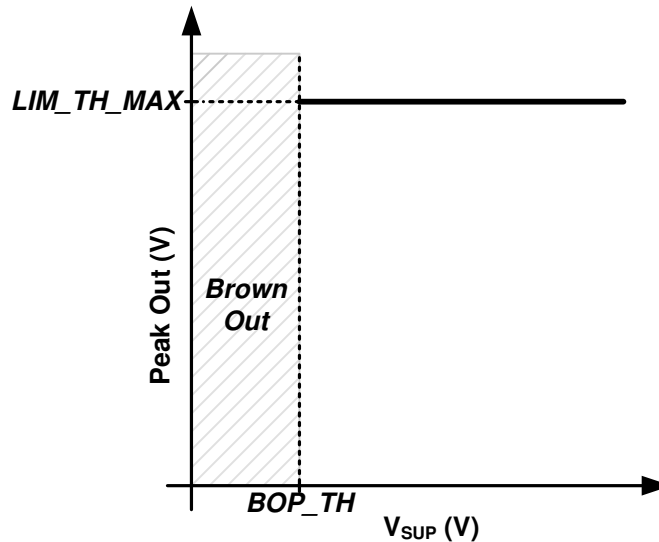


Figure 6-6. Limiter with Fixed Threshold

Figure 6-7 shows how to configure the limiter to track selected supply below a threshold without a minimum threshold. Set the *LIM\_TH\_MAX[23:0]* register to the desired threshold and *LIM\_INF\_PT[23:0]* register to the desired inflection point where the limiter begins to reduce the threshold with the selected supply. The *LIM\_SLOPE[23:0]* register bits can be used to change the slope of the limiter tracking the supply voltage in V/V. For example, a slope value of 1 V/V reduces the limiter threshold 1 V for every 1 V of drop in the supply voltage. Program the *LIM\_TH\_MIN[23:0]* below the minimum of the selected supply to prevent the limiter from having a minimum threshold reduction when tracking the selected supply.

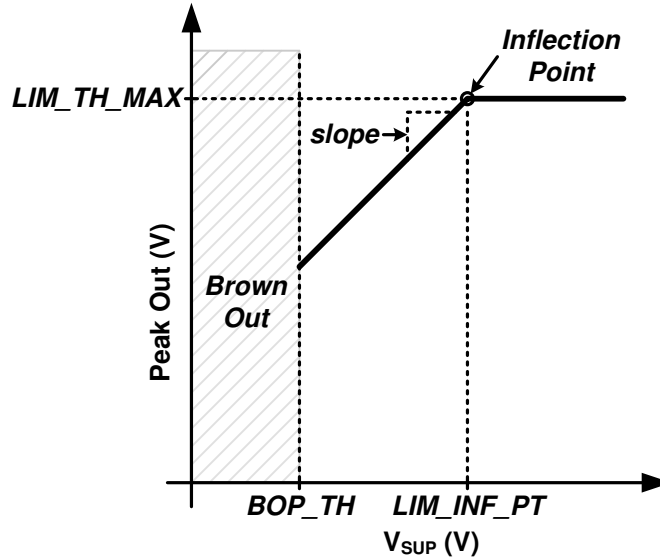


Figure 6-7. Limiter with Inflection Point

To achieve a limiter that tracks the selected supply below a threshold, configure the limiter as explained in the previous example, except program the `LIM_TH_MIN[23:0]` register to the desired minimum threshold. This is shown in Figure 6-8 below.

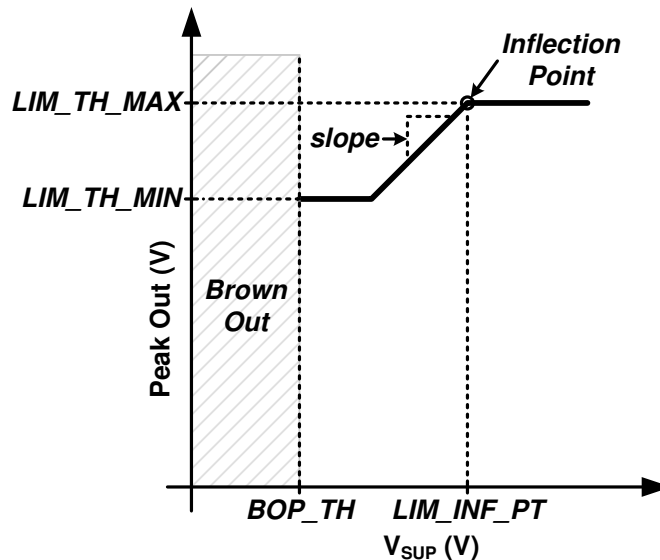


Figure 6-8. Limiter with Inflection Point and Minimum Threshold

The limiter has a configurable attack rate (dB/Sample), hold time ( no of samples) and release rate (db/Sample), which are available via the `LIM_ATK_RATE[23:0]`, `LIM_HLD_COUNT[23:0]`, `LIM_RLS_RATE[23:0]` register bits.

#### 6.4.2.5 Tone Generator

TAS2120 can generate internally a sine tone using an integrated tone generator. This feature can be enabled by configuring the register bit `INTERNAL_TONE_GEN_ENZ` to low. The tone signal will start playing back on the output by configuring the `INTERNAL_TONE_PLAYBACK_EN` bit high. When set high, the device will start generating a sine tone based on the programmed `TONE_GEN_CNTRL_xx` registers. The tone generator can generate any frequency from 16Hz to a maximum frequency of  $0.45 \cdot F_s$ , where  $F_s$  is the sampling rate of the input digital clocks. The amplitude of the tone signal can also be controlled using the `TONE_GEN_CNTRL_xx` registers. It is recommended to program the tone frequency and amplitude using the PPC3 Software.

The internally generated tone can be mixed with incoming audio stream, or can replace the input audio stream and only tone signal is generated using *INTERNAL\_TONE\_MIXING\_EN* register.

**Table 6-26. Internal tone generator mixing options**

<i>INTERNAL_TONE_MIXING_EN</i>	Configuration
0	Only internal tone is generated.
1(default)	Internally generated tone is mixed with input audio data and played together.

The tone generator can use external clock source like BCLK, or it can be generated using internal oscillator to generate tone signals even with no external clock sources using *INTERNAL\_TONE\_CLK\_SEL* register.

**Table 6-27. Internal tone clock source selection**

<i>INTERNAL_TONE_CLK_SEL</i>	Configuration
0 (default)	Tone generator uses external clocks
1	Tone generator uses internal oscillator

### 6.4.3 Digital Audio Serial Interface

The device provides a flexible Audio Serial Interface (ASI) port. The port can be configured to support a variety of formats including stereo I<sup>2</sup>S, Left Justified, and TDM. Mono audio playback is available via the SDIN pin. The SDOUT pin is used to transmit sample streams including PVDD voltage, VBAT voltage, die temperature, status and audio for echo reference.

The TDM serial audio port supports up to 16 32-bit time slots at 44.1/48 kHz, 8 32-bit time slots at a 88.2/96 kHz sample rate and 4 32-bit time slots at a 176.4/192 kHz sample rate. The device supports 2 time slots at 32 bits in width and 4 or 8 time slots at 16, 24 or 32 bits in width. The device automatically detects the number of time slots and this does not need to be programmed. PCM data sampling rate and SBCLK to FSYNC ratio detected on the TDM bus is reported back on the read-only register bits *FS\_RATE\_DETECTED[2:0]* and *FS\_RATIO\_DETECTED[3:0]* respectively.

**Table 6-28. PCM Data Sample Rate Detected**

<i>FS_RATE_DETECTED[2:0]</i> (Read Only)	Setting
000	Reserved
001	14.7 kHz / 16 kHz
010	22.05 kHz / 24 kHz
011	29.4 kHz / 32 kHz
100 (default)	44.1 kHz / 48 kHz
101	88.2 kHz / 96 kHz
110	176.4 kHz / 192 kHz
111	Error condition

A frame begins with the transition of FSYNC from either high to low or low to high (set by the *FRAME\_START* register bit). FSYNC and SDIN are sampled by SBCLK using either the rising or falling edge set by the *RX\_EDGE* register bit. The *RX\_OFFSET[4:0]* register bits define the number of SBCLK cycles from the transition of FSYNC until the beginning of time slot 0. This is typically set to a value of 0 for Left Justified format and 1 for an I<sup>2</sup>S format.

The *RX\_SLEN[1:0]* register bits set the length of the RX time slot to 16, 24 or 32 (default) bits. The length of the audio sample word within the time slot is configured by the *RX\_WLEN[1:0]* register bits. The RX port will

left justify the audio sample within the time slot by default, but this can be changed to right justification via the *RX\_JUSTIFY* register bit. The device supports mono and stereo down mix playback ( $[L+R]/2$ ). By default the device will playback mono from the time slot equal to the I<sup>2</sup>C base address offset (set by the AD1 and AD2 pins) for playback. The *RX\_SCFG[1:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX\_SLOT\_R[3:0]* and *RX\_SLOT\_L[3:0]* register bits.

If time slot selection places reception either partially or fully beyond the frame boundary, the receiver returns a null sample equivalent to a digitally muted sample.

The TDM port can transmit a number of sample streams on the SDOUT pin including interrupts and status, PVDD voltage, VBAT voltage and die temperature.

Either the rising or falling edge of SBCLK can be used to transmit data on the SDOUT pin. This can be configured by setting the *TX\_EDGE* register bit. The *TX\_OFFSET[2:0]* register bits define the number SBCLK cycles between the start of a frame and the beginning of time slot 0. This is programmed to 0 for Left Justified format and 1 for I<sup>2</sup>S format. The TDM TX can either transmit logic 0 or Hi-Z depending on the setting of the *TX\_FILL* register bit. An optional bus keeper can weakly hold the state of SDOUT pin when all devices are driving Hi-Z. Since only one bus keeper is required on SDOUT, this feature can be disabled via the *TX\_KEEPEEN* register bit. The bus keeper can be configured to hold the bus for only 1 LSB or Always (permanent) using *TX\_KEEPLN* register bit. Additionally, the keeper LSB can be driven for a full cycle or half of cycle using *TX\_KEEPCY* register bit.

The device also support monitoring and TDM transmit of PVDD and VBAT input voltages. For PVDD slot, enable and length settings *PVDD\_SLOT[5:0]*, *PVDD\_TX* and *PVDD\_SLEN* register bits can be use. Similarly for VBAT slot, enable and length settings *VBAT\_SLOT[5:0]*, *VBAT\_TX* and *VBAT\_SLEN* register bits can be used. Die temperature can also be transmitted from the device in same manner. Enable and slot settings for Die temperature are done using *TEMP\_TX* and *TEMP\_SLOT [5:0]* register bits.

Information about status of slots can be found in *STATUS\_SLOT[5:0]* register bits. *STATUS\_TX* register bit set high enables the status transmit. Status slot length is always 8bits and [Table 6-29](#) summarizes the status bit information that is transmitted when status transmit is enabled. If time slot selections place transmission beyond the frame boundary, the transmitter will truncate transmission at the frame boundary.

**Table 6-29. Status Bits transmitted**

<i>Status Slot bit location</i>	<i>Status signal</i>
Bit 0	PVDD UVLO status bit
Bit 1	Over current protection status bit
Bit 2	Over temperature protection status bit
Bit 3	Brown out protection active status bit
Bit 4	Limiter active status bit
Bit 5	Noise gate mode status bit
Bit 6	Y-bridge status bit. 1 = PVDD switching, 0 = VDD switching
Bit 7	Device Active status bit

#### 6.4.3.1 Digital Loopback

The device supports loop back feature to loop SDIN data to SDOUT at two levels. When this feature is enabled through *TDM\_LOOPBACK* register bit, loop back is done at the IO Pin level without any ASI data decoding within the device. Other option is to enable the loop back feature through *TDM\_DESER\_LOOPBACK* register bit in which case SDIN data first goes through ASI protocol decoding within the device and then sent back via SDOUT. These SDIN to SDOUT loop back options can be useful for board level debug of an audio system.

Device can also loop back echo reference digital audio data at the end of the internal signal processing blocks like Limiter, BOP etc. through SDOOUT signal. This allows audio system to perform noise and echo cancellation algorithms in a host processor that is connected to the device. The echo reference can be enabled by configuring AUDIO\_TX register bit. The slot length and the time slot can be selected using AUDIO\_SLEN and AUDIO\_SLOT[5:0] register bits.

#### 6.4.4 Boost

The TAS2120 internal processing algorithm automatically enables the boost when needed. A look-ahead algorithm monitors the battery voltage and the digital audio stream. When the speaker output approaches the battery voltage the boost is enabled in-time to supply the required speaker output voltage. When the boost is no longer required it is disabled and bypassed to maximize efficiency. The boost can be configured in one of two modes. The first is low in-rush (Class-G) supporting only boost on-off and has the lowest in-rush current. The second is high-efficiency (Class-H) where the boost voltage level is adjusted to a value just above what is needed. This mode is more efficient but has a higher in-rush current to quickly transition the levels. This can be configured using *BST\_MODE*[1:0] register bits.

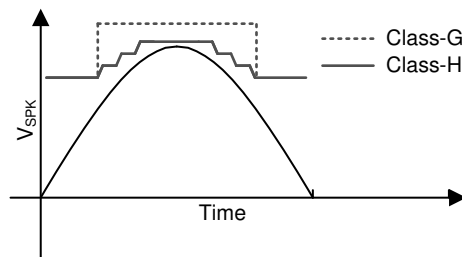


Figure 6-9. Boost Mode Signal Tracking Example

Table 6-30. Boost Mode

BST_MODE[1:0]	BOOST MODE
00	Class-H - High efficiency (default)
01	Class-G - Low in-rush
10	Always On
11	Always Off - Pass-through

The boost can be enabled and disabled using *BST\_EN* register. When driving the Class-D amplifier using an external supply through the PVDD pin, the boost should be disabled and the SW pin should be left floating.

Table 6-31. Boost Enable

BST_EN	BOOST IS
0	Disabled (External PVDD mode)
1	Enabled (default)

The maximum boost voltage is set by *VBOOST\_MAX\_CTRL*[7:0]. When operating in class-G mode, the boost when needed will be at this voltage. In class-H mode of operation the boost voltage is automatically selected based on the audio signal but will not exceed this set value. In class-H mode, the class-H controller controls the Boost with a minimum step size of 33mV to generate the required PVDD voltage. The max boost voltage that the device generates is controlled by *VBOOST\_MAX\_CTRL*[7:0] and it can be configured with a step size of 66mV.

Table 6-32. Boost Max Regulation Voltage

VBOOST_MAX_CTRL[7:0]	BOOST VOLTAGE (V)
0x00 - 0x53	Reserved
0x54	5.54 V
0x55	5.61 V

**Table 6-32. Boost Max Regulation Voltage  
(continued)**

<b>VBOOST_MAX_CTRL[7:0]</b>	<b>BOOST VOLTAGE (V)</b>
...	.....steps of 66mV per LSB step .....
0xA7	11.02 V (default)
...	.....steps of 66mV per LSB step .....
0xE0	14.75V
0xE6 - 0xFF	Reserved

At light loads (eg. near zero cross of sine waves), the boost automatically enters PFM mode to improve the system efficiency. When the Boost is running in PFM mode, the minimum pulse frequency can be adjusted using *BST\_MIN\_FREQ\_SEL*. Setting a higher PFM frequency will ensure the Boost frequency is always above the set threshold at the cost of increasing the system power consumption.

**Table 6-33. Active Mode PFM Lower Frequency Limit**

<b>BST_MIN_FREQ_SEL[1:0]</b>	<b>LOWER LIMIT</b>
00	No lower limit (default)
01	25 kHz
10	50 kHz
11	RESERVED

The peak current drawn by the boost is controlled using *BST\_ILIM[23:0]* register and it limits the current drawn from the VBAT supply. This setting allows flexibility in the inductor selection for various saturation currents. The system should always use inductors which have minimum saturation current ( $I_{SAT}$ ) atleast 5% higher than programmed *BST\_ILIM* setting. The Boost circuit can go unstable if the inductor's  $I_{SAT}$  is lower than the *BST\_ILIM* setting. The current limit can be adjusted in 39.1 mA steps with a range from 1.5A to 5.1A using PPC3 Software.

The change in boost configurations like *BST\_ILIM*, *VBOOST\_MAX\_CTRL* etc requires re-tuning of device parameters such as *CLASSH\_TUNING\_xx[23:0]* registers to achieve best performance while ensuring no functionality failures. This configuration should be changed using PPC3 tool to enable automatic reconfiguration of all the associated device parameters.

For multiple channel systems, the boost phase can be shifted to ensure each device will draw peak current from the battery at different instance of times and enable lower instantaneous peak current from the battery. The boost syncing among multiple devices is enabled using *BOOST\_PHASE\_SYNC\_EN*. The individual device boost phase can be automatically configured to different values using the i2c target address device detected by using *BOOST\_PHASE\_FROM\_ADDRESS\_PIN* register, or it can be manually configured using *BOOST\_PHASE* register. The Boost phase shift is done by each device using the FSYNC pulse to synchronize each device and all the devices which require the Boost phase synchronization should be connected to same FSYNC from the host in the system.

**Table 6-34. Boost Sync**

<b>BOOST_PHASE_SYNC_EN</b>	<b>Status</b>
0	Disabled
1	Enabled(default)

**Table 6-35. Boost Phase selection from i2c target address**

<b>BOOST_PHASE_FROM_ADDRESS_PIN</b>	<b>Status</b>
0	Disabled

**Table 6-35. Boost Phase selection from i2c target address (continued)**

<i>BOOST_PHASE_FROM_ADDR ESS_PIN</i>	Status
1	Enabled(default)

**Table 6-36. Boost Phase manual selection (when *BOOST\_PHASE\_FORM\_ADDRESS\_PIN = 0*)**

<i>BOOST_PHASE[1:0]</i>	Phase Delay
00	Phase shift is 0ns (default)
01	Phase shift is 65ns (~90° for max clock)
10	Phase shift is 130ns (~180° for max clock)
11	Phase shift is 195ns (~270° for max clock)

### 6.4.5 Supply Voltage Monitors

TAS2120 has integrated SAR ADC to monitor the supply voltage pins VBAT or VBAT\_SNS and PVDD. The sensed voltages are used for internal device features, protections and can also be streamed out over digital data bus or read through i2c registers.

The battery voltage can be sensed through either VBAT or VBAT\_SNS pins based on the register *SEL\_VBAT\_MODE[1:0]*

**Table 6-37. Battery mode selection**

<i>SEL_VBAT_MODE[1:0]</i>	Configuration
00 (default)	Voltage monitor on VBAT pin. 1S mode of operation
01	Voltage monitor on VBAT_SNS pin. 1S mode of operation
10	Voltage monitor on VBAT_SNS pin. 2S mode of operation
11	Reserved

The monitor ADC samples the VBAT pin at higher rate compared to PVDD pin voltage. This sampling speed can be swapped to prioritize PVDD pin sampling rate over VBAT, for example in case of external PVDD mode of operation.

**Table 6-38. Supply monitor sampling rate**

<i>SUPPLY_SAMPLING_RATE</i>	Configuration
0(default)	VBAT Sampling rate is higher than PVDD
1	PVDD Sampling rate is higher than VBAT

The VBAT and PVDD monitored voltages are stored in the register *VBAT\_CNV* and *PVDD\_CNV* registers and can be read using i2c commands.

The supply monitors are also used for voltage protection like VBAT under voltage, PVDD over voltage and under voltage and VBAT2S under voltage. The voltage protection features monitors the supply voltages, and shuts down the device when the voltage crosses the protection threshold levels. The device also sets the corresponding fault register and can generate an interrupt on IRQZ pin based on configured interrupt Mask register as described in [Section 6.3.2](#). Once the device is shutdown, the device can be re-powered up using the *MODE[1:0]* register bits.



PVDD over voltage protection is based on the monitored PVDD voltage compared against a programmable threshold which can be controlled using *PVDD\_OVLO\_TH\_SEL* in the internal boost mode, and *PVDD\_OVLO\_TH\_SEL\_EXT\_BOOST* in the external PVDD mode of operation. The PVDD Over voltage protection is enabled by default and can be disabled by setting *PVDD\_OV\_DET\_DIS* bit high.

**Table 6-39. PVDD Over voltage protection threshold, internal Boost mode**

<i>PVDD_OVLO_TH_SEL</i> [1:0]	Configuration
00	Over voltage threshold is 13.5V
01	Over voltage threshold is 14V
10	Over voltage threshold is 15V
11 (default)	Over voltage threshold is 16V

**Table 6-40. PVDD Over voltage protection threshold, External PVDD mode**

<i>PVDD_OVLO_TH_SEL_EXT_BOOST</i> [1:0]	Configuration
00	Over voltage threshold is 13.5V
01 (default)	Over voltage threshold is 14V
10	Over voltage threshold is 15V
11	Over voltage threshold is 16V

#### 6.4.6 Thermal Protection

TAS2120 has internal device junction temperature monitor which protects the device against over temperature. When the internal temperature rises above the Over temperature threshold, the device automatically shuts down and sets the Over temperature flag in the corresponding Interrupt registers. The device can automatically retry to power up if *OTE\_RETRY* bit is set high. When set high, the device attempts to re-power up after every *RETRY\_WAIT\_TIME* setting (default 1.5 seconds of retry)

Along with over temperature protection, the device has thermal warning thresholds to allow for system to raise interrupts or flags as the junction temperature is approaching the shutdown. There are four thermal warning flags available at the internal temperature of 105C, 115C, 125C and 135C. Each thermal warning flag can be independently set to control the Interrupt generation on the IRQZ pad. The minimum temperature and the step size of the temperature warning flag can be programmed using the registers *THERMAL\_WARN\_MIN\_TEMP*[23:0] and *THERMAL\_WARN\_TEMP\_STEP*[23:0]

The real time internal junction temperature is monitored are stored in the register *TMP\_CNV* and can be read using i2c commands.

#### 6.4.7 Clocks and PLL

In TDM/I<sup>2</sup>S Mode, the device operates from SBCLK. [Table 6-41](#) below shows the valid SBCLK frequencies for each sample rate and SBCLK to FSYNC ratio. For 44.1kHz based clocking, the same table is applicable with the associated ratio change between 48ksps to 44.1ksps.

While the sampling rate of 192kHz is supported, data is internally down-sampled to 96kHz. Therefore audio content greater than 40kHz should not be applied to prevent aliasing. This additionally affects all processing blocks like BOP and limiter which should use 96 kHz fs when accepting 192 kHz audio.

If the sample rate is properly configured via the *SAMPLE\_RATE\_CFG* bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device automatically detects the input PCM FSYNC and BCLK frequency and auto configures itself to playback audio signal. The detected clock rates can be read using the read only registers *FS\_RATIO\_DETECTED* and *FS\_RATE\_DETECTED*. The device will

detect improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts.

**Table 6-41. Supported SBCLK Frequencies (MHz) (48 kHz based sample rates)**

Sample Rate (kHz)	SBCLK to FSYNC Ratio													
	16	24	32	48	64	96	128	192	256	384	512	125	250	500
16 kHz	NA	0.384	0.512	0.768	1.024	1.536	2.048	3.072	4.096	6.144	8.192	2	4	8
24 kHz	0.384	0.576	0.768	1.152	1.536	2.304	3.072	4.608	6.144	9.216	12.288	3	6	12
32 kHz	0.512	0.768	1.024	1.536	2.048	3.072	4.096	6.144	8.192	12.288	16.384	4	8	16
48 kHz	0.768	1.152	1.536	2.304	3.072	4.608	6.144	9.216	12.288	18.432	24.576	6	12	24
96 kHz	1.536	2.304	3.072	4.608	6.144	9.216	12.288	18.432	24.576	NA	NA	12	24	NA
192 kHz	3.072	4.608	6.144	9.216	12.288	18.432	24.576	NA	NA	NA	NA	24	NA	NA

#### 6.4.7.1 Auto clock based wakeup and clock errors

TAS2120 supports flexible operating mode transition from active to shutdown and vice-verse using ASI clock auto detection feature. When `MODE[1:0]` is configured as '11' the device toggles between Active and Software shutdown state based on valid ASI clock signals applied on the ASI input pins, ie BCLK and FSYNC. If no ASI clocks are detected in this mode, the device remains in software shutdown, with software shutdown mode  $I_Q$  on VDD pin, until a valid BCLK and FSYNC clock is detected. Once a valid clock is detected, the device is powered up in active state until the clocks are valid or device is shutdown using software or hardware shutdown commands.

The device can detect and raise interrupt flags on detection of incorrect clock configurations based on status of `CLK_ERR_PWR_EN`. When this bit is set high, the device monitors for activity on the clock pins and flags any error using the latched interrupts status register. The device can also raise interrupts using IRQZ pin based on status of the corresponding interrupt MASK registers. When the error protection bit is enabled, if a clock error is detected, the device will automatically shutdown with proper shutdown sequencing and minimize any clicks and pops due to invalid clocks.

When the device is in shutdown state, the clock error detection can be delayed to provide system with time required to settle the input clocks. This power up delay in clock error detection is controlled using an internal pre-power up clock error detection timer configured by `CLK_HALT_TIMER`. If device doesn't detect a valid clock at the end of the `CLK_HALT_TIMER` expiry, the Pre-Power-up Clock error is flagged on `INT_LTCH4[2]` bit, and corresponding interrupt can be generated on IRQZ pin based on status of `INT_MASK4[2]` bit. When `MODE[1:0]` is configured as '11' (Wake-up on ASI mode), `CLK_HALT_TIMER` of '000' is not recommended and it stops the device from entering the software shutdown and increases the VDD  $I_Q$  while the device is shutdown.

Once the device is powered up, the external and internally generated clocks are constantly monitored based on status of `CLK_ERR_PWR_EN` bit. If enabled, any error in external or internal clock is flagged using the clock error status register `INT_LTCH2[3]` bit, and corresponding interrupt can be generated on IRQZ pin based on status of `INT_MASK2[3]`.

For system flexibility, the device will also set the error status for the type of detected clock error. The device can also be configured to raise an interrupt on IRQZ pin for any specific type of clock error, instead of using the generic clock error interrupt generation. [Table 6-44](#) below explains the different type of clock errors and corresponding status bits and interrupt MASK register bits. One or more register bits in the table below can be set based on the type of clock error detected.

If the device shuts down due to any type of clock error, it can attempt to re-power itself automatically when `MODE[1:0]` is set to '11'.

**Table 6-42. Clock Error detection control**

CLK_ERR_PWR_EN	Setting
0	Disabled

**Table 6-42. Clock Error detection control (continued)**

CLK_ERR_PWR_EN	Setting
1	Enabled (default)

**Table 6-43. Clock Halt Timer**

CLK_HALT_TIMER[2:0]	Setting
000	Disabled (infinite time).
001	0.8 ms (default)
010	3.2 ms
011	34.1 ms
100	68.3 ms
101	256 ms
110	768 ms
111	1.3 s

**Table 6-44. Clock error type description**

Clock error type	Description	Status flag register bit	IRQZ generation Mask bit
Clock error	Clock error for any internal or external clocking configuration errors. This bit will be set along with specific clock errors detected in the rest of the table below except for Pre-Power-up Clock errors.	INT_LTCH2[3]	INT_MASK2[3]
Pre-Power-up Clock error	Clock error detected during shutdown mode after clock error is detected at end of CLK_HALT_TIMER.	INT_LTCH4[2]	INT_MASK4[2]
Clock ratio change error	Clock error detected due to on the fly change in FSYNC to SBCLK ratio.	INT_LTCH2[2]	INT_MASK2[2]
Fs change error	Clock error detected due to on the fly change in FSYNC clock frequency	INT_LTCH2[1]	INT_MASK2[1]
Fs invalid error	Clock error detected due to incorrect FSYNC clock frequency	INT_LTCH2[0]	INT_MASK2[0]
Frame out of sync	Clock error detected due to Frame out of sync	INT_LTCH2[5]	INT_MASK2[5]
Internal PLL Clock error	Clock error detected due to internally generated clock frequency error.	INT_LTCH2[4]	INT_MASK2[4]

The device also has a digital watchdog timer which monitors for errors in the internal digital state machine and shuts down the device on detection of such errors. This error can also raise an interrupt on IRQZ pin and flag to the host device of the error state.

#### 6.4.8 Digital IO pins

TAS2120 supports 1.8V and 3.3V IO voltage supply based on the voltage applied on the IOVDD pin.

I2S digital input pin has an optional weak pull down to prevent the pin from floating. Pull downs are not enabled during HW shutdown. The pull downs are disabled by default and can be enabled by setting the corresponding Pull down enable bit high.

**Table 6-45. Digital pin weak pull down**

Pin Name	Pull down control register name
SDOUT	SDOUT_PD_EN
SDIN	SDIN_PD_EN
FSYNC	FSYNC_PD_EN
SBCLK	SBCLK_PD_EN

## 6.5 Programming

The device contains configuration registers and programming coefficients that can be set to the desired values for a specific system and application use. These registers are called device control registers and are each eight bits in width, mapped using a page scheme.

Each page contains 128 configuration registers. All key device configuration registers are stored in page 0, which is the default page setting at power up and after a software reset. All programmable coefficient registers are located in page 2, page 3 and later pages. The current page of the device can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

### 6.5.1 I<sup>2</sup>C Control Interface

The device supports the I<sup>2</sup>C control protocol as a target device, and is capable of operating in standard mode, fast mode, and fast mode plus. Device configuration and status are provided via the SDA and SCL pins using the I<sup>2</sup>C protocol.

### 6.5.2 I<sup>2</sup>C Address Selection

The TAS2120 can operate using one of four selectable device addresses. I<sup>2</sup>C target addresses is defined as the 7 MSBs followed by read/write bit. [Table 6-46](#) below illustrates how to select the device I<sup>2</sup>C address and the address corresponds to R/W bit set to 0 (ie ADDR[6:0],1b'0). The I<sup>2</sup>C address is detected by sampling the address pins when SDZ pin is released or when device is reset using software reset bit.

**Table 6-46. I<sup>2</sup>C Mode Address Selection**

I <sup>2</sup> C TARGET ADDRESS	AD2 PIN	AD1 PIN
0x80 (global address)	NA	NA
0x90	GND	GND
0x92	GND	IOVDD
0x94	IOVDD	GND
0x96	IOVDD	IOVDD

The TAS2120 has a global 7-bit I<sup>2</sup>C address 0x40 (0x80 in 8-bit format with R/W bit set to 0). When enabled the device will additionally respond to I<sup>2</sup>C commands at this address regardless of the address pins selected. This is used to speed up device configuration when using multiple TAS2120 devices and programming similar settings across all devices. The I<sup>2</sup>C ACK / NACK cannot be used during the multi-device writes since multiple devices are responding to the I<sup>2</sup>C command. The I<sup>2</sup>C CRC function should be used to ensure each device properly received the I<sup>2</sup>C commands. At the completion of writing multiple devices using the global address, the CRC at *I2C\_CKSUM* register should be checked on each device using the local address for a proper value. The global I<sup>2</sup>C address can be disabled using *I2C\_GBL\_EN* register.

**Table 6-47. I<sup>2</sup>C Global Address Enable**

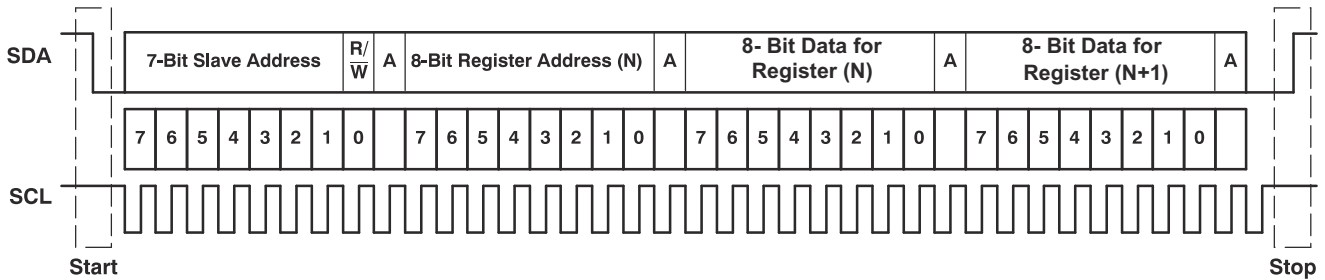
<i>I2C_GBL_EN</i>	SETTING
0	Disabled
1	Enabled (default)

### 6.5.3 General I<sup>2</sup>C Operation

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred MSB first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the controller device driving a start condition on the bus and ends with the controller device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The controller device drives a start condition followed by the 7-bit target address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledgment condition. The target device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the controller device transmits the next byte of the sequence. Each target device is addressed by a unique 7-bit target address plus the R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the controller device generates a stop condition to release the bus. Figure 6-10 shows a generic data transfer sequence.



**Figure 6-10. Typical I<sup>2</sup>C Sequence**

In the system, use external pullup resistors for the SDA and SCL signals to set the logic high level for the bus. The SDA and SCL voltages must not exceed the device supply voltage, IOVDD.

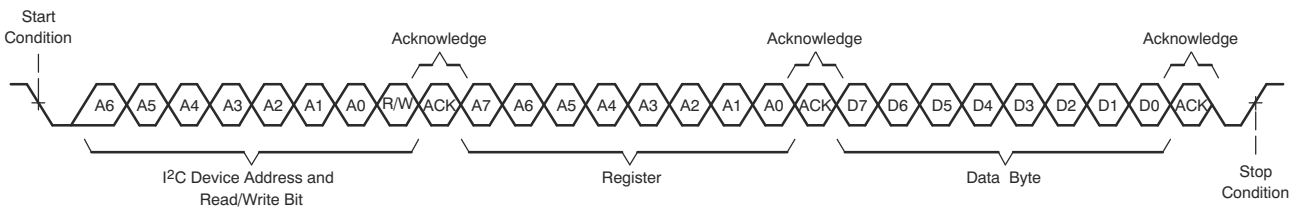
#### 6.5.4 I<sup>2</sup>C Single-Byte and Multiple-Byte Transfers

The device I<sup>2</sup>C interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the device responds with data, a byte at a time, starting at the register assigned, as long as the controller device continues to respond with acknowledges.

The device supports sequential I<sup>2</sup>C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I<sup>2</sup>C write transaction takes place. For I<sup>2</sup>C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many registers are written.

#### 6.5.5 I<sup>2</sup>C Single-Byte Write

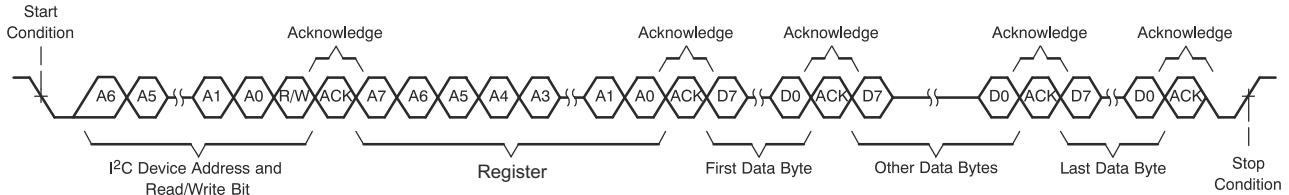
As shown in Figure 6-11, a single-byte data write transfer begins with the controller device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I<sup>2</sup>C target address and the read/write bit, the device responds with an acknowledge bit (ACK). Next, the controller device transmits the register byte corresponding to the device internal register address being accessed. After receiving the register byte, the device again responds with an acknowledge bit (ACK). Then, the controller transmits the byte of data to be written to the specified register. When finished, the target device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition to complete the single-byte data write transfer.



**Figure 6-11. I<sup>2</sup>C Single-Byte Write Transfer**

### 6.5.6 I<sup>2</sup>C Multiple-Byte Write

As shown in Figure 6-12, a multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the controller device to the target device. After receiving each data byte, the device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition after the last data-byte write transfer.

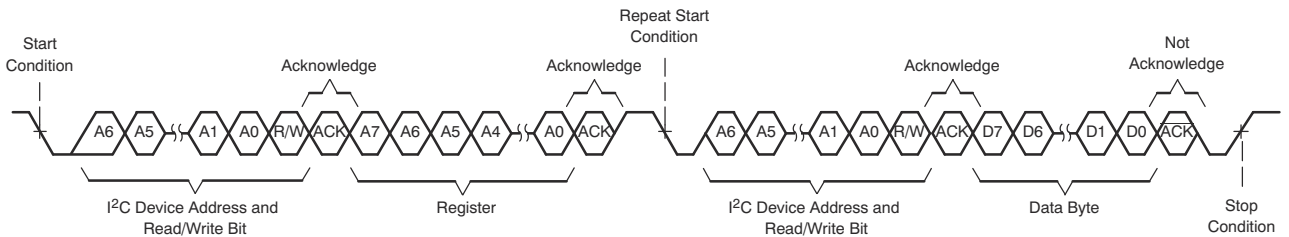


**Figure 6-12. I<sup>2</sup>C Multiple-Byte Write Transfer**

### 6.5.7 I<sup>2</sup>C Single-Byte Read

As shown in Figure 6-13, a single-byte data read transfer begins with the controller device transmitting a start condition followed by the I<sup>2</sup>C target address and the read/write bit. For the data read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte of the internal register address to be read. As a result, the read/write bit is set to 0.

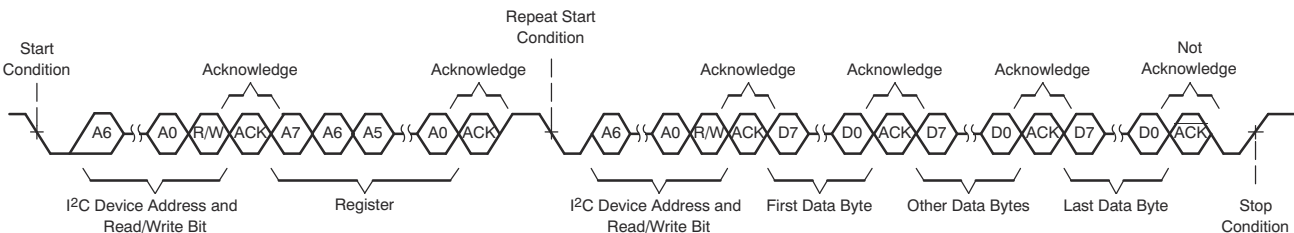
After receiving the target address and the read/write bit, the device responds with an acknowledge bit (ACK). The controller device then sends the internal register address byte, after which the device issues an acknowledge bit (ACK). The controller device transmits another start condition followed by the target address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the device transmits the data byte from the register address being read. After receiving the data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the single-byte data read transfer.



**Figure 6-13. I<sup>2</sup>C Single-Byte Read Transfer**

### 6.5.8 I<sup>2</sup>C Multiple-Byte Read

As shown in Figure 6-14, a multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the device to the controller device. With the exception of the last data byte, the controller device responds with an acknowledge bit after receiving each data byte. After receiving the last data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the data read transfer.



**Figure 6-14. I<sup>2</sup>C Multiple-Byte Read Transfer**



## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Application Information

TAS2120 is a mono channel digital-in Class-D amplifier with integrated Boost, battery voltage and temperature monitoring capabilities. I<sup>2</sup>S audio data is supplied by host processor via SDIN data port along with the bit clock and frame sync signals. I<sup>2</sup>C bus is used for configuration and control.

The device needs external power supply voltage rails of VBAT: 2.5V to 5.5V, VDD : 1.65V to 1.95V and IOVDD: 1.8V or 3.3V for operation.

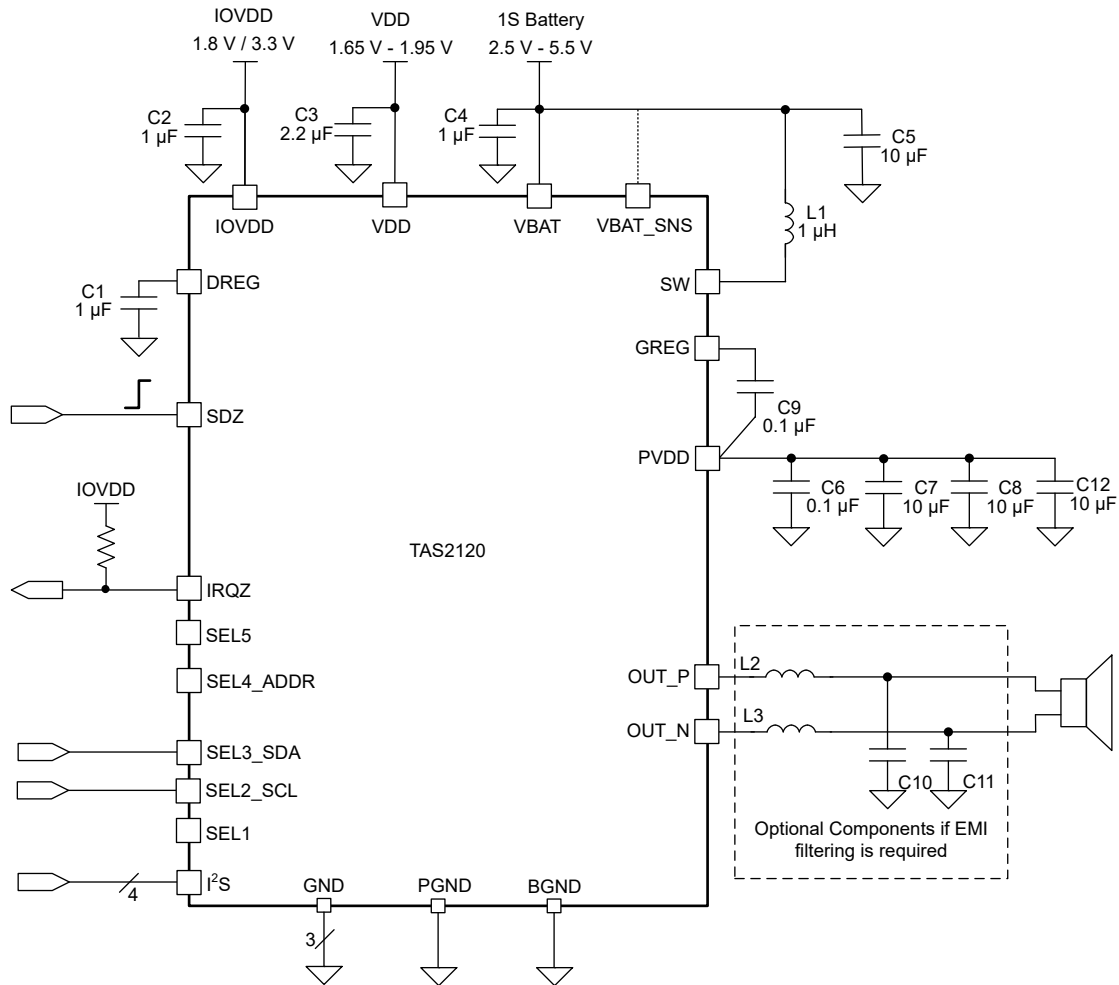
PurePath™ Console 3 (PPC3) software is the recommended tool to configure the device, and it enables optimization of device performance parameters depending on different application scenarios.

### 7.2 Typical Application

Diagrams below shows the typical application connections for 1S and 2S Li-Ion battery and for the external PVDD or 3S Battery connection. VBAT\_SNS pin connection is optional and if not used, this pin should be grounded. SEL1 is used for HW Mode selection or I<sup>2</sup>C Mode selection of the Device.

System can use same 1.8V supply source to power the IOVDD and VDD if required. The decoupling caps C2 and C3 should still be placed close to the device pins.

VBAT, VDD, PVDD power rails are critical for device performance and wide trace should be used from the source PMIC to these pins to minimize parasitic inductance. Supply ripple should be kept at minimum for these rails and should be connected to common supply planes.



**Figure 7-1. Application Diagram for 1S Battery system**

**ADVANCE INFORMATION**

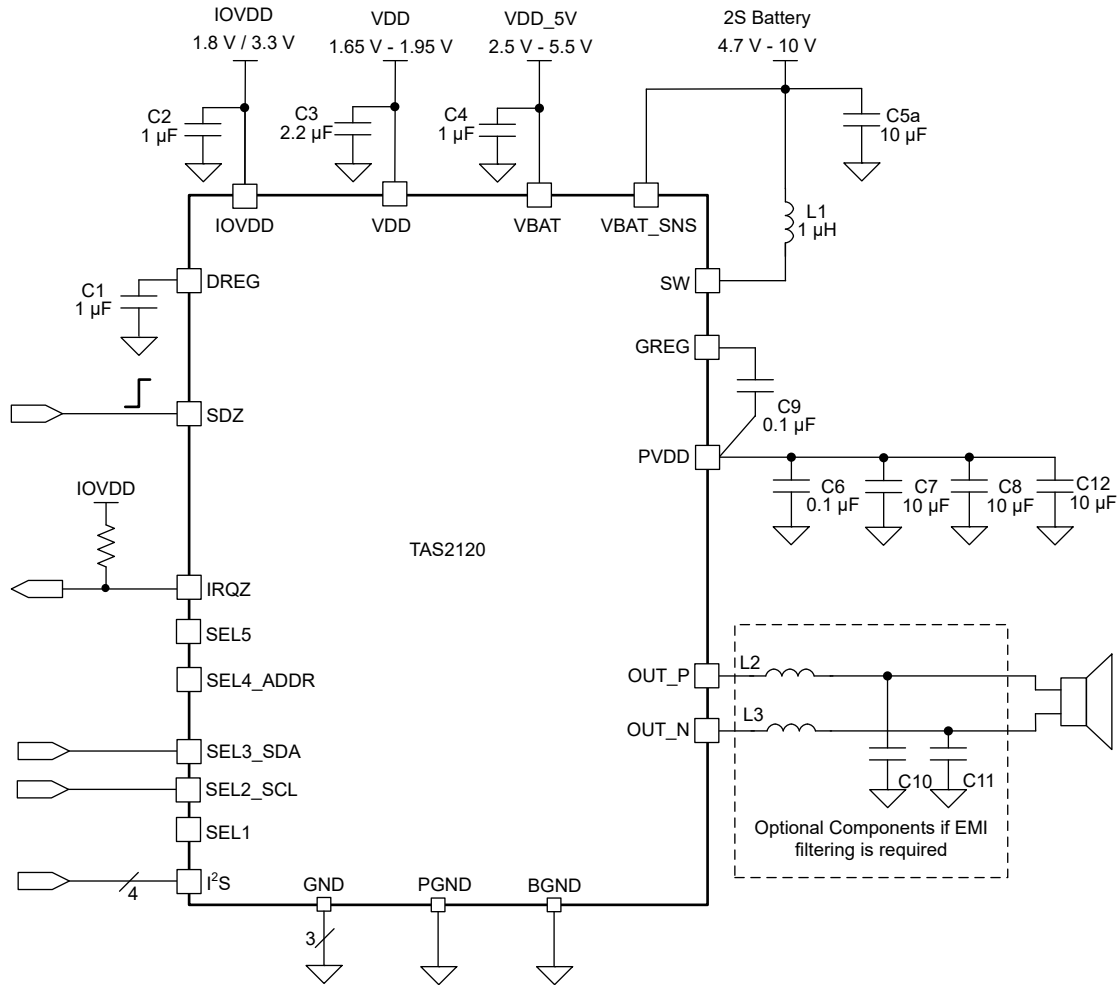
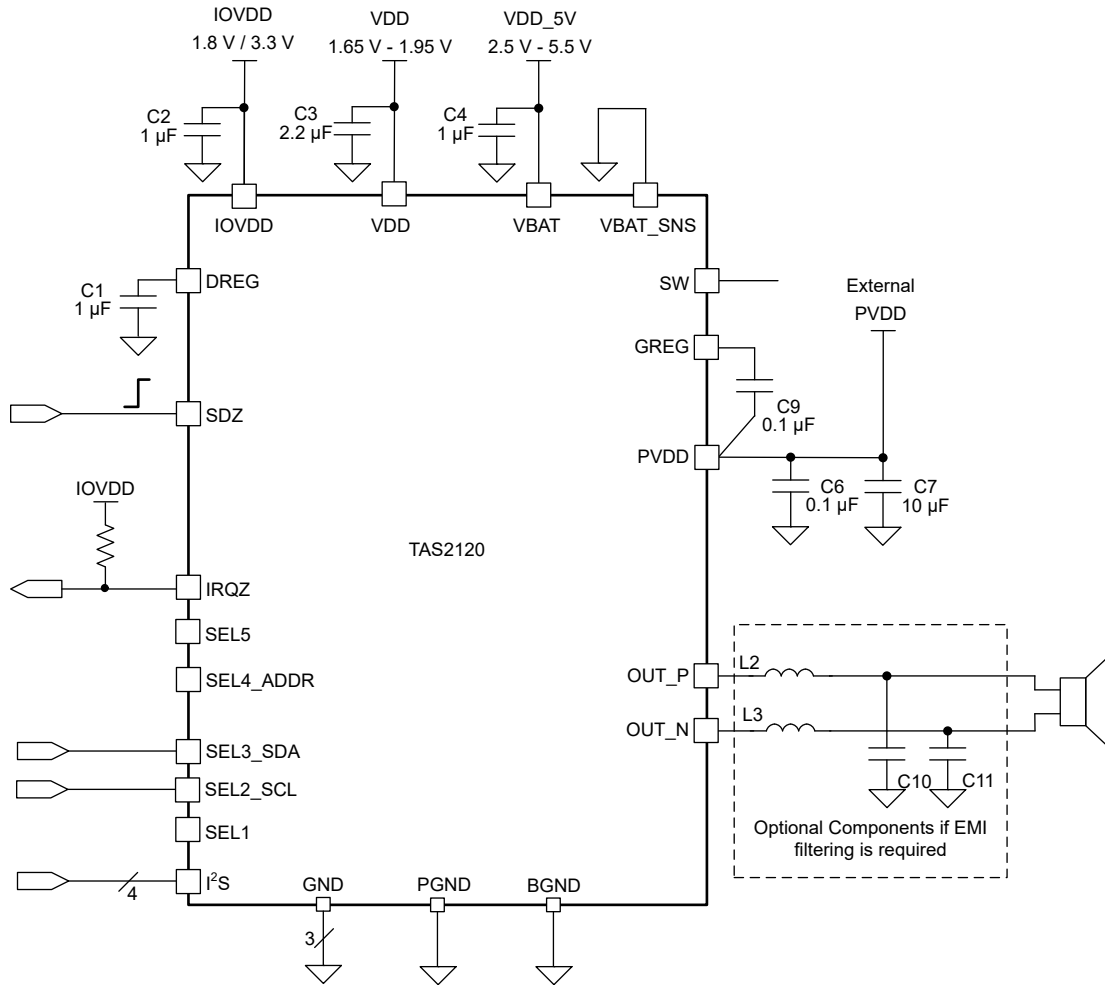


Figure 7-2. Application Diagram for 2S Battery system



**Figure 7-3. Application Diagram for External PVDD or 3S Battery system**

**ADVANCE INFORMATION**

**Table 7-1. Recommended External Components**

Component	Description	Specification	Min	Typ	Max	Unit
L1	Boost Convertor Inductor	Inductance, 20% Tolerance	0.47	1		μH
		Saturation current		5.3		A
L2, L3	Optional EMI Filter Inductors (must use C10, C11 if L2, L3 are used)	DC Current	2			A
C1, C2	DREG, IOVDD decap	Capacitance, 20% tolerance		1		μF
		Voltage rating	2	6.3		V
C3	VDD decap	Capacitance, 20% tolerance		2.2		μF
		Voltage rating	2	6.3		V
C4	VBAT decap	Capacitance, 20% tolerance		1		μF
		Voltage rating	6.3	10		V
C5	1S Battery Power decap	Capacitance, 20% tolerance		10		μF
		Voltage rating	6.3	10		V
C5a	2S Battery Power decap	Capacitance, 20% tolerance		10		μF
		Voltage rating	10	16		V
C6	PVDD Low ESL decap	Capacitance, 20% tolerance		0.1		μF
		Voltage rating	16	25		V
C7, C8, C12	PVDD Power decap	Capacitance, 20% tolerance		10		μF
		Voltage rating	16	25		V
		Effective total PVDD Capacitance at 13V DC after deratings for 1S battery systems	3			μF
		Effective total PVDD Capacitance at 13V DC after deratings for 2S battery system <i>Note: C12 is not required for 2S system to meet the derating spec.</i>	2			μF
C9	GREG decap	Capacitance, 20% tolerance		0.1		μF
		Voltage rating	6.3	10		V
C10, C11	Optional EMI Filter capacitors (must use L2, L3 if C10, C11 are used)	Voltage rating	2xPVDD			V

ADVANCE INFORMATION

### 7.2.1 Design Requirements

Table 7-1 lists the BOM components required for the application. Table 7-2 lists other requirements for the application.

**Table 7-2. Design Parameters**

PARAMETER	CONDITION	SPECIFICATION
VDD supply current <sup>(1)</sup>	VDD Y-bridge disabled, 48ksps mode, all blocks enabled	< 15mA
	VDD Y-bridge disabled, 96ksps mode, all blocks enabled	< 20mA
IOVDD supply current	1.8V mode	< 1mA
	3.3V mode	< 1mA

**Table 7-2. Design Parameters (continued)**

PARAMETER	CONDITION	SPECIFICATION
VBAT supply current	1S or 2S mode of operation. <i>Note:</i> Current only through device VBAT pin, and not battery current taken through Boost inductor/SW pin.	< 10mA

- (1) When VDD Y-bridge is enabled, additional power taken from VDD supply based on the selected switchover threshold voltage and the output load impedance.

## 7.2.2 Detailed Design Procedure

(2)

### 7.2.2.1 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See [Section 6.5.2](#) for information on changing the I<sup>2</sup>C address of the TAS2120 to support stereo or multi-channel operation. Mono or stereo configuration does not impact the device performance.

### 7.2.2.2 Boost Converter Passive Devices

The boost converter requires multiple passive devices that are labeled L1, C7, C8, C12 in [Section 7.2](#) and whose specifications are provided in [Table 7-1](#). These specifications are based on the design of the TAS2120 and are necessary to meet the performance targets of the device. In particular, L1 should not be allowed to enter in the current saturation region. The saturation current ( $I_{SAT}$ ) for L1 should be  $> (I_{LIM} + 5\%)$  to deliver Class-D peak power.  $I_{SAT}$  and  $I_{LIM}$  values should be selected based on peak output power required in the application.

Additionally, the ratio of L1/C (the derated value of C7,C8,C12) has to be less than 1/3 for boost stability. This ratio is relaxed to 1/2 in 2S battery mode of operation. This ratio should be maintained including the worst case variation of boost inductor and output capacitors.

To satisfy sufficient energy transfer, L1 needs to be  $\geq 0.47\mu\text{H}$  at the boost switching frequency (100kHz to 4MHz). Using a  $0.47\mu\text{H}$  will help in reducing the capacitor requirements and save board space, but comes at the cost of increased voltage ripple on VBAT and reduces average input current and hence max  $P_{OUT}$  of the device. High PSRR of TAS2120 should minimize the effect from the additional ripple on VBAT supply.

The L1 inductor series resistance (ESR) is another critical parameter to be selected in the application. Lower ESR reduces power loss and helps in improving overall system efficiency. Based on available board space, smallest ESR inductors which meet the application needs will give better efficiency performance.

### 7.2.2.3 EMI Passive Devices

The TAS2120 supports edge-rate control to minimize EMI, but the system designer may want to include passive devices on the Class-D output for further reduction in EMI. These passive devices that are labeled L2, L3, C10 and C11 in [Section 7.2](#). If C10 and C11 are used, L2 and L3 must also be installed, and C10 and C11 must be placed after L2 and L3 respectively to maintain the stability of the output stage.

The component value selection for the EMI filters depends on the application need on the frequency band that needs to be suppressed using these filters. Higher cutoff frequency helps in reducing the BOM size and reduces the switching power loss associated with the filters. Application should select the highest cutoff frequency filter which will meet the system's frequency suppression target to get better efficiency performance.

The DC resistance of the inductors or ferrite beads used in the EMI filters also plays a critical role in system efficiency. Lower resistance reduces power loss and helps in improving overall system efficiency. Based on available board space, smallest DC resistance components which meet the application needs will give better efficiency performance.

### 7.2.2.4 Miscellaneous Passive Devices

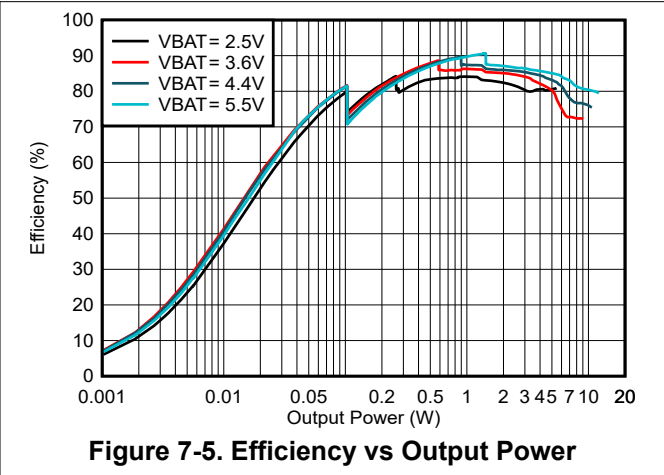
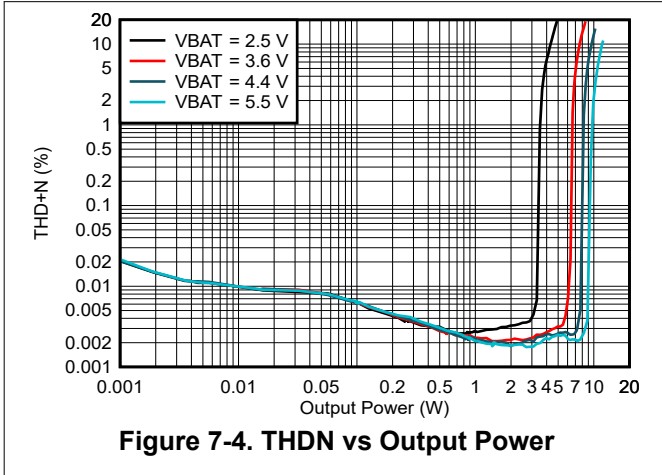
The GREG Capacitor requires 100 nF to meet boost and Class-D power delivery and efficiency specs. For device functionality, the GREG capacitor should be kelvin/star connected to PVDD pin of the device.

In order to maintain the device performance and keep the supply ripple within the device specification, minimizing the parasitic inductance on supply/ground paths for decoupling capacitors is required. All supply decapacitors should be selected as smallest package footprint to minimize the ESL of the capacitors. The layout placement and routing of the capacitors is critical for minimizing the trace parasitic inductance. Refer to Layout section ([Section 9.1](#)) to get detailed recommendations.



### 7.2.3 Application Performance Plots

$T_A = 25\text{ }^\circ\text{C}$ ,  $V_{BAT} = 3.6\text{ V}$ ,  $V_{DD} = 1.8\text{ V}$ ,  $I_{OVDD} = 1.8\text{ V}$ , Load =  $8\ \Omega + 33\ \mu\text{H}$ ,  $L_{BOOST} = 1\ \mu\text{H}$ ,  $F_{IN} = 1\text{ kHz}$ ,  $F_s = 48\text{ kHz}$ , Gain = 21dBV,  $BST\_ILIM = 5.1\text{ A}$ ,  $SDZ = 1$ , Noise gate mode disabled, Measured on EVM with typical application use case (Section 7.2). Measured filter free with an Audio Precision with a 22Hz to 20kHz un-weighted bandwidth, unless otherwise noted.



## 8 Power Supply Recommendations

TAS2120 supports supply voltages to ramp up/down in any order of sequence for the externally supplied voltages on VDD, IOVDD, VBAT and PVDD(for external PVDD mode).

SDZ pin must be held low when supplies are not in stable operating condition. Once all the supplies are stable, SDZ pin can be asserted high for device to start operating. SDZ pin must be pulled low before any supply is ramped down below its recommended operating voltage.

If using the device in external PVDD mode, the SW pad must be kept floating.

Once all the supplies are valid and SDZ pin is released to high, the digital core voltage regulator powers up, and starts the internal initialization sequence. After a hardware or software reset, additional i2c commands to the device should be delayed by at-least 300us to allow the device internal blocks to be initialized.

## 9 Layout

### 9.1 Layout Guidelines

- Use wide traces for signals that carry high current and avoid VIAs wherever possible. If VIAs can't be avoided, multiple VIAs should be added to enable low parasitic inductance and high current capability. These include traces for PVDD, VBAT, VDD, PGND, BGND, GND, OUT\_P and OUT\_N.
- PGND and BGND signals should be directly connected and shorted to the ground plane of board to minimize parasitic inductance. Common inductance between ground pins (eg GND and PGND or GND and BGND common routing) before connecting to ground plane should be avoided.
- The coupling between high switching signal traces like OUT\_P, OUT\_N, SW should be avoided from sensitive low voltage signals.
- Minimize capacitance between high switching lines like OUT\_P, OUT\_N, SW to ground/static nodes. Larger capacitance will result in efficiency drop. Coupling between OUT\_P and OUT\_N will also cause degraded efficiency.
- VBAT routing to the boost inductor and the device VBAT pin should be star connected to the common VBAT supply plane. Ensure the decoupling capacitor C4 is placed close to the device and decoupling capacitor C5 is placed close to the inductor.
- Place the boost inductor between VBAT and SW close to the device terminal with no VIAs between device terminal and the inductor. VBAT routing to the boost inductor should be routed with minimal routing resistance to achieve best performance from device.
- Decoupling capacitors should be placed close to the device. Smallest possible package size is recommended for the decaps to achieve best performance from device. DREG, VDD, IOVDD, VBAT (C4 cap), PVDD low ESL (C6 cap) are recommended to be 0201 case size or lower. VIAs between decapacitors and device pins should be avoided, or multiple VIAs added to minimize parasitic inductances.
- All decoupling capacitor's ground terminal should be strongly connected to the ground plane with multiple ground VIAs. The ground routing loop between the cap ground and the device ground pins should be minimized.
- For VDD Y-bridge functionality, the routing from the host PMIC to the device VDD should be wide supply plane trace with minimal routing parasitic inductance.
- For the capacitor between GREG-PVDD (C9 cap), PVDD side of capacitor should not be connected directly to the PVDD decoupling capacitors (C6, C7 and C8), and should be connected as close as possible to the device PVDD pin.
- In external PVDD mode of operation, SW pin should be left floating and not connected to any supply or ground signals.

## 9.2 Layout Example

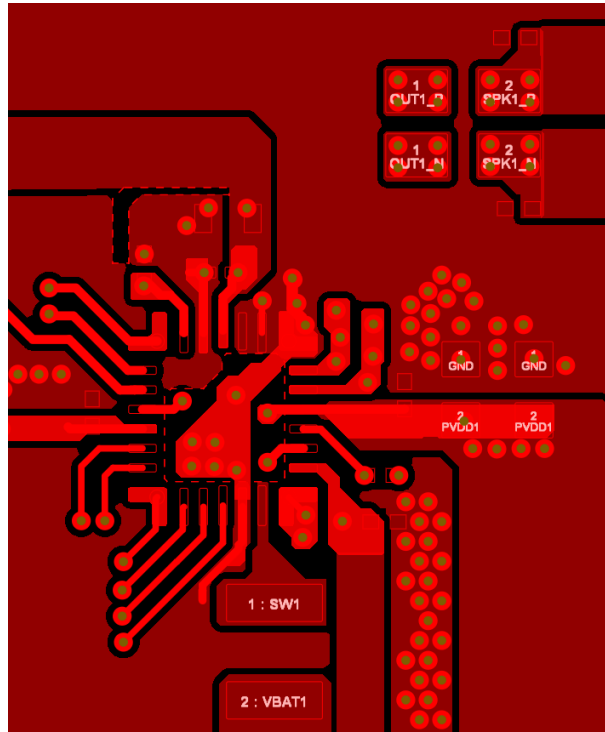


Figure 9-1. Example Layout Top

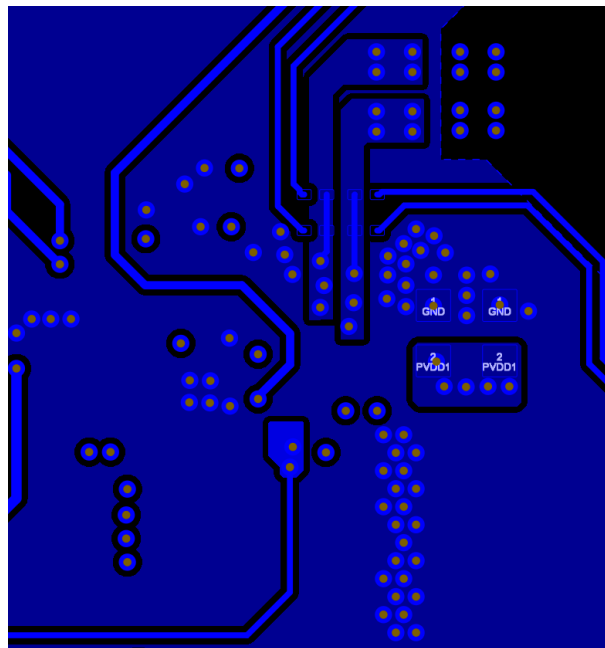


Figure 9-2. Example Layout Bottom

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 10.1 Documentation Support

### 10.1.1 Related Documentation

For related documents see the following

- Texas Instruments, [Purepath Console 3 \(PPC3\) Software](#)

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

## 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2024	*	Initial Release

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 12.1 Package Option Addendum

### Packaging Information

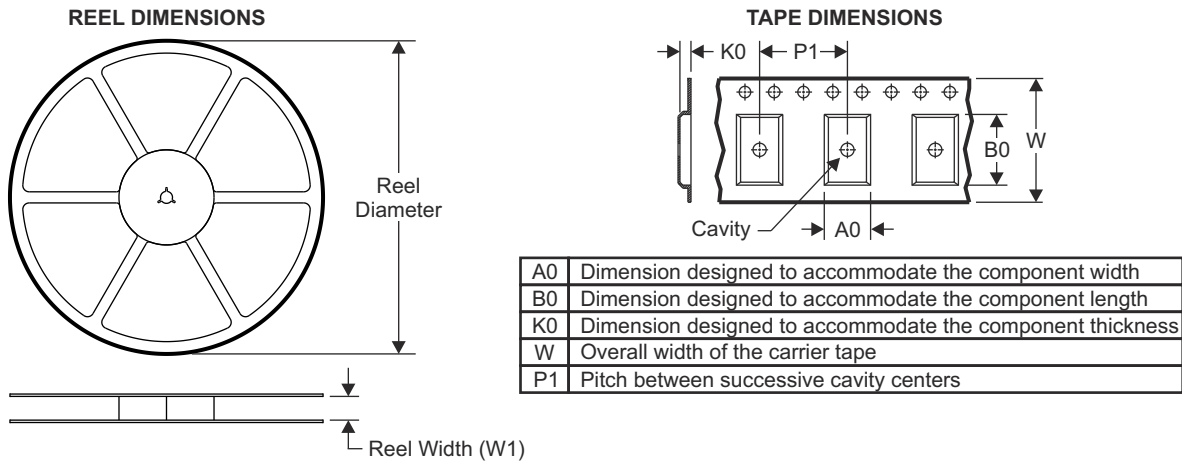
Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish <sup>(6)</sup>	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4) (5)</sup>
PTAS2120RBGR	ACTIVE	VQFN-HR	RBG	26	3000	RoHS & Green	NiPdAu	Level-1-260C -UNLIM	-40 to 85	PTS2X20

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

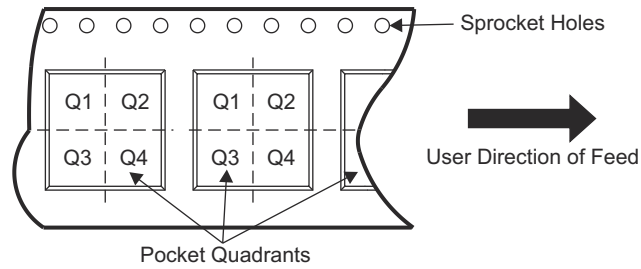
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## 12.2 Tape and Reel Information



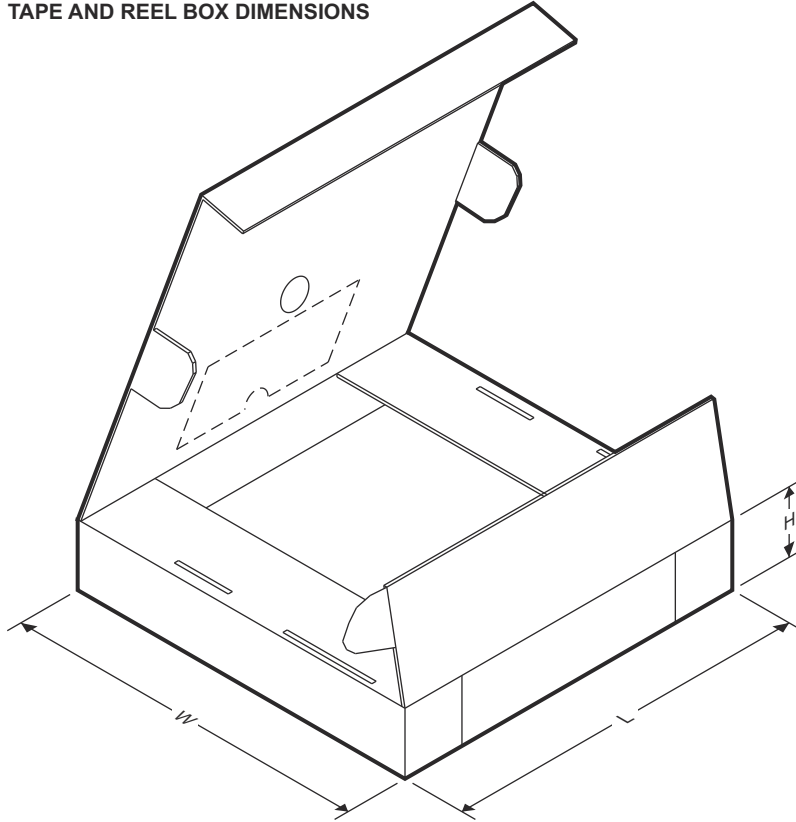
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTAS2120RBGR	VQFN-HR	RBG	26	3000	330	12.4	3.8	4.3	1.5	8	12	Q1

**ADVANCE INFORMATION**

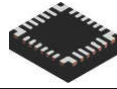
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTAS2120RBGR	VQFN-HR	RGB	26	3000	360.0	360.0	35

ADVANCE INFORMATION

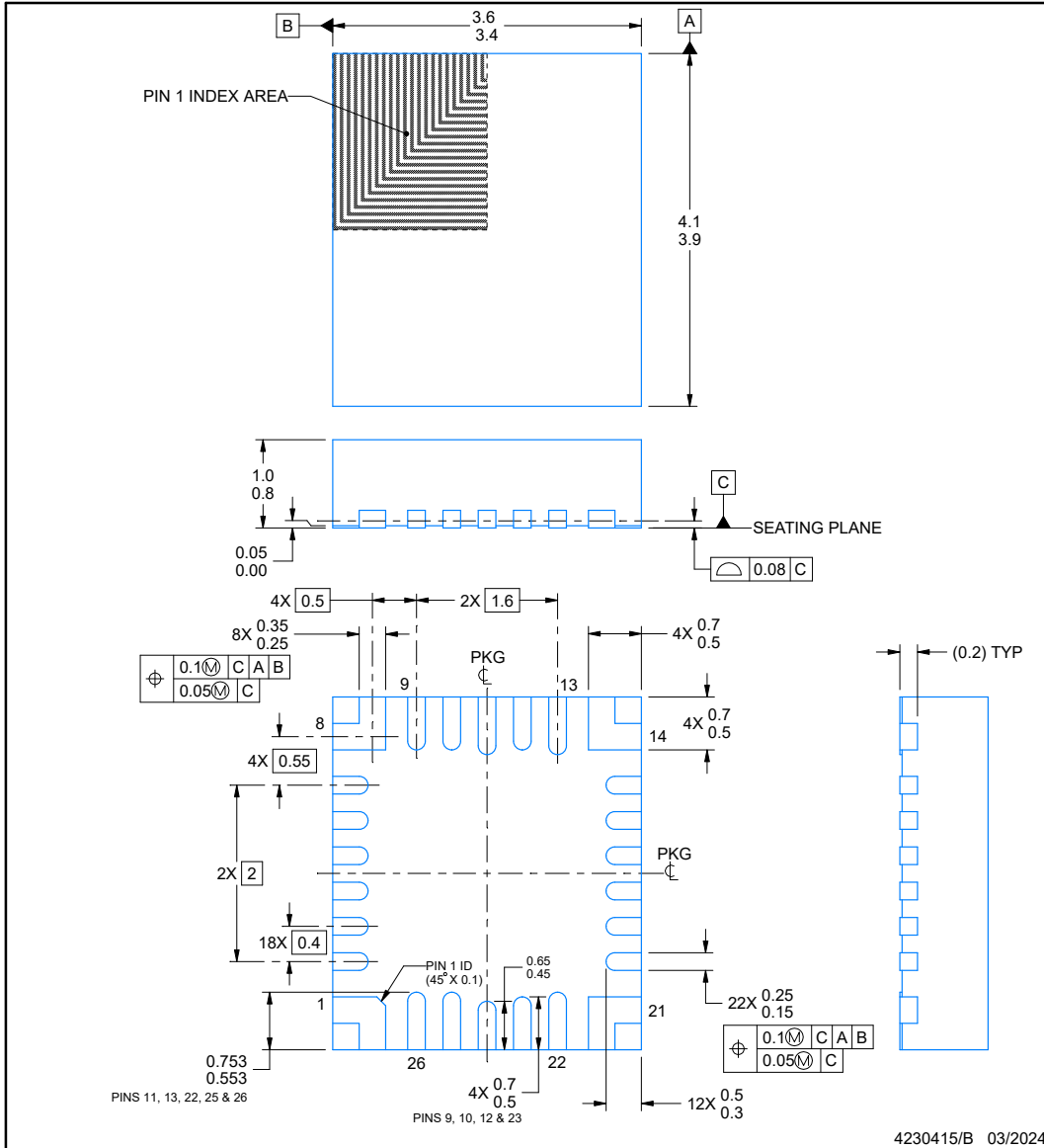




**RBG0026A**

**PACKAGE OUTLINE**  
**VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

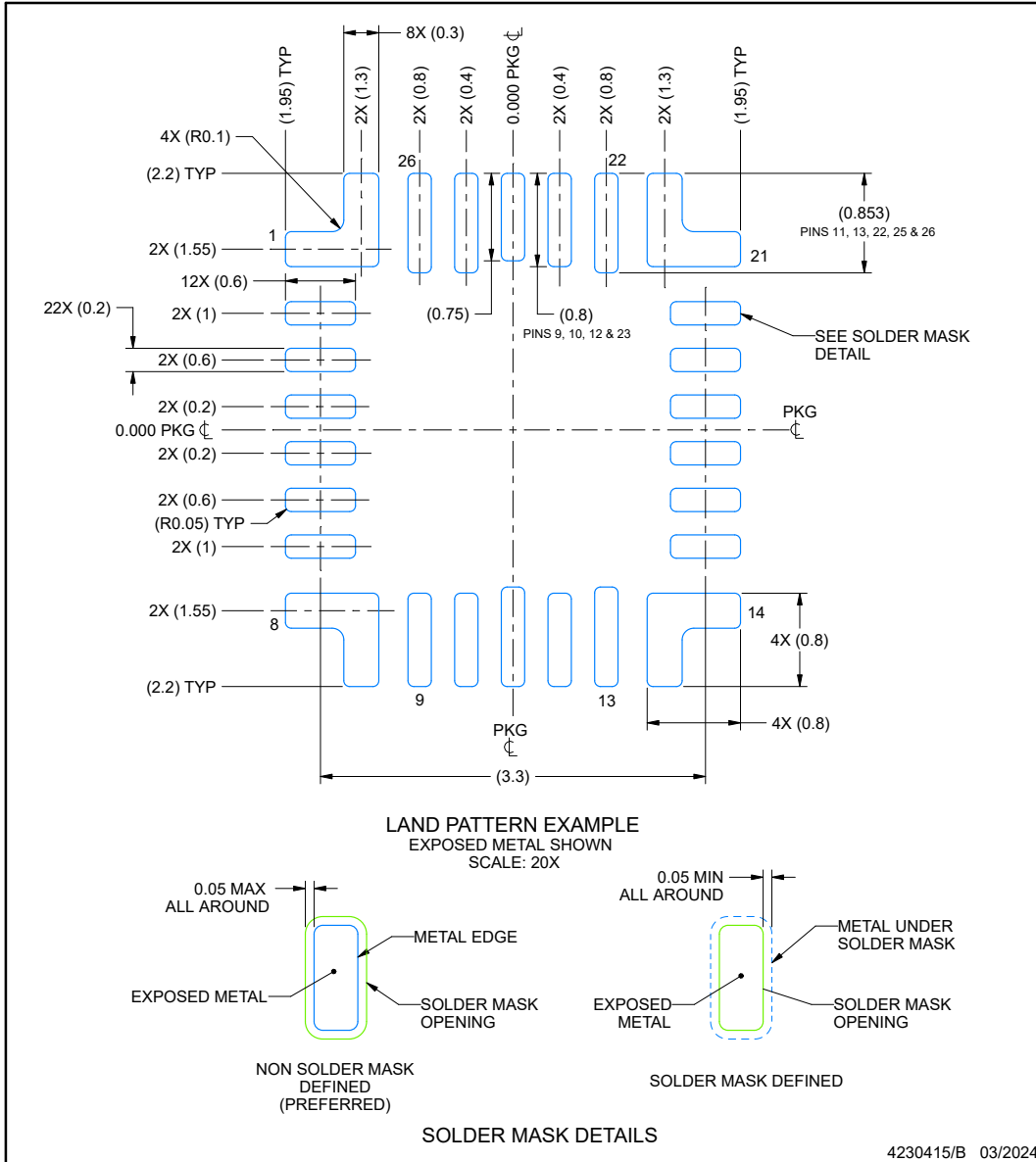
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

**EXAMPLE BOARD LAYOUT**

**RBG0026A**

**VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

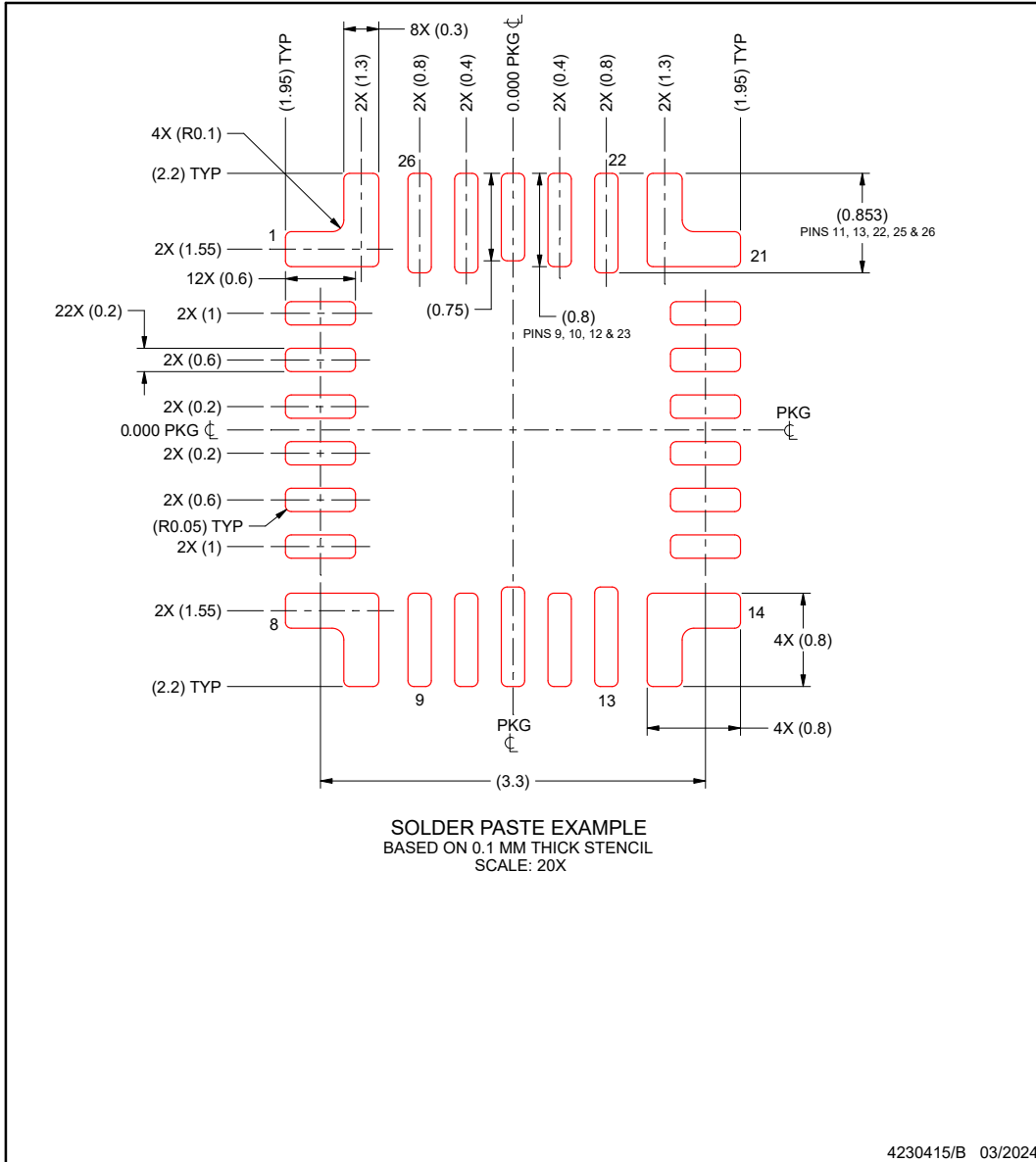
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

**EXAMPLE STENCIL DESIGN**

**RBG0026A**

**VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**ADVANCE INFORMATION**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTAS2120RBGR	ACTIVE	VQFN-HR	RBG	26	3000	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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