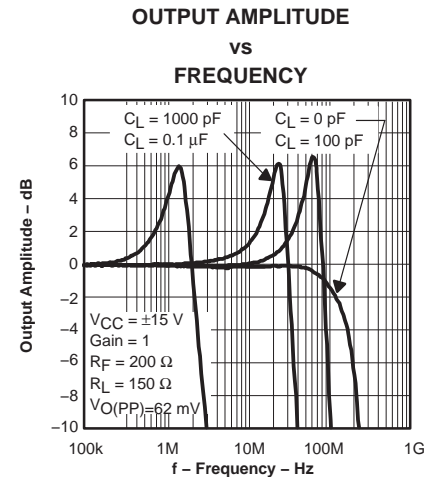
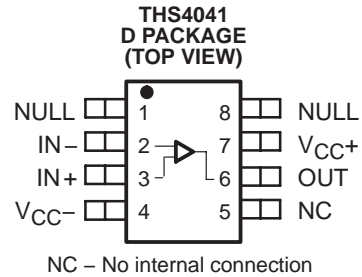


THS4041-Q1 165-MHz C-STABLE HIGH-SPEED AMPLIFIER

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- Qualified for Automotive Applications
- C-Stable Amplifier Drives Any Capacitive Load
- High Speed
 - 165 MHz Bandwidth (–3 dB); $C_L = 0$ pF
 - 100 MHz Bandwidth (–3 dB); $C_L = 100$ pF
 - 35 MHz Bandwidth (–3 dB); $C_L = 1000$ pF
 - 400 V/ μ s Slew Rate
- Unity Gain Stable
- High Output Drive, $I_O = 100$ mA (typ)
- Low Distortion
 - THD = –75 dBc ($f = 1$ MHz, $R_L = 150$ Ω)
 - THD = –89 dBc ($f = 1$ MHz, $R_L = 1$ k Ω)
- Wide Range of Power Supplies
 - $V_{CC} = \pm 5$ V to ± 15 V
- Evaluation Module Available



description/ordering information

The THS4041 is a single, high-speed voltage feedback amplifier capable of driving any capacitive load. This makes it ideal for a wide range of applications including driving video lines or buffering ADCs. The device features high 165-MHz bandwidth and 400-V/ μ s slew rate. The THS4041 is stable at all gains for both inverting and noninverting configurations. For video applications, the THS4041 offers excellent video performance with 0.01% differential gain error and 0.01° differential phase error. This amplifier can drive up to 100 mA into a 20- Ω load and operate off power supplies ranging from ± 5 V to ± 15 V.

ORDERING INFORMATION†

T_A	NUMBER OF CHANNELS	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	1	SOIC (D)	Tape and Reel	THS4041IDRQ1	4041Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



CAUTION: The THS4041 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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functional block diagram

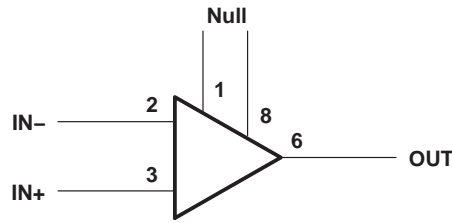


Figure 1. THS4041 – Single Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC}	± 16.5 V
Input voltage, V_I	$\pm V_{CC}$
Output current, I_O	150 mA
Differential input voltage, V_{IO}	± 4 V
Maximum junction temperature, T_J (see Figure 2)	150°C
Package thermal impedance, θ_{JA} (see Note 1)	215°C/W
Operating free-air temperature, T_A : I-suffix	-40°C to 85°C
Storage temperature, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 3 seconds	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC proposed High-K test PCB, the θ_{JA} is 126°C/W.

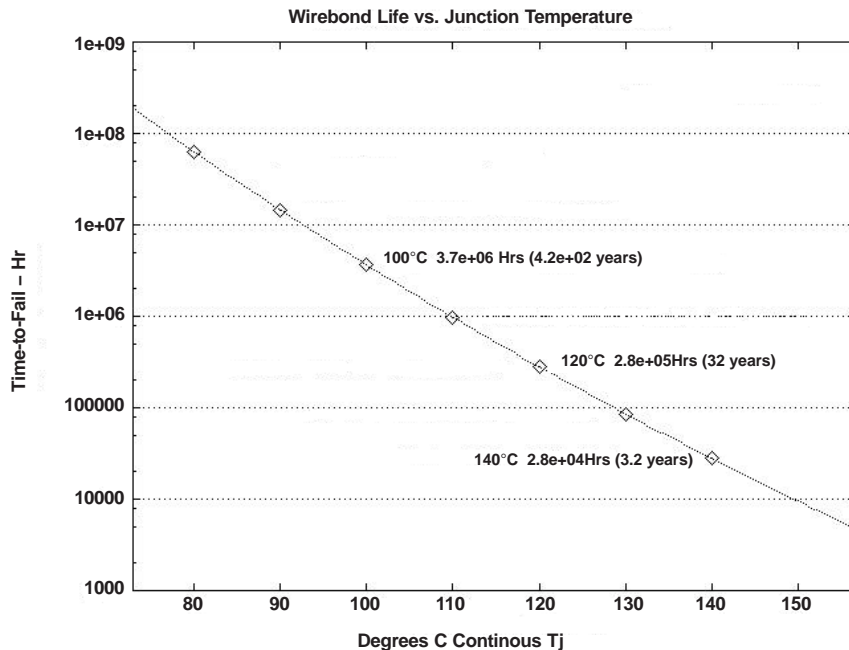


Figure 2. Estimated Wirebond Life

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	I-suffix	-40		85	°C

electrical characteristics at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, $R_L = 150\ \Omega$ (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
BW	Dynamic performance small-signal bandwidth (-3 dB)	$V_{CC} = \pm 15\text{ V}$	$R_f = 200\ \Omega$	Gain = 1	165		MHz
			$R_f = 200\ \Omega$		150		
		$V_{CC} = \pm 15\text{ V}$	$R_f = 1.3\text{ k}\Omega$	Gain = 2	60		MHz
			$R_f = 1.3\text{ k}\Omega$		60		
	Bandwidth for 0.1 dB flatness	$V_{CC} = \pm 15\text{ V}$	$R_f = 200\ \Omega$	Gain = 1	45		MHz
			$R_f = 200\ \Omega$		45		
Full power bandwidth§		$V_{O(pp)} = 20\text{ V}$, $V_{CC} = \pm 15\text{ V}$		6.3		MHz	
		$V_{O(pp)} = 5\text{ V}$, $V_{CC} = \pm 5\text{ V}$		20			
SR	Slew rate‡	$V_{CC} = \pm 15\text{ V}$, 20-V step,	Gain = 5	400		V/ μs	
		$V_{CC} = \pm 5\text{ V}$, 5-V step,	Gain = -1	325			
t_s	Settling time to 0.1%	$V_{CC} = \pm 15\text{ V}$, 5-V step	Gain = -1	120		ns	
				$V_{CC} = \pm 5\text{ V}$, 2-V step	120		
	Settling time to 0.01%	$V_{CC} = \pm 15\text{ V}$, 5-V step	Gain = -1	250		ns	
				$V_{CC} = \pm 5\text{ V}$, 2-V step	280		

† Full range = -40°C to 85°C for I suffix

‡ Slew rate is measured from an output level range of 25% to 75%.

§ Full power bandwidth = slew rate / $2\pi V_{O(Peak)}$.

noise/distortion performance

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	$V_{O(pp)} = 2\text{ V}$, $f = 1\text{ MHz}$, Gain = 2	$V_{CC} = \pm 15\text{ V}$	$R_L = 150\ \Omega$	-75		dBc
				$R_L = 1\text{ k}\Omega$	-89		
			$V_{CC} = \pm 5\text{ V}$	$R_L = 150\ \Omega$	-75		
				$R_L = 1\text{ k}\Omega$	-86		
V_n	Input voltage noise	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$,	$f = 10\text{ kHz}$		14		nV/ $\sqrt{\text{Hz}}$
I_n	Input current noise	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$,	$f = 10\text{ kHz}$		0.9		pA/ $\sqrt{\text{Hz}}$
	Differential gain error	Gain = 2, 40 IRE modulation,	NTSC, $\pm 100\text{ IRE ramp}$	$V_{CC} = \pm 15\text{ V}$	0.01%		
	Differential phase error	Gain = 2, 40 IRE modulation,	NTSC, $\pm 100\text{ IRE ramp}$	$V_{CC} = \pm 15\text{ V}$	0.01°		
				$V_{CC} = \pm 5\text{ V}$	0.02°		

† Full range = -40°C to 85°C for I suffix



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electrical characteristics at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, $R_L = 150\ \Omega$ (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Open loop gain	$V_{CC} = \pm 15\text{ V}$, $R_L = 1\text{ k}\ \Omega$	$V_O = \pm 10\text{ V}$	$T_A = 25^\circ\text{C}$	74	80		dB
			$T_A = \text{full range}$	69			
	$V_{CC} = \pm 5\text{ V}$, $R_L = 250\ \Omega$	$V_O = \pm 2.5\text{ V}$	$T_A = 25^\circ\text{C}$	69	76		
			$T_A = \text{full range}$	66			
V_{OS} Input offset voltage	$V_{CC} = \pm 5\text{ V or } \pm 15\text{ V}$		$T_A = 25^\circ\text{C}$	2.5	10		mV
			$T_A = \text{full range}$		13		
Offset voltage drift	$V_{CC} = \pm 5\text{ V or } \pm 15\text{ V}$		$T_A = \text{full range}$	10			$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current	$V_{CC} = \pm 5\text{ V or } \pm 15\text{ V}$		$T_A = 25^\circ\text{C}$	2.5	6		μA
			$T_A = \text{full range}$		8		
I_{OS} Input offset current	$V_{CC} = \pm 5\text{ V or } \pm 15\text{ V}$		$T_A = 25^\circ\text{C}$	35	250		nA
			$T_A = \text{full range}$		400		
Offset current drift	$T_A = \text{full range}$			0.3			$\text{nA}/^\circ\text{C}$

† Full range = -40°C to 85°C for I suffix

input characteristics

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{ICR} Common-mode input voltage range	$V_{CC} = \pm 15\text{ V}$			± 13.8	± 14.3		V
	$V_{CC} = \pm 5\text{ V}$			± 3.8	± 4.3		
CMRR Common mode rejection ratio	$V_{CC} = \pm 15\text{ V}$,	$V_{ICR} = \pm 12\text{ V}$	$T_A = \text{full range}$	70	90		dB
	$V_{CC} = \pm 5\text{ V}$,	$V_{ICR} = \pm 2.5\text{ V}$		80	100		
r_i Input resistance				1			$\text{M}\Omega$
C_i Input capacitance				1.5			pF

† Full range = -40°C to 85°C for I suffix



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electrical characteristics at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, $R_L = 150\ \Omega$ (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITION [†]		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	$V_{CC} = \pm 15\text{ V}$	$R_L = 250\ \Omega$	± 11.5	± 13		V
		$V_{CC} = \pm 5\text{ V}$	$R_L = 150\ \Omega$	± 3.2	± 3.5		
		$V_{CC} = \pm 15\text{ V}$	$R_L = 1\text{ k}\Omega$	± 13	± 13.6		V
		$V_{CC} = \pm 5\text{ V}$		± 3.5	± 3.8		
I_O	Output current [‡]	$V_{CC} = \pm 15\text{ V}$	$R_L = 20\ \Omega$	80	100		mA
		$V_{CC} = \pm 5\text{ V}$		50	65		
I_{SC}	Short-circuit current [‡]	$V_{CC} = \pm 15\text{ V}$			150		mA
R_O	Output resistance	Open loop			13		Ω

[†] Full range = -40°C to 85°C for I suffix

[‡] Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the *absolute maximum ratings* section of this data sheet for more information.

power supply

PARAMETER		TEST CONDITION [†]		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		± 4.5		± 16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	$V_{CC} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$		8	9.5	mA
			$T_A = \text{full range}$			11	
		$V_{CC} = \pm 5\text{ V}$	$T_A = 25^\circ\text{C}$		7	8.5	
			$T_A = \text{full range}$			10	
PSRR	Power supply rejection ratio	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$		$T_A = 25^\circ\text{C}$	75	84	dB
				$T_A = \text{full range}$	70		

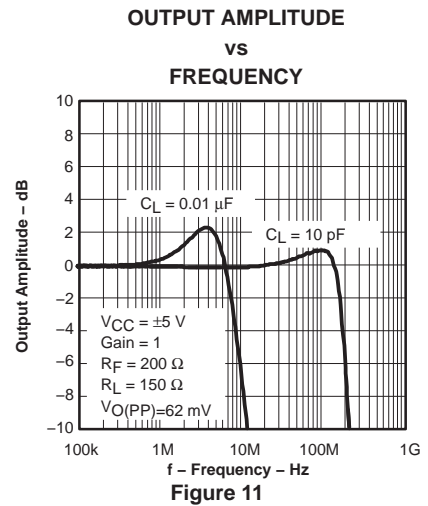
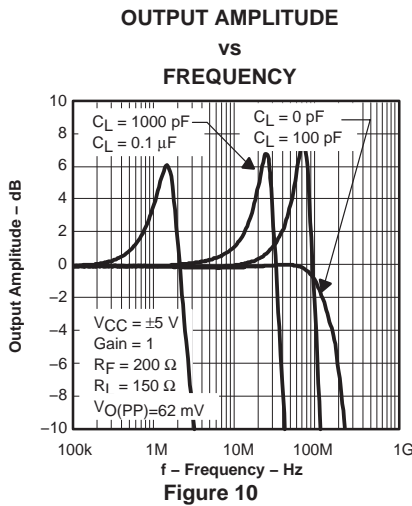
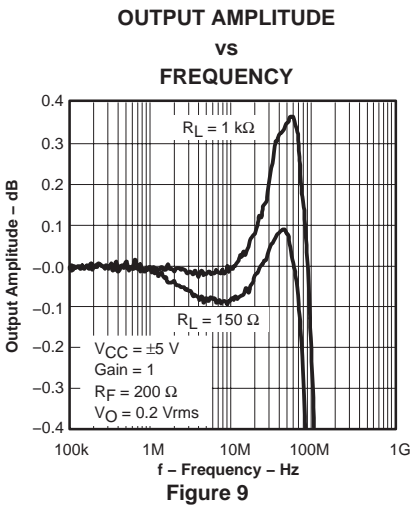
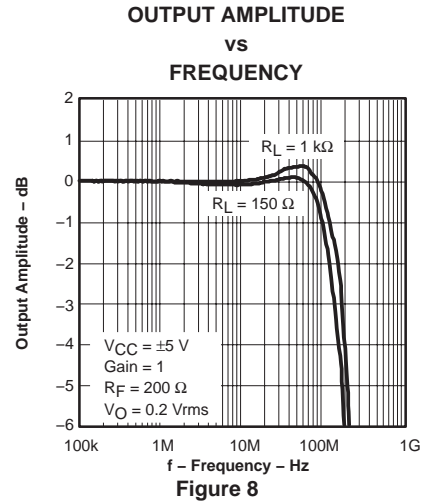
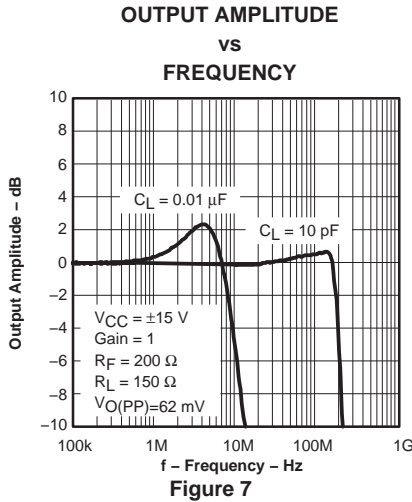
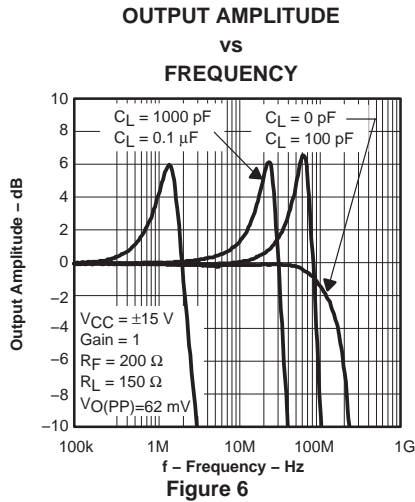
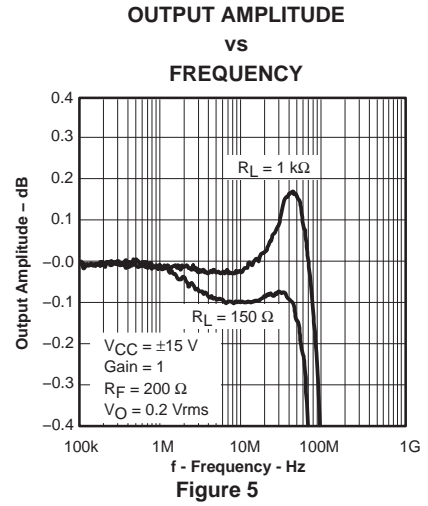
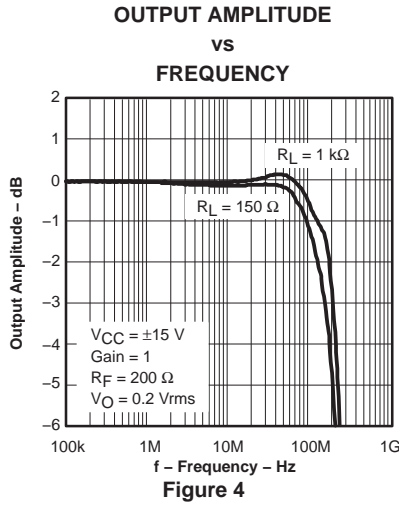
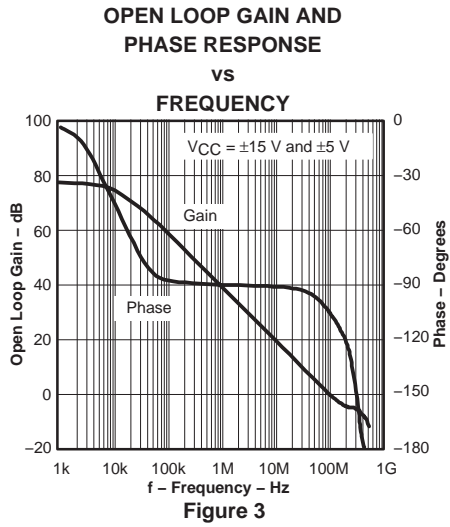
[†] Full range = -40°C to 85°C for I suffix

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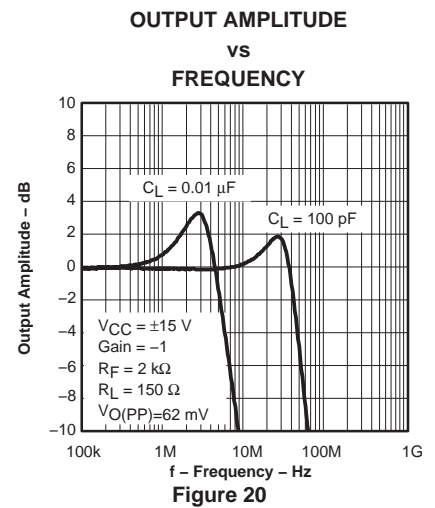
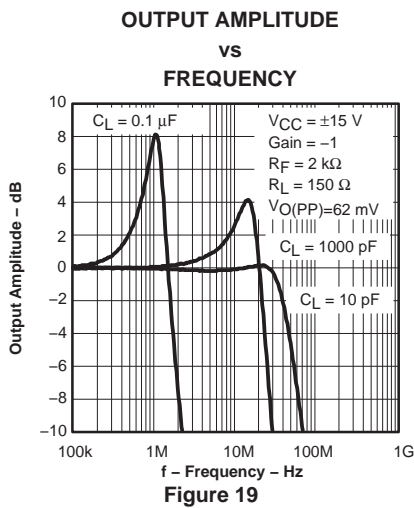
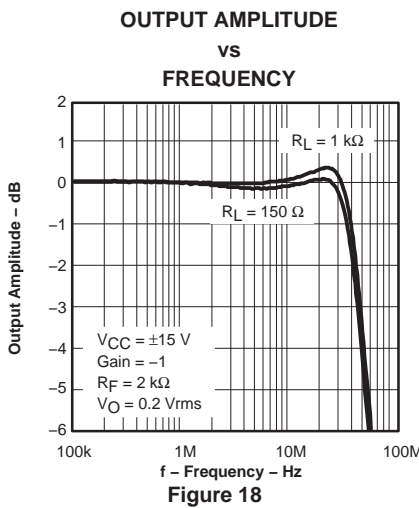
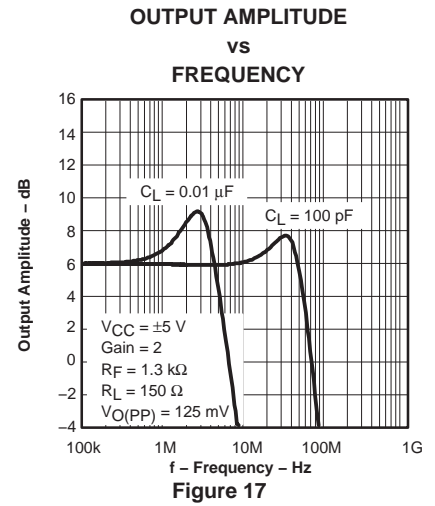
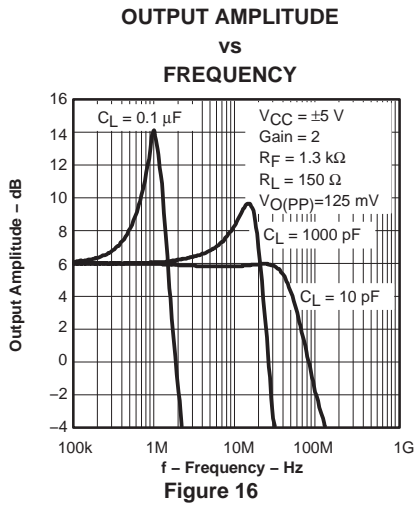
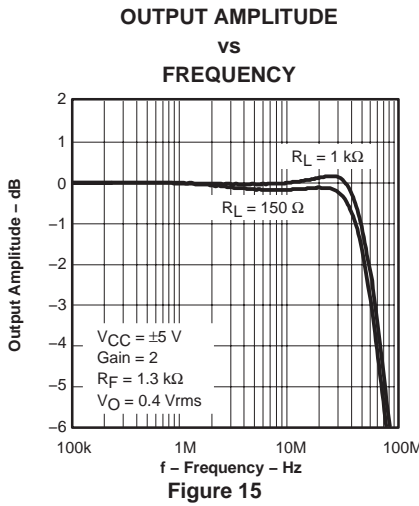
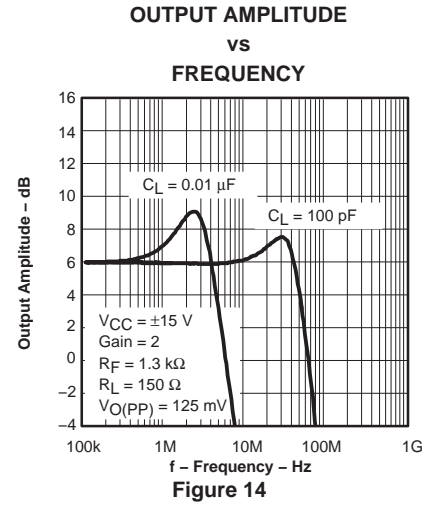
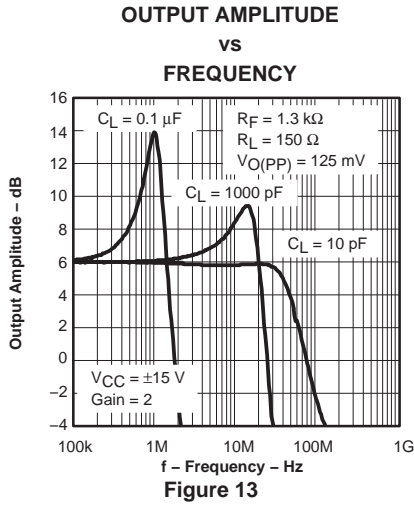
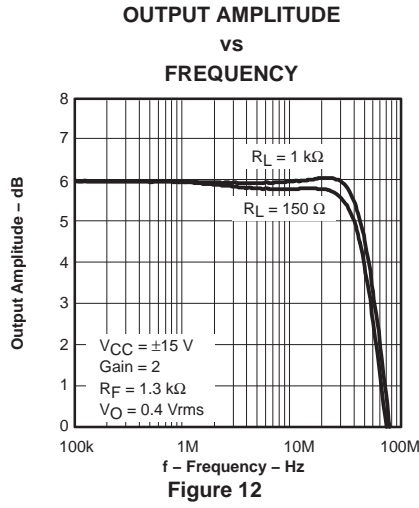
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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

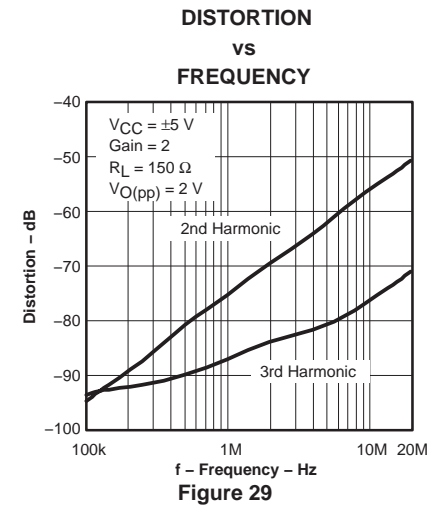
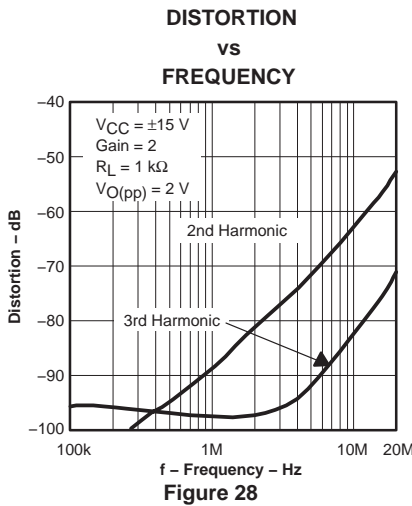
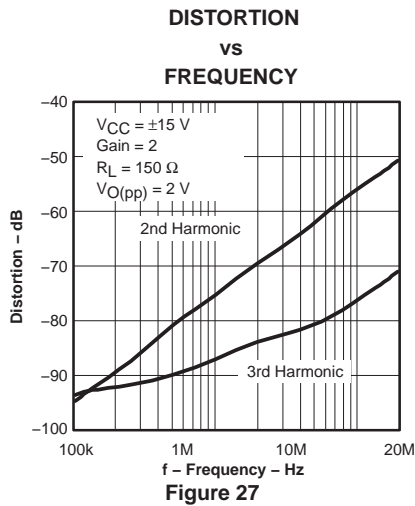
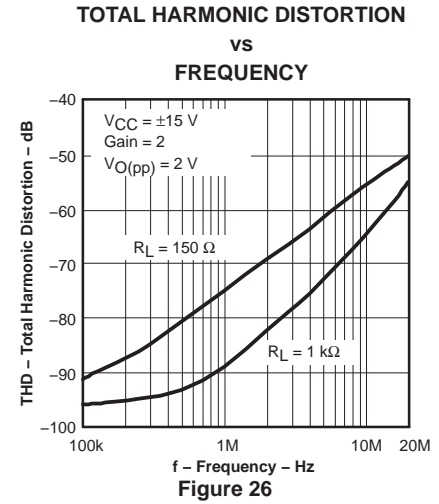
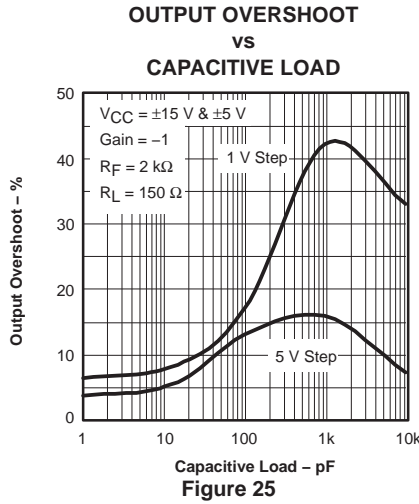
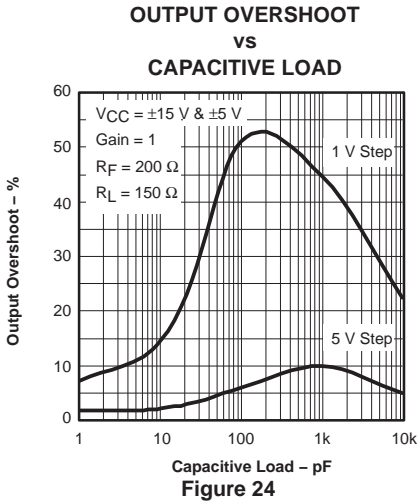
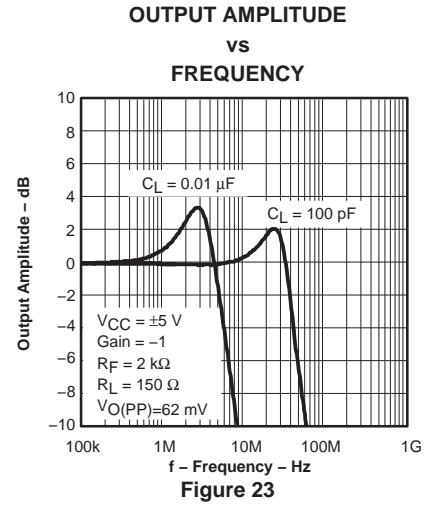
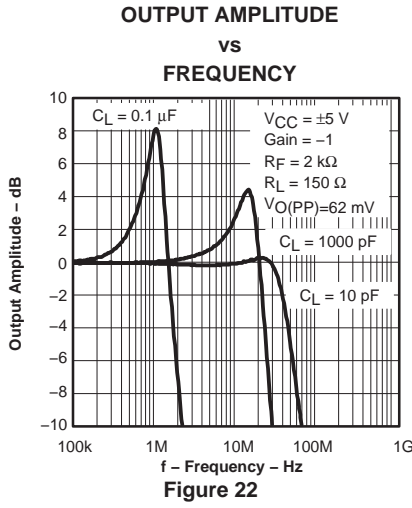
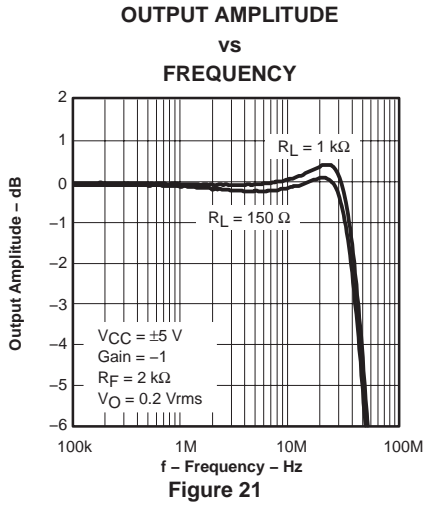


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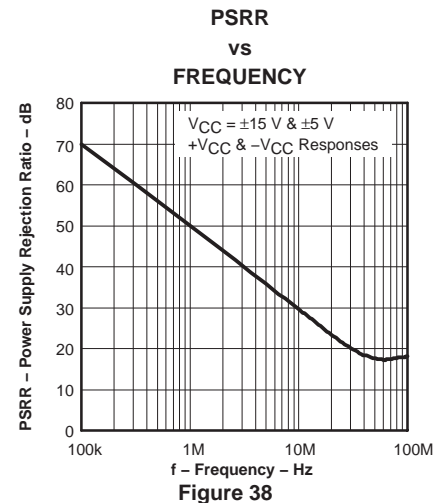
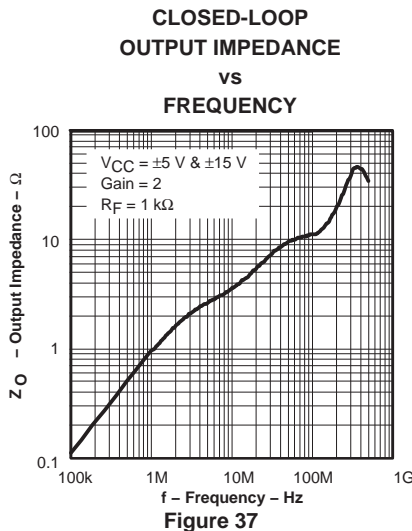
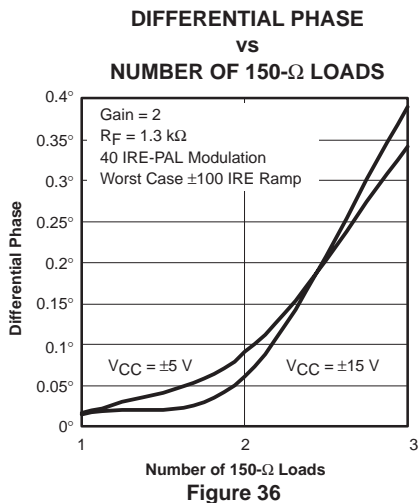
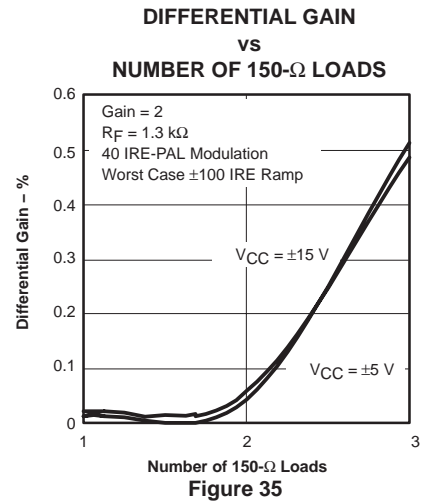
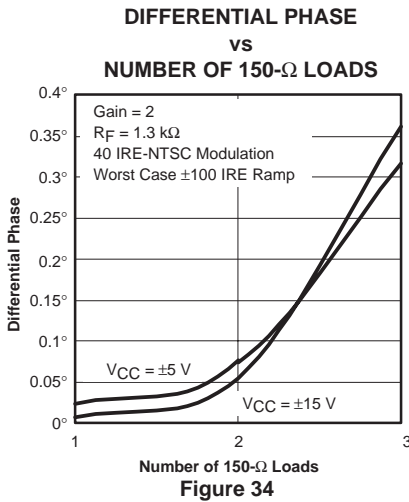
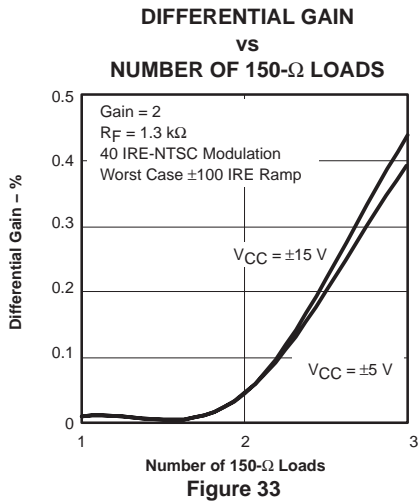
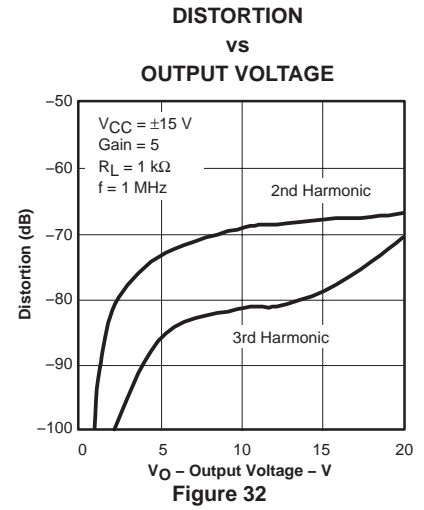
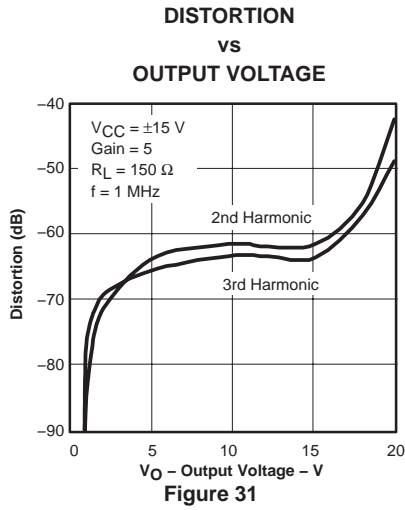
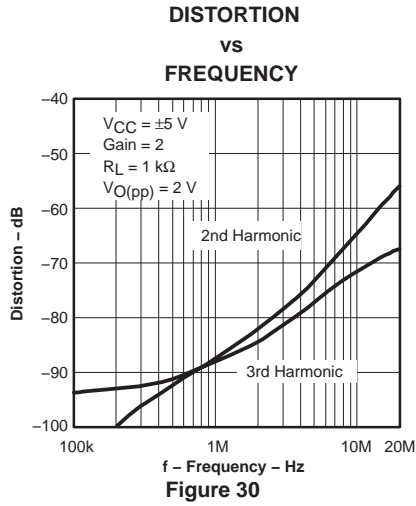
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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

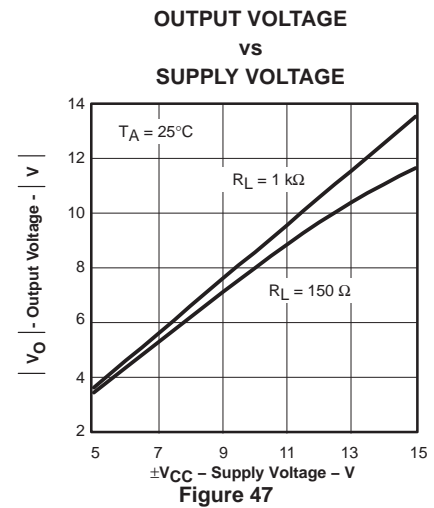
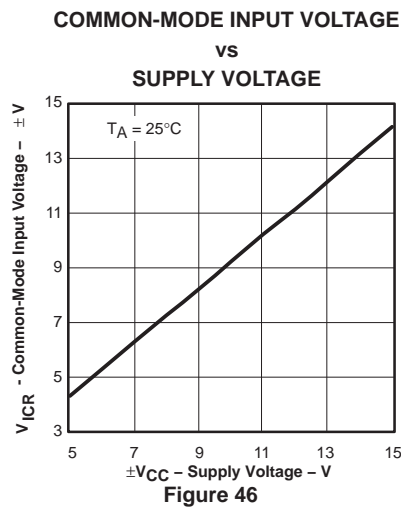
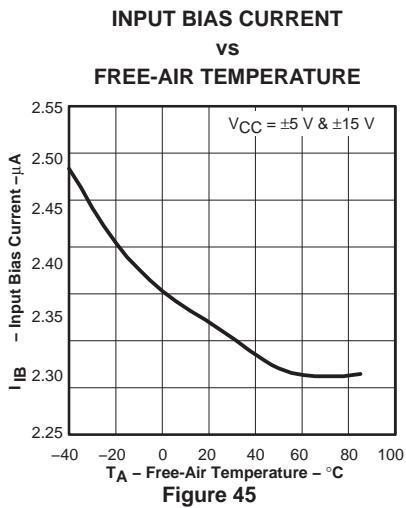
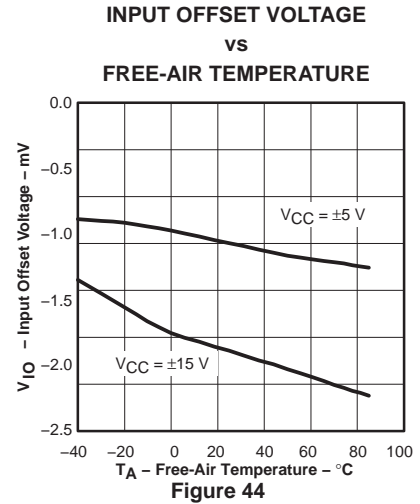
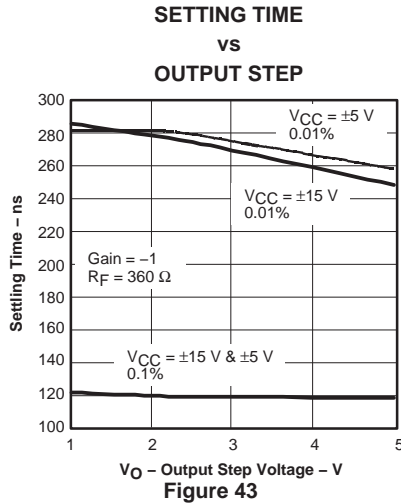
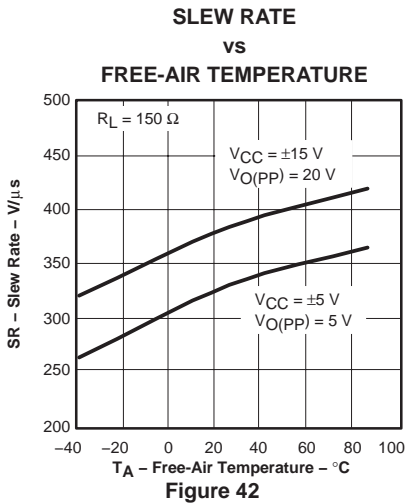
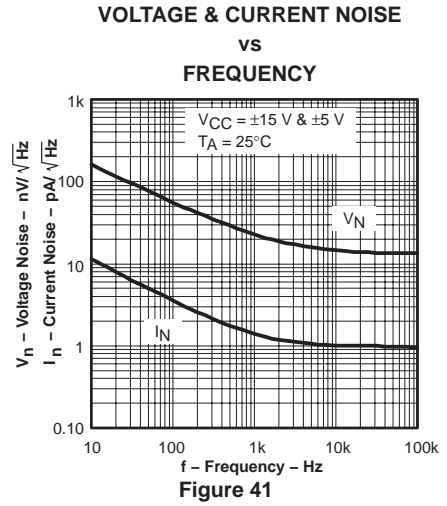
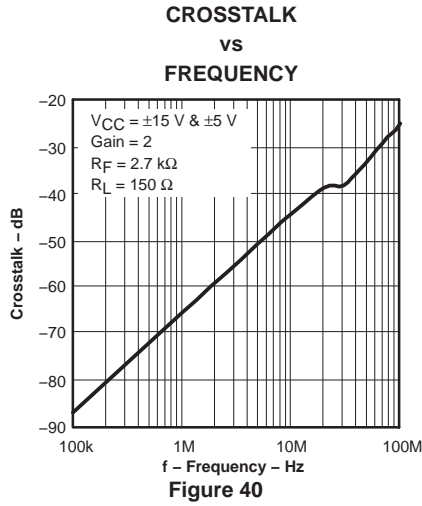
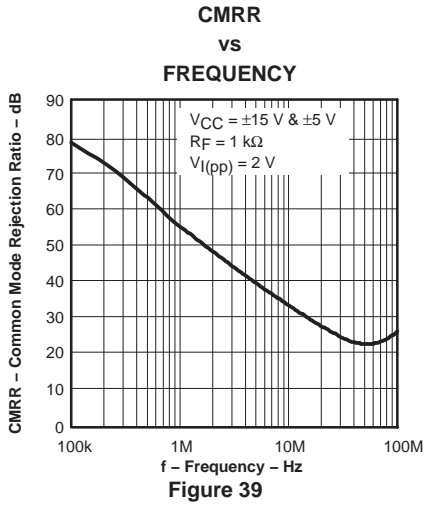


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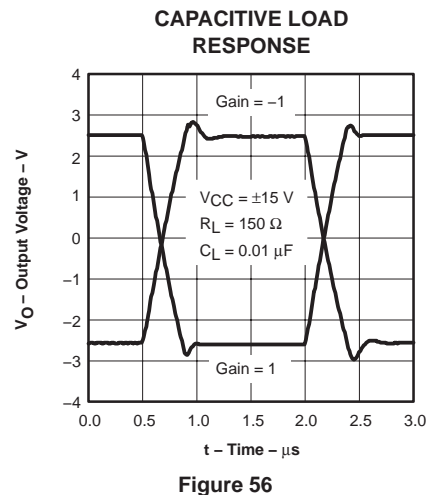
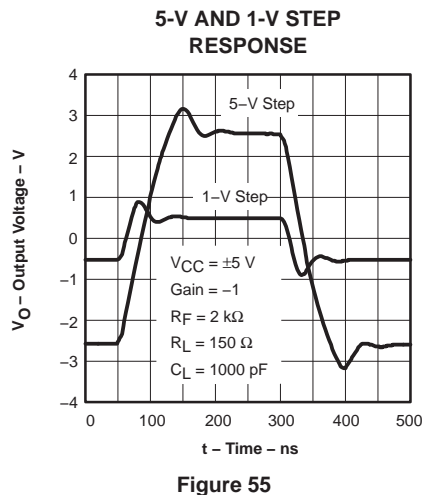
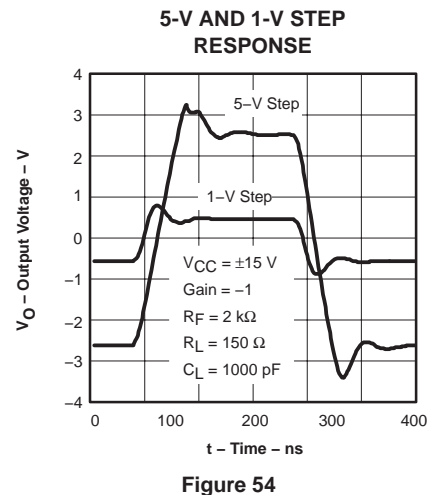
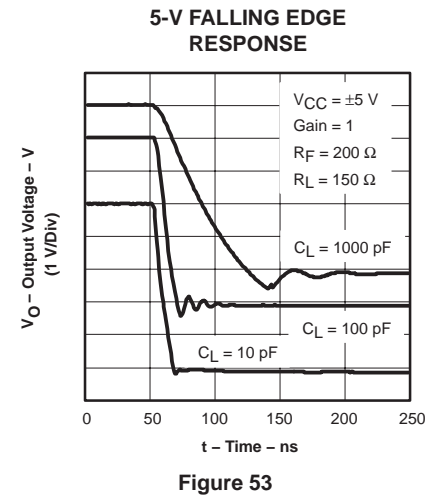
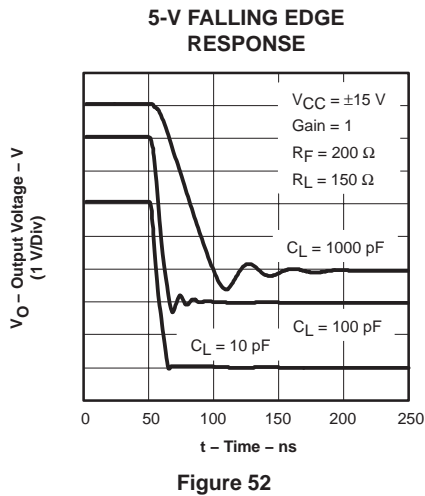
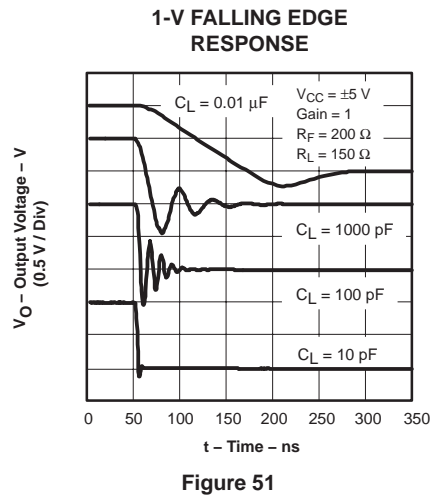
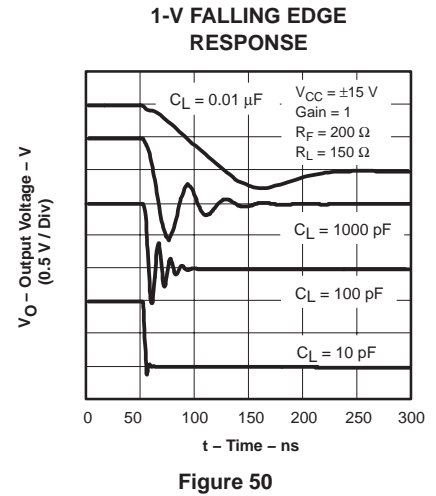
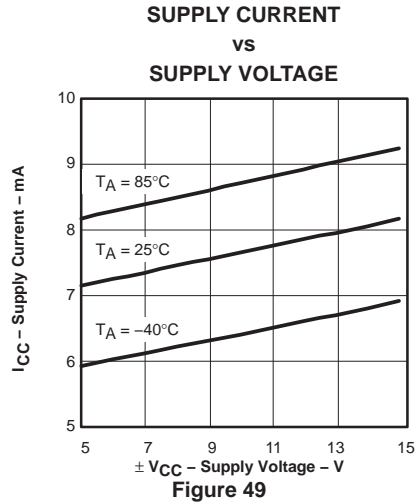
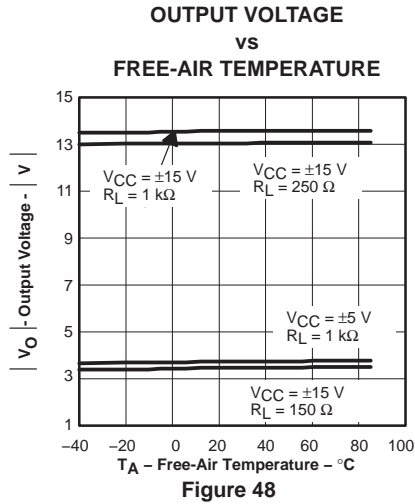
165-MHz C-STABLE HIGH-SPEED AMPLIFIER

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

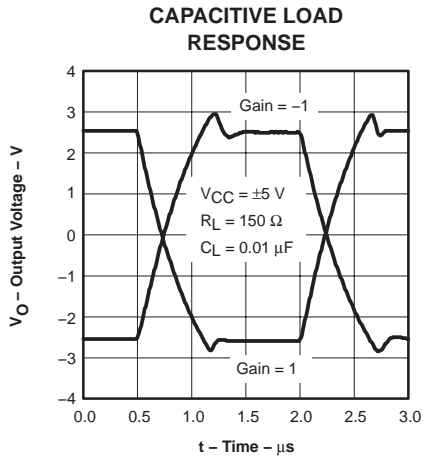


Figure 57

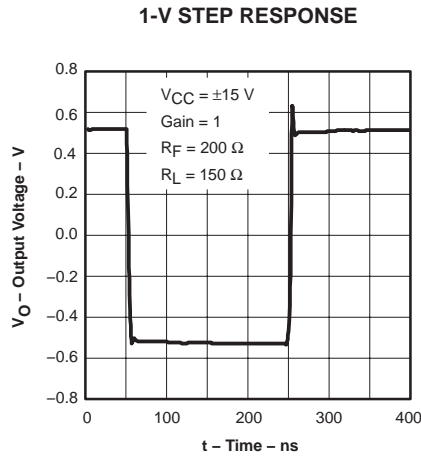


Figure 58

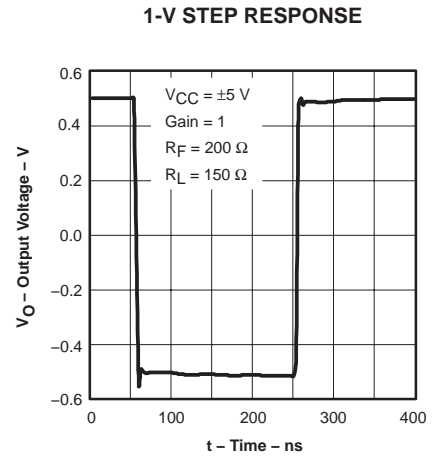


Figure 59

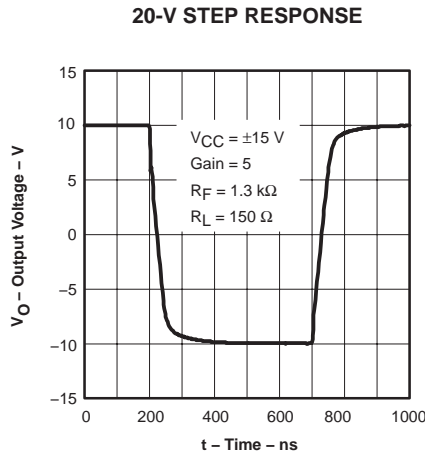


Figure 60

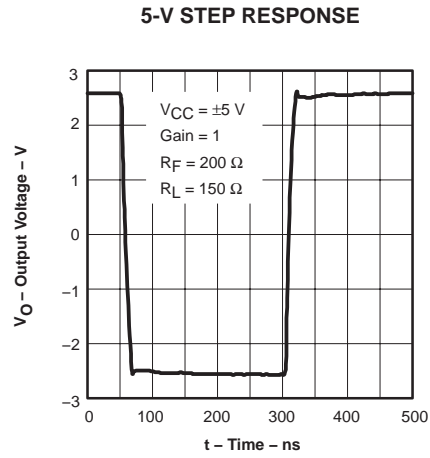


Figure 61

APPLICATION INFORMATION

theory of operation

The THS404x is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_T s of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 62.

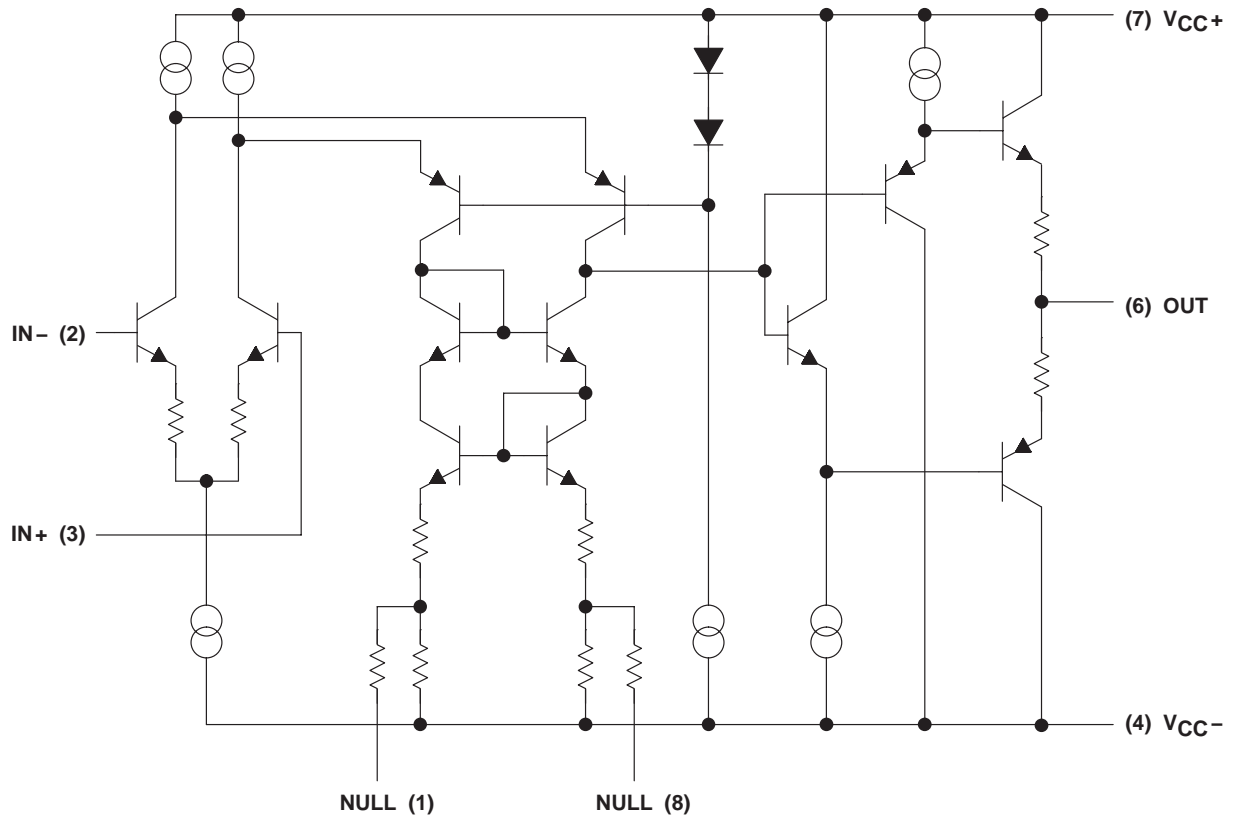


Figure 62. THS4041 Simplified Schematic

noise calculations and noise figure

Noise can cause errors on small signals. This is especially true when amplifying small signals, where signal-to-noise ratio (SNR) is important. The noise model for the THS404x is shown in Figure 63. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/\sqrt{Hz})
- $IN+$ = Noninverting current noise (pA/\sqrt{Hz})
- $IN-$ = Inverting current noise (pA/\sqrt{Hz})
- e_{RX} = Thermal voltage noise associated with each resistor ($e_{RX} = 4 kTR_x$)

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APPLICATION INFORMATION

noise calculations and noise figure (continued)

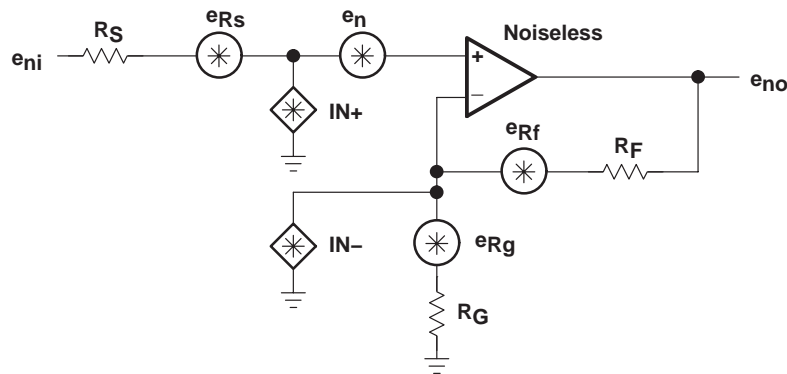


Figure 63. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + (IN+ \times R_S)^2 + (IN- \times (R_F \parallel R_G))^2 + 4kTR_S + 4kT(R_F \parallel R_G)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}

T = Temperature in degrees Kelvin ($273 + ^\circ\text{C}$)

$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni} A_V = e_{ni} \left(1 + \frac{R_F}{R_G} \right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, see the *Noise Analysis* section in the *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). The noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log \left[\frac{e_{ni}^2}{(e_{Rs})^2} \right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log \left[1 + \frac{\left[(e_n)^2 + (IN + \times R_S)^2 \right]}{4 kTR_S} \right]$$

Figure 64 shows the noise figure graph for the THS404x.

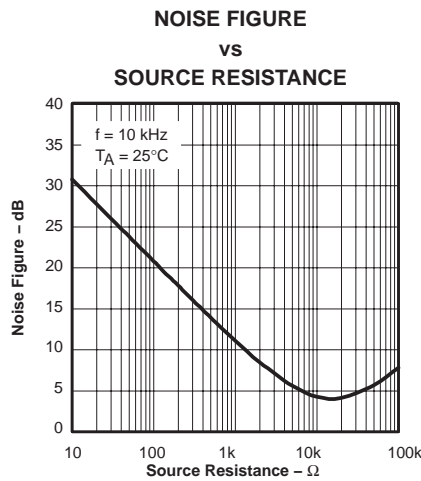


Figure 64.

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APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS404x has been internally compensated to maximize its bandwidth and slew rate performance. Typically when the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin, leading to high frequency ringing or oscillations. However, the THS404x has added internal circuitry that senses a capacitive load and adds extra compensation to the internal dominant pole. As the capacitive load increases, the amplifier remains stable. But, it is not uncommon to see a small amount of peaking in the frequency response. There are typically two ways to compensate for this. The first is to simply increase the gain of the amplifier. This helps by increasing the phase margin to keep peaking minimized. The second is to place an isolation resistor in series with the output of the amplifier, as shown in Figure 65. A minimum value of $20\ \Omega$ should work well for most applications. For example, in $75\text{-}\Omega$ transmission systems, setting the series resistor value to $75\ \Omega$ both isolates any capacitance loading and provides the proper line impedance matching at the source end. For more information about driving capacitive loads, see the *Output Resistance and Capacitance* section of the *Parasitic Capacitance in Op Amp Circuits Application Report* (literature number SLOA013).

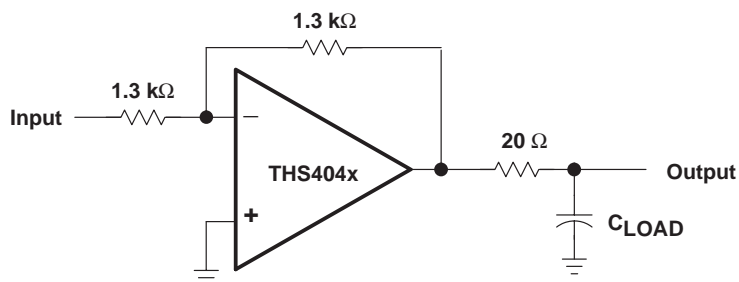


Figure 65. Driving a Capacitive Load for Extra Stability

offset nulling

The THS404x has low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided on the THS4041. The input offset can be adjusted by placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply. This is shown in Figure 66.

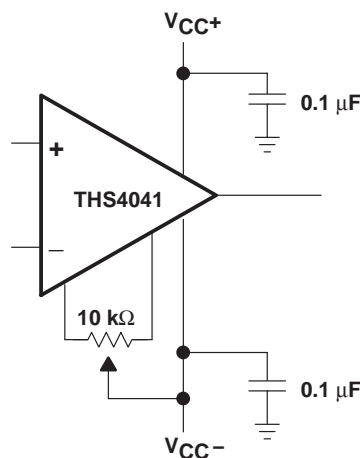


Figure 66. Offset Nulling Schematic

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

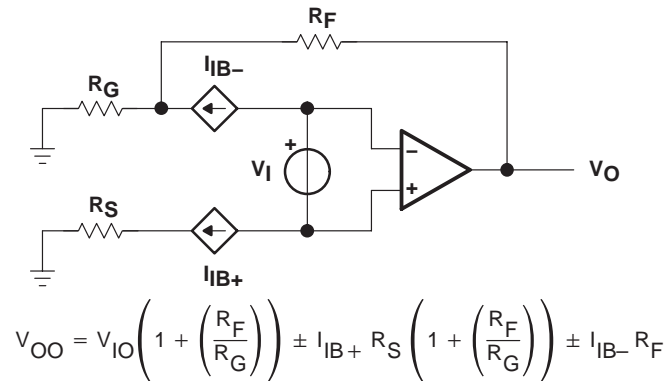


Figure 67. Output Offset Voltage Model

optimizing unity gain response

Internal frequency compensation of the THS404x was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the $G=+1$ configuration. For optimum settling time and minimum ringing, a feedback resistor of $200\ \Omega$ should be used as shown in Figure 68. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

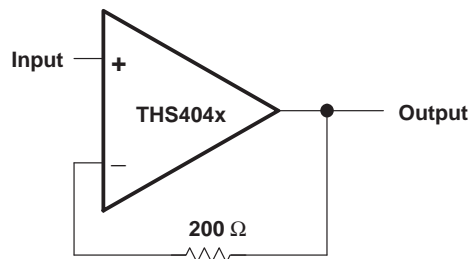


Figure 68. Noninverting, Unity Gain Schematic

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APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high frequency performance of the THS404x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS404x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.



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APPLICATION INFORMATION

evaluation board

An evaluation board is available for the THS4041 (literature number SLOP219). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 69. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, see the *THS4041 EVM User's Guide*. To order the evaluation board, contact your local Texas Instruments sales office or distributor.

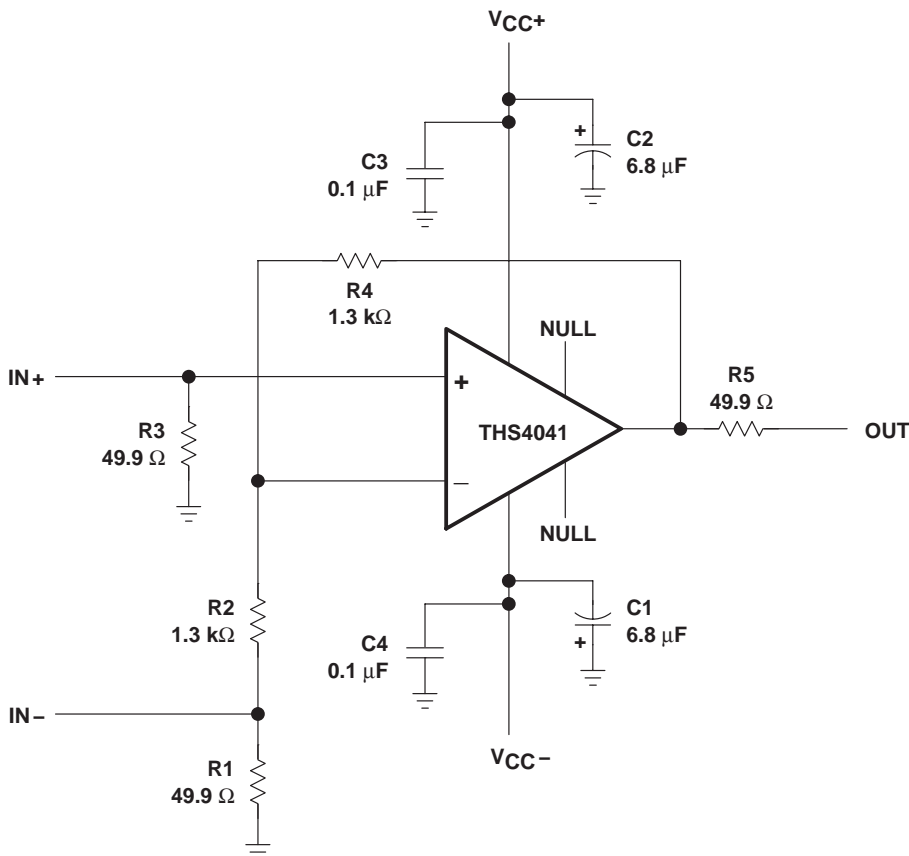


Figure 69. THS4041 Evaluation Board

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4041IDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4041Q1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF THS4041-Q1 :

- Catalog : [THS4041](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4041IDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4041IDRQ1	SOIC	D	8	2500	350.0	350.0	43.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

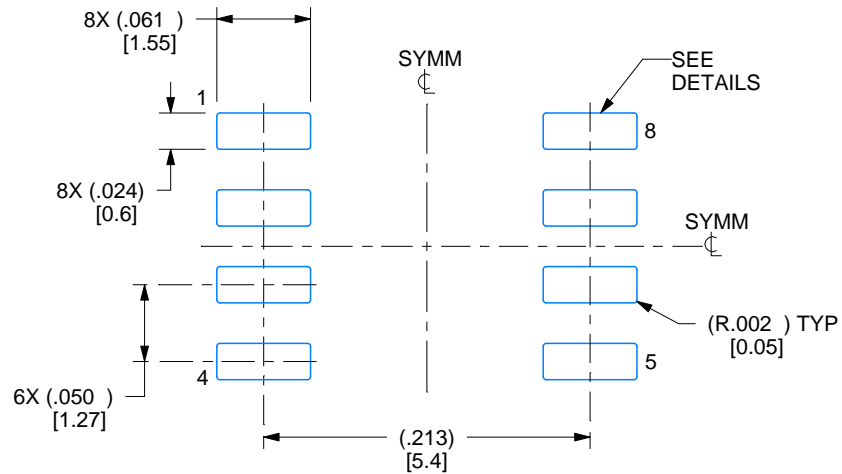
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

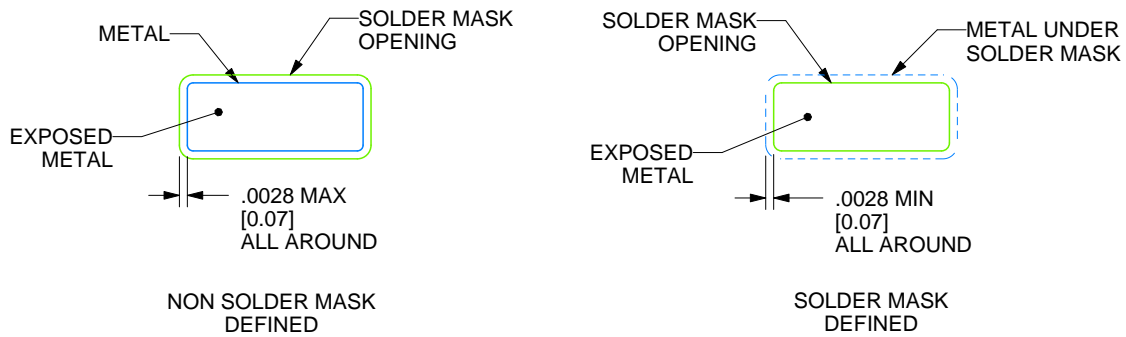
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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