TLVx387 High Precision, Zero-Drift, Low-Input-Bias-Current Op Amps

1 Features

- Ultra-low offset voltage: ±10 µV (maximum)
- Zero drift: ±0.01 µV/°C
- Low-input bias current: 300 pA (maximum)
- Low noise: 8.5 nV/√Hz at 1 kHz
- No 1/f noise: 177 nV_{PP} (0.1 Hz to 10 Hz)
- Common-mode input range ±100 mV beyond supply rails
- Gain bandwidth: 5.7 MHz
- Quiescent current: 570 µA per amplifier
- Single supply: 1.7 V to 5.5 V
- Dual supply: ±0.85 V to ±2.75 V
- EMI and RFI filtered inputs

2 Applications

- Electronic thermometer
- Weigh scale
- Temperature transmitter
- Ventilators
- Data acquisition (DAQ)
- Semiconductor test
- Lab and field instrumentation
- Merchant network and server PSU
- Analog input module
- Pressure transmitter

3 Description

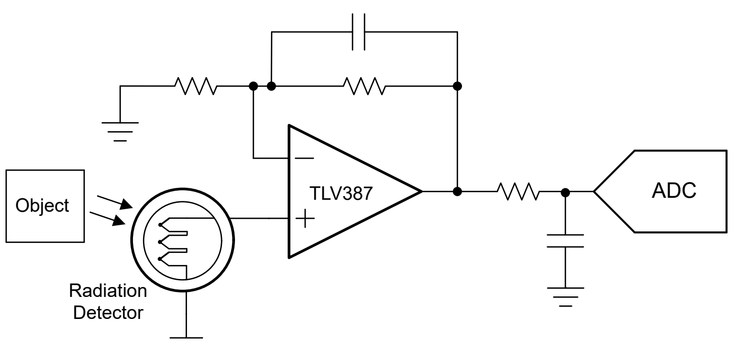
The TLV387, TLV2387, and TLV4387 (TLVx387) family of precision amplifiers offers state-of-the-art performance. With zero-drift technology, the TLVx387 offset voltage and offset drift provide unparalleled long-term stability. With a mere 570 µA of quiescent current, the TLVx387 are able to achieve 5.7 MHz of bandwidth, a broadband noise of 8.5 nV/√Hz, and a 1/f noise at 177 nV_{PP}. These specifications are crucial to achieve extremely-high precision and no degradation of linearity in 16-bit to 24-bit analog to digital converters (ADCs). The TLVx387 feature flat bias current over temperature; therefore, little to no calibration is needed in high input impedance applications over temperature.

All versions are specified over the industrial temperature range of –40°C to +125°C.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
TLV387	Single	DBV (SOT-23, 5)
TLV2387	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)
TLV4387	Quad	PW (TSSOP, 14)

(1) For more information, see Section 10.



The TLV387 as a Precision, Low-Noise ADC Driver

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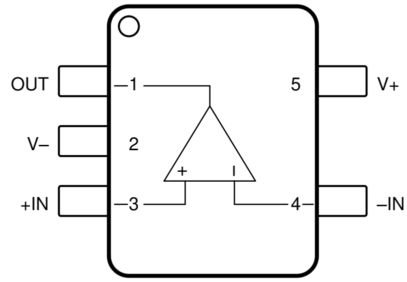
4 Pin Configuration and Functions

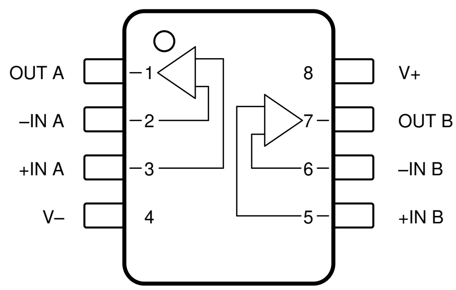


Not to scale

Figure 4-1. TLV387: DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions: TLV387

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	3	Input	Inverting input
+IN	4	Input	Noninverting input
OUT	6	Output	Output
V–	5	Power	Negative (lowest) power supply
V+	1	Power	Positive (highest) power supply



Not to scale

Figure 4-2. TLV2387: D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

Table 4-2. Pin Functions: TLV2387

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK (VSSOP)	DSG (WSON)		
–IN A	2	2	Input	Inverting input, channel A
–IN B	6	6	Input	Inverting input, channel B
+IN A	3	3	Input	Noninverting input, channel A
+IN B	5	5	Input	Noninverting input, channel B
OUT A	1	1	Output	Output, channel A
OUT B	7	7	Output	Output, channel B
V–	4	4	Power	Negative (lowest) power supply
V+	8	8	Power	Positive (highest) power supply
Thermal Pad	—	Thermal pad	—	Connect thermal pad to V–

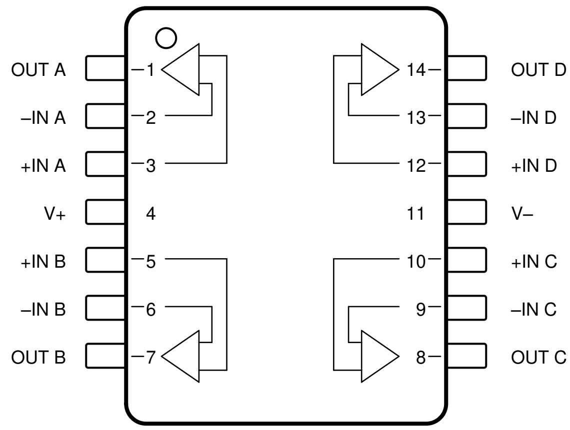


Figure 4-3. TLV4387: PW Package, 14-Pin TSSOP (Top View)

Table 4-3. Pin Functions: TLV4387

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V–	11	Power	Negative (lowest) power supply
V+	4	Power	Positive (highest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply Voltage, V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Input voltage, all pins	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Input current, all pins			±10	mA
	Output short circuit[2]		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply	1.7		5.5	V
		Dual-supply	±0.85		±2.75	
T_A	Specified temperature		–40		125	°C

5.4 Thermal Information: TLV387

THERMAL METRIC(1)		TLV387 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	107.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Thermal Information: TLV2387

THERMAL METRIC(1)		TLV2387		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.9	165	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.9	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.4	87	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	21.5	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.7	85	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Thermal Information: TLV4387

THERMAL METRIC(1)		TLV4387 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.7 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_S = 1.7 V to 5.5 V, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5.5 V		±1	±5	µV
		V_S = 1.7 V		±1.25	±6	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C[1]		±0.01	±0.05	µV/°C
PSRR	Power supply rejection ratio			±0.05	±0.5	µV/V
		T_A = –40°C to +125°C[1]			±1	
INPUT BIAS CURRENT						
I_B	Input bias current			±60	±300	pA
		T_A = –40°C to +125°C[1]			±350	
I_{OS}	Input offset current			±60	±500	pA
		T_A = –40°C to +125°C[1]			±700	
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		177		nV_{PP}
				27		nV_{RMS}
e_N	Input voltage noise density	f = 1 Hz		8.5		nV/√Hz
		f = 10 Hz		8.5		
		f = 100 Hz		8.5		
		f = 1 kHz		8.5		
i_N	Input current noise	f = 1 kHz		70		fA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range	V_S = 1.7 V	(V–) – 0.1		(V+)	V
		V_S = 5.5 V	(V–) – 0.2		(V+) + 0.1	
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+), V_S = 1.7 V	115	138		dB
		(V–) – 0.2 V < V_{CM} < (V+) + 0.1 V, V_S = 5.5 V	130	150		
		(V–) – 0.1 V < V_{CM} < (V+), T_A = –40°C to +125°C[1]	110	132		
		(V–) – 0.2 V < V_{CM} < (V+) + 0.1, V_S = 5.5 V, T_A = –40°C to +125°C[1]	130			
INPUT CAPACITANCE						
Z_{ID}	Differential			100 || 3		MΩ || pF
Z_{ICM}	Common-mode			60 || 3		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_{OUT} < (V+) – 100 mV	120	145		dB
		(V–) + 100 mV < V_{OUT} < (V+) – 100 mV; T_A = –40°C to +125°C[1]	115			
		(V–) + 150 mV < V_{OUT} < (V+) – 150 mV, R_L = 2 kΩ	120	145		
		(V–) + 150 mV < V_{OUT} < (V+) – 150 mV, R_L = 2 kΩ; T_A = –40°C to +125°C[1]	115			

5.7 Electrical Characteristics (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_S = 1.7 V to 5.5 V, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.7		MHz
SR	Slew rate	4-V step, G = +1			2.8		V/µs
t_S	Settling time	To 0.1%, 1-V step, G = +1			1.5		µs
		To 0.01%, 1-V step, G = +1			2.5		
	Overload recovery time	V_{IN} × G > V_S			500		ns
	Chopping clock frequency[(1)]			100	150		kHz
THD+N	Total harmonic distortion + noise	V_{OUT} = 1 V_{RMS}, G = +1, f = 1 kHz, R_L = 10 kΩ			0.002 %		
OUTPUT							
	Voltage output swing from rail	no load			1	20	mV
					5	30	
		R_L = 2 kΩ			20	75	
		T_A = –40°C to +125°C[(1)]				30	
	High linearity output swing range[(1)]	A_{OL} > 120 dB		(V–) + 0.075		(V+) – 0.075	V
			R_L = 2 kΩ	(V–) + 0.150		(V+) – 0.150	
I_{SC}	Short-circuit current	V_S = 5.5 V			±55		mA
		V_S = 1.7 V			±15		
	Phase margin	C_L = 100 pF, G = +1			40		degrees
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			570	675	µA
			T_A = –40°C to 125°C[(1)]			700	µA
	Turn-on time	V_S = 5.5 V, V_S ramp rate > 0.3 V/µs, settle to 1%			25	100	µs

(1) Specification established from device population bench system measurements across multiple lots.

5.8 Typical Characteristics

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)

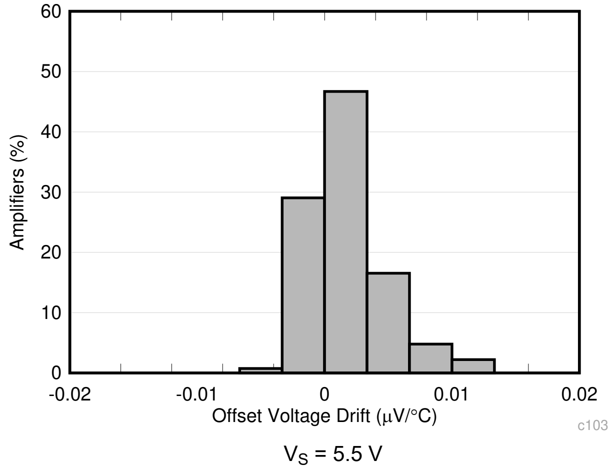


Figure 5-1. Offset Voltage Drift Distribution

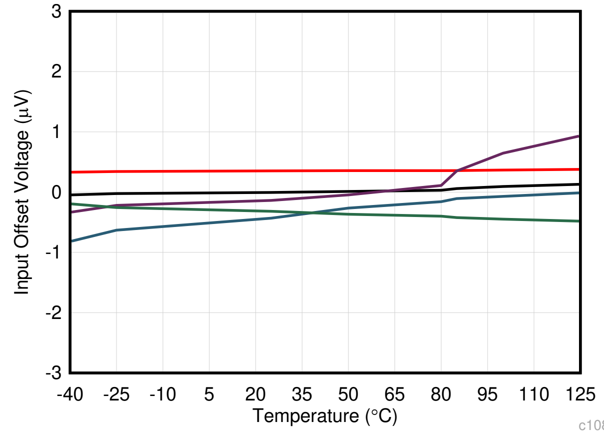


Figure 5-2. Offset Voltage vs Temperature

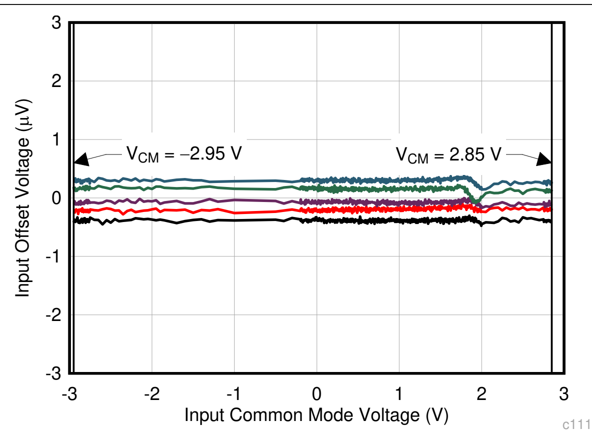


Figure 5-3. Offset Voltage vs Common-Mode Voltage

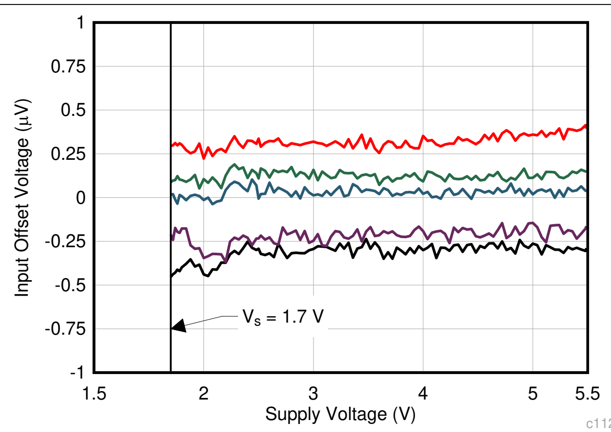


Figure 5-4. Offset Voltage vs Supply Voltage

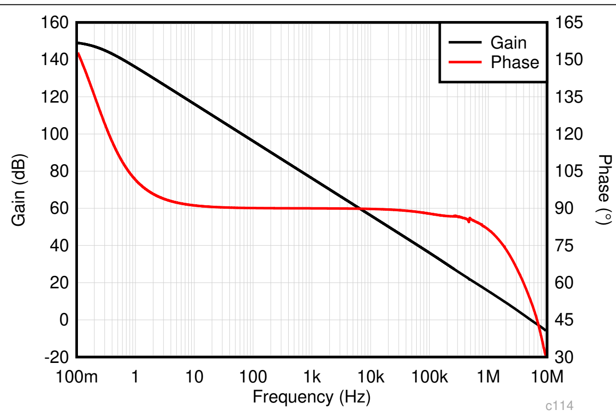


Figure 5-5. Open-Loop Gain and Phase vs Frequency

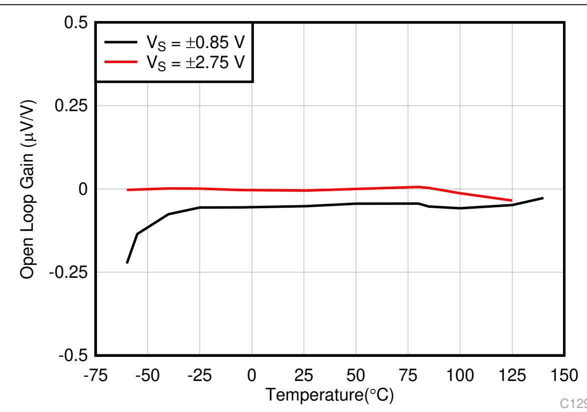


Figure 5-6. Open-Loop Gain vs Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)

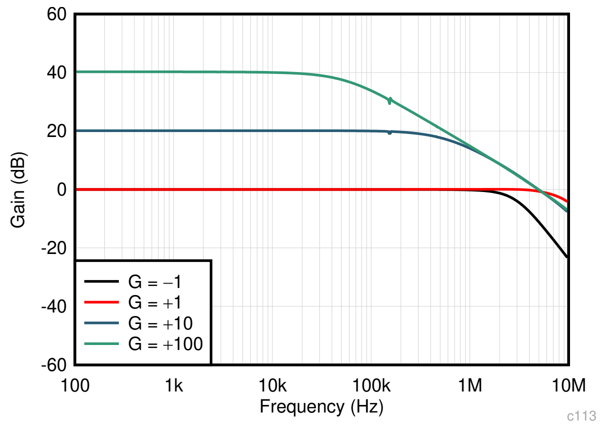


Figure 5-7. Closed-Loop Gain and Phase vs Frequency

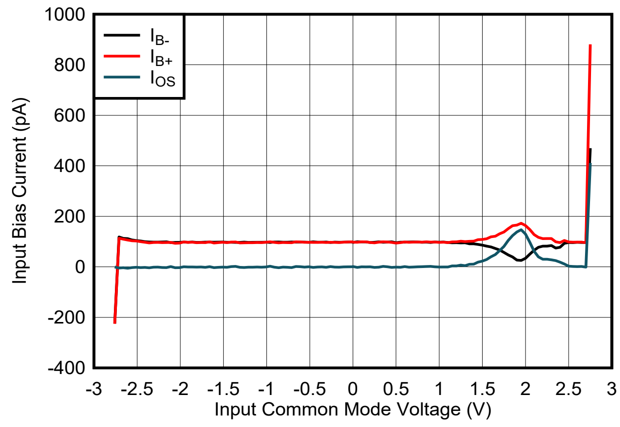


Figure 5-8. Input Bias Current vs Common-Mode Voltage

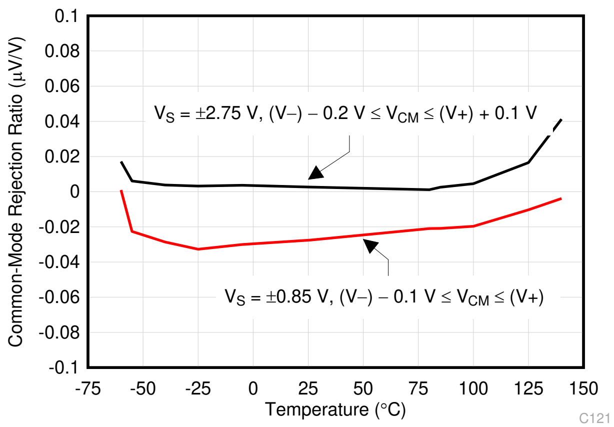


Figure 5-9. CMRR vs Temperature

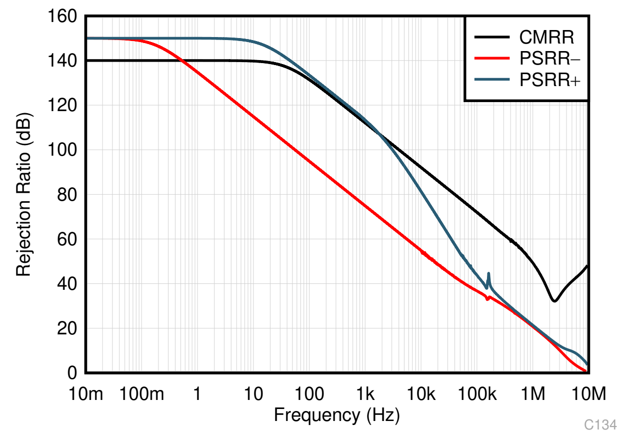


Figure 5-10. PSRR and CMRR vs Frequency

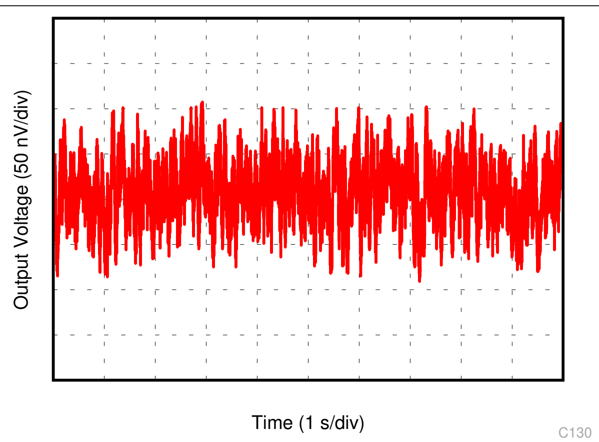


Figure 5-11. 0.1-Hz to 10-Hz Noise

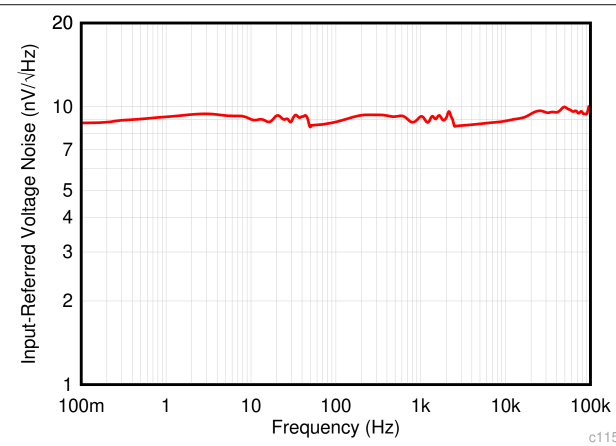


Figure 5-12. Input Voltage Noise Spectral Density vs Frequency

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)

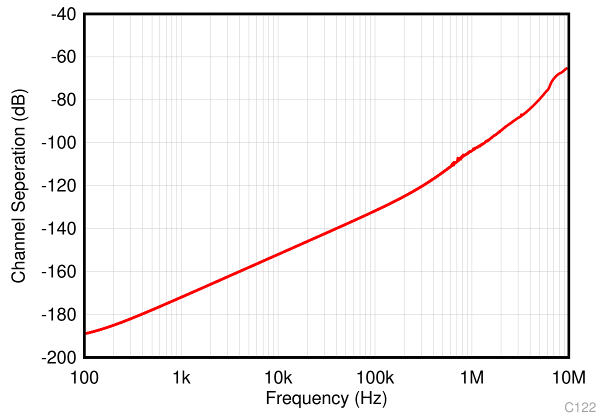
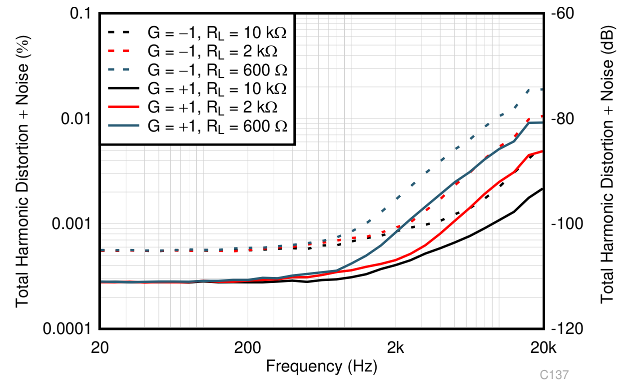
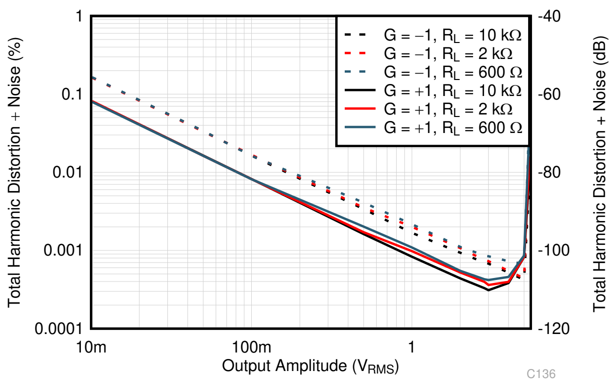


Figure 5-13. Channel-to-Channel Crosstalk



V_S = 5.5 V, V_{OUT} = 3 V_{RMS}, BW = 80 kHz

Figure 5-14. THD+N Ratio vs Frequency



V_S = 5.5 V, f = 1 kHz, BW = 80 kHz

Figure 5-15. THD+N vs Output Amplitude

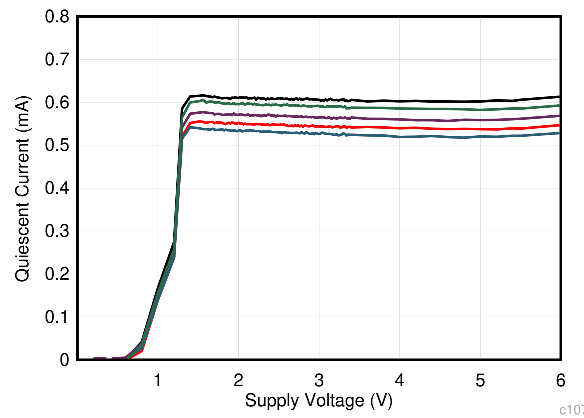


Figure 5-16. Quiescent Current vs Supply Voltage

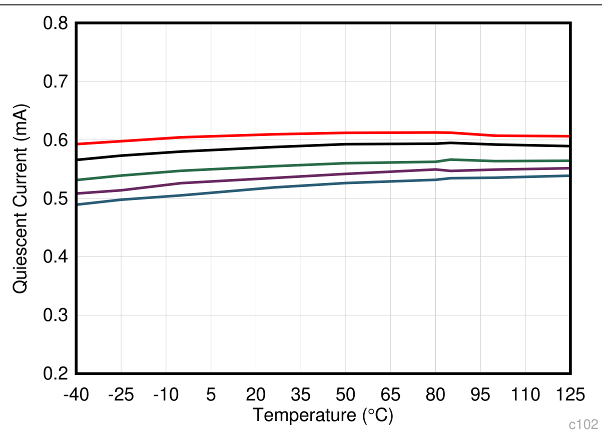


Figure 5-17. Quiescent Current vs Temperature

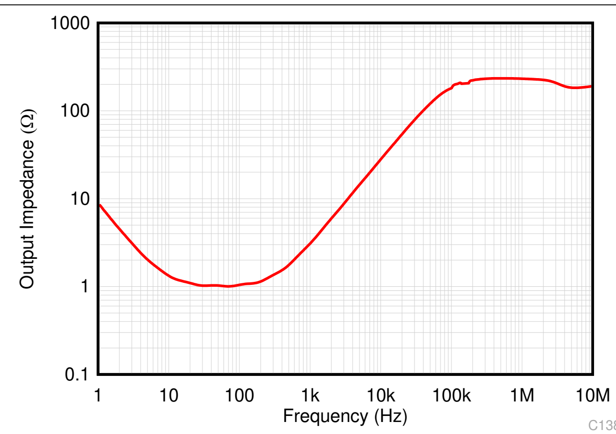
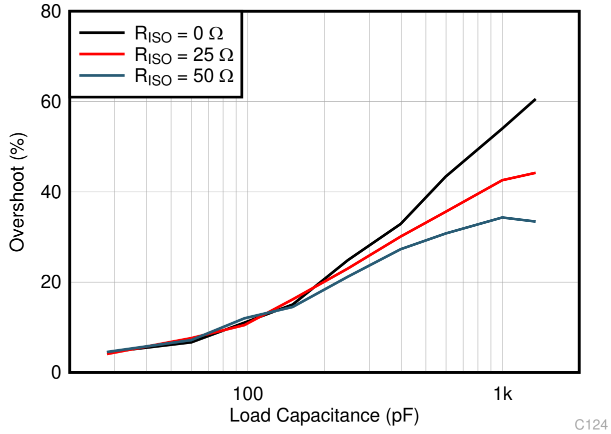


Figure 5-18. Open-Loop Output Impedance vs Frequency

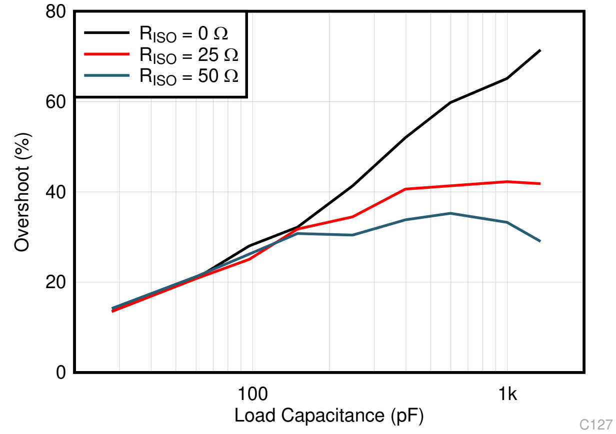
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)



G = –1, 10 mV step

Figure 5-19. Small-Signal Overshoot vs Capacitive Load



G = +1, 10 mV step

Figure 5-20. Small-Signal Overshoot vs Capacitive Load

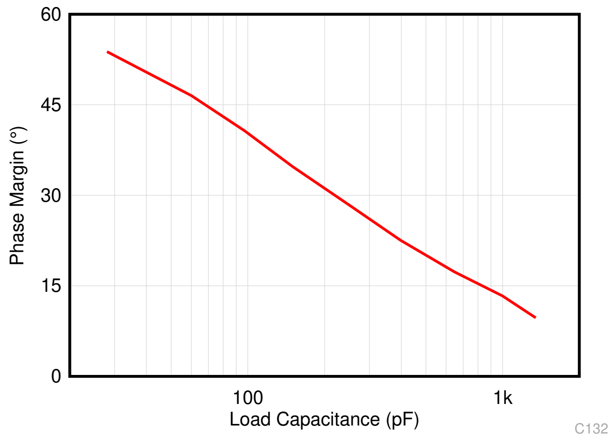


Figure 5-21. Phase Margin vs Capacitive Load

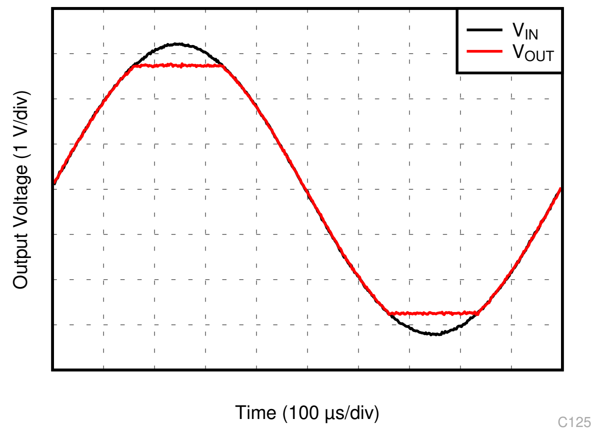
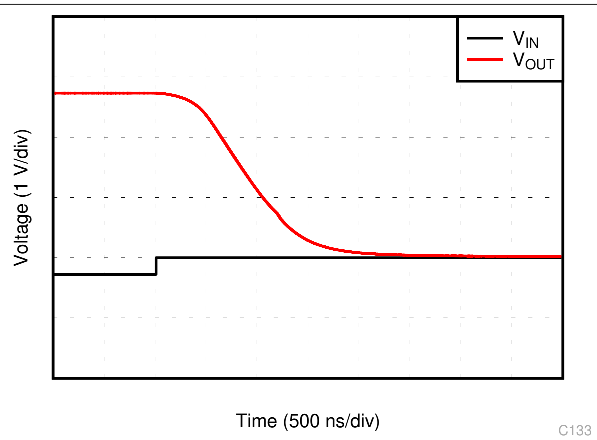
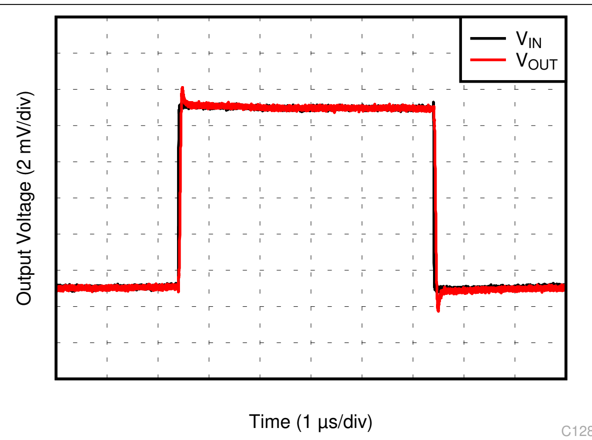


Figure 5-22. No Phase Reversal



G = –1

Figure 5-23. Overload Recovery



G = +1

Figure 5-24. Small-Signal Step Response

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)

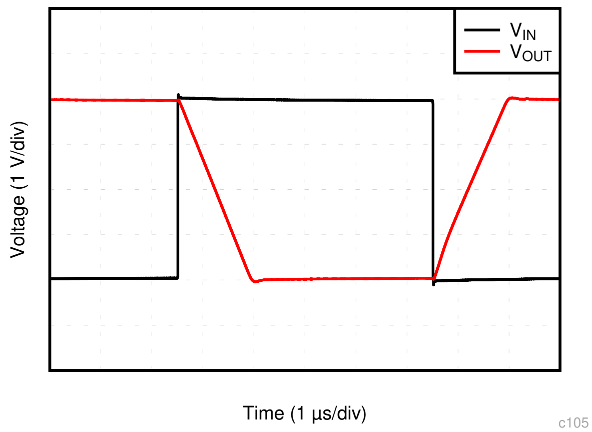


Figure 5-25. Large-Signal Step Response (4-V Step)

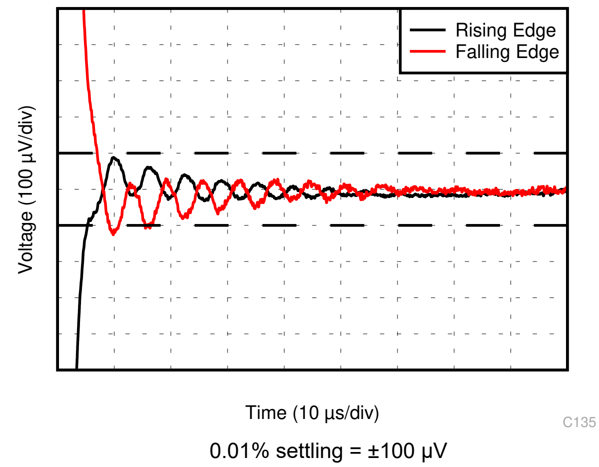


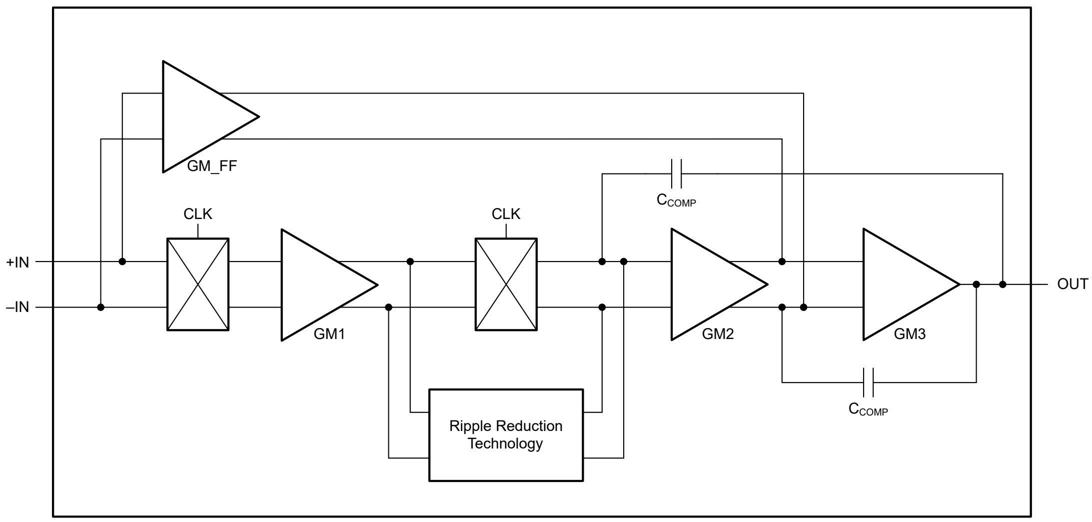
Figure 5-26. Settling Time

6 Detailed Description

6.1 Overview

The TLVx387 family of zero-drift amplifiers is engineered with state-of-the-art, proprietary, precision zero-drift technology. These amplifiers offer ultra-low input offset voltage and drift, and achieve excellent input and output dynamic linearity. The TLVx387 operate from 1.7 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications. The TLVx387 strengths also include a 5.7-MHz bandwidth, 8.5-nV/√Hz noise spectral density, and no 1/f noise, making the TLVx387 an excellent choice for interfacing with sensor modules, and buffering high-fidelity, digital-to-analog converters (DACs).

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Bias Current

During normal operation, the typical input bias current of the TLVx387 is 30 pA. The device exhibits low drift over the full temperature range of –40°C to +125°C. There are no antiparallel diodes between the input pins (+IN and –IN); therefore, the differential input maximum voltage is limited only by diodes connected to the supply voltage pins. However, use caution in cases where the input differential voltage exceeds the nominal operating input differential voltage. When inputs are separated, the switching offset-cancellation path internal to the amplifier exceeds normal operating conditions, and can potentially create long settling behavior upon return to normal operation. The equivalent input circuit of TLVx387 is shown in Figure 6-1.

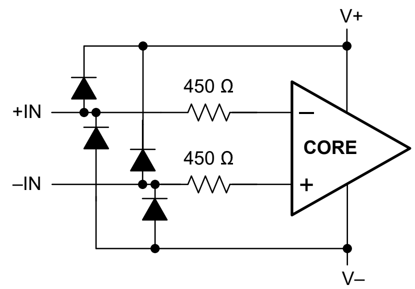


Figure 6-1. Equivalent Input Circuit

6.3.2 EMI Susceptibility and Input Filtering

Operational amplifiers can exhibit sensitivity to electromagnetic interference (EMI). Typically, conducted EMI (that is, EMI that enters the device through conduction) is more commonly observed than radiated EMI (that is, EMI that enters the device through radiation). When conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from the nominal value. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The TLVx387 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The conducted EMI rejection of the TLVx387 is seen in Figure 6-2.

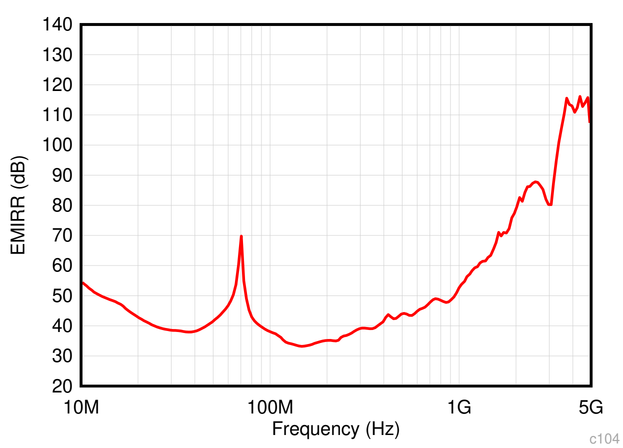


Figure 6-2. EMI Rejection Ratio

6.4 Device Functional Modes

The TLVx387 have a single functional mode and are operational when the power-supply voltage is greater than 1.7 V (±0.85 V). The maximum specified power-supply voltage for the TLVx387 is 5.5 V (±2.75 V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLVx387 are unity-gain stable, precision, operational amplifiers featuring state-of-the-art, zero-drift technology. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lower 1/f noise component. As a result of the high PSRR, the devices work well in applications that run directly from battery power without regulation. The TLVx387 family is optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies without input crossover distortion, and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The TLVx387 precision amplifiers are designed for upstream analog signal-chain applications in low or high gains, as well as downstream signal-chain functions, such as DAC buffering.

7.1.1 Zero-Drift Clocking

The TLVx387 use an advanced zero-drift architecture to achieve ultra-low offset and offset drift. This architecture uses a clock and switches internally to create a dc error-correction path. The clocking is filtered internally, and typically not observable for most configurations. Take the following precautions to minimize clock noise in the signal chain. The clocking creates a small charge-injection pulse at the input of the amplifier; therefore, do not use high-value resistors (> 100 kΩ) in series with the inputs to avoid higher clock voltage noise at the output. The charge injection pulses are minimized when the impedance to the input pins is matched. If higher value resistors are used, then use matching impedances on both amplifier input pins.

7.2 Typical Applications

7.2.1 Bidirectional Current Sensing

This single-supply, low-side, bidirectional current-sensing design example detects load currents from –1 A to +1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the TLVx387 because of the device low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage. Figure 7-1 shows the design example schematic.

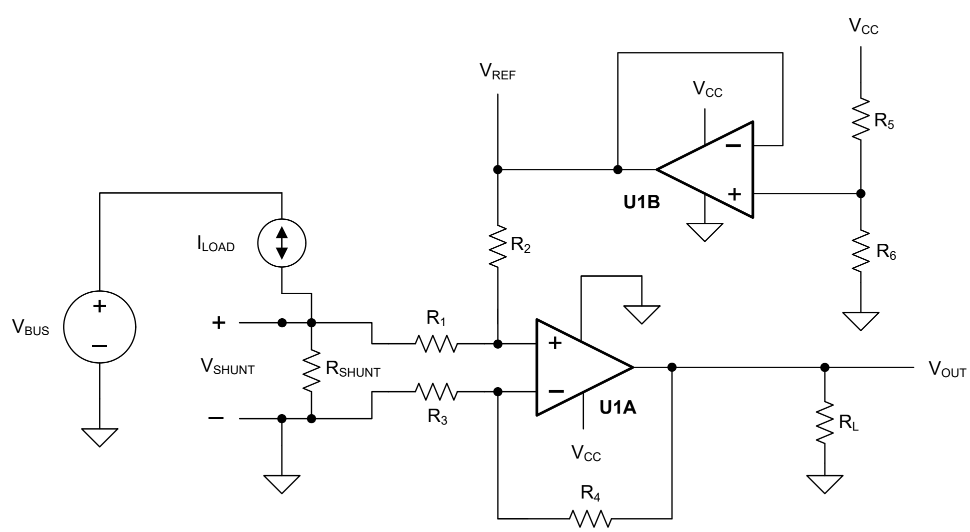


Figure 7-1. Bidirectional Current-Sensing Schematic

7.2.1.1 Design Requirements

This design example has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to +1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

7.2.1.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor, R_{SHUNT}, to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF} \tag{1}$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6}\right)$

There are two types of errors in this design: gain and offset. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \tag{2}$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% is selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to +100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Use an operational amplifier, such as the TLVx387, that has a common-mode range that extends below the negative supply voltage. The offset error is minimal because the TLVx387 has a typical offset voltage of merely ±0.25 µV (±5 µV, maximum).

Given a symmetric load current of –1 A to +1 A, the voltage divider resistors, R_5 and R_6, must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% is selected. To minimize power consumption, 10-kΩ resistors are used.

To set the gain of the difference amplifier, the common-mode range and output swing of the TLVx387 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the TLVx387 given a 3.3-V supply.

$$-100\ mV < V_{CM} < 3.4\ V \tag{3}$$

$$100\ mV < V_{OUT} < 3.2\ V \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$Gain_{Diff\_Amp} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ V - 100\ mV}{100\ m\Omega \times [1\ A - (-\ 1A)]} = 15.5\ \frac{V}{V} \quad (5)$$

The resistor value selected for R_1 and R_3 is 1 kΩ. 15.4 kΩ is selected for R_2 and R_4 because this number is the nearest standard value. Therefore, in this example, the calculated gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

7.2.1.3 Application Curve

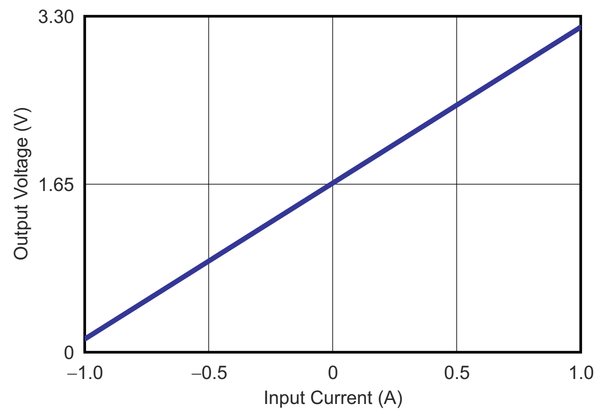


Figure 7-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

7.2.2 Load Cell Measurement

Figure 7-3 shows the TLVx387 in a high-CMRR dual-op amp instrumentation amplifier with a trim resistor and six-wire load cell for precision measurement.

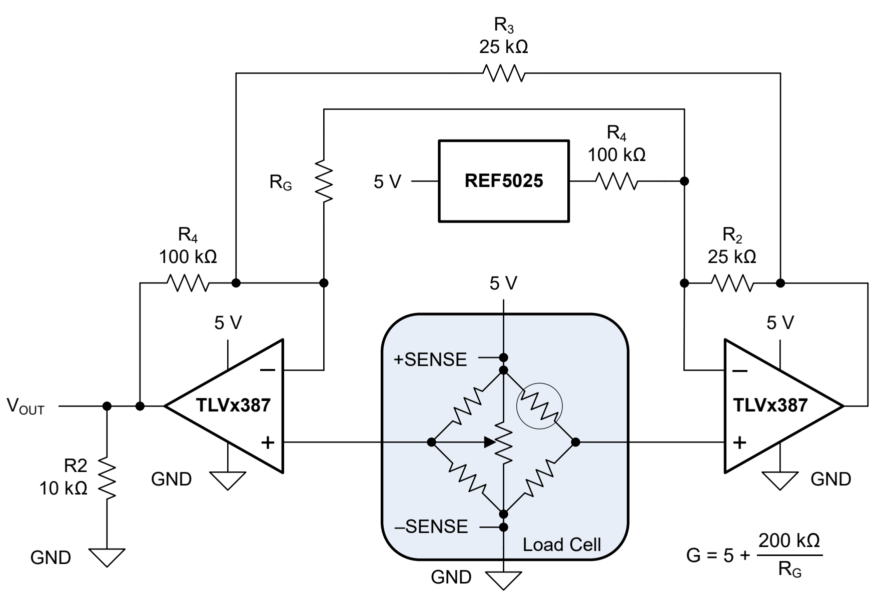


Figure 7-3. Load Cell Measurement Schematic

7.3 Power Supply Recommendations

The TLVx387 family of devices is specified for operation from 1.7 V to 5.5 V for single supplies, and ±0.85 V to ±2.75 V for dual supplies. Key parameters that can exhibit significant variance with regard to operating voltage are presented in Section 5.8.

CAUTION

Supply voltages greater than 6 V can permanently damage the device (see Section 5.1).

7.4 Layout

7.4.1 Layout Guidelines

Pay attention to good layout practice. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor close to the supply pins. These guidelines must be applied throughout the analog circuit to improve performance, and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by making sure that the potentials are equal on both input pins. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or higher depending on materials used.

7.4.2 Layout Example

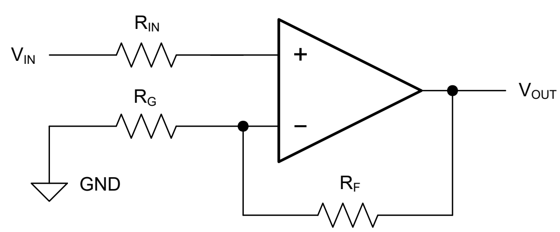


Figure 7-4. Schematic Representation

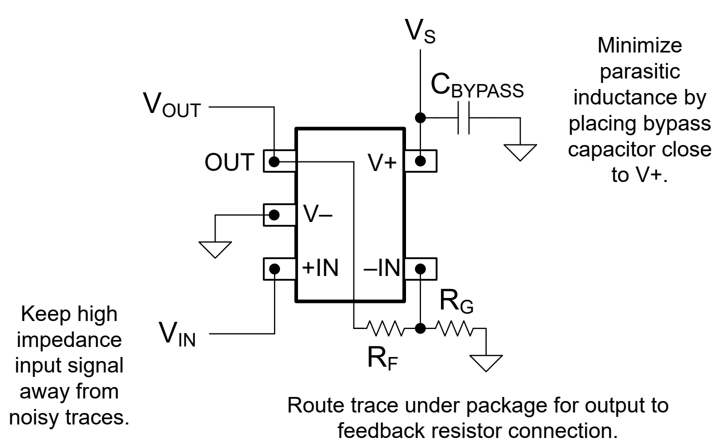


Figure 7-5. Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following: Texas Instruments, *Circuit board layout techniques*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2023) to Revision B (December 2023) **Page**

- Changed document status from production mix to production data.. 1
- Changed TLV2387 D (SOIC, 8) package status from preview to production data (active)............................... 1

Changes from Revision * (December 2021) to Revision A (November 2023) **Page**

- Changed document status from production data to production mix with addition of preview D package...........1
- Changed TLV2387 and TLV4387 device statuses from preview to active.. 1
- Added TLV2387 preview D package (SOIC, 8) and associated content.. 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2387DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	3BBT	Samples
TLV2387DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL2387	Samples
TLV387DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2LOT	Samples
TLV387DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2LOT	Samples
TLV4387PWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TLV4387	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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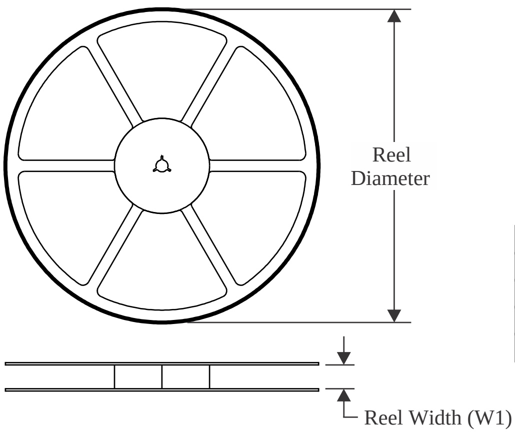
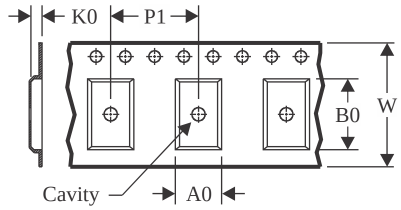
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

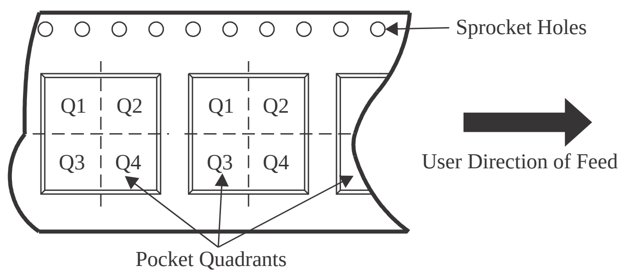


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

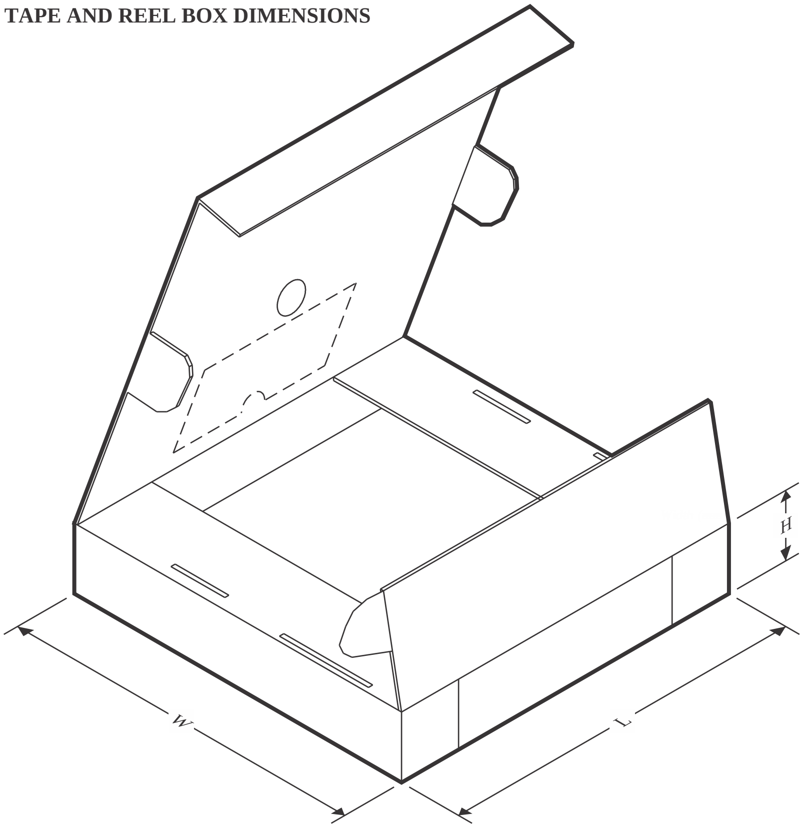
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

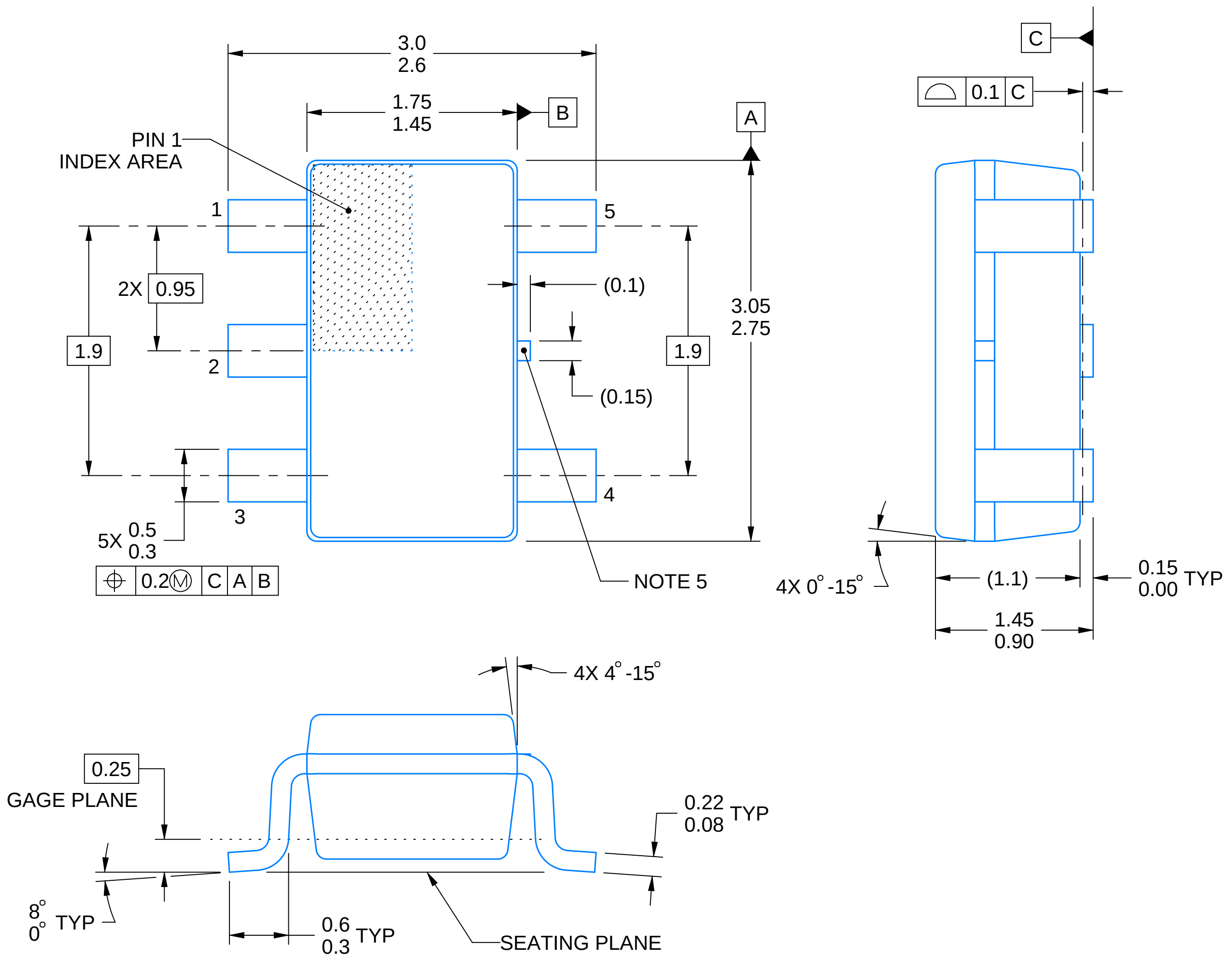
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2387DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV2387DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV387DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV387DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV4387PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

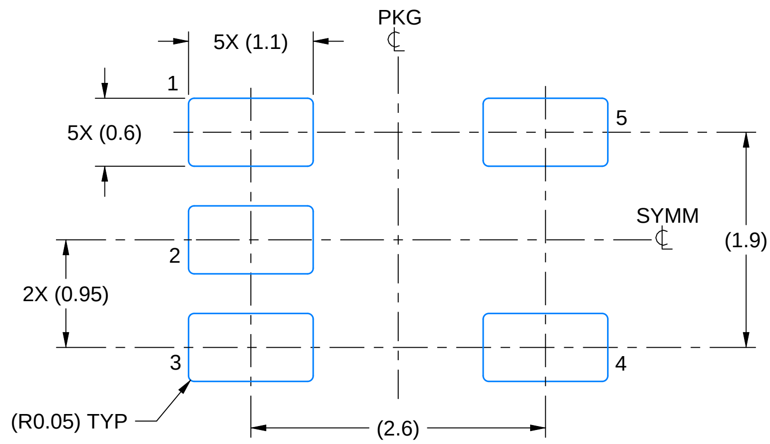
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2387DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2387DR	SOIC	D	8	3000	356.0	356.0	35.0
TLV387DBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
TLV387DBVT	SOT-23	DBV	5	250	190.0	190.0	30.0
TLV4387PWR	TSSOP	PW	14	3000	356.0	356.0	35.0



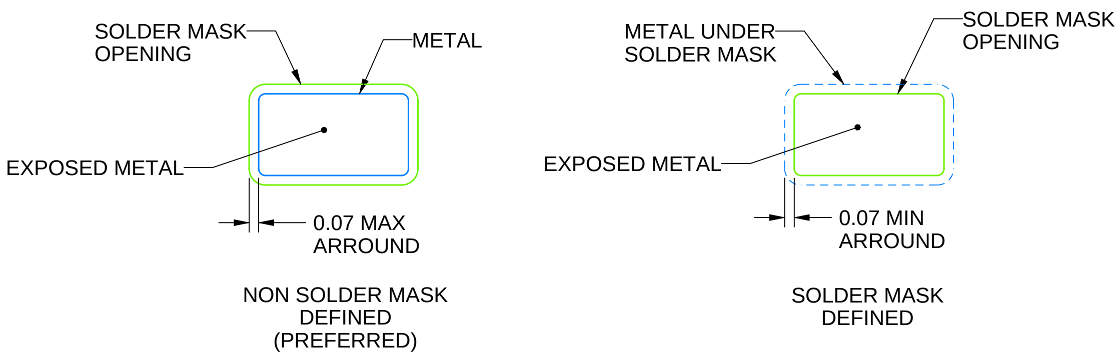
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

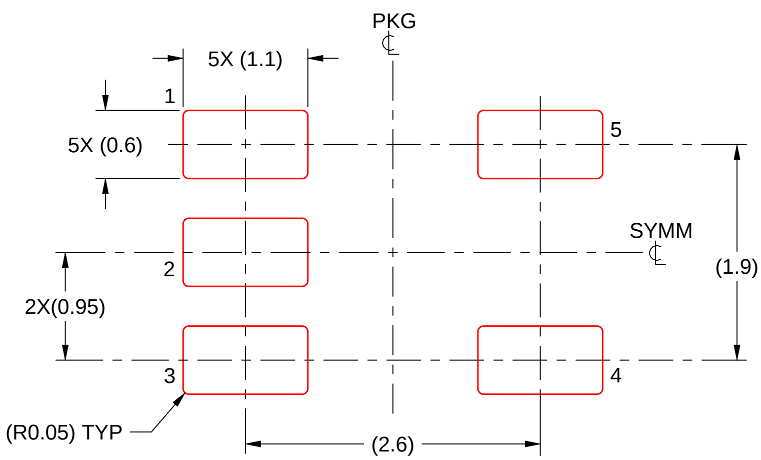


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

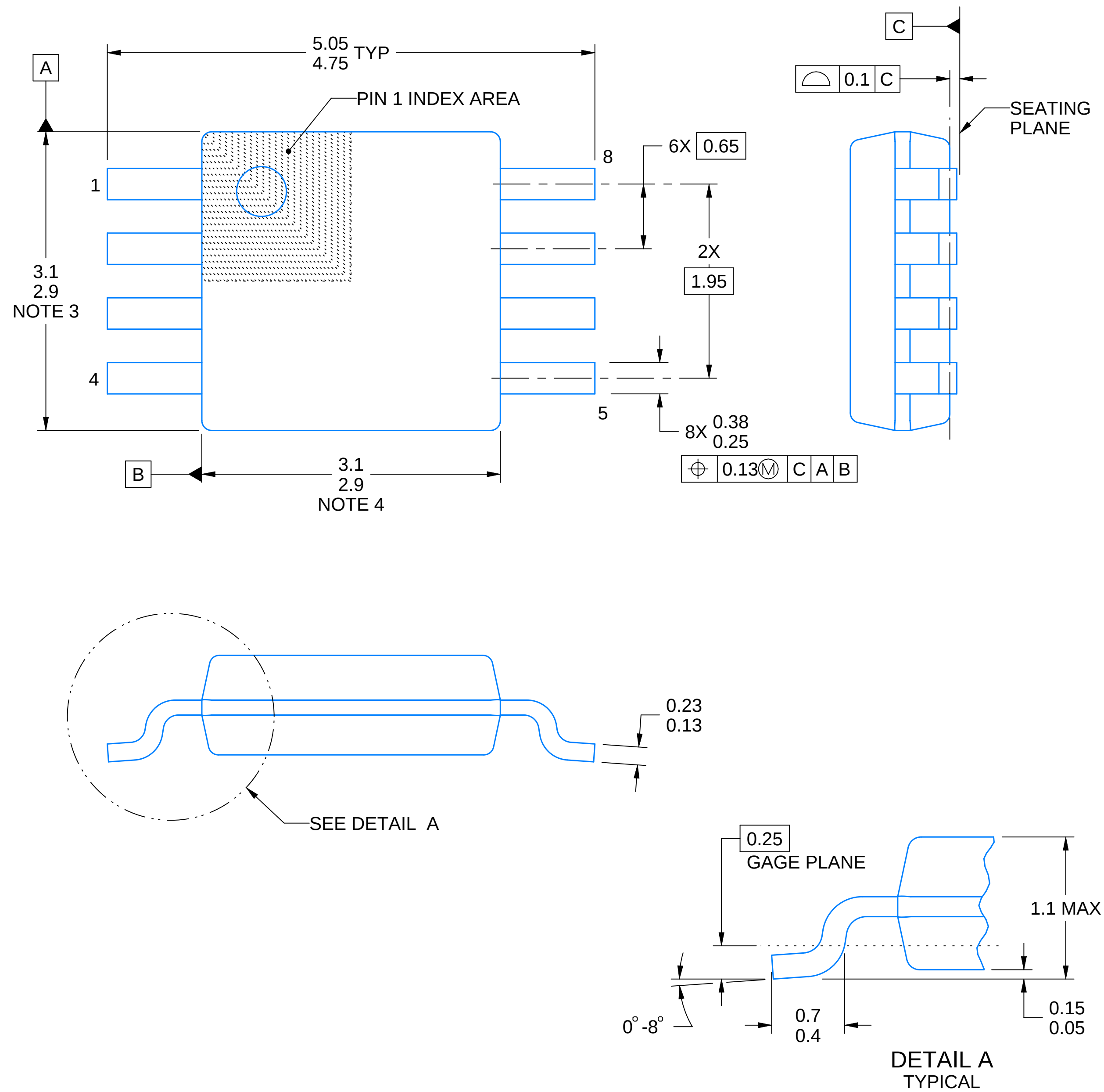
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

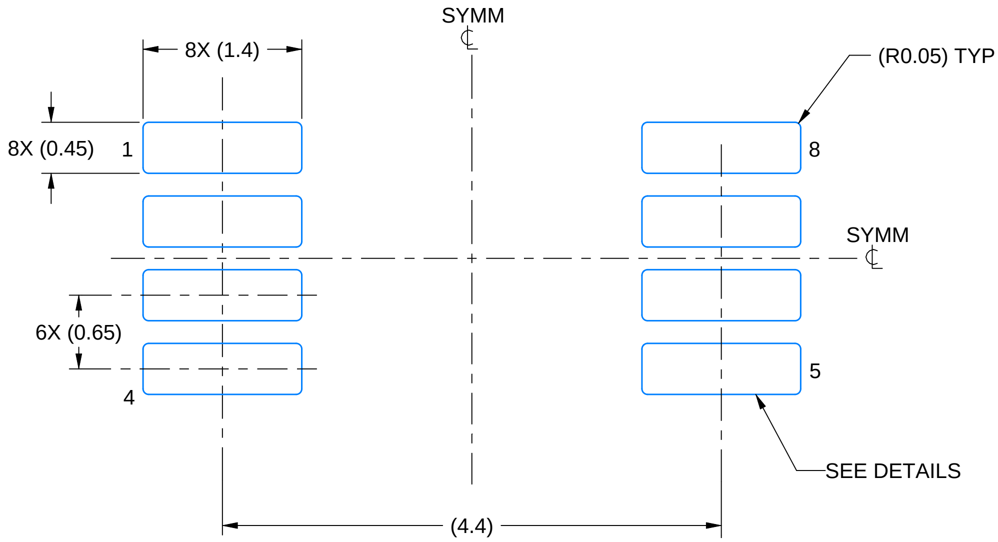


4214862/A 04/2023

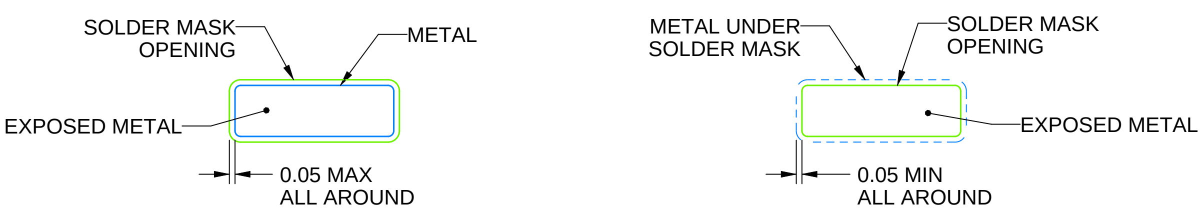
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

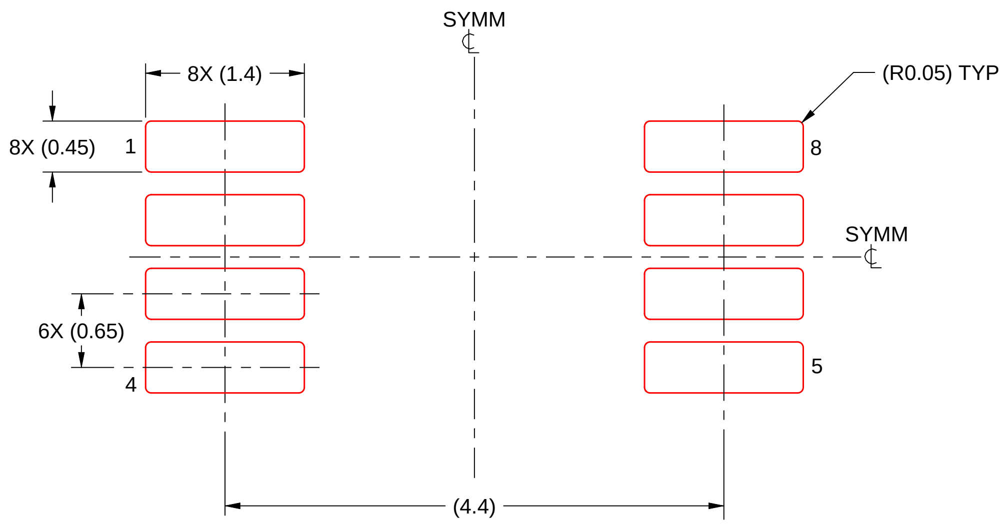


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

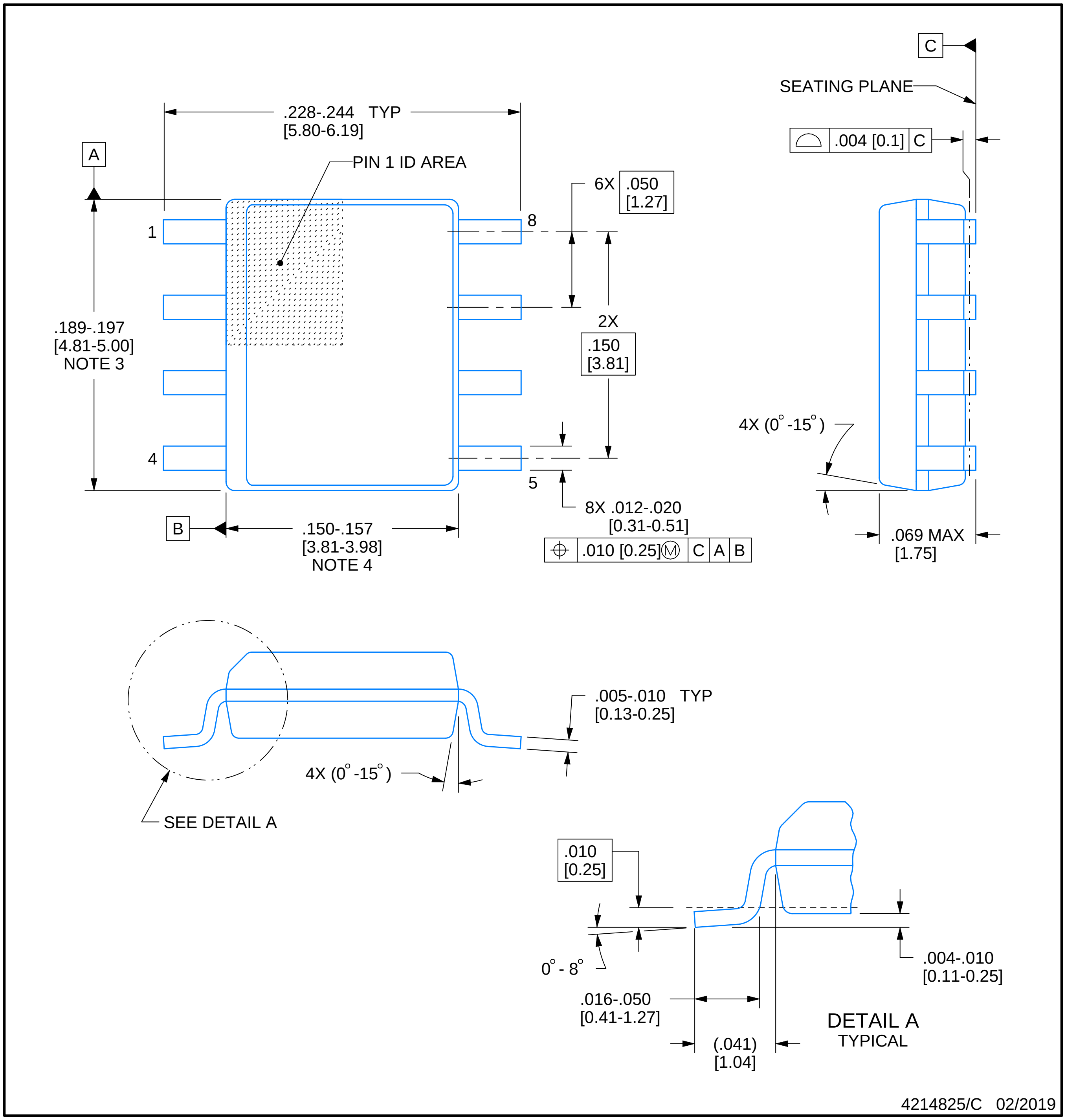


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

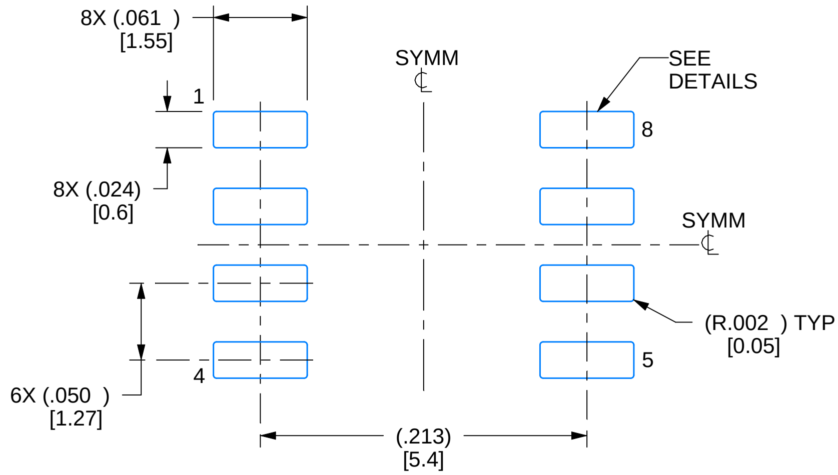
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

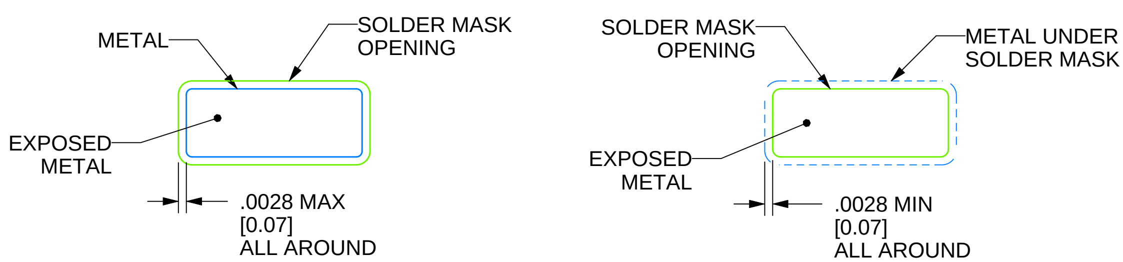


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

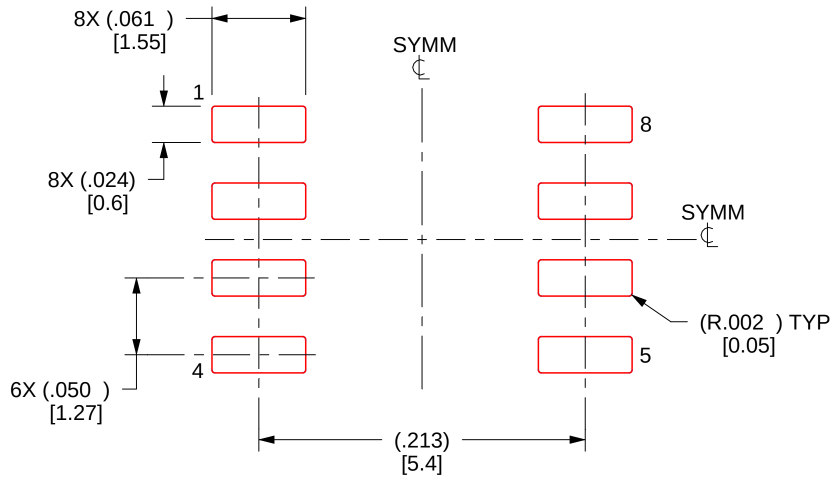
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

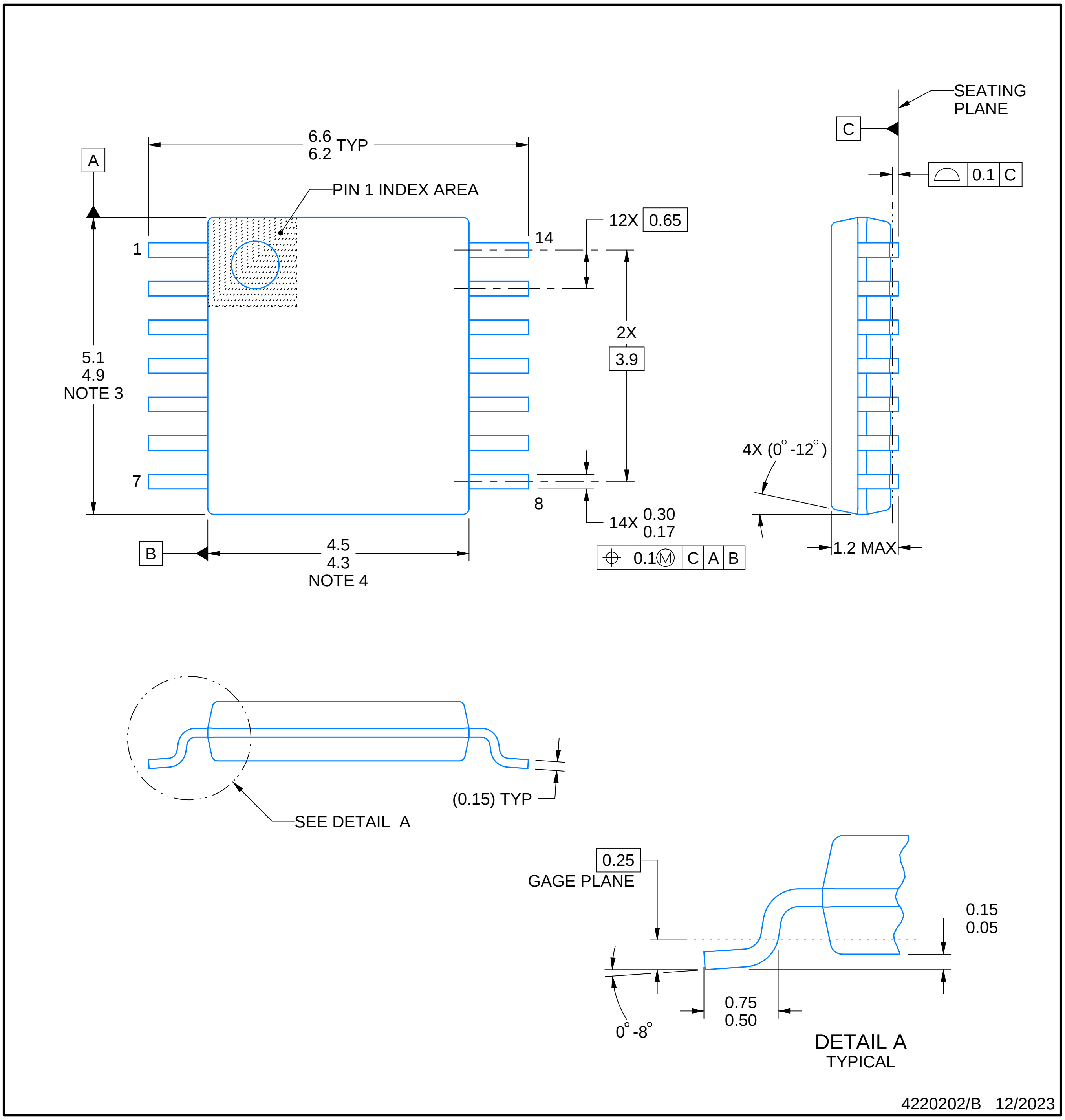


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

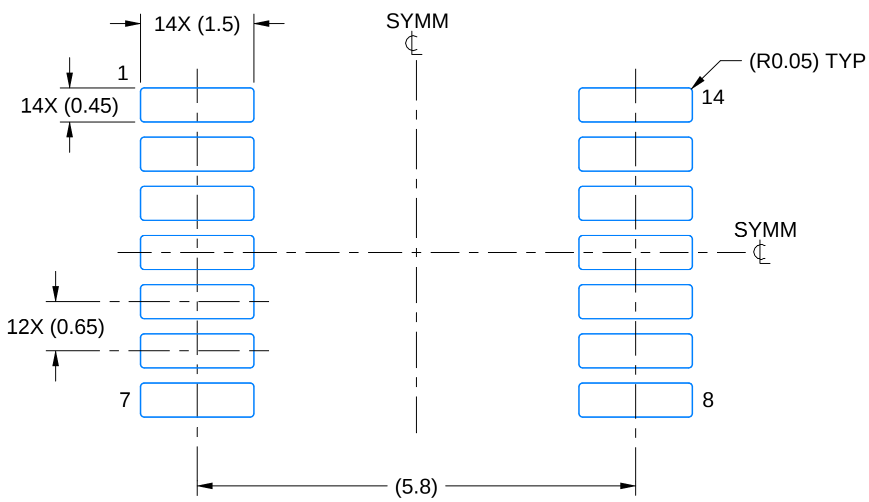
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

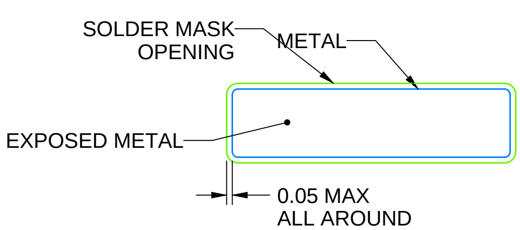


NOTES:

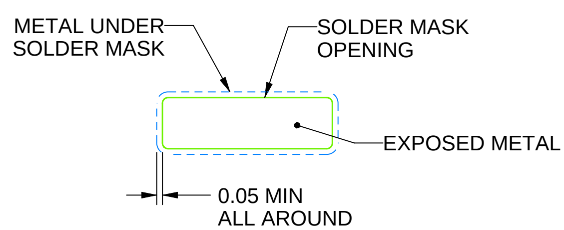
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)



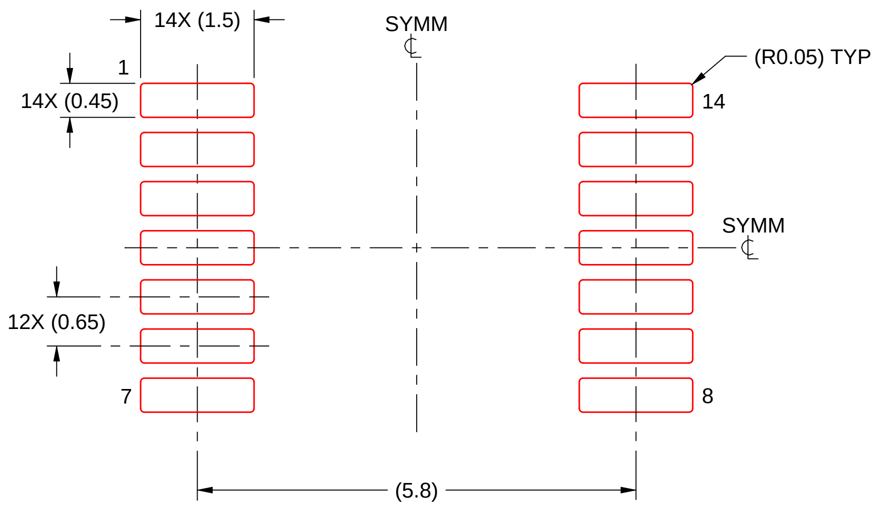
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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