TMP127-Q1 Automotive Grade, 0.8 °C SPI Temperature Sensor With 175 °C Operation

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade-0: –55 °C to 175 °C ambient operating temperature
  - Device HBM classification level 2
  - Device CDM classification level C2b
- Functional Safety Capable
  - Documentation available to aid functional safety system design
- High accuracy
  - ±0.8 °C (maximum) from –55 °C to 150 °C
  - ±1 °C (maximum) from 150 °C to 175 °C
- Supply range of 1.62 V to 5.5 V
- Automated continuous conversion mode
- Shutdown mode
- Low power consumption
  - Typical standby current of 0.5 µA
  - Typical shutdown current of 0.35 µA
- Factory calibrated
- 3-wire SPI interface

2 Applications

- Transmission control units
- On-board chargers (OBC)
- Brake systems
- Field transmitters
- Building and factory automation
- Avionics
- Ultrasonic level sensing
- Vehicle control units (VCU)
- Powertrain exhaust sensor
- Electric power steering (EPS)

3 Description

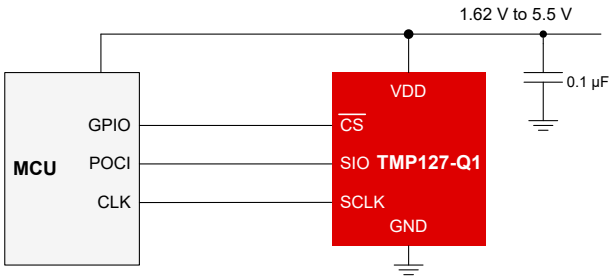
The TMP127-Q1 is a high accuracy 0.8 °C digital temperature sensor that supports an ambient temperature range of -55 °C to 175 °C. The TMP127-Q1 features a 14-bit signed temperature resolution (0.03125 °C per LSB) while operating over a supply range of 1.62 V to 5.5 V. The device has excellent PSR, able to maintain accuracy over the entire supply range. With a fast conversion rate, low supply current, simple SPI compatible interface, and an enhanced operational temperature range it is ideal for a wide range of applications.

The TMP127-Q1 SPI interface features a simplified no register map protocol, with a read-only 3-Wire configuration and an optional read-write 4-Wire configuration. The TMP127-Q1 is a drop-in, software compatible replacement to the LM71 and is available in a small SOT package for close placement to heat sources and quick response times.

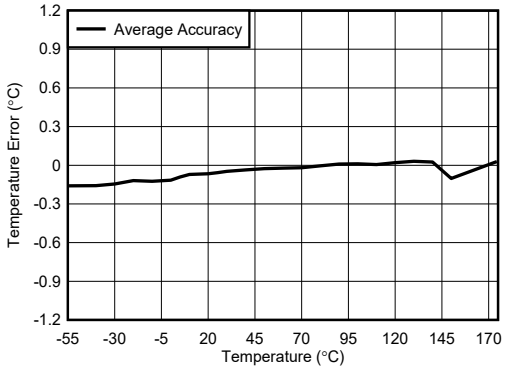
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TMP127-Q1	SOT-23 (6)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application



Temperature Accuracy

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (March 2022)	Page
• Changed data sheet status from: Advanced Information to: Production Data	1

5 Device Comparison

Table 5-1. Device Comparison

Feature	TMP127-Q1	TMP127-Q1
Accuracy	0.25 °C	0.8 °C
Packages	DBV, DCK	DBV
Continuous and shutdown mode	•	•
175 °C operation	•	•
Grade-0	•	•
NIST Traceable	•	
Alert pin functionality	•	
Slew rate warning	•	
CRC option	•	

6 Pin Configuration and Functions

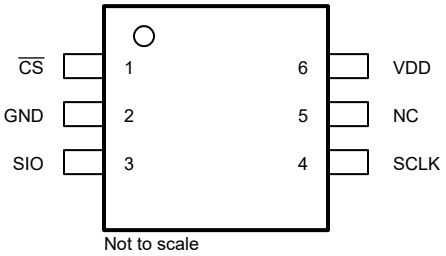


Figure 6-1. DBV 6-Pin SOT-23 (Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CS}$	1	I	Active low chip select signal to activate SPI interface
GND	2	–	Ground
SIO	3	I/O	Peripheral input/output
SCLK	4	I	Peripheral clock input
NC	5	NC	No Connect. Must be left floating or grounded.
VDD	6	–	Supply voltage

7 Specifications

7.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	6	V
I/O voltage	SIO	–0.3	V_{DD} + 0.2 V	V
I/O voltage	$\overline{CS}$, SCLK	–0.3	6	V
Operating junction temperature, T_J		–65	180	°C
Storage temperature, T_{stg}		–65	180	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 HBM classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C2b	±750	V

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.62	3.3	5.5	V
$V_{I/O}$	SIO	0		V_{DD}	V
$V_{I/O}$	$\overline{CS}$, SCLK	0		5.5	V
T_A	Operating ambient temperature(1)	-55		175	°C

(1) HTOL was performed at 175 °C for 1410 hours

7.4 Thermal Information

THERMAL METRIC(1)		TMP127-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over free-air temperature range and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR						
T_{ERR}	Temperature accuracy	-55 ℃ to 150 ℃	-0.8		0.8	°C
	Temperature accuracy	150 ℃ to 175 ℃	-1		1	°C
PSR	DC power supply rejection			12.7		m°C/V
T_{RES}	Temperature resolution	Including sign bit		14		Bits
		LSB		31.25		m°C
T_{REPEAT}	Repeatability(1)	V_{DD} = 3.3 V		±1		LSB
T_{LTD}	Long-term stability and drift(2)	1000 hours at 175 °C		0.07		°C
	Temperature cycling and hysteresis(3)			±0.5		LSB
t_{CONV_PERIOD}	Conversion Period			200	270	ms
t_{CONV}	Active conversion time		4.5	6	7.5	ms
DIGITAL INPUT/OUTPUT						
C_{IN}	Input capacitance	f = 1 MHz			20	pF
V_{IH}	Input logic high level	SCLK, SIO, $\overline{CS}$	0.7 * V_{DD}		V_{DD}	V
V_{IL}	Input logic low level	SCLK, SIO, $\overline{CS}$	0		0.3 * V_{DD}	V
I_{IN}	Input leakage current	SCLK, SIO, $\overline{CS}$	-0.5		0.5	µA
V_{OH}	SIO output high level	I_{OH} = 3 mA	V_{DD} - 0.4		V_{DD}	V
V_{OL}	SIO output low level	I_{OL} = -3 mA	0		0.4	V

Over free-air temperature range and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD_ACTIVE}	Supply current during active conversion	$\overline{CS}$ = V_{DD}	T_A = 25 °C		77	87	µA
			T_A = -55 °C to 150 °C			135	
			T_A = 175 °C			160	
I_{DD}	Average current consumption	$\overline{CS}$ = V_{DD}	T_A = 25 °C		2.65	4	µA
			T_A = -55 °C to 150 °C			19	
			T_A = 175 °C			38	
I_{SB}	Standby current(4)	$\overline{CS}$ = V_{DD}	T_A = 25 °C		0.5	0.75	µA
			T_A = -55 °C to 150 °C			15	
			T_A = -55 °C to 175 °C			34	
I_{SD}	Shutdown current	$\overline{CS}$ = V_{DD}	T_A = 25 °C		0.35	0.5	µA
			T_A = -55 °C to 150 °C			15	
			T_A = -55 °C to 175 °C			34	
V_{POR}	Power-on reset threshold voltage	Supply rising			1.3		V
	Brownout detect	Supply falling			1.1		V
t_{RESET}	Reset Time	Time required by device to reset			0.5		ms

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) Long term stability is determined using accelerated operational life testing at a junction temperature of 150 °C.
(3) Hysteresis is defined as the ability to reproduce a temperature reading as the temperature varies from room → hot →room→cold→room. The temperatures used for this test are -40 °C, 25 °C, and 150 °C.
(4) Quiescent current between conversions

7.6 SPI Interface Timing

Over free-air temperature range and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted)

		SPI BUS		UNIT
		MIN	MAX	
f_{CLK}	SCLK frequency		10	MHz
t_{CLK}	SCLK Period	100		ns
t_{LEAD}	Falling edge of $\overline{CS}$ to rising edge of SCLK setup time	100		ns
t_{LAG}	Rising edge of SCLK to rising edge of $\overline{CS}$ setup time	20		ns
t_{SU}	SIO to SCLK rising edge setup time	10		ns
t_{HOLD}	SIO hold time after rising edge of SCLK	20		ns
t_{VALID}	Time from falling edge of SLCK to valid SIO data		35	ns
$t_{SIO(DIS)}$	Time from rising edge of $\overline{CS}$ to SIO high-impedance		200	ns
$t_{SIO(EN)}$	Time from falling edge of $\overline{CS}$ to SIO low impedance		70	ns
t_{RISE}	SIO, SCLK, $\overline{CS}$ rise time		100	ns
t_{FALL}	SIO, SCLK, $\overline{CS}$ fall time		100	ns
$t_{INTERFRAME}$	Delay between two SPI communication sequences ($\overline{CS}$ high)	100		ns
$t_{INITIATION}$	Delay between valid V_{DD} volage and initial SPI communication	0.5		ms

7.7 Timing Diagrams

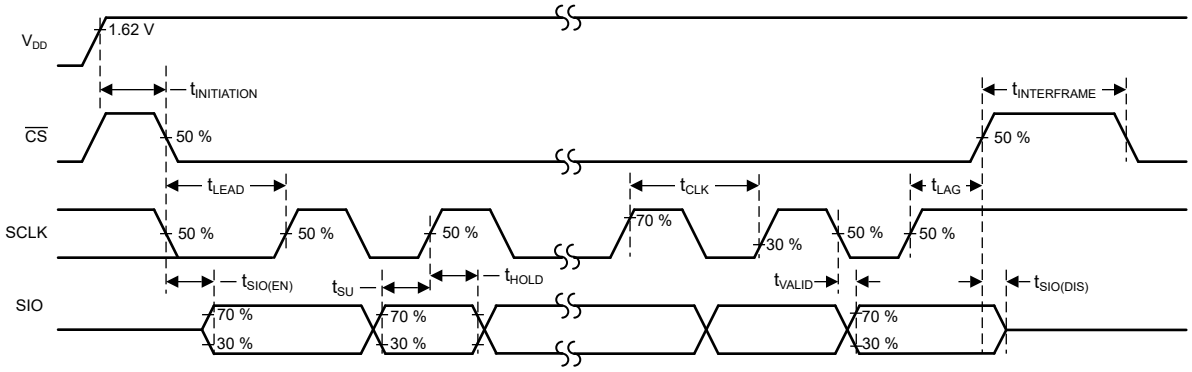


Figure 7-1. SPI Interface Timing Diagram

7.8 Typical Characteristics

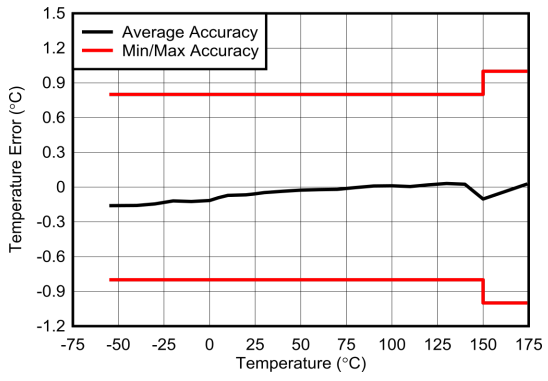


Figure 7-2. Temperature Accuracy

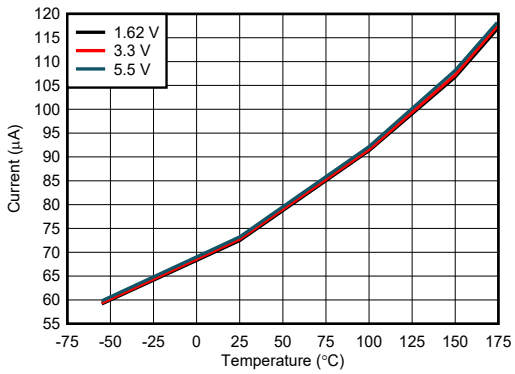


Figure 7-3. Active Conversion Current vs. Temperature

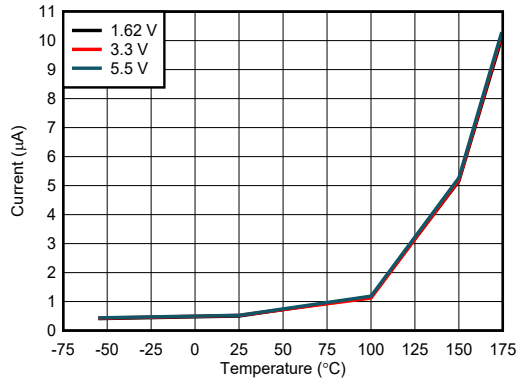


Figure 7-4. Standby Current vs. Temperature

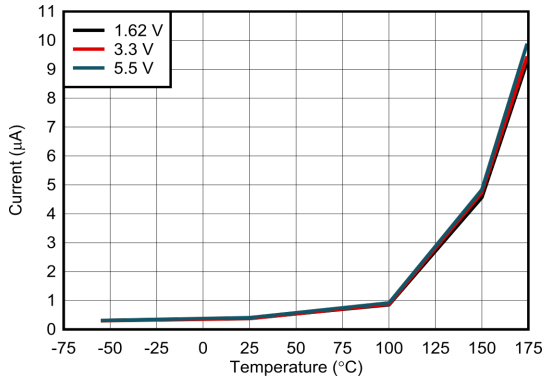


Figure 7-5. Shutdown Current vs. Temperature

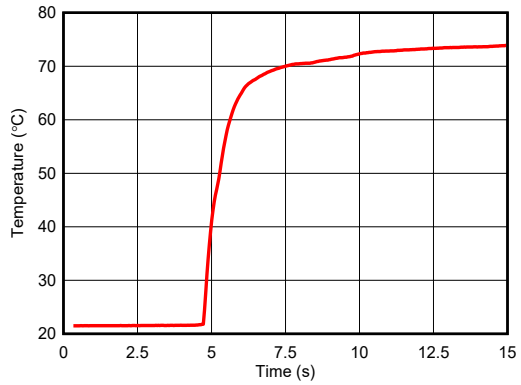


Figure 7-6. Stirred Liquid Single Layer Response Time (DBV)

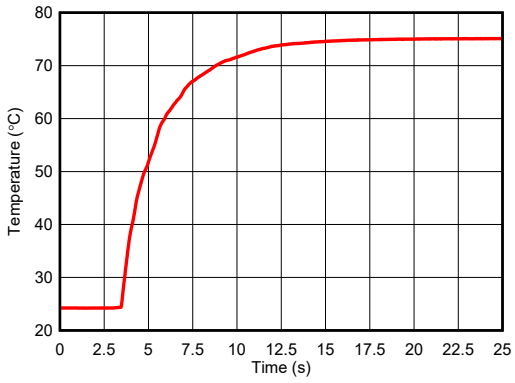


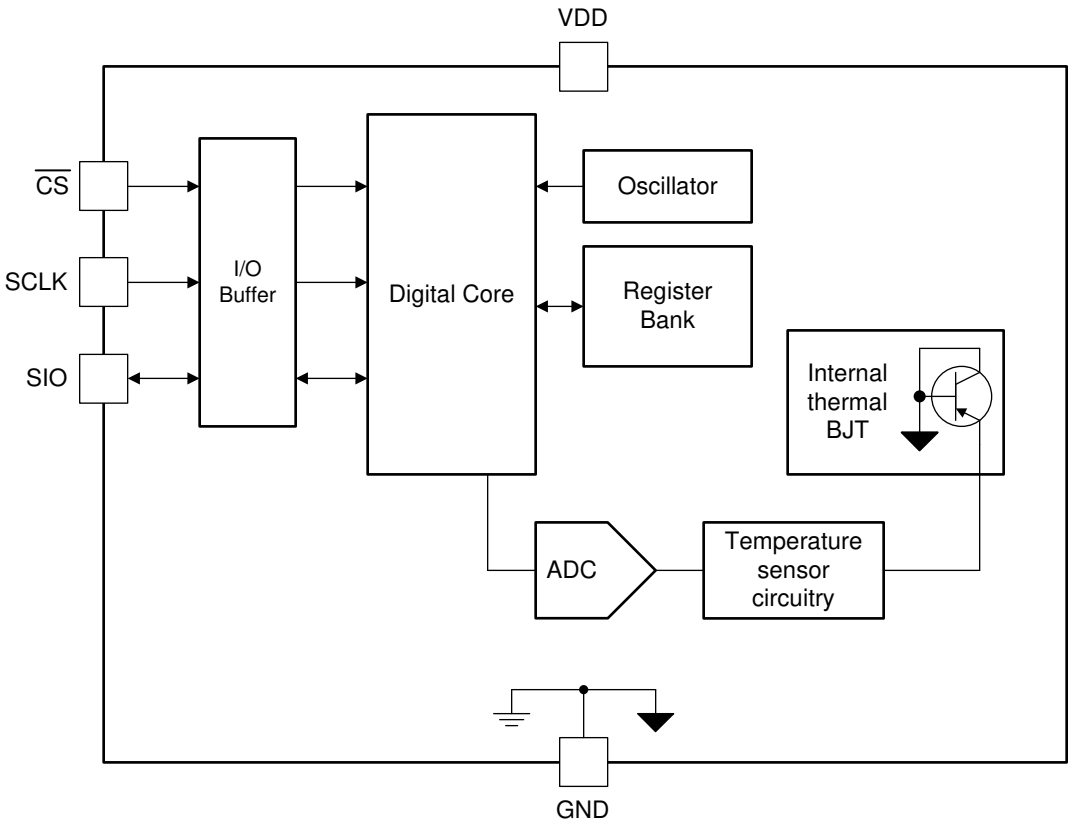
Figure 7-7. Stirred Liquid 2-Layer Response Time (DBV)

8 Detailed Description

8.1 Overview

The TMP127-Q1 is a factory-calibrated digital output temperature sensor designed for thermal management and thermal protection applications. The TMP127-Q1 has a 3-wire SPI-compatible interface with continuous conversion and shutdown modes. The shutdown mode can be used to optimize current consumption for low power applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Low Power Consumption

The TMP127-Q1 features a power optimized conversion period with minimized conversion time to reduce system power consumption. By minimizing the conversion time, the TMP127-Q1 operates mainly in the low-power, standby portion of the conversion period. This feature is designed for low-power or battery applications that operate in continuous conversion mode. The device also features a further power reduced shutdown mode for greater power savings.

8.4 Device Functional Modes

The TMP127-Q1 has two operation modes: continuous conversion mode and shutdown mode.

8.4.1 Continuous Conversion Mode

The TMP127-Q1 always powers up in the continuous conversion mode. Immediately after power up, the TMP127-Q1 temperature register will contain an erroneous code until the first temperature conversion has completed. In the continuous conversion mode, the TMP127-Q1 will run a temperature conversion every 200 ms. To enter continuous conversion mode from the shutdown mode, the user must write XX00h to the configuration register. If user writes XX00h to the configuration register, the continous conversion mode will repeatedly run and the device will continue the conversion period uninterrupted. Repeatedly reading and writing to the TMP127-Q1 will not cause adverse behavior. The temperature register output will update to the latest conversion results when $\overline{CS}$ is pulled low to start a temperature read.

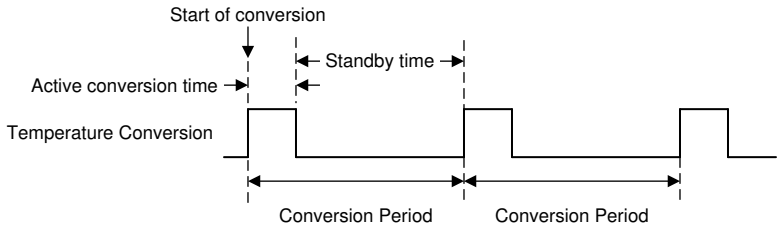


Figure 8-1. Conversion Period Timing Diagram

8.4.2 Shutdown Mode

If the user writes XXFFh to the configuration register, the device will enter shutdown mode. In shutdown mode, the serial bus is still active and the TMP127-Q1 will always output the device ID, 900Fh. If the TMP127-Q1 is performing a temperature conversion, the device will stop the temperature conversion and discard the data to enter shutdown mode immediately.

8.5 Programming

8.5.1 Temperature Data Format

Temperature data is represented by a 14-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.03125 °C. The last two bits of the register are always 11b.

Table 8-1. 14-Bit Temperature Data Format

Temperature	Digital Output	
	Binary	Hex
175 °C	0101 0111 1000 0011	5783
150 °C	0100 1011 0000 0011	4B03
125 °C	0011 1110 1000 0011	3E83
25 °C	0000 1100 1000 0011	0C83
0.03125 °C	0000 0000 0000 0111	0007
0°C	0000 0000 0000 0011	0003
−0.03125 °C	1111 1111 1111 1111	FFFF
−25 °C	1111 0011 1000 0011	F383
−40 °C	1110 1100 0000 0011	EC03
−55 °C	1110 0001 0000 0011	E483

The first data byte is the Most Significant Byte (MSB) with most significant bit first, permitting only as much data as necessary that must be read to determine temperature condition. For example, if the first four bits of the temperature data indicate an overtemperature condition, the host controller could immediately take action to remedy the excessive temperatures.

8.5.2 Serial Bus Interface

The TMP127-Q1 operates as a peripheral and is compatible with SPI or MICROWIRE bus specifications. Data is clocked out on the falling edge of the serial clock (SCLK), while data is clocked in on the rising edge of SCLK. A complete transmit/receive communication will consist of 32 serial clocks. The first 16 clocks comprise the transmit phase of communication from the Device ID or Temperature Register, while the second 16 clocks are the receive phase to the Configuration Register. There is no issue using 8-bit SPI with the 16-bit interface as long as the $\overline{CS}$ remains low during the transaction. Mode transitions through writes to the configuration register will occur on the 16th rising clock edge during the 16-bit write.

Two modes of SPI communication are supported:

- Mode 0:
  - CPOL = 0
  - CPHA = 0
- Mode 3:
  - CPOL = 1
  - CPHA = 1

When $\overline{CS}$ is high, SIO will be in low-impedance tri-state. The user should take the chip select ($\overline{CS}$) low to initiate communication. This should not be done when SCLK is changing from a low to high state. When $\overline{CS}$ is low, the serial I/O pin (SIO) will transmit the first bit of data. The controller can then read this bit with the rising edge of SCLK. The remainder of the data will be clocked out by the falling edge of SCLK. $\overline{CS}$ can be taken high at any time during the transmit phase. If $\overline{CS}$ is brought low in the middle of a conversion, the TMP127-Q1 will complete the conversion and the output shift register will be updated after $\overline{CS}$ is brought back high.

The receive phase of a communication starts after 16 SCLK periods. $\overline{CS}$ can remain low as long as required. After 32 SCLK rising edges, the TMP127-Q1 will take control of the SIO pin and be ready for another read write cycle. The TMP127-Q1 will read the data available on the SIO line on the rising edge of the serial clock. The last 8 bits of the configuration register are the Mode[7:0] bits and place the device into shutdown or continuous conversion mode. The receive phase can last up to 16 SCLK periods. Only the following operation codes will affect the TMP127-Q1 and any other codes placed into the Mode[7:0] field will be ignored

- 00 hex for continuous conversion
- FF hex for shutdown

Figure 8-2 shows an overview of the communication protocol.

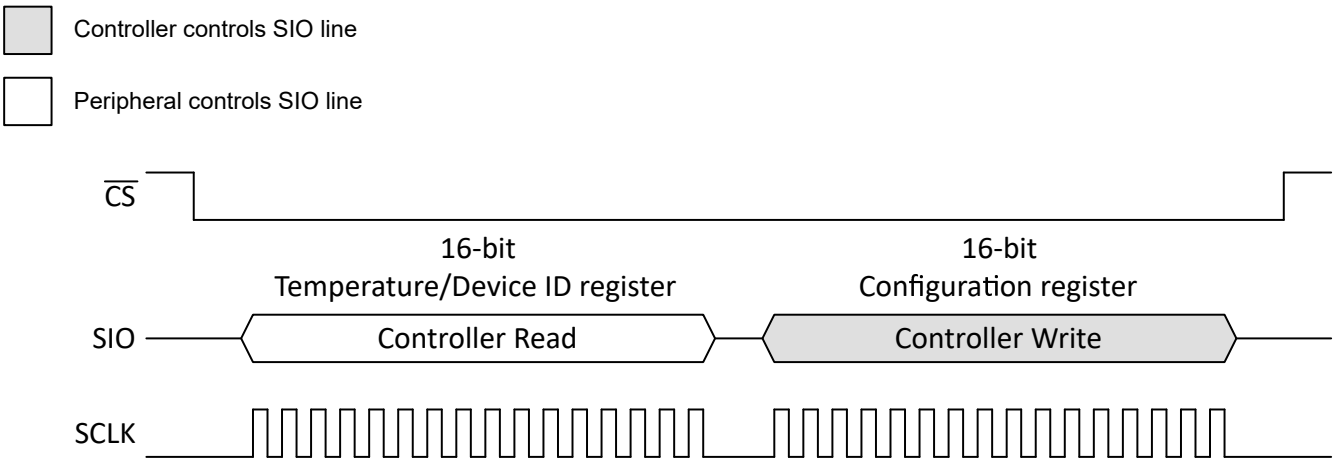


Figure 8-2. TMP127-Q1 Communication overview

After start-up or upon entering continuous mode, 200 ms must pass for a conversion to complete before the TMP127-Q1 transmits accurate temperature data.

The following communication can be used to determine the Manufacturer's/Device ID and then immediately place the part into continuous conversion mode. With $\overline{CS}$ continuously low:

- Read 16 bits of temperature data
- Write 16 bits of data commanding Shutdown Mode(00FFh)
- Read 16 bits of Manufacture's/Device ID data
- Write 16 bits of data commanding Continuous Conversion Mode (0000h)
- Take $\overline{CS}$ HIGH.

8.5.2.1 Communication in Shutdown Mode

Shutdown mode is enabled by writing XXFFh to the Mode byte in the configuration register. While in shutdown mode, the TMP127-Q1 will output the device ID information on the SIO pin for the first 16 clock cycles. After the 16th rising SCLK edge, the TMP127-Q1 will tri-state the SIO pin and be ready for the controller to write to the configuration register.

Figure 8-3 shows a diagram of the communication in shutdown mode.

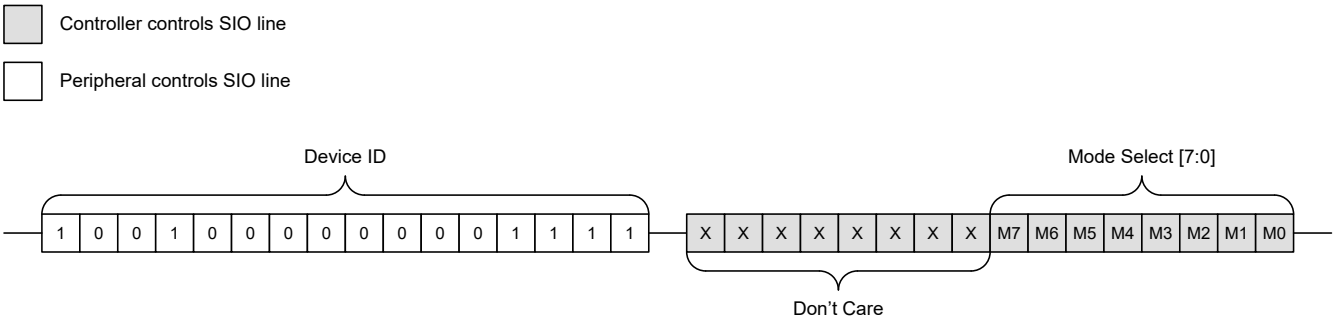


Figure 8-3. Shutdown Mode SPI Communication

8.5.2.2 Communication in Continuous Conversion Mode

Continuous Conversion mode is enabled by writing XX00h to the Mode byte in the configuration register. While in continuous conversion mode, the TMP127-Q1 will output the latest Temperature information on the SIO pin for the first 16 clock cycles. After the 16th falling SCLK edge, the TMP127-Q1 will tri-state the SIO pin and be ready for the Controller to drive the SIO pin to write to the configuration register.

Figure 8-3 shows a diagram of the communication in continuous conversion mode.

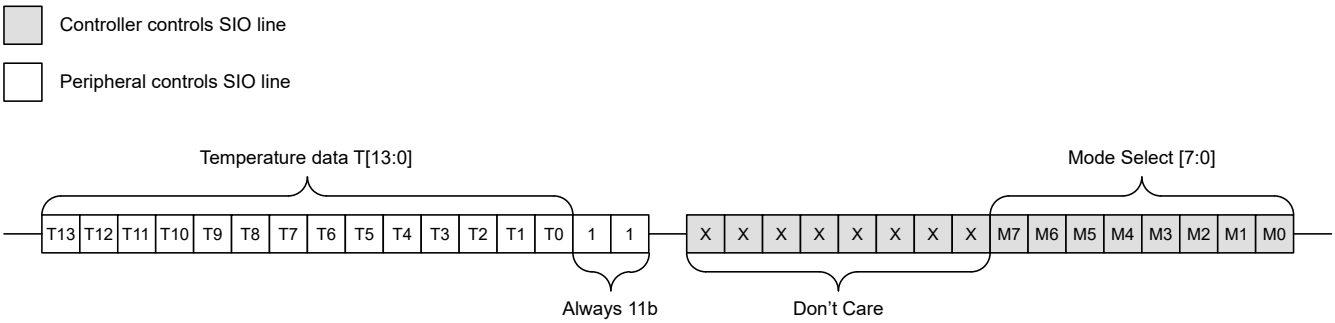


Figure 8-4. Continuous Conversion Mode SPI Communication

8.5.2.3 Internal Register Structure

The TMP127-Q1 has three registers that can be accessed depending on the operating mode of the device. The temperature register is accessible in the continuous conversion mode and is read-only. The device ID register is accessible in the shutdown mode and is read-only. The configuration register is accessible in either shutdown or continuous mode and is write-only.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMP127-Q1 operate in 2 different configurations to fit the system requirements: a standard read/write configuration or a read-only configuration.

9.2 Typical Applications

9.2.1 Read-Only Configuration

The TMP127-Q1 can operate in a read-only configuration when the host only needs to read the temperature data without changing the mode of device operation. In this configuration, the host does not need to connect the PICO pin to the SIO pin of the TMP127-Q1. Only the POCI pin is connected to SIO for read only operations.

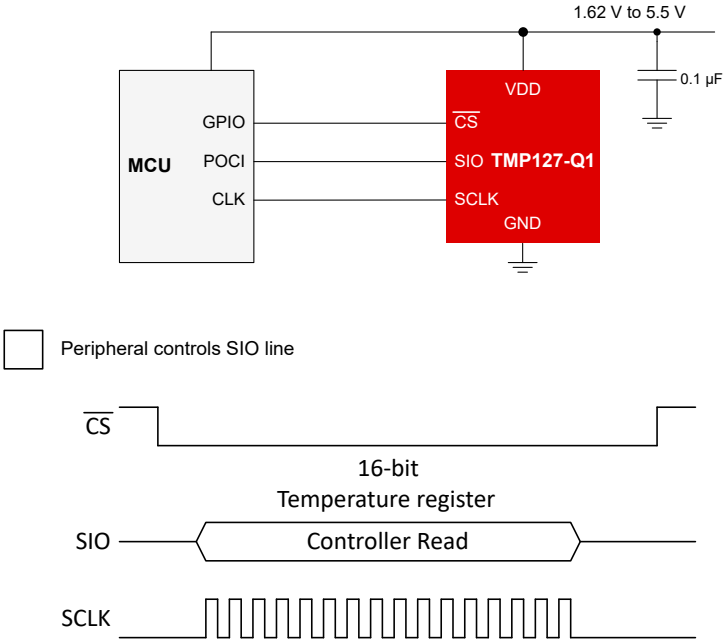


Figure 9-1. Read-Only Configuration

9.2.1.1 Design Requirements

For this design example, use the parameters listed below.

PARAMETER	Value
Supply (V_{DD})	1.62 V to 5.5 V

9.2.1.2 Detailed Design Procedure

The TMP127-Q1 will convert temperature at a 200-ms interval with a maximum conversion period of 270 ms per the *Electrical Characteristics* table. Reading from the TMP127-Q1 faster than the conversion period can result in data being retrieved twice before new data is available. Therefore TI recommends to read from the TMP127-Q1 in intervals greater than the maximum conversion period (like every 300 ms, for example). Reading faster than the conversion period will not disrupt device operation and can safely be done if desired.

In the read-only configuration, the TMP127-Q1 is not connected to a controller PICO pin. Due to this if the SCLK pin were to continue to be clocked for the write portion of the transaction, the SIO pin would be floating and the write value undetermined. It is for this reason that TI recommends to only perform the first 16 clock cycles to read the TMP127-Q1 temperature date and pull $\overline{CS}$ high after, as shown in Figure 9-1. This will ensure the TMP127-Q1 is never written to with a floating input.

9.2.2 Read/Write Configuration

The TMP127-Q1 can operate in a read/write configuration when the controller must both read and write to the TMP127-Q1.

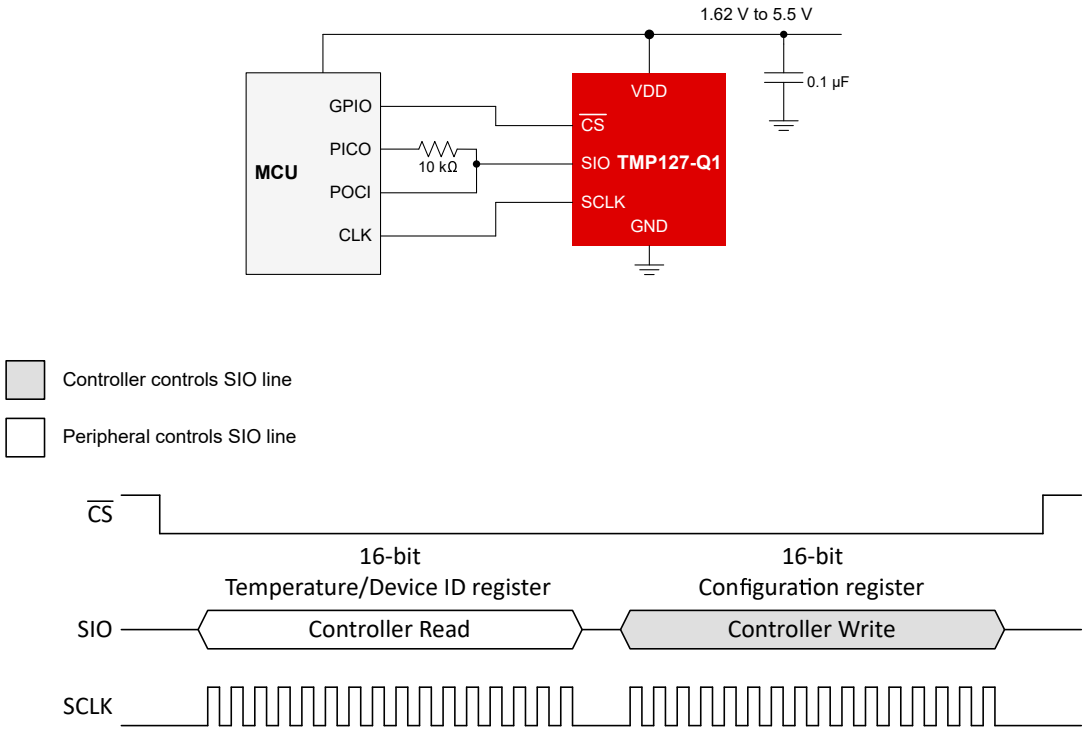


Figure 9-2. 4-Wire Configuration

9.2.2.1 Design Requirements

For this design example, use the parameters listed below.

PARAMETER	Value
Supply (V_{DD})	1.62 V to 5.5 V
Isolation Resistor	10 kΩ

9.2.2.2 Detailed Design Procedure

In this configuration, an isolation resistor is used between the PICO pin of the controller and the SIO pin of the TMP127-Q1 to prevent bus contention. Being able to write to the TMP127-Q1 will allow the system to use the shutdown mode and read the device ID.

10 Power Supply Recommendations

The TMP127-Q1 operates from a single supply VDD. This pin operates with a wide range of 1.62 V to 5.5 V and maintains accuracy across the entire supply range. A decoupling capacitor of 0.1 µF is recommended for the VDD pin. Place the capacitor as close to the pin as possible.

11 Layout

11.1 Layout Guidelines

Place the power-supply decoupling capacitor as close to the supply and ground pins as possible. The recommended value of this decoupling capacitor is 0.1 µF. Separation between the SCLK trace and the SI/O traces is recommended to reduce coupling of the clock onto the data line.

11.2 Layout Example

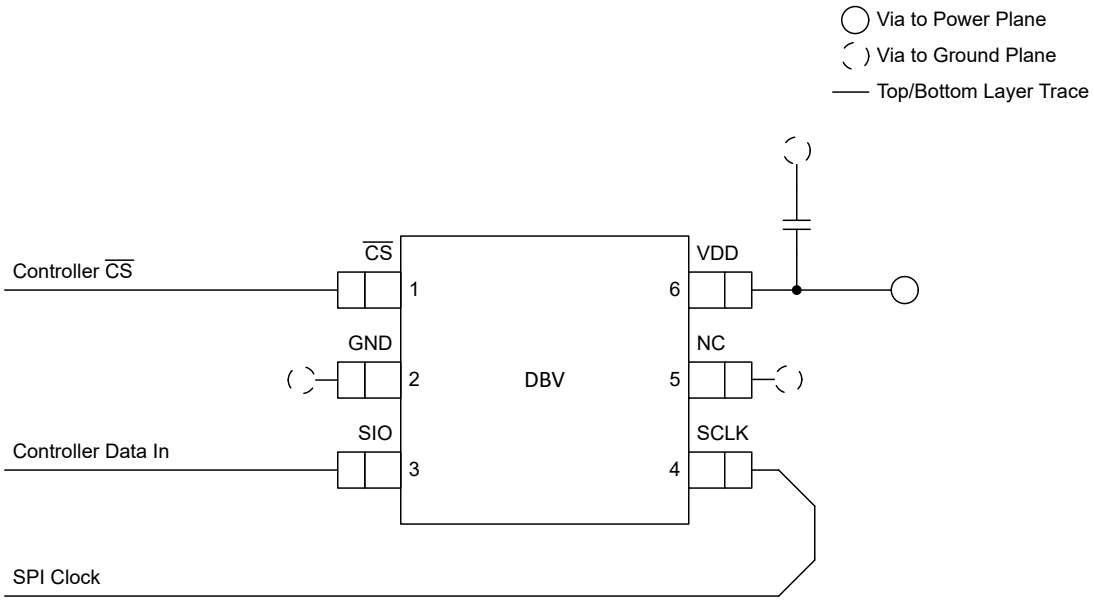


Figure 11-1. Read-Only Configuration Layout Example

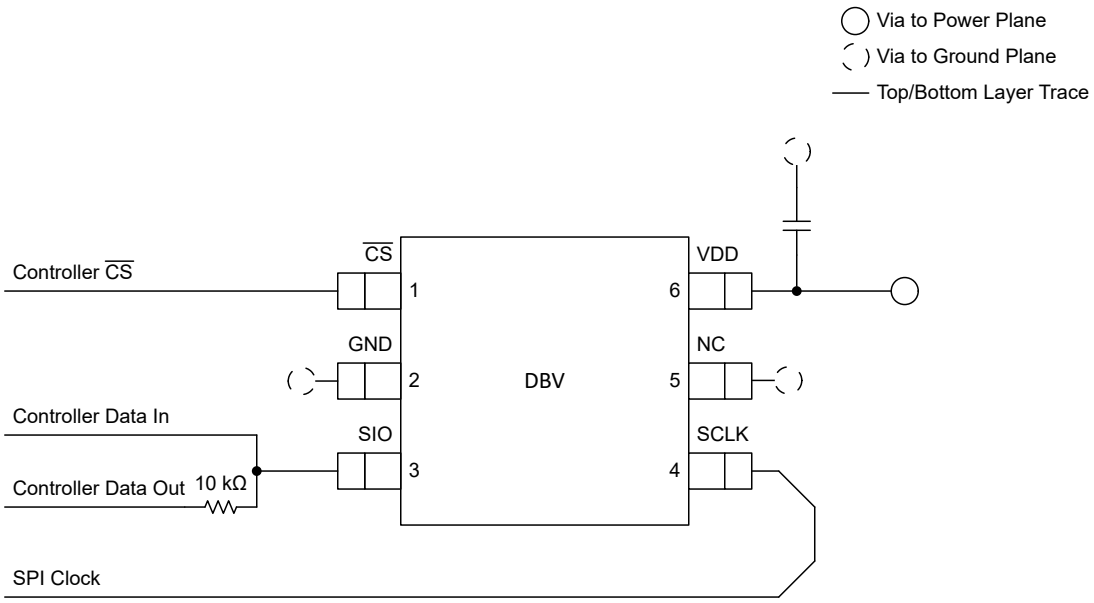


Figure 11-2. Read/Write Configuration Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP127EDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 175	2NGA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

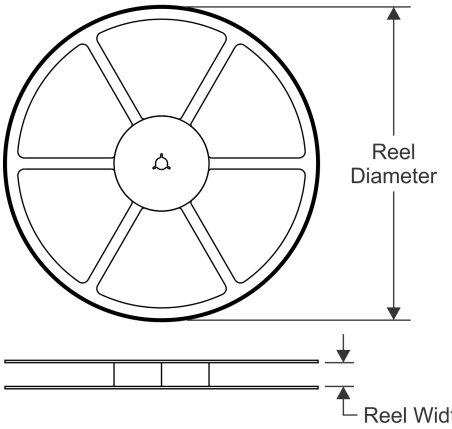
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

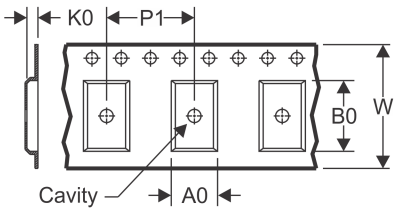
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

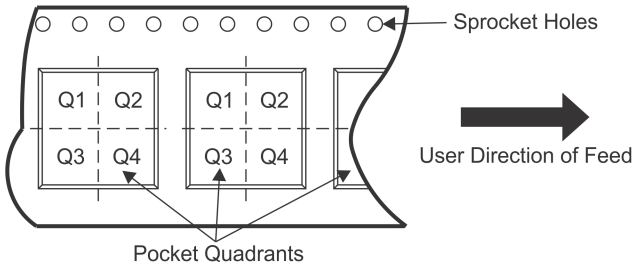


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

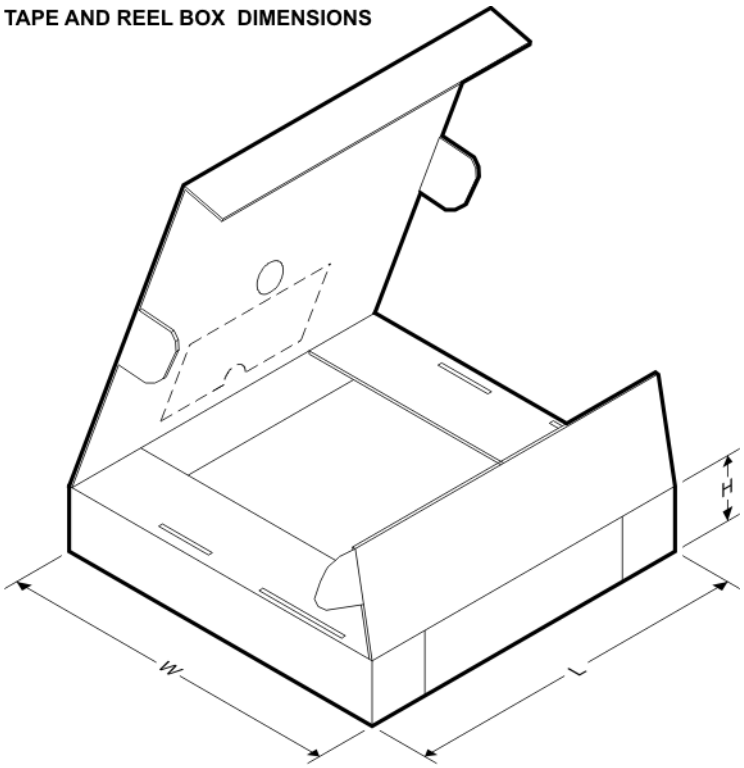
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP127EDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

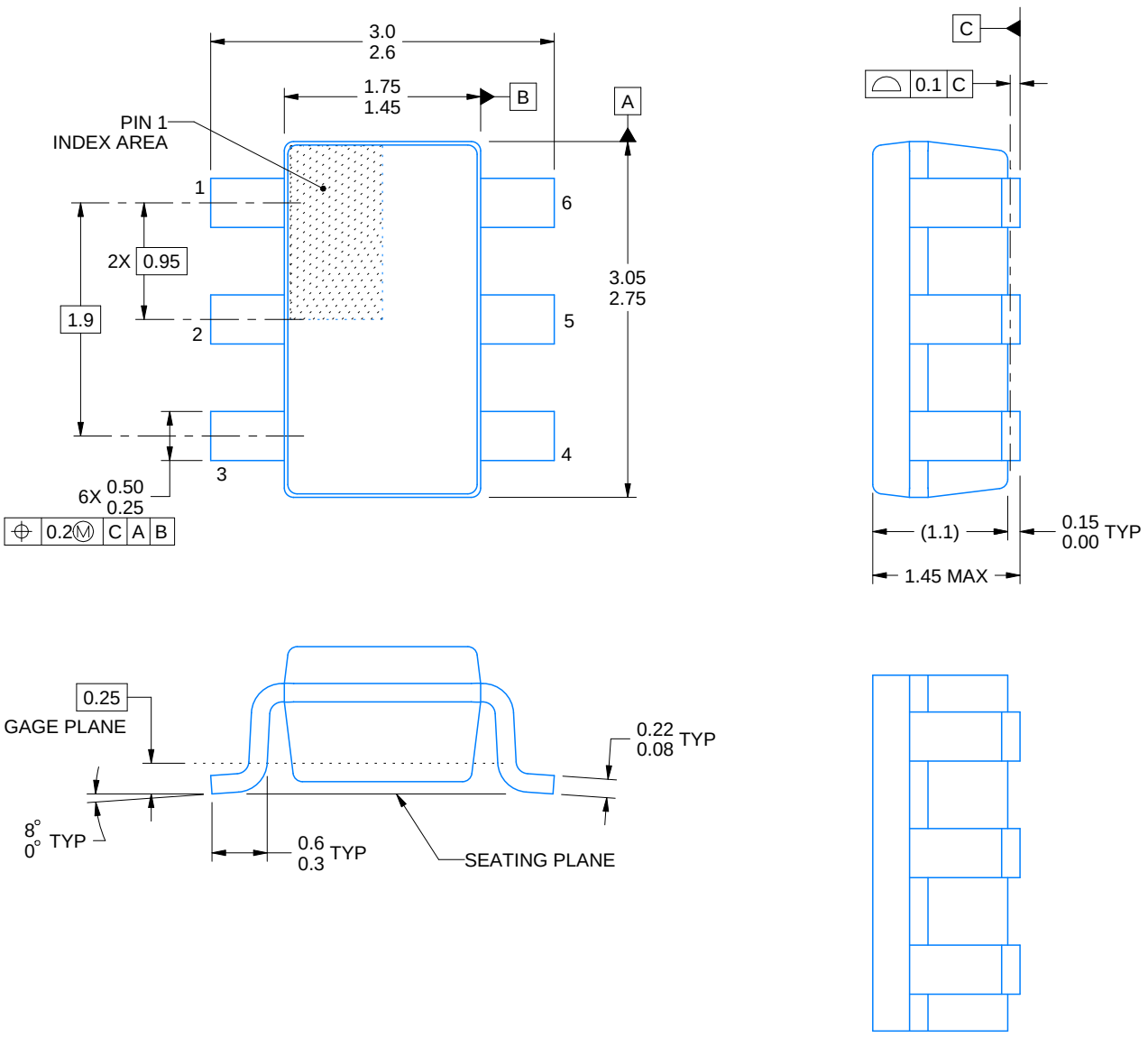
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP127EDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

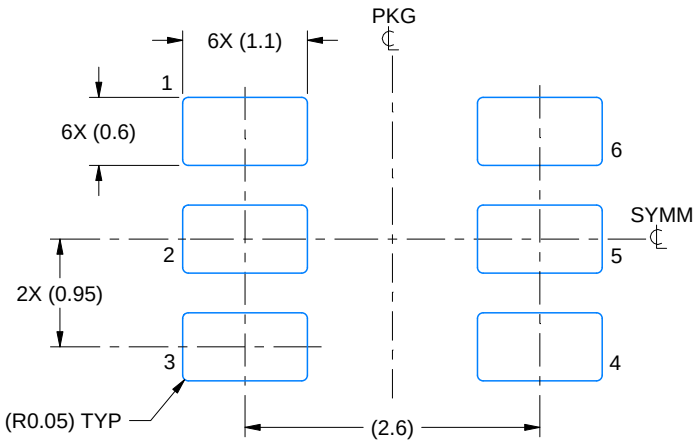


ALTERNATIVE PACKAGE SINGULATION VIEW

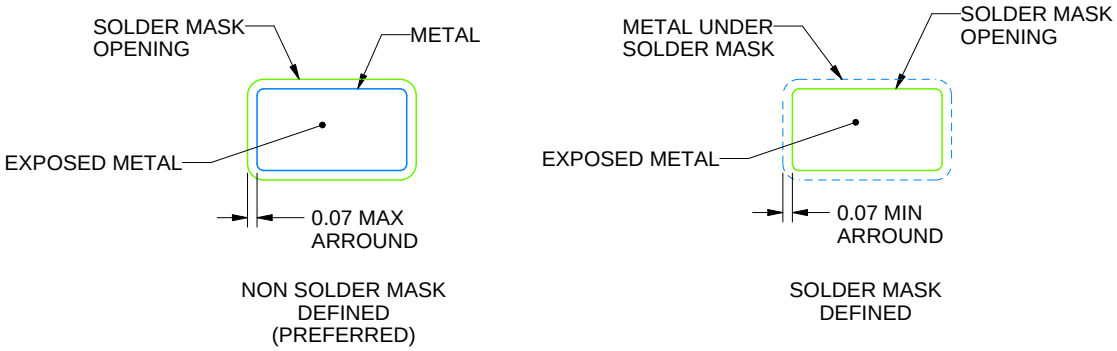
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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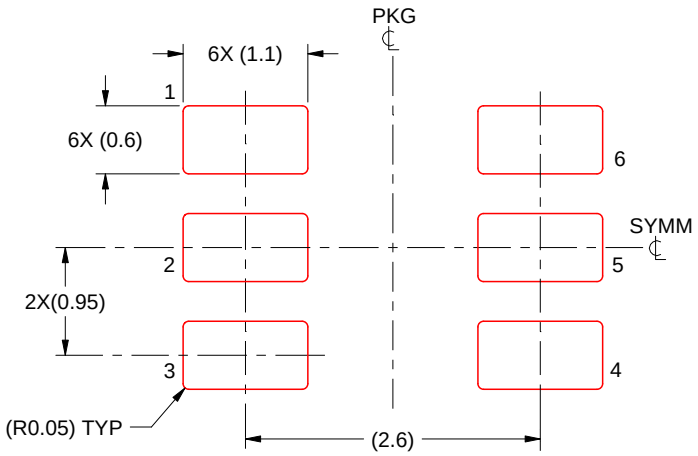
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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