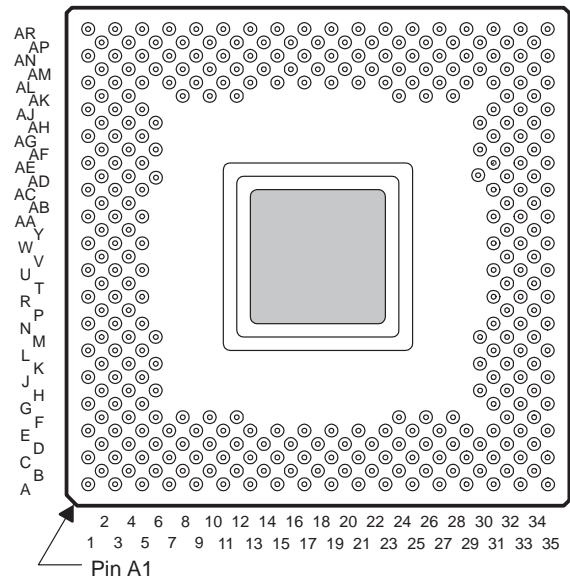


- **Highest Performance Floating-Point Digital Signal Processor (DSP)**
 - '320C40-60:
 - 33-ns Instruction Cycle Time,
 - 330 MOPS, 60 MFLOPS,
 - 30 MIPS, 384M Bytes/s
 - '320C40-50:
 - 40-ns Instruction Cycle Time
 - '320C40-40:
 - 50-ns Instruction Cycle Time
- **Six Communications Ports**
- **Six-Channel Direct Memory Access (DMA) Coprocessor**
- **Single-Cycle Conversion to and From IEEE-754 Floating-Point Format**
- **Single Cycle, $1/x$, $1/\sqrt{x}$**
- **Source-Code Compatible With TMS320C3x**
- **Single-Cycle 40-Bit Floating-Point, 32-Bit Integer Multipliers**
- **Twelve 40-Bit Registers, Eight Auxiliary Registers, 14 Control Registers, and Two Timers**
- **IEEE 1149.1† (JTAG) Boundary Scan Compatible**
- **Two Identical External Data and Address Buses Supporting Shared Memory Systems and High Data-Rate, Single-Cycle Transfers:**
 - High Port-Data Rate of 120M Bytes/s ('C40-60) (Each Bus)
 - 16G-Byte Continuous Program/Data/Peripheral Address Space
 - Memory-Access Request for Fast, Intelligent Bus Arbitration
 - Separate Address-Bus, Data-Bus, and Control-Enable Pins
 - Four Sets of Memory-Control Signals Support Different Speed Memories in Hardware
- **325-Pin Ceramic Grid Array (GF Suffix)**
- **Fabricated Using 0.72- μ m Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**
- **Software-Communication-Port Reset**
- **NMI With Bus-Grant Feature**

**325-PIN GF GRID ARRAY PACKAGE
(BOTTOM VIEW)‡**



‡ See Pin Assignments table and Pin Functions table for location and description of all pins.

- **Separate Internal Program, Data, and DMA Coprocessor Buses for Support of Massive Concurrent Input/Output (I/O) of Program and Data Throughput, Maximizing Sustained Central Processing Unit (CPU) Performance**
- **On-Chip Program Cache and Dual-Access/Single-Cycle RAM for Increased Memory-Access Performance**
 - 512-Byte Instruction Cache
 - 8K Bytes of Single-Cycle Dual-Access Program or Data RAM
 - ROM-Based Boot Loader Supports Program Bootup Using 8-, 16-, or 32-Bit Memories or One of the Communication Ports
- **IDLE2 Clock-Stop Power-Down Mode**
- **5-V Operation**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† IEEE Standard 1149.1–1990 Standard Test-Access Port and Boundary-Scan Architecture
EPIC and TI are trademarks of Texas Instruments Incorporated.

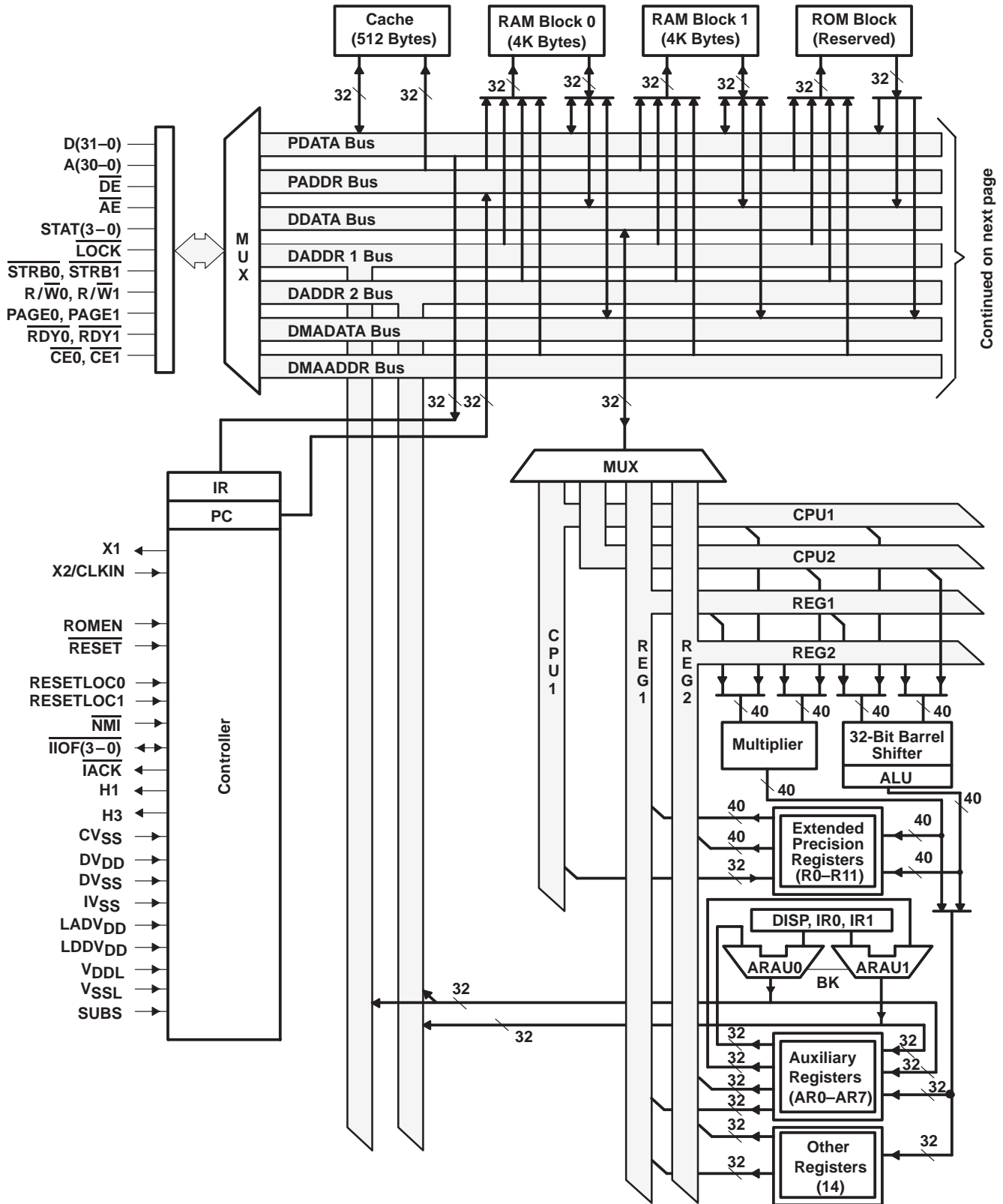
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



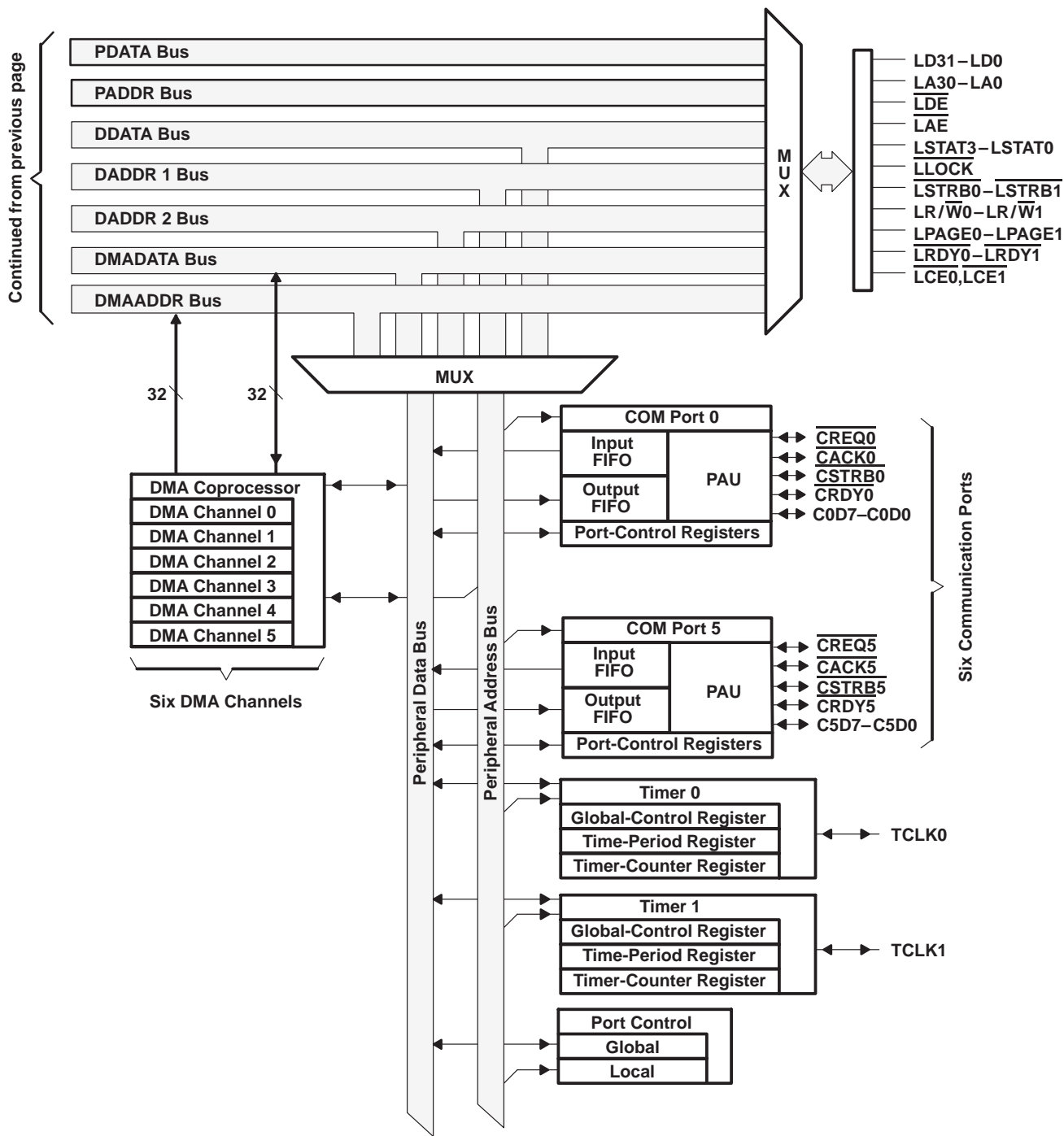
TMS320C40 DIGITAL SIGNAL PROCESSOR

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block diagram



block diagram (continued)



TMS320C40 DIGITAL SIGNAL PROCESSOR

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functions

This section lists signal descriptions for the '320C40 device. The '320C40 pin functions table lists each signal, number of pins, operating mode(s) (that is, input, output, or high-impedance state as indicated by I, O, or Z, respectively), and function. The signals are grouped according to function.

Pin Functions

| NAME | NO. OF PINS | TYPE† | DESCRIPTION |
|--|-------------|-------|--|
| GLOBAL-BUS EXTERNAL INTERFACE (80 PINS) | | | |
| D31–D0 | 32 | I/O/Z | 32-bit data port of the global-bus external interface |
| \overline{DE} | 1 | I | Data-bus-enable signal for the global-bus external interface |
| A30–A0 | 31 | O/Z | 31-bit address port of the global-bus external interface |
| \overline{AE} | 1 | I | Address-bus-enable signal for the global-bus external interface |
| STAT3–STAT0 | 4 | O | Status signals for the global-bus external interface |
| \overline{LOCK} | 1 | O | Lock signal for the global-bus external interface |
| $\overline{STRB0}‡$ | 1 | O/Z | Access strobe 0 for the global-bus external interface |
| R/ $\overline{W0}‡$ | 1 | O/Z | Read/write signal for $\overline{STRB0}$ accesses |
| PAGE0‡ | 1 | O/Z | Page signal for $\overline{STRB0}$ accesses |
| $\overline{RDY0}‡$ | 1 | I | Ready signal for $\overline{STRB0}$ accesses |
| $\overline{CE0}‡$ | 1 | I | Control enable for the $\overline{STRB0}$, PAGE0, and R/ $\overline{W0}$ signals |
| $\overline{STRB1}‡$ | 1 | O/Z | Access strobe 1 for the global-bus external interface |
| R/ $\overline{W1}‡$ | 1 | O/Z | Read/write signal for $\overline{STRB1}$ accesses |
| PAGE1‡ | 1 | O/Z | Page signal for $\overline{STRB1}$ accesses |
| $\overline{RDY1}‡$ | 1 | I | Ready signal for $\overline{STRB1}$ accesses |
| $\overline{CE1}‡$ | 1 | I | Control enable for the $\overline{STRB1}$, PAGE1, and R/ $\overline{W1}$ signals |
| LOCAL-BUS EXTERNAL INTERFACE (80 PINS) | | | |
| LD31–LD0 | 32 | I/O/Z | 32-bit data port of the local-bus external interface |
| \overline{LDE} | 1 | I | Data-bus-enable signal for the local-bus external interface |
| LA30–LA0 | 31 | O/Z | 31-bit address port of the local-bus external interface |
| \overline{LAE} | 1 | I | Address-bus-enable signal for the local-bus external interface |
| LSTAT3–LSTAT0 | 4 | O | Status signals for the local-bus external interface |
| \overline{LLOCK} | 1 | O | Lock signal for the local-bus external interface |
| $\overline{LSTRB0}‡$ | 1 | O/Z | Access strobe 0 for the local-bus external interface |
| LR/ $\overline{W0}$ | 1 | O/Z | Read/write signal for $\overline{LSTRB0}$ accesses |
| LPAGE0 | 1 | O/Z | Page signal for $\overline{LSTRB0}$ accesses |
| $\overline{LRDY0}$ | 1 | I | Ready signal for $\overline{LSTRB0}$ accesses |
| $\overline{LCE0}$ | 1 | I | Control enable for the $\overline{LSTRB0}$, LPAGE0, and LR/ $\overline{W0}$ signals |
| $\overline{LSTRB1}‡$ | 1 | O/Z | Access strobe 1 for the local-bus external interface |
| LR/ $\overline{W1}$ | 1 | O/Z | Read/write signal for $\overline{LSTRB1}$ accesses |
| LPAGE1 | 1 | O/Z | Page signal for $\overline{LSTRB1}$ accesses |
| $\overline{LRDY1}$ | 1 | I | Ready signal for $\overline{LSTRB1}$ accesses |
| $\overline{LCE1}$ | 1 | I | Control enable for the $\overline{LSTRB1}$, LPAGE1, and LR/ $\overline{W1}$ signals |

† I = input, O = output, Z = high impedance

‡ Signal's effective address range is defined by the local/global STRB ACTIVE bits.



Pin Functions (Continued)

| NAME | NO. OF PINS | TYPE† | DESCRIPTION |
|---|-------------|-------|---|
| COMMUNICATION PORT 0 INTERFACE (12 PINS) | | | |
| C0D7–C0D0 | 8 | I/O | Communication port 0 data bus |
| $\overline{\text{CREQ0}}$ | 1 | I/O | Communication port 0 token-request signal |
| $\overline{\text{CACK0}}$ | 1 | I/O | Communication port 0 token-request-acknowledge signal |
| $\overline{\text{CSTRB0}}$ | 1 | I/O | Communication port 0 data-strobe signal |
| $\overline{\text{CRDY0}}$ | 1 | I/O | Communication port 0 data-ready signal |
| COMMUNICATION PORT 1 INTERFACE (12 PINS) | | | |
| C1D7–C1D0 | 8 | I/O | Communication port 1 data bus |
| $\overline{\text{CREQ1}}$ | 1 | I/O | Communication port 1 token-request signal |
| $\overline{\text{CACK1}}$ | 1 | I/O | Communication port 1 token-request-acknowledge signal |
| $\overline{\text{CSTRB1}}$ | 1 | I/O | Communication port 1 data-strobe signal |
| $\overline{\text{CRDY1}}$ | 1 | I/O | Communication port 1 data-ready signal |
| COMMUNICATION PORT 2 INTERFACE (12 PINS) | | | |
| C2D7–C2D0 | 8 | I/O | Communication port 2 data bus |
| $\overline{\text{CREQ2}}$ | 1 | I/O | Communication port 2 token-request signal |
| $\overline{\text{CACK2}}$ | 1 | I/O | Communication port 2 token-request-acknowledge signal |
| $\overline{\text{CSTRB2}}$ | 1 | I/O | Communication port 2 data-strobe signal |
| $\overline{\text{CRDY2}}$ | 1 | I/O | Communication port 2 data-ready signal |
| COMMUNICATION PORT 3 INTERFACE (12 PINS) | | | |
| C3D7–C3D0 | 8 | I/O | Communication port 3 data bus |
| $\overline{\text{CREQ3}}$ | 1 | I/O | Communication port 3 token-request signal |
| $\overline{\text{CACK3}}$ | 1 | I/O | Communication port 3 token-request-acknowledge signal |
| $\overline{\text{CSTRB3}}$ | 1 | I/O | Communication port 3 data-strobe signal |
| $\overline{\text{CRDY3}}$ | 1 | I/O | Communication port 3 data-ready signal |
| COMMUNICATION PORT 4 INTERFACE (12 PINS) | | | |
| C4D7–C4D0 | 8 | I/O | Communication port 4 data bus |
| $\overline{\text{CREQ4}}$ | 1 | I/O | Communication port 4 token-request signal |
| $\overline{\text{CACK4}}$ | 1 | I/O | Communication port 4 token-request-acknowledge signal |
| $\overline{\text{CSTRB4}}$ | 1 | I/O | Communication port 4 data-strobe signal |
| $\overline{\text{CRDY4}}$ | 1 | I/O | Communication port 4 data-ready signal |
| COMMUNICATION PORT 5 INTERFACE (12 PINS) | | | |
| C5D7–C5D0 | 8 | I/O | Communication port 5 data bus |
| $\overline{\text{CREQ5}}$ | 1 | I/O | Communication port 5 token-request signal |
| $\overline{\text{CACK5}}$ | 1 | I/O | Communication port 5 token-request-acknowledge signal |
| $\overline{\text{CSTRB5}}$ | 1 | I/O | Communication port 5 data-strobe signal |
| $\overline{\text{CRDY5}}$ | 1 | I/O | Communication port 5 data-ready signal |

† I = input, O = output, Z = high impedance

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Pin Functions (Continued)

| NAME | NO. OF PINS | TYPE† | DESCRIPTION |
|---|-------------|-------|--|
| INTERRUPTS, I/O FLAGS, RESET, TIMER (12 PINS) | | | |
| $\overline{\text{IIOF3}}-\overline{\text{IIOF0}}$ | 4 | I/O | Interrupt and I/O flags |
| $\overline{\text{NMI}}$ | 1 | I | Nonmaskable interrupt. $\overline{\text{NMI}}$ is sensitive to a low-going edge. |
| $\overline{\text{IACK}}$ | 1 | O | Interrupt acknowledge |
| $\overline{\text{RESET}}$ | 1 | I | Reset signal |
| $\overline{\text{RESETLOC1}}-\overline{\text{RESETLOC0}}$ | 2 | I | Reset-vector location pins |
| ROMEN | 1 | I | On-chip ROM enable (0 = disable, 1 = enable) |
| TCLK0 | 1 | I/O | Timer 0 pin |
| TCLK1 | 1 | I/O | Timer 1 pin |
| CLOCK (4 PINS) | | | |
| X1 | 1 | O | Crystal pin |
| X2/CLKIN | 1 | I | Crystal/oscillator pin |
| H1 | 1 | O | H1 clock |
| H3 | 1 | O | H3 clock |
| POWER (70 PINS) | | | |
| CVSS | 15 | I | Ground pins |
| DVSS | 15 | I | Ground pins |
| IVSS | 6 | I | Ground pins |
| DVDD | 13 | I | 5- V_{DC} supply pins |
| GADVDD | 3 | I | 5- V_{DC} supply pins |
| GDDVDD | 3 | I | 5- V_{DC} supply pins |
| LADVDD | 3 | I | 5- V_{DC} supply pins |
| LDDVDD | 3 | I | 5- V_{DC} supply pins |
| SUBS | 1 | I | Substrate pin (tie to ground) |
| VDDL | 4 | I | 5- V_{DC} supply pins |
| VSSL | 4 | I | Ground pins |
| EMULATION (7 PINS) | | | |
| TCK | 1 | I | IEEE 1149.1 test port clock |
| TDO | 1 | O/Z | IEEE 1149.1 test port data out |
| TDI | 1 | I | IEEE 1149.1 test port data in |
| TMS | 1 | I | IEEE 1149.1 test port mode select |
| $\overline{\text{TRST}}$ | 1 | I | IEEE 1149.1 test port reset |
| EMU0 | 1 | I/O | Emulation pin 0 |
| EMU1 | 1 | I/O | Emulation pin 1 |

† I = input, O = output, Z = high impedance



GF Package Pin Assignments — Alphabetical Listing

| PIN | | PIN | | PIN | | PIN | | PIN | |
|-----------------|------|------|------|---------------------|------|------|------|-----------------|------|
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| A0 | D32 | C0D6 | AN7 | C5D4 | AM30 | CVSS | E35 | D31 | F32 |
| A1 | B32 | C0D7 | AK8 | C5D5 | AP32 | CVSS | AR25 | \overline{DE} | AA31 |
| A2 | D30 | C1D0 | AL7 | C5D6 | AM32 | CVSS | AE1 | DVDD | AR11 |
| A3 | C29 | C1D1 | AP8 | C5D7 | AL31 | CVSS | AR13 | DVDD | AR29 |
| A4 | B30 | C1D2 | AM8 | $\overline{CACK0}$ | AN11 | CVSS | A19 | DVDD | A13 |
| A5 | F28 | C1D3 | AK12 | $\overline{CACK1}$ | AN13 | CVSS | R35 | DVDD | A7 |
| A6 | F24 | C1D4 | AK10 | $\overline{CACK2}$ | AM14 | CVSS | AL1 | DVDD | A17 |
| A7 | E29 | C1D5 | AN9 | $\overline{CACK3}$ | AM16 | D0 | U33 | DVDD | L35 |
| A8 | C27 | C1D6 | AL9 | $\overline{CACK4}$ | AK32 | D1 | V32 | DVDD | AR23 |
| A9 | D28 | C1D7 | AP10 | $\overline{CACK5}$ | AJ31 | D2 | T34 | DVDD | A29 |
| A10 | B28 | C2D0 | AM18 | $\overline{CE0}$ | AA33 | D3 | U31 | DVDD | L1 |
| A11 | F26 | C2D1 | AN19 | $\overline{CE1}$ | V34 | D4 | R33 | DVDD | AC1 |
| A12 | C25 | C2D2 | AL19 | $\overline{CRDY0}$ | AP12 | D5 | P34 | DVDD | AR17 |
| A13 | E27 | C2D3 | AP20 | $\overline{CRDY1}$ | AP14 | D6 | T32 | DVDD | A23 |
| A14 | B26 | C2D4 | AM20 | $\overline{CRDY2}$ | AL15 | D7 | N33 | DVDD | AJ1 |
| A15 | D26 | C2D5 | AN21 | $\overline{CRDY3}$ | AL17 | D8 | R31 | DVSS | AJ35 |
| A16 | C23 | C2D6 | AL21 | $\overline{CRDY4}$ | AH30 | D9 | M34 | DVSS | A21 |
| A17 | B24 | C2D7 | AP22 | $\overline{CRDY5}$ | AH32 | D10 | P32 | DVSS | A25 |
| A18 | E25 | C3D0 | AM22 | $\overline{CREQ0}$ | AM10 | D11 | L33 | DVSS | G35 |
| A19 | C21 | C3D1 | AN23 | $\overline{CREQ1}$ | AM12 | D12 | N31 | DVSS | A11 |
| A20 | D24 | C3D2 | AL23 | $\overline{CREQ2}$ | AN15 | D13 | K34 | DVSS | AG1 |
| A21 | B22 | C3D3 | AP24 | $\overline{CREQ3}$ | AN17 | D14 | M32 | DVSS | AM2 |
| A22 | E23 | C3D4 | AM24 | $\overline{CREQ4}$ | AN33 | D15 | J33 | DVSS | R1 |
| A23 | C19 | C3D5 | AN25 | $\overline{CREQ5}$ | AL33 | D16 | L31 | DVSS | AR21 |
| A24 | D22 | C3D6 | AL25 | $\overline{CSTRB0}$ | AL11 | D17 | M30 | DVSS | AR15 |
| A25 | B20 | C3D7 | AP26 | $\overline{CSTRB1}$ | AL13 | D18 | K32 | DVSS | A15 |
| A26 | E21 | C4D0 | AN27 | $\overline{CSTRB2}$ | AP16 | D19 | H34 | DVSS | AR27 |
| A27 | B18 | C4D1 | AM26 | $\overline{CSTRB3}$ | AP18 | D20 | J31 | DVSS | G1 |
| A28 | C17 | C4D2 | AK24 | $\overline{CSTRB4}$ | AM34 | D21 | G33 | DVSS | N35 |
| A29 | D20 | C4D3 | AL27 | $\overline{CSTRB5}$ | AK34 | D22 | K30 | DVSS | AR9 |
| A30 | B16 | C4D4 | AP28 | CVSS | AR19 | D23 | F34 | EMU0 | AA35 |
| \overline{AE} | AG31 | C4D5 | AK26 | CVSS | AR7 | D24 | H32 | EMU1 | AD34 |
| C0D0 | AP4 | C4D6 | AN29 | CVSS | N1 | D25 | E33 | GADVDD | B2 |
| C0D1 | AL5 | C4D7 | AM28 | CVSS | AL35 | D26 | D34 | GADVDD | AR1 |
| C0D2 | AN5 | C5D0 | AL29 | CVSS | A27 | D27 | G31 | GADVDD | U35 |
| C0D3 | AM4 | C5D1 | AP30 | CVSS | A9 | D28 | C33 | GDDVDD | V2 |
| C0D4 | AP6 | C5D2 | AK28 | CVSS | E1 | D29 | H30 | GDDVDD | A35 |
| C0D5 | AM6 | C5D3 | AN31 | CVSS | J35 | D30 | E31 | GDDVDD | A1 |

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GF Package Pin Assignments — Alphabetical Listing (Continued)

| PIN | | PIN | | PIN | | PIN | |
|---------------------------|------|--------------------------|------|----------------------------|------|---------------------------|------|
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| H1 | AC3 | LA25 | R5 | LD26 | B4 | STAT0 | AD32 |
| H3 | AC5 | LA26 | T2 | LD27 | F8 | STAT1 | AE33 |
| $\overline{\text{IACK}}$ | W3 | LA27 | U3 | LD28 | D6 | STAT2 | AF34 |
| $\overline{\text{IIOF0}}$ | AN3 | LA28 | T4 | LD29 | C3 | STAT3 | AE31 |
| $\overline{\text{IIOF1}}$ | AL3 | LA29 | V4 | LD30 | E5 | $\overline{\text{STRB0}}$ | AD30 |
| $\overline{\text{IIOF2}}$ | AH6 | LA30 | U5 | LD31 | F6 | $\overline{\text{STRB1}}$ | AC33 |
| $\overline{\text{IIOF3}}$ | AK2 | LADV _{DD} | B34 | LDDV _{DD} | AR35 | SUBS | C31 |
| IV _{SS} | AR5 | LADV _{DD} | AB2 | LDDV _{DD} | AP2 | TCK | Y34 |
| IV _{SS} | AR31 | LADV _{DD} | AP34 | LDDV _{DD} | U1 | TCLK0 | AE3 |
| IV _{SS} | AG35 | $\overline{\text{LAE}}$ | AB4 | $\overline{\text{LDE}}$ | AD4 | TCLK1 | AD2 |
| IV _{SS} | A31 | $\overline{\text{LCE0}}$ | AG5 | $\overline{\text{LLOCK}}$ | AA5 | TDO | AB34 |
| IV _{SS} | J1 | $\overline{\text{LCE1}}$ | AF2 | $\overline{\text{LOCK}}$ | W33 | TDI | AC35 |
| IV _{SS} | A5 | LD0 | E19 | LPAGE0 | AH2 | TMS | W35 |
| LA0 | D2 | LD1 | C15 | LPAGE1 | AG3 | $\overline{\text{TRST}}$ | AE35 |
| LA1 | D4 | LD2 | D18 | $\overline{\text{LRDY0}}$ | AF6 | VDDL | AN1 |
| LA2 | E3 | LD3 | B14 | $\overline{\text{LRDY1}}$ | AE5 | VDDL | AN35 |
| LA3 | F4 | LD4 | E17 | LR/ $\overline{\text{W0}}$ | AH4 | VDDL | C35 |
| LA4 | H6 | LD5 | D16 | LR/ $\overline{\text{W1}}$ | AF4 | VDDL | C1 |
| LA5 | F2 | LD6 | C13 | LSTAT0 | AA3 | VSSL | A3 |
| LA6 | G5 | LD7 | E15 | LSTAT1 | Y4 | VSSL | AR3 |
| LA7 | G3 | LD8 | B12 | LSTAT2 | Y2 | VSSL | AR33 |
| LA8 | H4 | LD9 | D14 | LSTAT3 | W5 | VSSL | A33 |
| LA9 | H2 | LD10 | C11 | $\overline{\text{LSTRB0}}$ | AJ3 | X1 | W1 |
| LA10 | K6 | LD11 | E13 | $\overline{\text{LSTRB1}}$ | AD6 | X2/CLKIN | AA1 |
| LA11 | M6 | LD12 | B10 | $\overline{\text{NMI}}$ | AJ5 | | |
| LA12 | J5 | LD13 | D12 | PAGE0 | AG33 | | |
| LA13 | J3 | LD14 | C9 | PAGE1 | AB32 | | |
| LA14 | K4 | LD15 | E11 | $\overline{\text{RDY0}}$ | Y32 | | |
| LA15 | K2 | LD16 | F12 | $\overline{\text{RDY1}}$ | W31 | | |
| LA16 | L3 | LD17 | D10 | RESETLOC0 | AF30 | | |
| LA17 | L5 | LD18 | B8 | RESETLOC1 | AH34 | | |
| LA18 | M2 | LD19 | E9 | $\overline{\text{RESET}}$ | AJ33 | | |
| LA19 | M4 | LD20 | C7 | ROMEN | AK4 | | |
| LA20 | N3 | LD21 | F10 | R/ $\overline{\text{W0}}$ | AF32 | | |
| LA21 | N5 | LD22 | B6 | R/ $\overline{\text{W1}}$ | AC31 | | |
| LA22 | P2 | LD23 | D8 | | | | |
| LA23 | P4 | LD24 | C5 | | | | |
| LA24 | R3 | LD25 | E7 | | | | |



GF Package Pin Assignments — Numerical Listing

| PIN | | PIN | | PIN | | PIN | |
|------|--------------------|------|--------------------|------|--------------------|------|--------------------|
| NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME |
| A1 | GDDV _{DD} | AD30 | STRB ₀ | AK24 | C4D2 | AM30 | C5D4 |
| A3 | V _{SSL} | AD32 | STAT0 | AK26 | C4D5 | AM32 | C5D6 |
| A5 | I _{VSS} | AD34 | EMU1 | AK28 | C5D2 | AM34 | CSTRB ₄ |
| A7 | DV _{DD} | AE1 | CV _{SS} | AK32 | CACK ₄ | AN1 | V _{DDL} |
| A9 | CV _{SS} | AE3 | TCLK0 | AK34 | CSTRB ₅ | AN3 | IIOF ₀ |
| A11 | DV _{SS} | AE5 | LRDY ₁ | AL1 | CV _{SS} | AN5 | C0D2 |
| A13 | DV _{DD} | AE31 | STAT3 | AL3 | IIOF ₁ | AN7 | C0D6 |
| A15 | DV _{SS} | AE33 | STAT1 | AL5 | C0D1 | AN9 | C1D5 |
| A17 | DV _{DD} | AE35 | TRST | AL7 | C1D0 | AN11 | CACK ₀ |
| A19 | CV _{SS} | AF2 | LCE ₁ | AL9 | C1D6 | AN13 | CACK ₁ |
| A21 | DV _{SS} | AF4 | LR/W ₁ | AL11 | CSTRB ₀ | AN15 | CREQ ₂ |
| A23 | DV _{DD} | AF6 | LRDY ₀ | AL13 | CSTRB ₁ | AN17 | CREQ ₃ |
| A25 | DV _{SS} | AF30 | RESETLOC0 | AL15 | CRDY ₂ | AN19 | C2D1 |
| A27 | CV _{SS} | AF32 | R/W ₀ | AL17 | CRDY ₃ | AN21 | C2D5 |
| A29 | DV _{DD} | AF34 | STAT2 | AL19 | C2D2 | AN23 | C3D1 |
| A31 | I _{VSS} | AG1 | DV _{SS} | AL21 | C2D6 | AN25 | C3D5 |
| A33 | V _{SSL} | AG3 | LPAGE1 | AL23 | C3D2 | AN27 | C4D0 |
| A35 | GDDV _{DD} | AG5 | LCE ₀ | AL25 | C3D6 | AN29 | C4D6 |
| AA1 | X2/CLKIN | AG31 | AE | AL27 | C4D3 | AN31 | C5D3 |
| AA3 | LSTAT0 | AG33 | PAGE0 | AL29 | C5D0 | AN33 | CREQ ₄ |
| AA5 | LLOCK | AG35 | I _{VSS} | AL31 | C5D7 | AN35 | V _{DDL} |
| AA31 | DE | AH2 | LPAGE0 | AL33 | CREQ ₅ | AP2 | LDDV _{DD} |
| AA33 | CE ₀ | AH4 | LR/W ₀ | AL35 | CV _{SS} | AP4 | C0D0 |
| AA35 | EMU0 | AH6 | IIOF ₂ | AM2 | DV _{SS} | AP6 | C0D4 |
| AB2 | LADV _{DD} | AH30 | CRDY ₄ | AM4 | C0D3 | AP8 | C1D1 |
| AB4 | LAE | AH32 | CRDY ₅ | AM6 | C0D5 | AP10 | C1D7 |
| AB32 | PAGE1 | AH34 | RESETLOC1 | AM8 | C1D2 | AP12 | CRDY ₀ |
| AB34 | TDO | AJ1 | DV _{DD} | AM10 | CREQ ₀ | AP14 | CRDY ₁ |
| AC1 | DV _{DD} | AJ3 | LSTRB ₀ | AM12 | CREQ ₁ | AP16 | CSTRB ₂ |
| AC3 | H1 | AJ5 | NMI | AM14 | CACK ₂ | AP18 | CSTRB ₃ |
| AC5 | H3 | AJ31 | CACK ₅ | AM16 | CACK ₃ | AP20 | C2D3 |
| AC31 | R/W ₁ | AJ33 | RESET | AM18 | C2D0 | AP22 | C2D7 |
| AC33 | STRB ₁ | AJ35 | DV _{SS} | AM20 | C2D4 | AP24 | C3D3 |
| AC35 | TDI | AK2 | IIOF ₃ | AM22 | C3D0 | AP26 | C3D7 |
| AD2 | TCLK1 | AK4 | ROMEN | AM24 | C3D4 | AP28 | C4D4 |
| AD4 | LDE | AK8 | C0D7 | AM26 | C4D1 | AP30 | C5D1 |
| AD6 | LSTRB ₁ | AK10 | C1D4 | AM28 | C4D7 | AP32 | C5D5 |
| | | AK12 | C1D3 | | | AP34 | LADV _{DD} |

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GF Package Pin Assignments — Numerical Listing (Continued)

| PIN | | PIN | | PIN | | PIN | | PIN | |
|------|--------------------|-----|------------------|-----|------------------|-----|------------------|-----|--------------------|
| NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME |
| AR1 | GADV _{DD} | C1 | V _{DDL} | E1 | CV _{SS} | H2 | LA9 | P2 | LA22 |
| AR3 | V _{SSL} | C3 | LD29 | E3 | LA2 | H4 | LA8 | P4 | LA23 |
| AR5 | IV _{SS} | C5 | LD24 | E5 | LD30 | H6 | LA4 | P32 | D10 |
| AR7 | CV _{SS} | C7 | LD20 | E7 | LD25 | H30 | D29 | P34 | D5 |
| AR9 | DV _{SS} | C9 | LD14 | E9 | LD19 | H32 | D24 | R1 | DV _{SS} |
| AR11 | DV _{DD} | C11 | LD10 | E11 | LD15 | H34 | D19 | R3 | LA24 |
| AR13 | CV _{SS} | C13 | LD6 | E13 | LD11 | J1 | IV _{SS} | R5 | LA25 |
| AR15 | DV _{SS} | C15 | LD1 | E15 | LD7 | J3 | LA13 | R31 | D8 |
| AR17 | DV _{DD} | C17 | A28 | E17 | LD4 | J5 | LA12 | R33 | D4 |
| AR19 | CV _{SS} | C19 | A23 | E19 | LD0 | J31 | D20 | R35 | CV _{SS} |
| AR21 | DV _{SS} | C21 | A19 | E21 | A26 | J33 | D15 | T2 | LA26 |
| AR23 | DV _{DD} | C23 | A16 | E23 | A22 | J35 | CV _{SS} | T4 | LA28 |
| AR25 | CV _{SS} | C25 | A12 | E25 | A18 | K2 | LA15 | T32 | D6 |
| AR27 | DV _{SS} | C27 | A8 | E27 | A13 | K4 | LA14 | T34 | D2 |
| AR29 | DV _{DD} | C29 | A3 | E29 | A7 | K6 | LA10 | U1 | LDDV _{DD} |
| AR31 | IV _{SS} | C31 | SUBS | E31 | D30 | K30 | D22 | U3 | LA27 |
| AR33 | V _{SSL} | C33 | D28 | E33 | D25 | K32 | D18 | U5 | LA30 |
| AR35 | LDDV _{DD} | C35 | V _{DDL} | E35 | CV _{SS} | K34 | D13 | U31 | D3 |
| B2 | GADV _{DD} | D2 | LA0 | F2 | LA5 | L1 | DV _{DD} | U33 | D0 |
| B4 | LD26 | D4 | LA1 | F4 | LA3 | L3 | LA16 | U35 | GADV _{DD} |
| B6 | LD22 | D6 | LD28 | F6 | LD31 | L5 | LA17 | V2 | GDDV _{DD} |
| B8 | LD18 | D8 | LD23 | F8 | LD27 | L31 | D16 | V4 | LA29 |
| B10 | LD12 | D10 | LD17 | F10 | LD21 | L33 | D11 | V32 | D1 |
| B12 | LD8 | D12 | LD13 | F12 | LD16 | L35 | DV _{DD} | V34 | $\overline{CE1}$ |
| B14 | LD3 | D14 | LD9 | F24 | A6 | M2 | LA18 | W1 | X1 |
| B16 | A30 | D16 | LD5 | F26 | A11 | M4 | LA19 | W3 | \overline{IACK} |
| B18 | A27 | D18 | LD2 | F28 | A5 | M6 | LA11 | W5 | LSTAT3 |
| B20 | A25 | D20 | A29 | F32 | D31 | M30 | D17 | W31 | $\overline{RDY1}$ |
| B22 | A21 | D22 | A24 | F34 | D23 | M32 | D14 | W33 | \overline{LOCK} |
| B24 | A17 | D24 | A20 | G1 | DV _{SS} | M34 | D9 | W35 | TMS |
| B26 | A14 | D26 | A15 | G3 | LA7 | N1 | CV _{SS} | Y2 | LSTAT2 |
| B28 | A10 | D28 | A9 | G5 | LA6 | N3 | LA20 | Y4 | LSTAT1 |
| B30 | A4 | D30 | A2 | G31 | D27 | N5 | LA21 | Y32 | $\overline{RDY0}$ |
| B32 | A1 | D32 | A0 | G33 | D21 | N31 | D12 | Y34 | TCK |
| B34 | LADV _{DD} | D34 | D26 | G35 | DV _{SS} | N33 | D7 | | |
| | | | | | | N35 | DV _{SS} | | |



memory map

Figure 1 shows the memory map for the '320C40. Refer to the *TMS320C4x User's Guide* (literature number SPRU063B) for a detailed description of this memory mapping.

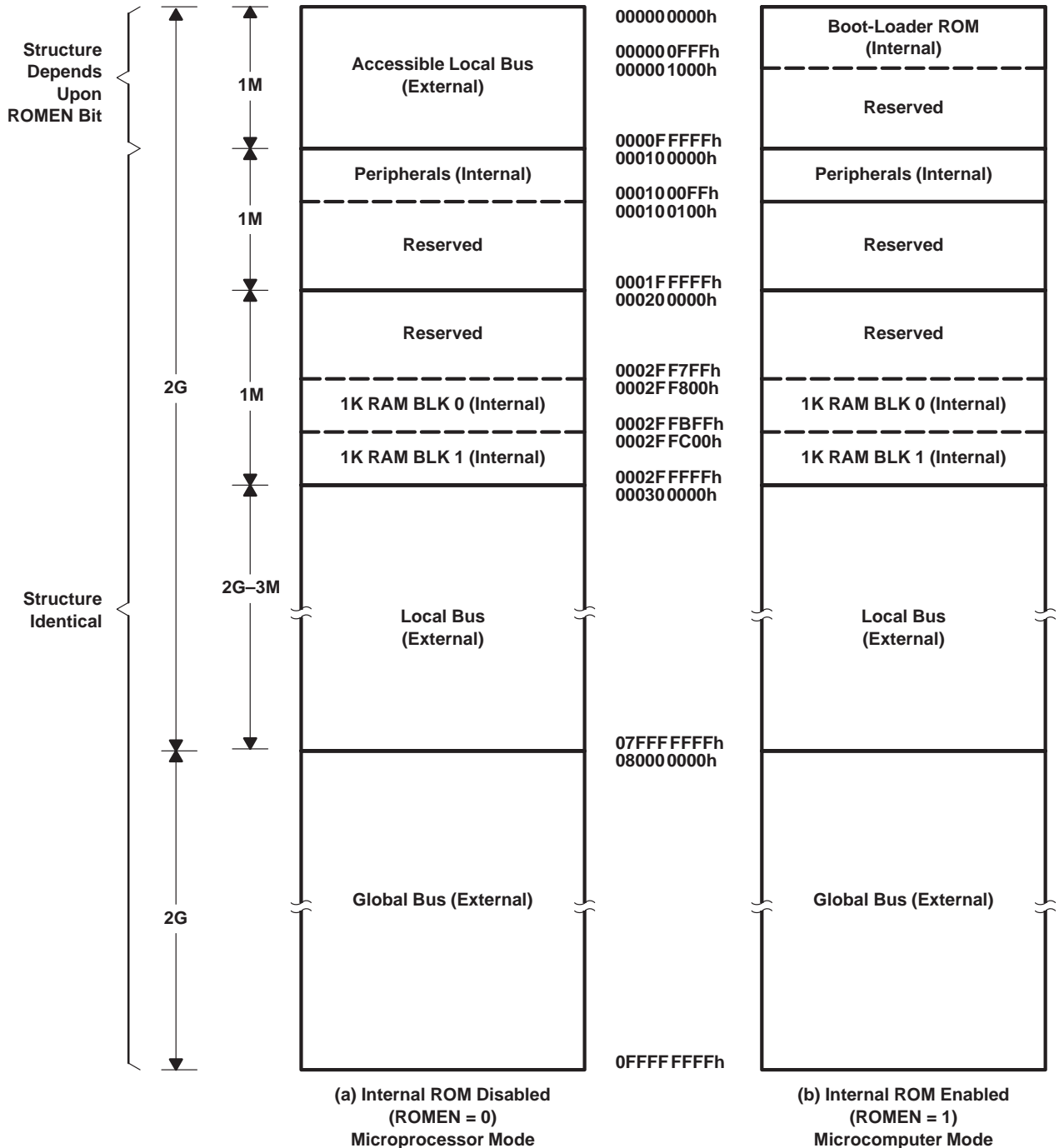


Figure 1. Memory Map for '320C40

TMS320C40

DIGITAL SIGNAL PROCESSOR

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description

The '320C40 digital signal processors (DSPs) are 32-bit, floating-point processors manufactured in 0.72- μ m, double-level metal CMOS technology. The '320C40 is a part of the fourth generation of DSPs from Texas Instruments and is designed primarily for parallel processing.

operation

The '320C40 has six on-chip communication ports for processor-to-processor communication with no external hardware and simple communication software. This allows connectivity to other 'C4x processors with no external-glue logic. The communication ports remove input/output bottlenecks, and the independent smart DMA coprocessor is able to handle the CPU input/output burden.

central processing unit

The '320C40 CPU is configured for high-speed internal parallelism for the highest sustained performance. The key features of the CPU are:

- Eight operations/cycle:
 - 40/32-bit floating-point/integer multiply
 - 40/32-bit floating-point/integer ALU operation
 - Two data accesses
 - Two address register updates
- IEEE floating-point conversion
- Divide and square-root support
- 'C3x assembly language compatibility
- Byte and halfword accessibility

DMA coprocessor

The DMA coprocessor allows concurrent I/O and CPU processing for the highest sustained CPU performance. The key features of the DMA processor are:

- Link pointers allow DMA channels to auto-initialize without CPU intervention.
- Parallel CPU operation and DMA transfers
- Six DMA channels support memory-to-memory data transfers.
- Split-mode operation doubles the available DMA channel to 12 when data transfers to and from a communication port are required.

communication ports

The '320C40 is the first DSP with on-chip communication ports for processor-to-processor communication with no external hardware and simple communication software. The features of the communication ports are:

- Direct interprocessor communication and processor I/O
- Six communication ports for direct interprocessor communication and processor I/O
- 20M-bytes/s bidirectional interface on each communication port for high-speed multiprocessor interface
- Separate input and output 8-word-deep FIFO buffers for processor-to-processor communication and I/O
- Automatic arbitration and handshaking for direct processor-to-processor connection



communication-port software reset ('C40 silicon revision \geq 5.0)

The input and output FIFO levels for a communication port can be flushed by writing at least two back-to-back values to its communication-port-software reset address as specified in Table 1. This feature is not present in 'C40 silicon revision $<$ 5.0. This software reset flushes any word or byte already present in the FIFOs but it does not affect the status of the communication-port pins. Figure 2 shows an example of communication-port-software reset.

Table 1. Communication-Port Software-Reset Address

| COMMUNICATION PORT | SOFTWARE RESET ADDRESS |
|--------------------|------------------------|
| 0 | 0x0100043 |
| 1 | 0x0100053 |
| 2 | 0x0100063 |
| 3 | 0x0100073 |
| 4 | 0x0100083 |
| 5 | 0x0100093 |

```

; -----;
; RESET1:Flush's FIFO data for communication port 1;
; -----;
RESET1 push  AR0          ; Save registers
      push  R0           ;
      push  RC           ;
      ldhi  010h,AR0     ; Set AR0 to base address of COM 1
      or   050h,AR0     ;
flush: rpts  1           ; Flush FIFO data with back-to-back write
      sti  R0,*+AR0(3)  ;
      rpts  10          ; Wait
      nop                ;
      ldi  *+AR0(0),R0  ; Check for new data from other port
      and  01FE0h,R0    ;
      bnz  flush        ;
      pop  RC           ; Restore registers
      pop  R0           ;
      pop  AR0          ;
      rets              ; Return

```

Figure 2. Example of Communication-Port-Software Reset

$\overline{\text{NMI}}$ with bus-grant feature ('C40 silicon revision \geq 5.0)

The '320C40 devices have a software-configurable feature which allows forcing the internal-peripheral bus to ready when the $\overline{\text{NMI}}$ signal is asserted. This feature is not present in 'C40 silicon revision $<$ 5.0. The $\overline{\text{NMI}}$ bus-grant feature is enabled when bits 19–18 of the status register (ST) are set to 10b. When enabled, a peripheral bus-grant signal is generated on the falling edge of $\overline{\text{NMI}}$. When $\overline{\text{NMI}}$ is asserted and this feature is not enabled, the CPU stalls on access to the peripheral bus if it is not ready. A stall condition occurs when writing to a full FIFO or reading an empty FIFO. This feature is useful in correcting communication-port errors when used in conjunction with the communication-port software-reset feature.

IDLE2 clock-stop power-down mode ('C40 silicon revision \geq 5.0)

The '320C40 has a clock-stop mode or power-down mode (IDLE2) to achieve extremely low-power consumption. When an IDLE2 instruction is executed, the clocks are halted with H1 being held high. To exit IDLE2, assert one of the $\overline{\text{IIOF3}}$ – $\overline{\text{IIOF0}}$ pins configured as an external interrupt instead of a general-purpose I/O. A macro showing how to generate the IDLE2 opcode is given in Figure 3. During this power-down mode:

- No instructions are executed.
- The CPU, peripherals, and internal memory retain their previous state.
- The external-bus outputs are idle. The address lines remain in their previous state, the data lines are in the high-impedance state, and the output-control signals are inactive.

```
; -----;
; IDLE2: Macro to generate idle2 opcode      ;
; -----;
IDLE2      .macro
           .word      06000001h
           .endm
```

Figure 3. Example of Software Subroutine Using IDLE2

IDLE2 is exited when one of the five external interrupts ($\overline{\text{NMI}}$ and $\overline{\text{IIOF3}}$ – $\overline{\text{IIOF0}}$) is asserted low for at least four input clocks (two H1 cycles). The clocks then start after a delay of two input clocks (one H1 cycle). The clocks can start in the opposite phase; that is, H1 can be high when H3 was high before the clocks were stopped. However, the H1 and H3 clocks remain 180° out of phase with each other.

During IDLE2 operation, an external interrupt can be recognized and serviced by the CPU if it is enabled before entering IDLE2 and asserted for at least two H1 cycles. For the processor to recognize only one interrupt, the interrupt pin must be configured for edge-trigger mode or asserted less than three cycles in level-trigger mode. Any external interrupt pin can wake up the device from IDLE2, but for the CPU to recognize that interrupt, it must also be enabled. If an interrupt is recognized and executed by the CPU, the instruction following the IDLE2 instruction is not executed until after execution of a return opcode.

When the device is in emulation mode, the CPU executes an IDLE2 instruction as if it were an IDLE instruction. The clocks continue to run for correct operation of the emulator.

development tools

The 'C40 is supported by a host of parallel-processing development tools for developing and simulating code easily and for debugging parallel-processing systems. The code generation tools include:

- An ANSI C compiler optimized with a runtime support library that supports use of communication ports and DMA.
- Third party support for C, C++ and Ada compilers
- Several operating systems available for parallel-processing support, as well as DMA and communication port drivers
- An assembler and linker with support for mapping program and data to parallel processors

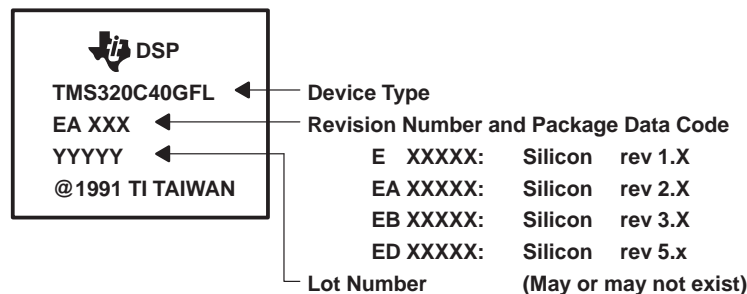
The simulation tools include:

- Parallel DSP system-level simulation with LAI hardware verification (HV) model and full function (FF) model.
- TI software simulator with high-level language debugger interface for simulating a single processor.

The hardware development and verification tools include:

- Parallel processor in-circuit emulator and high-level language debugger: XDS510.
- Parallel processor development system (PPDS) with four '320C40s, local and global memory, and communication port connections.

silicon revision identification



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absolute maximum ratings over specified temperature range (unless otherwise noted)[†]

| | |
|---|-----------------|
| Supply voltage range, V_{DD} (see Note 1) | – 0.3 V to 7 V |
| Voltage range on any pin | – 0.3 V to 7 V |
| Output voltage range | – 0.3 V to 7 V |
| Operating case temperature range, T_C | 0°C to 85°C |
| Storage temperature range, T_{stg} | – 55°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions (see Note 2)

| | | MIN | TYP [‡] | MAX | UNIT |
|----------|--------------------------------------|--------------------|------------------|-----------------------------|---------|
| V_{DD} | Supply voltages (DD V_{DD} , etc.) | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | X2/CLKIN | 2.6 | $V_{DD} + 0.3$ [§] | V |
| | | All other pins | 2 | $V_{DD} + 0.3$ [§] | |
| V_{IL} | Low-level input voltage | – 0.3 [§] | | 0.8 | V |
| I_{OH} | High-level output current | | | – 300 | μ A |
| I_{OL} | Low-level output current | | | 2 | mA |
| T_C | Operating case temperature | | | 85 | °C |

[‡] All typical values are at $V_{DD} = 5$ V, T_A (ambient air temperature) = 25°C.

[§] This parameter is characterized but not tested.

NOTE 2: All input and output voltage levels are TTL compatible, except for CLKIN. CLKIN can be driven by CMOS clock.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP ^{††} | MAX | UNIT |
|-----------|---|-------|-------------------|-----------------|---------|
| V_{OH} | High-level output voltage $V_{DD} = \text{MIN}, I_{OH} = \text{MAX}$ | 2.4 | 3 | | V |
| V_{OL} | Low-level output voltage $V_{DD} = \text{MIN}, I_{OL} = \text{MAX}$ | | 0.3 | 0.6 | V |
| I_Z | Three-state current $V_{DD} = \text{MAX}$ | – 20 | | 20 | μ A |
| I_{IC} | Input current, X2/CLKIN only $V_I = V_{SS}$ to V_{DD} | – 30 | | 30 | μ A |
| I_{IP} | Input current Inputs with internal pullups (See Note 3) | – 400 | | 20 | μ A |
| I_I | Input current $V_I = V_{SS}$ to V_{DD} | – 10 | | 10 | μ A |
| I_{CC} | Supply current $T_A = 25^\circ\text{C}, V_{DD} = \text{MAX}, f_X = \text{MAX}$ (See Note 4) | | 350 | 850 | mA |
| | | | | '320C40-40 | |
| | | | | '320C40-60 | |
| C_I | Input capacitance | | | 15 [#] | pF |
| C_O | Output capacitance | | | 15 [#] | pF |

^{††} All typical values are at $V_{DD} = 5$ V, T_A (ambient air temperature) = 25°C.

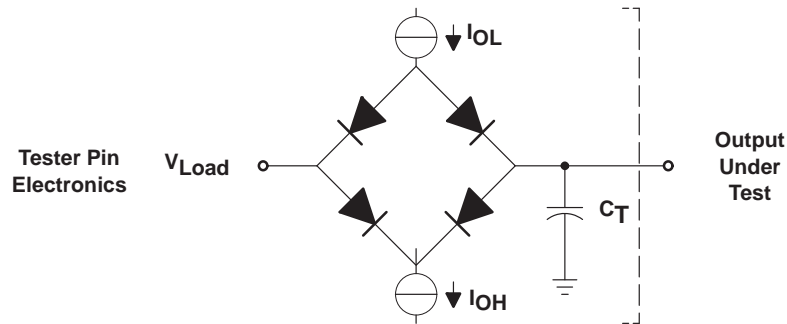
[#] This parameter is specified by design but not tested.

NOTES: 3. Pins with internal pullup devices: TDI, TCK, TMS. Pin with internal pulldown device: $\overline{\text{TRST}}$.

4. f_X is the input clock frequency. The maximum value (max) for the '320C40-40, '320C40-50, and '320C40-60 is 40, 50 and 60 MHz, respectively.



PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
 I_{OH} = 300 μ A (all outputs)
 V_{Load} = 2.15 V
 C_T = 80 pF typical load circuit capacitance.

Figure 4. Test Load Circuit

signal transition levels

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows.

For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V. For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V. See Figure 5.

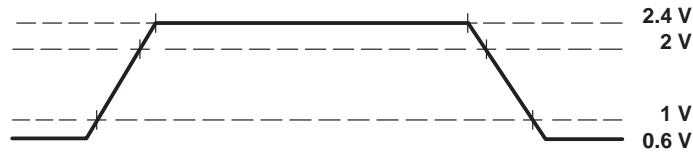


Figure 5. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows. For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2 V and the level at which the input is said to be low is 0.8 V. For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V and the level at which the input is said to be high is 2 V. See Figure 6.



Figure 6. TTL-Level Inputs

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, pin names that have both global and local applications are generally represented with (L) immediately preceding the basic signal name (for example, (L)RDYx represents both the global term RDYx and local term LRDYx). Other pin names and related terminology have been abbreviated as follows, unless otherwise noted:

| | | | |
|---------|---|-------|---|
| A | (L)A30–(L)A0 or (L)Ax | IACK | $\overline{\text{IACK}}$ |
| AE | $\overline{\text{(L)AE}}$ | IF | $\overline{\text{IIOF(3–0)}}$ or $\overline{\text{IIOF}x}$ |
| ASYNCH | Asynchronous reset signals in the high-impedance state | IIOF | $\overline{\text{IIOF(3–0)}}$ or $\overline{\text{IIOF}x}$ |
| BYTE | Byte transfer | LOCK | $\overline{\text{(L)LOCK}}$ |
| CA | $\overline{\text{CACK(0–5)}}$ or $\overline{\text{CACK}x}$ | P | $t_{c(H)}$ |
| CD | C(0–5)D7–C(0–5)D0 or CxDx | PAGE | (L)PAGE0 and (L)PAGE1 or (L)PAGEx |
| CE | $\overline{\text{(L)CE0}}$, $\overline{\text{(L)CE1}}$, or $\overline{\text{(L)CE}x}$ | RDY | $\overline{\text{(L)RDY0}}$, $\overline{\text{(L)RDY1}}$, or $\overline{\text{(L)RDY}x}$ |
| CI | CLKIN | RESET | $\overline{\text{RESET}}$ |
| COMM | Asynchronous reset signals | RW | (L)R/ $\overline{\text{W0}}$, (L)R/ $\overline{\text{W1}}$, or (L)R/ $\overline{\text{W}x}$ |
| CONTROL | Control signals | S | $\overline{\text{(L)STRB0}}$, $\overline{\text{(L)STRB1}}$ or $\overline{\text{(L)STRB}x}$ |
| CRQ | $\overline{\text{CREQ(0–5)}}$ or $\overline{\text{CREQ}x}$ | ST | (L)STAT3–(L)STAT0 or (L)STATx |
| CRDY | $\overline{\text{CRDY(0–5)}}$ or $\overline{\text{CRDY}x}$ | TCK | TCK |
| CS | $\overline{\text{CSTRB(0–5)}}$ or $\overline{\text{CSTRB}x}$ | TCLK | TCLK0, TCLK1, or TCLKx |
| D | (L)D31–(L)D0 or (L)Dx | TDO | TDO |
| DE | $\overline{\text{(L)DE}}$ | TMS | TMS/TDI |
| H | H1, H3 | WORD | 32-bit word transfer |

timing for X2/CLKIN, H1, H3 (see Figure 7 and Figure 8)

| NO. | | TMS320C40-40 | | TMS320C40-50 | | TMS320C40-60 | | UNIT | | |
|-----|---------------------|---|-----|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| 1 | $t_f(\text{Cl})$ | Fall time, CLKIN | | 5† | | 5† | | ns | | |
| 2 | $t_w(\text{ClL})$ | Pulse duration, CLKIN low, $t_c(\text{Cl}) = \text{MIN}$ | | 8 | | 5 | | ns | | |
| 3 | $t_w(\text{ClH})$ | Pulse duration, CLKIN high, $t_c(\text{Cl}) = \text{MIN}$ | | 8 | | 5 | | ns | | |
| 4 | $t_r(\text{Cl})$ | Rise time, CLKIN | | 5† | | 5† | | ns | | |
| 5 | $t_c(\text{Cl})$ | Cycle time, CLKIN | | 25 | 242.5 | 20 | 242.5 | 16.67 | 242.5 | ns |
| 6 | $t_f(\text{H})$ | Fall time, H1 and H3 | | 3 | | 3 | | ns | | |
| 7 | $t_w(\text{HL})$ | Pulse duration, H1 and H3 low | | $t_c(\text{Cl}) - 6$ | $t_c(\text{Cl}) + 6$ | $t_c(\text{Cl}) - 6$ | $t_c(\text{Cl}) + 6$ | $t_c(\text{Cl}) - 6$ | $t_c(\text{Cl}) + 6$ | ns |
| 8 | $t_w(\text{HH})$ | Pulse duration, H1 and H3 high | | $t_c(\text{Cl}) - 6$ | $t_c(\text{Cl}) + 6$ | $t_c(\text{Cl}) - 6$ | $t_c(\text{Cl}) + 6$ | $t_c(\text{Cl}) - 6$ | $t_c(\text{Cl}) + 6$ | ns |
| 9 | $t_r(\text{H})$ | Rise time, H1 and H3 | | 4 | | 4 | | ns | | |
| 9.1 | $t_d(\text{HL-HH})$ | Delay time from H1 low to H3 high or from H3 low to H1 high | | -1 | 4 | -1 | 4 | -1 | 4 | ns |
| 10 | $t_c(\text{H})$ | Cycle time, H1 and H3 | | 50 | 485 | 40 | 485 | 33.3 | 485 | ns |

† This value is specified by design but not tested.

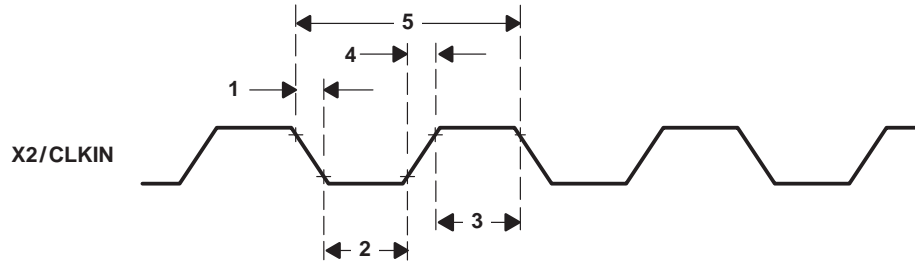


Figure 7. X2/CLKIN Timing

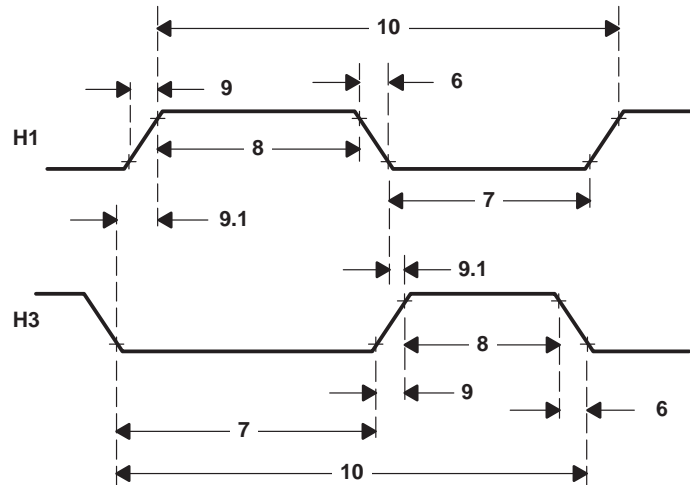


Figure 8. H1 and H3 Timings

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memory-read-cycle and memory-write-cycle timing [$\overline{(L)STRBx} = 0$] (see Note 5, Figure 9 and Figure 10)

| NO. | | TMS320C40-40 | | TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|--|--------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(H1L-SL)}$ Delay time, H1 low to $\overline{(L)STRBx}$ low | 0† | 9 | 0† | 9 | 0† | 8 | ns |
| 2 | $t_{d(H1L-SH)}$ Delay time, H1 low to $\overline{(L)STRBx}$ high | 0† | 9 | 0† | 9 | 0† | 8 | ns |
| 3 | $t_{d(H1H-RWL)}$ Delay time, H1 high to $(L)R/\overline{Wx}$ low | 0† | 9 | 0† | 9 | 0† | 8 | ns |
| 4 | $t_{d(H1L-A)}$ Delay time, H1 low to $(L)Ax$ valid | 0† | 9 | 0† | 9 | 0† | 8 | ns |
| 5 | $t_{su(D-H1L)R}$ Setup time, $(L)Dx$ valid before H1 low (read) | 15 | | 10 | | 9 | | ns |
| 6 | $t_h(H1L-D)R$ Hold time, $(L)Dx$ after H1 low (read) | 0 | | 0 | | 0 | | ns |
| 7 | $t_{su(RDY-H1L)}$ Setup time, $\overline{(L)RDYx}$ valid before H1 low | 25‡ | | 20‡ | | 18† | | ns |
| 8 | $t_h(H1L-RDY)$ Hold time, $\overline{(L)RDYx}$ after H1 low | 0 | | 0 | | 0 | | ns |
| 8.1 | $t_{d(H1L-ST)}$ Delay time, H1 low to $(L)STAT3-(L)STAT0$ valid | | 9 | | 8 | | 8 | ns |
| 9 | $t_{d(H1H-RWH)W}$ Delay time, H1 high to $(L)R/\overline{Wx}$ high (write) | 0† | 9 | 0† | 9 | 0† | 8 | ns |
| 10 | $t_v(H1L-D)W$ Valid time, $(L)Dx$ after H1 low (write) | | 16 | | 16 | | 13 | ns |
| 11 | $t_h(H1H-D)W$ Hold time, $(L)Dx$ after H1 high (write) | 0 | | 0 | | 0 | | ns |
| 12 | $t_{d(H1H-A)}$ Delay time, H1 high to address valid on back-to-back write cycles | | 13 | | 9 | | 8 | ns |

† This value is specified by design but not tested.

‡ If this setup time is not met, the read/write operation is not assured.

NOTE 5: For consecutive reads, $(L)R/\overline{Wx}$ stays high and $\overline{(L)STRBx}$ stays low.



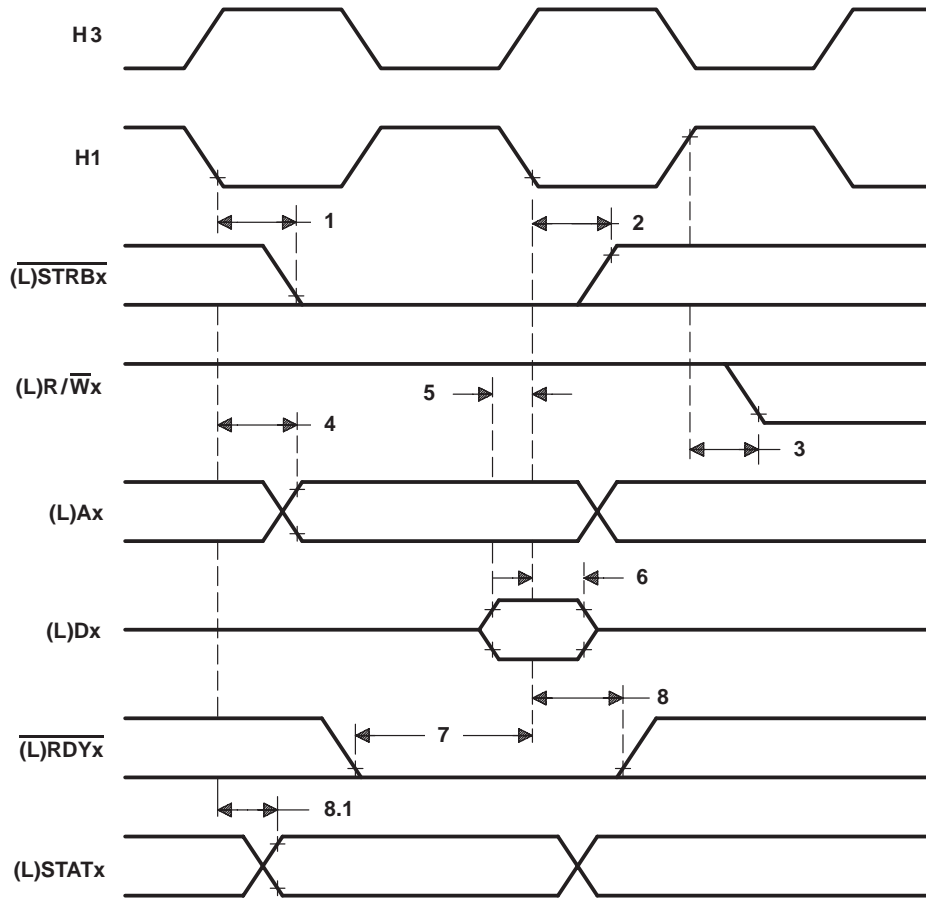


Figure 9. Memory-Read-Cycle Timing [(L)STRBx = 0]

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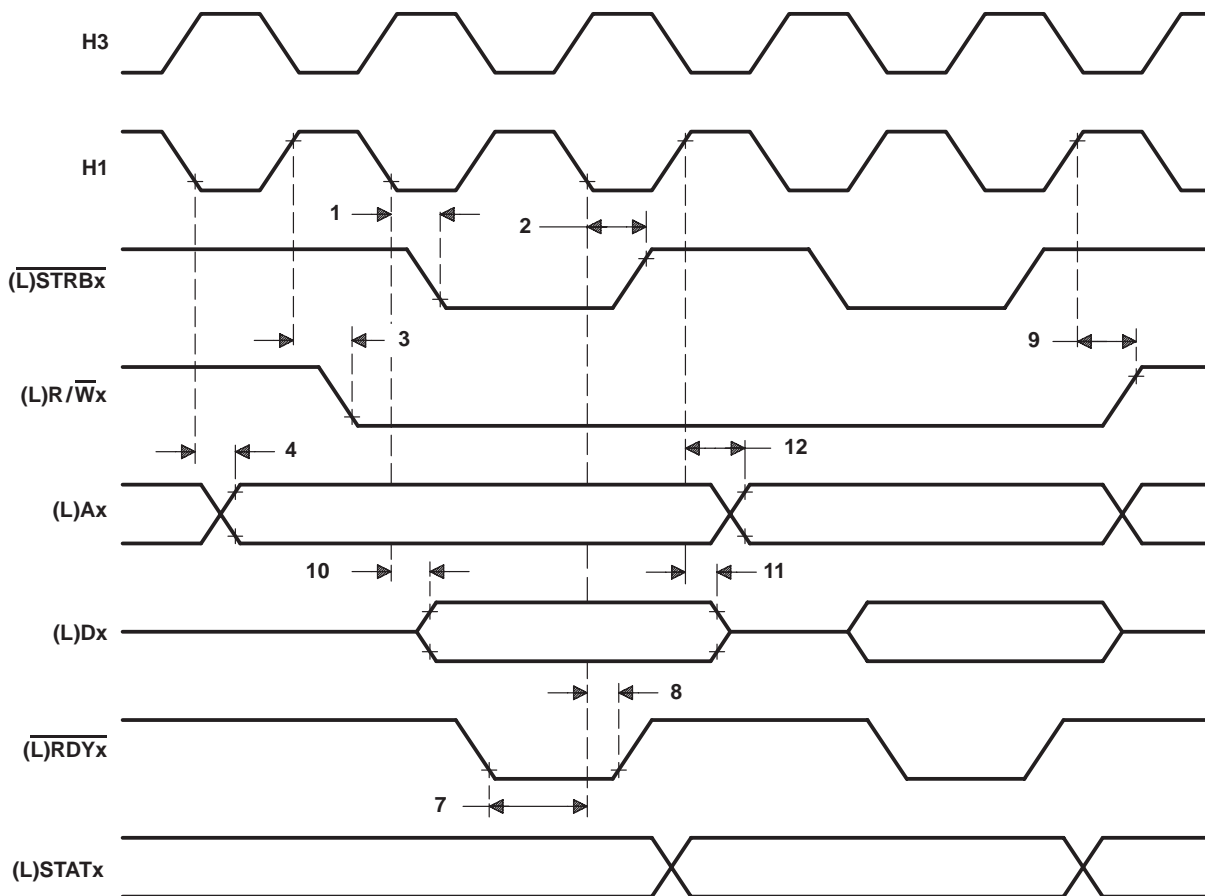


Figure 10. Memory-Write-Cycle Timing [(L)STRBx = 0]

(L)DE-, (L)AE-, and (L)CEx-enable timing (see Figure 11)

| NO. | | TMS320C40-40 TMS320C40-50 | TMS320C40-60 | | UNIT | |
|-----|---|------------------------------|--------------|-----|------|-----|
| | | | MIN | MAX | | MIN |
| 1 | $t_{d(DEH-DZ)}$ Delay time, $\overline{(L)DE}$ high to (L)D0–(L)D31 in the high-impedance state | 0† | 15‡ | 0† | 15‡ | ns |
| 2 | $t_{d(DEL-DV)}$ Delay time, $\overline{(L)DE}$ low to (L)D0–(L)D31 valid | 0† | 21 | 0† | 16 | ns |
| 3 | $t_{d(AEH-AZ)}$ Delay time, $\overline{(L)AE}$ high to (L)A0–(L)A30 in the high-impedance state | 0† | 15‡ | 0† | 15‡ | ns |
| 4 | $t_{d(AEL-AV)}$ Delay time, $\overline{(L)AE}$ low to (L)A0–(L)A30 valid | 0† | 18 | 0† | 16 | ns |
| 5 | $t_{d(CEH-RWZ)}$ Delay time, $\overline{(L)CEx}$ high to (L)R/ \overline{W} 0, (L)R/ \overline{W} 1 in the high-impedance state | 0† | 15‡ | 0† | 15‡ | ns |
| 6 | $t_{d(CEL-RWV)}$ Delay time, $\overline{(L)CEx}$ low to (L)R/ \overline{W} 0, (L)R/ \overline{W} 1 valid | 0† | 21 | 0† | 16 | ns |
| 7 | $t_{d(CEH-SZ)}$ Delay time, $\overline{(L)CEx}$ high to (L)STRB0, (L)STRB1 in the high-impedance state | 0† | 15‡ | 0† | 15‡ | ns |
| 8 | $t_{d(CEL-SV)}$ Delay time, $\overline{(L)CEx}$ low to (L)STRB0, (L)STRB1 valid | 0† | 21 | 0† | 16 | ns |
| 9 | $t_{d(CEH-PAGEZ)}$ Delay time, $\overline{(L)CEx}$ high to (L)PAGE0, (L)PAGE1 in the high-impedance state | 0† | 15‡ | 0† | 15‡ | ns |
| 10 | $t_{d(CEL-PAGEV)}$ Delay time, $\overline{(L)CEx}$ low to (L)PAGE0, (L)PAGE1 valid | 0† | 21 | 0† | 16 | ns |

† This value is specified by design but not tested.

‡ This value is characterized but not tested.

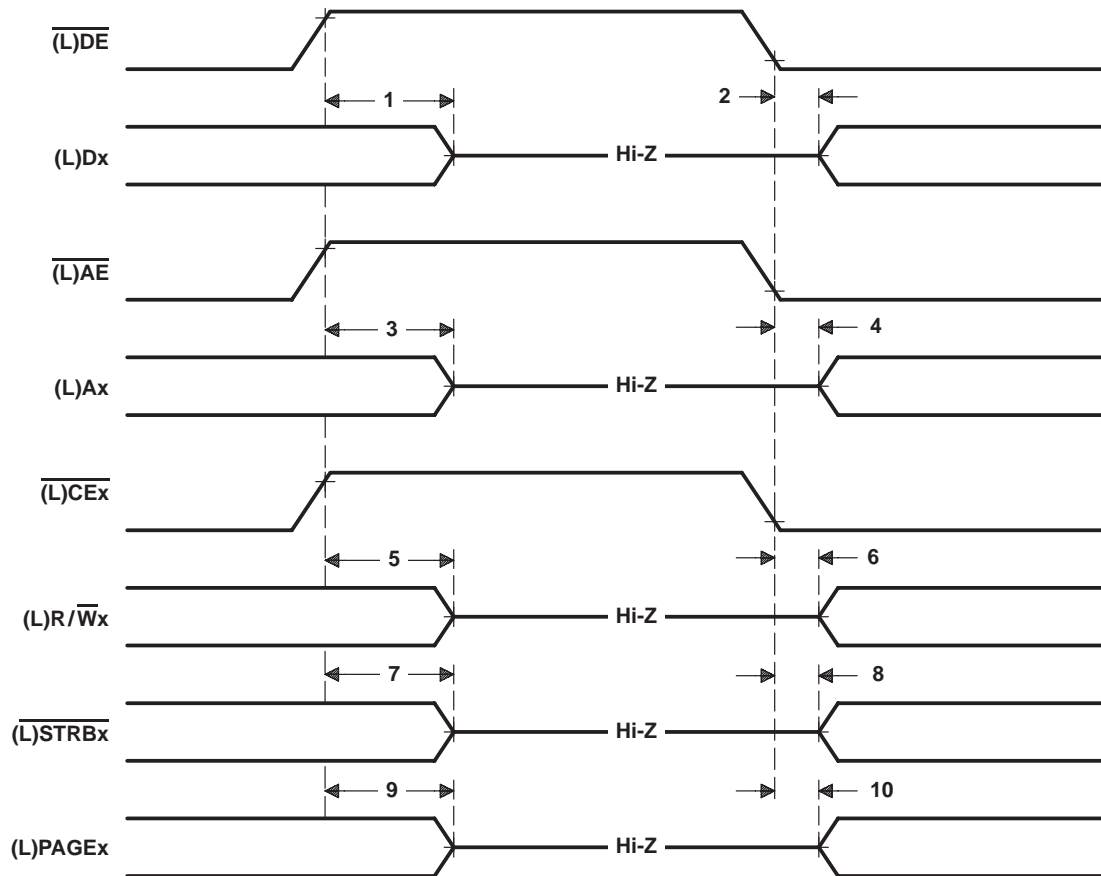


Figure 11. $\overline{(L)DE}$ -, $\overline{(L)AE}$ -, and $\overline{(L)CEx}$ -Enable Timings

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timing for $\overline{\text{(L)LOCK}}$ when executing LDFI or LDII (see Figure 12)

| NO. | | TMS320C40-40 | | TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|--|--------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(\text{H1L}-\text{LOCKL})}$ Delay time, H1 low to $\overline{\text{(L)LOCK}}$ low | | 11 | | 8 | | 8 | ns |

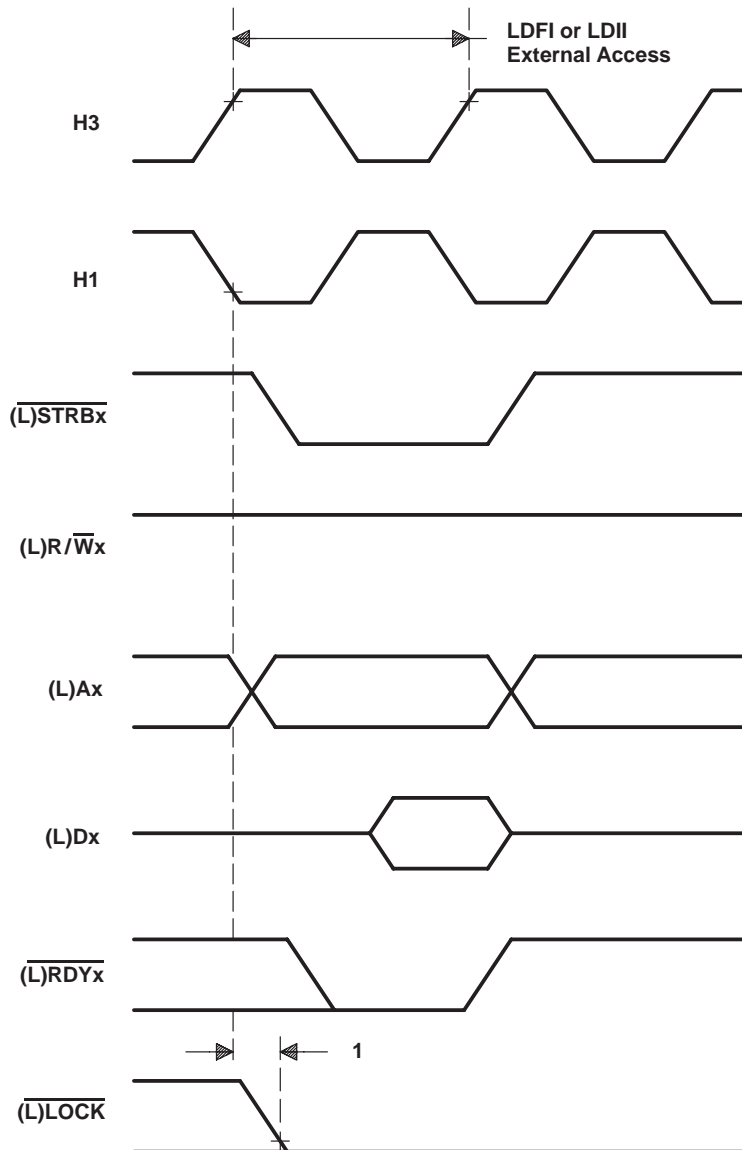


Figure 12. Timing for $\overline{\text{(L)LOCK}}$ When Executing LDFI or LDII

timing for $\overline{\text{(L)LOCK}}$ when executing STFI or STII (see Figure 13)

| NO. | | TMS320C40-40 | | TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|--|--------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(\text{H1L-LOCKH})}$ Delay time, H1 low to $\overline{\text{(L)LOCK}}$ high | | 11 | | 8 | | 8 | ns |

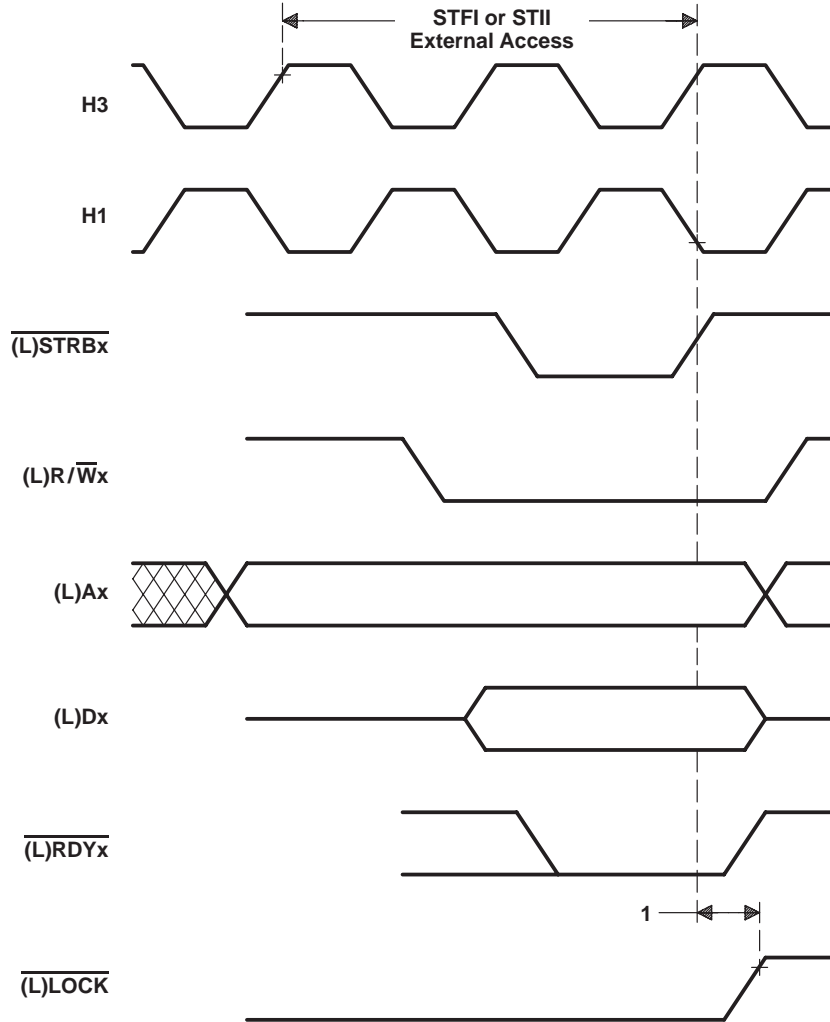


Figure 13. Timing for $\overline{\text{(L)LOCK}}$ When Executing STFI or STII

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timing for $\overline{(L)LOCK}$ when executing SIGI (see Figure 14)

| NO. | | TMS320C40-40 | | TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|--|--------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(H1L-LOCKL)}$ Delay time, H1 low to $\overline{(L)LOCK}$ low | | 11 | | 8 | | 8 | ns |
| 2 | $t_{d(H1L-LOCKH)}$ Delay time, H1 low to $\overline{(L)LOCK}$ high | | 11 | | 8 | | 8 | |

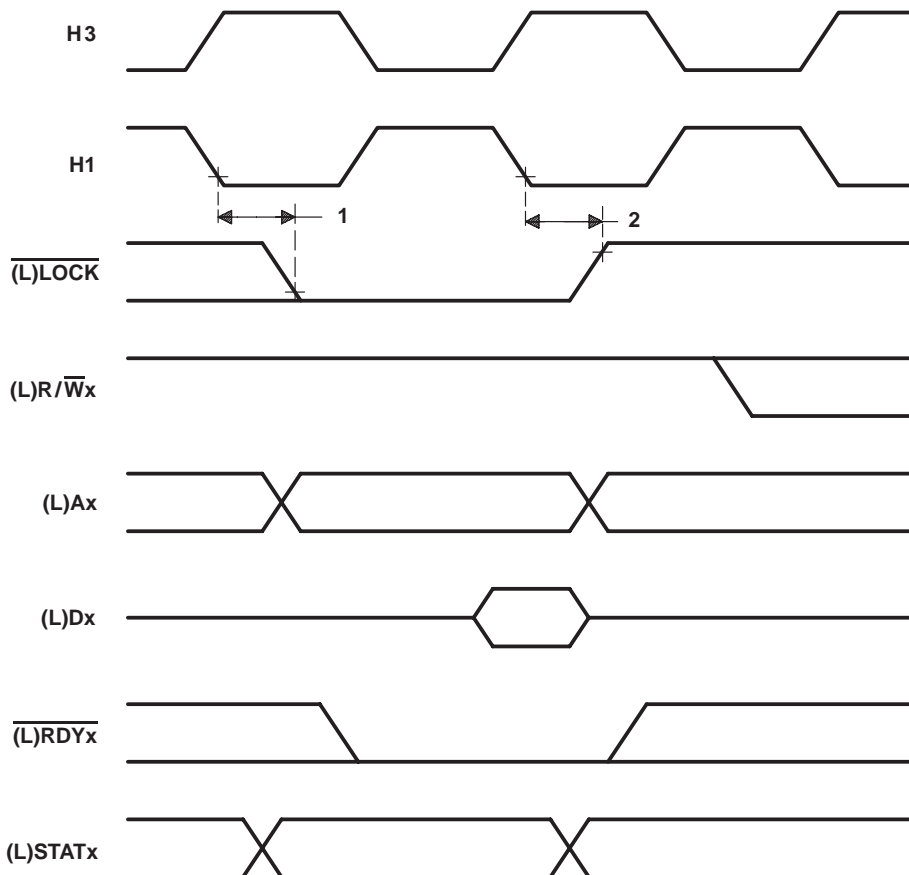


Figure 14. Timing for $\overline{(L)LOCK}$ When Executing SIGI

timing for (L)PAGE0, (L)PAGE1 during memory access to a different page (see Figure 15)

| NO. | | TMS320C40-40 TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|---|------------------------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(H1L-PAGEH)}$ Delay time, H1 low to (L)PAGE _x high for access to different page | 0 | 9 | 0 | 8 | ns |
| 2 | $t_{d(H1L-PAGEL)}$ Delay time, H1 low to (L)PAGE _x low for access to different page | 0 | 9 | 0 | 8 | ns |

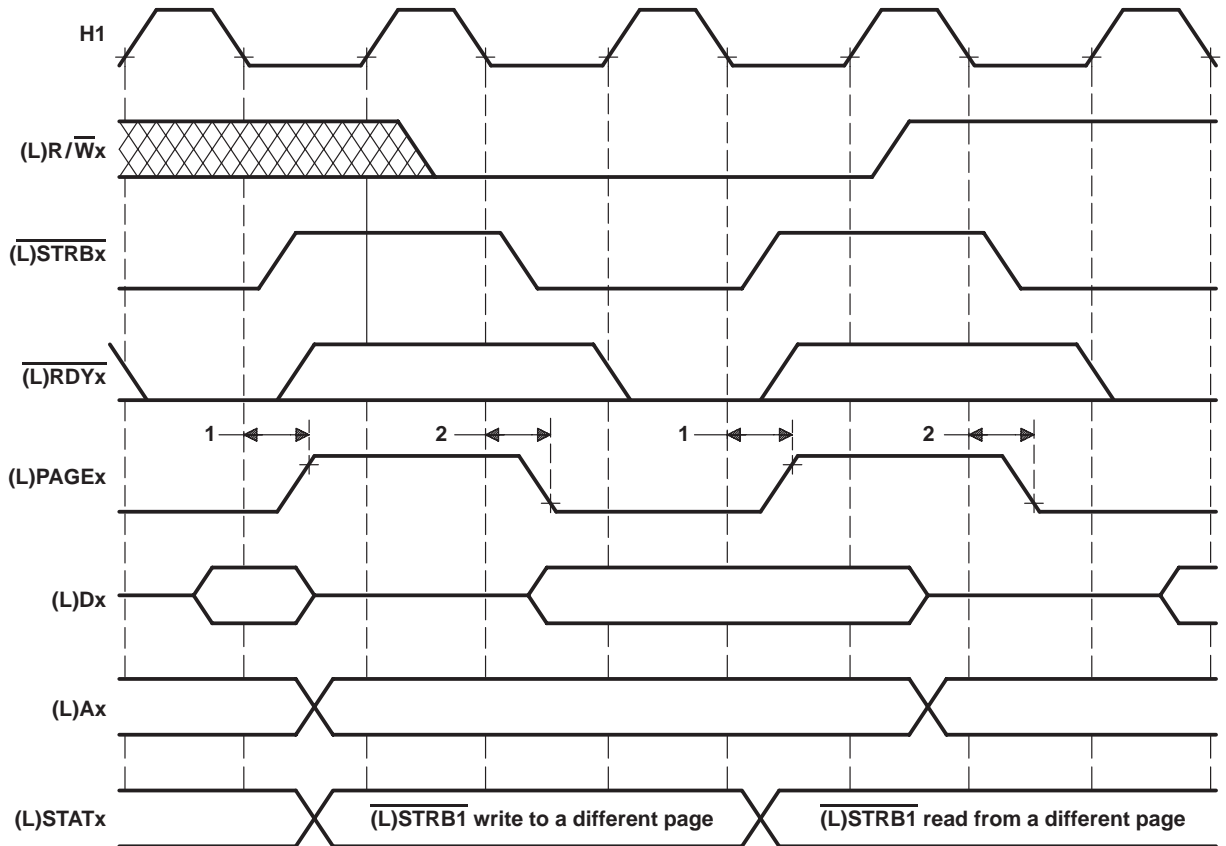


Figure 15. (L)PAGE0, (L)PAGE1 Timing Cycle, Memory Access to a Different Page

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timing for the $\overline{\text{IIOF}}_x$ when configured as an output (see Figure 16)

| NO. | | TMS320C40-40 | | TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|--|--------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{V(\text{H1L}-\text{IIOF})}$ H1 low to $\overline{\text{IIOF}}_x$ valid | | 16 | | 14 | | 14 | ns |

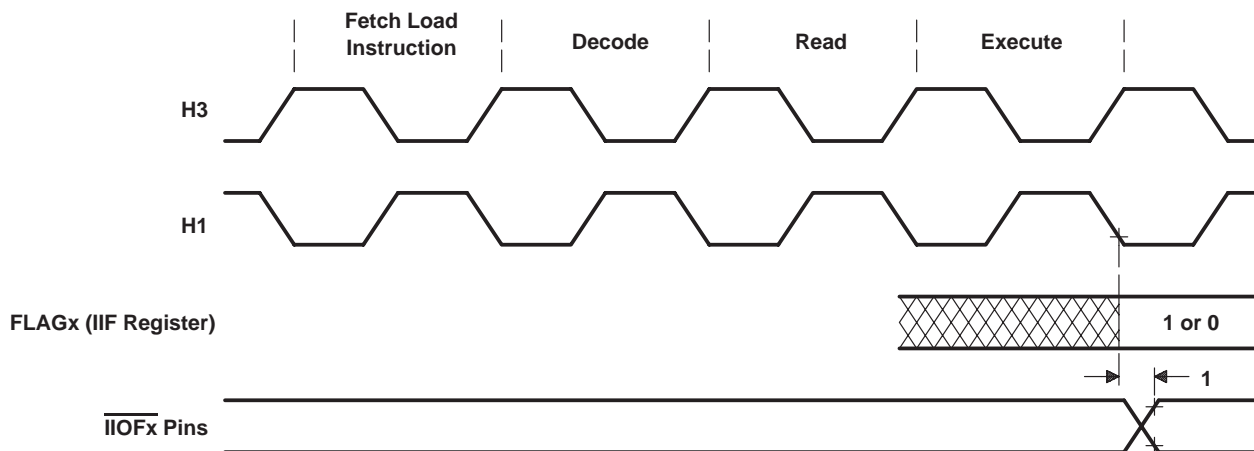


Figure 16. Timing for the $\overline{\text{IIOF}}_x$ When Configured as an Output

timing of $\overline{\text{IIOF}}_x$ changing from output to input mode (see Figure 17)

| NO. | | TMS320C40-40 TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|--|------------------------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_h(\text{H1L}-\overline{\text{IIOF}}_x)$ Hold time, $\overline{\text{IIOF}}_x$ after H1 low | | 14† | | 14† | ns |
| 2 | $t_{su}(\overline{\text{IIOF}}_x\text{-H1L})$ Setup time, $\overline{\text{IIOF}}_x$ before H1 low | 11 | | 11 | | ns |
| 3 | $t_h(\text{H1L}-\overline{\text{IIOF}}_x)$ Hold time, $\overline{\text{IIOF}}_x$ after H1 low | 0 | | 0 | | ns |

† This value is specified by design but not tested.

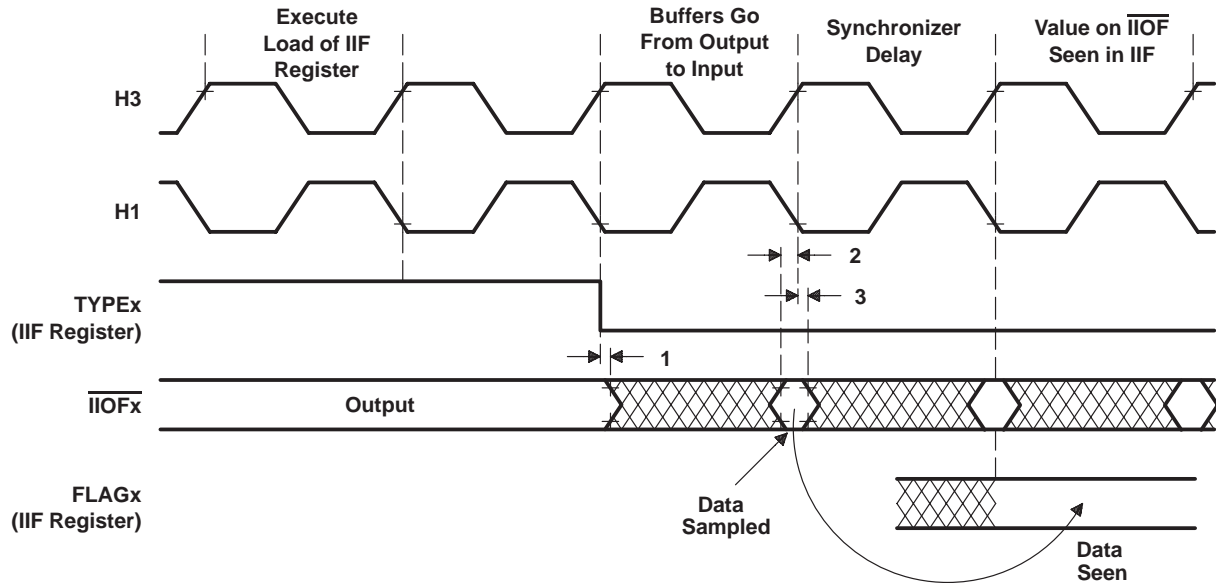


Figure 17. Change of $\overline{\text{IIOF}}_x$ From Output to Input Mode

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timing of $\overline{\text{IIOF}}_x$ changing from input to output mode (see Figure 18)

| NO. | | TMS320C40-40 | | TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|---|--------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(\text{H1L}-\text{IFIO})}$ Delay time, H1 low to $\overline{\text{IIOF}}_x$ switching from input to output | | 16 | | 14 | | 14 | ns |

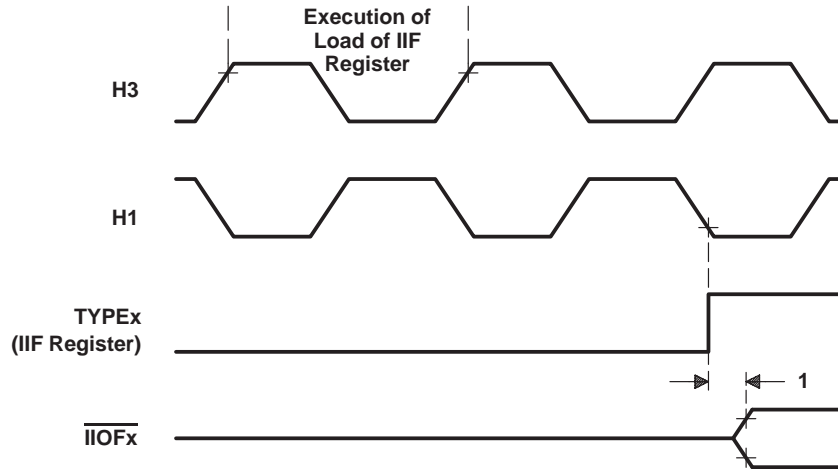


Figure 18. Change of $\overline{\text{IIOF}}_x$ From Input to Output Mode

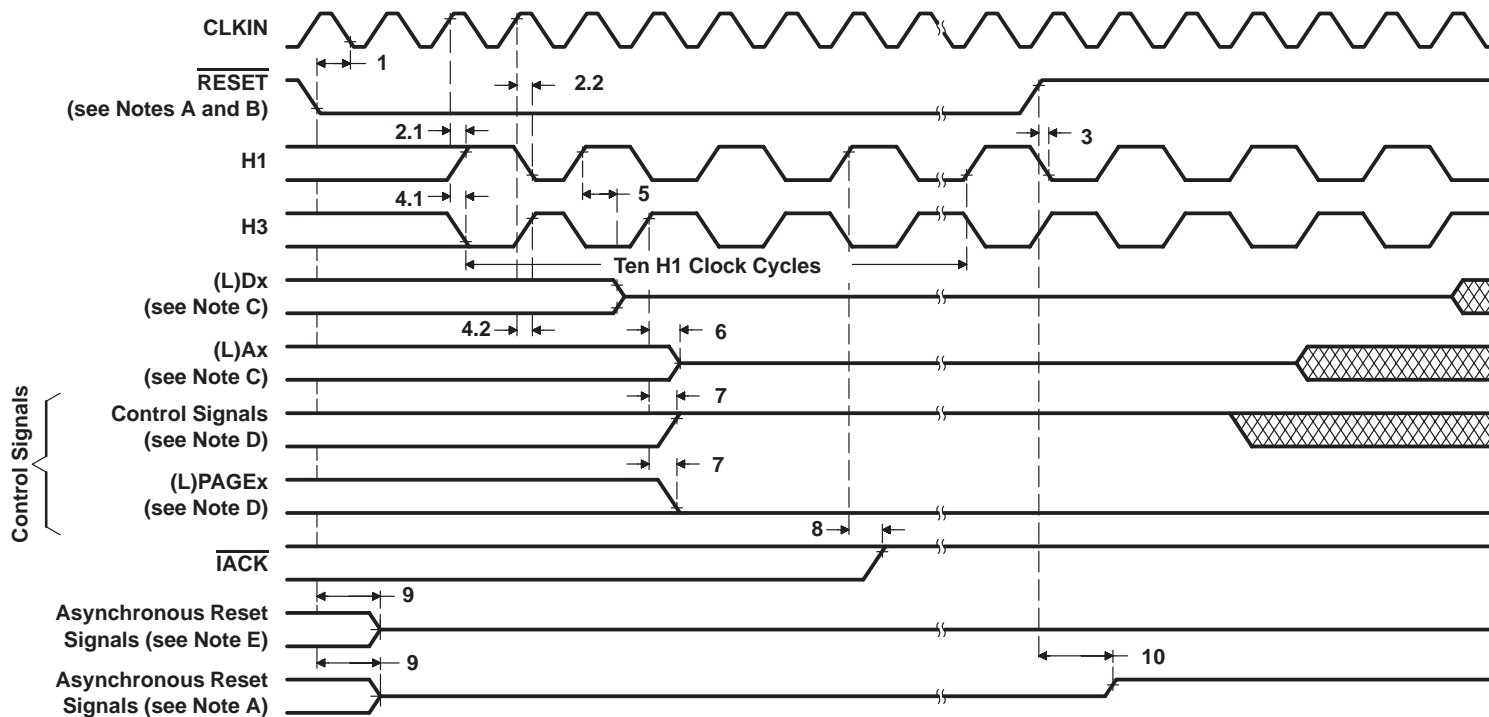
RESET timing (see Figure 19)

| NO. | | TMS320C40-40 | | TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|--|--------------|----------------------------|--------------|----------------------------|--------------|----------------------------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(\text{RESET}-\text{C1L})}$ Setup time for $\overline{\text{RESET}}$ before CLKIN low | 11 | $t_{c(\text{Cl})}^\dagger$ | 11 | $t_{c(\text{Cl})}^\dagger$ | 11 | $t_{c(\text{Cl})}^\dagger$ | ns |
| 2.1 | $t_{d(\text{ClH}-\text{H1H})}$ Delay time, CLKIN high to H1 high | 3 | 10 | 2 | 10 | 2 | 10 | ns |
| 2.2 | $t_{d(\text{ClH}-\text{H1L})}$ Delay time, CLKIN high to H1 low | 3 | 10 | 2 | 10 | 2 | 10 | ns |
| 3 | $t_{su(\text{RESETH}-\text{H1L})}$ Setup time for $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles | 13 | | 13 | | 13 | | ns |
| 4.1 | $t_{d(\text{ClH}-\text{H3L})}$ Delay time, CLKIN high to H3 low | 3 | 10 | 2 | 10 | 2 | 10 | ns |
| 4.2 | $t_{d(\text{ClH}-\text{H3H})}$ Delay time, CLKIN high to H3 high | 3 | 10 | 2 | 10 | 2 | 10 | ns |
| 5 | $t_{d(\text{H1H}-\text{DZ})}$ Delay time, H1 high to (L)Dx in the high-impedance state | | 13‡ | | 13‡ | | 13‡ | ns |
| 6 | $t_{d(\text{H3H}-\text{AZ})}$ Delay time, H3 high to (L)Ax in the high-impedance state | | 9‡ | | 9‡ | | 9‡ | ns |
| 7 | $t_{d(\text{H3H}-\text{CONTROLH})}$ Delay time, H3 high to control signals high [low for (L)PAGE] | | 9‡ | | 9‡ | | 9‡ | ns |
| 8 | $t_{d(\text{H1H}-\text{IACKH})}$ Delay time, H1 high to $\overline{\text{IACK}}$ high | | 9‡ | | 9‡ | | 9‡ | ns |
| 9 | $t_{d(\text{RESETL}-\text{ASYNCH})}$ Delay time, $\overline{\text{RESET}}$ low to asynchronous reset signals in the high-impedance state | | 21‡ | | 21‡ | | 21‡ | ns |
| 10 | $t_{d(\text{RESETH}-\text{COMMH})}$ Delay time, $\overline{\text{RESET}}$ high to asynchronous reset signals high | | 15‡ | | 15‡ | | 15‡ | ns |

$^\dagger t_{c(\text{Cl})}$, the CLKIN period as shown in Figure 7

‡ This value is characterized but not tested.





- NOTES:
- Asynchronous reset signals that go to a high logic level after $\overline{\text{RESET}}$ returns to a high state include $\overline{\text{CREQ}}_y$, $\overline{\text{CACK}}_x$, $\overline{\text{CSTRB}}_x$, and $\overline{\text{CRDY}}_y$ (where $x = 0, 1$ or 2 and $y = 3, 4$ or 5).
 - $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.
 - For Figure 19 only, (L)Dx includes D31–D0, LD31–LD0, and CxD7–CxD0, (L)Ax includes LA(30–0) and A(30–0).
 - Control signals LSTRB0, LSTRB1, STRB0, STRB1, (L)STAT3–(L)STAT0, (L)LOCK, (L)R/W0, and (L)R/W1 go high while (L)PAGE0 and (L)PAGE1 go low.
 - Asynchronous reset signals that go into the high-impedance state after $\overline{\text{RESET}}$ goes low include TCLK0, TCLK1, IIOF3–IIOF0, and the communication-port control signals CREQx, CACKy, CSTRBy, and CRDYx (where $x = 0, 1$ or 2 , and $y = 3, 4$ or 5). At reset, ports 0, 1, and 2 become outputs, while ports 3, 4, and 5 become inputs.

Figure 19. $\overline{\text{RESET}}$ Timing

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timing for $\overline{\text{IIOF}}_x$ interrupt response [$P = t_{c(H)}$] (see Notes 6, 7 and Figure 20)

| NO. | | TMS320C40-40 TMS320C40-50 | | | TMS320C40-60 | | | UNIT |
|-----|---|------------------------------|------|-------|--------------|------|-------|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su}(\overline{\text{IIOF}}_x)$ Setup time, $\overline{\text{IIOF}}_x$ before H1 low | 1† | | | 1† | | | ns |
| 2 | $t_w(\text{INT})$ Pulse duration, to assure one interrupt is seen (see Note 8) | P | 1.5P | < 2P‡ | P | 1.5P | < 2P‡ | ns |

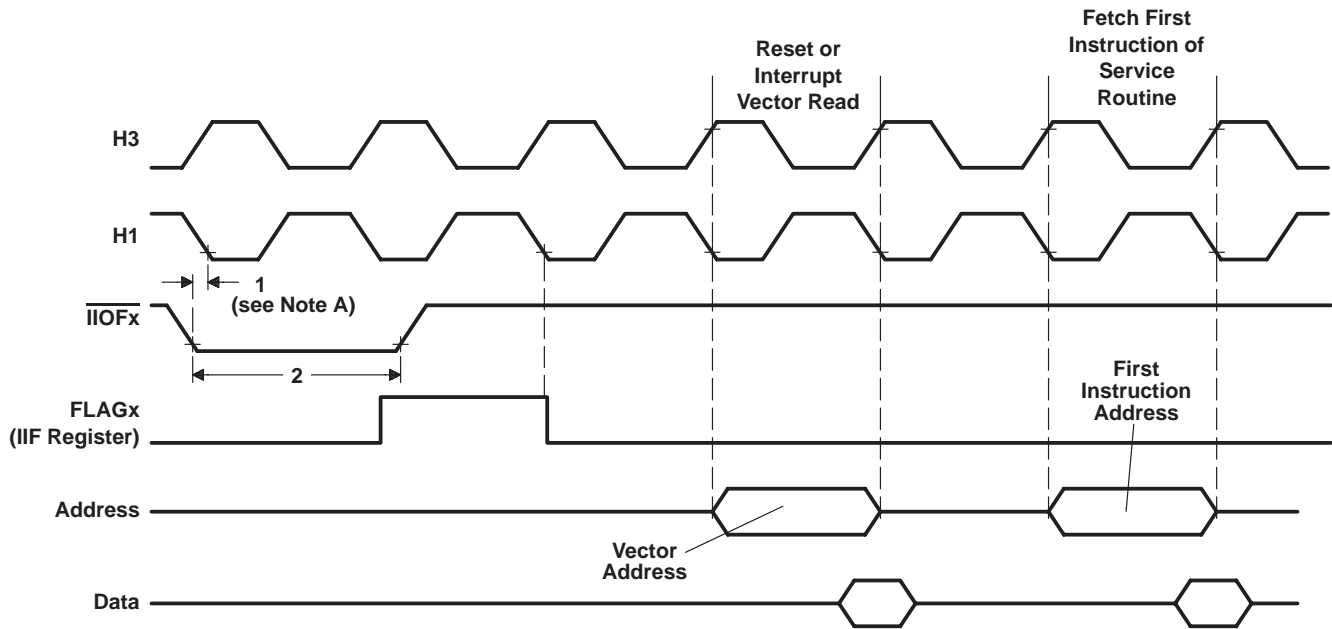
† If this timing is not met, the interrupt is recognized in the next cycle.

‡ This value applies only to level-triggered interrupts and is specified by design but not tested.

NOTES: 6. $\overline{\text{IIOF}}_x$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.

7. Edge-triggered interrupts require a setup of time (1) and a minimum duration of P. No maximum duration limit exists.

8. Level-triggered interrupts require interrupt-pulse duration of at least 1P wide (P = one H1 period) to assure it will be seen. It must be less than 2P wide to assure it will be responded to only once. Recommended pulse duration is 1.5P.



NOTE A: The 'C40 can accept an interrupt from the same source every two H1 clock cycles.

Figure 20. $\overline{\text{IIOF}}_x$ Interrupt-Response Timing [$P = t_{c(H)}$]

timing for $\overline{\text{IACK}}$ (see Note 9 and Figure 21)

| NO. | | TMS320C40-40 TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|---|------------------------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(H1L - \overline{\text{IACKL}})}$ Delay time, H1 low to $\overline{\text{IACK}}$ low | | 9 | | 7 | ns |
| 2 | $t_{d(H1L - \overline{\text{IACKH}})}$ Delay time, H1 low to $\overline{\text{IACK}}$ high during first cycle of IACK instruction data read | | 9 | | 7 | ns |

NOTE 9: The $\overline{\text{IACK}}$ output is active for the entire duration of the bus cycle and is, therefore, extended if the bus cycle utilizes wait states.

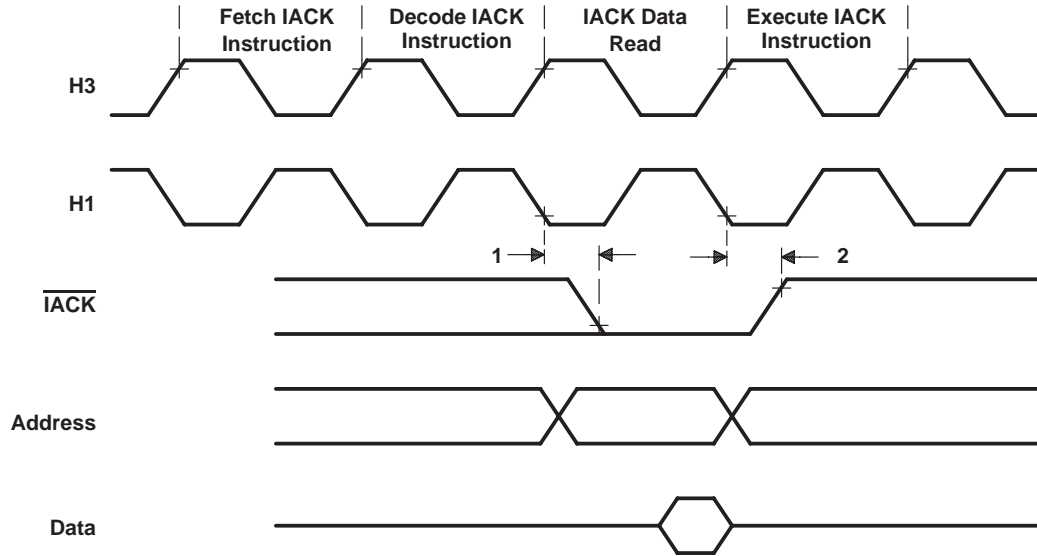


Figure 21. $\overline{\text{IACK}}$ Timing

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communication-port word-transfer-cycle timing† [P = t_{c(H)}] (see Note 10 and Figure 22)

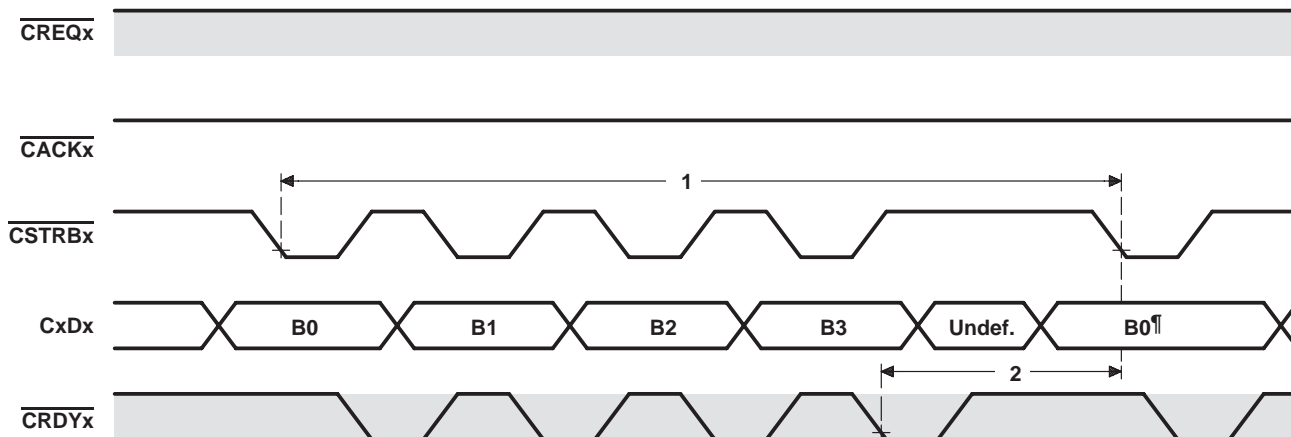
| NO. | | TMS320C40-40 TMS320C40-50† | | TMS320C40-60† | | UNIT |
|-----|--|-------------------------------|----------|---------------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | t _{c(WORD)} ‡§ Cycle time, word transfer (4 bytes = 1 word) | 1.5P+7 | 2.5P+170 | 1.5P+7 | 2.5P+170 | ns |
| 2 | t _{d(CRDYL-CSL)W} ‡ Delay time, CRDYx low to CSTRBx low between back-to-back write cycles | 1.5P+7 | 2.5P+28 | 1.5P+7 | 2.5P+28 | ns |

† For these timing values, it is assumed that the receiving 'C4x is ready to receive data. Line propagation delay is not considered.

‡ This value is characterized but not tested.

§ t_{c(WORD)} max = 2.5P + 28 ns + the maximum summed values of 4 × t_{d(CSL-CRDYL)R}, 3 × t_{d(CRDYL-CSH)}, 3 × t_{d(CSH-CRDYH)R}, and 3 × t_{d(CRDYH-CSL)W} as seen in Figure 23. This timing assumes two 'C4xs are connected.

NOTE 10: These timings apply only to two communicating 'C4xs. When a non-'C4x device communicates with a 'C40, timings can be longer. No restriction exists in this case on how slow the transfer could be except when using early silicon (C40 PG 1.x or 2.x). Refer to the CSTRB width restriction in Section 8.9.1 of the *TMS320C4x User's Guide* (literature number SPRU063B).



■ = When signal is an input (clear = when signal is an output).

† Begins byte 0 of the next word.

NOTE A: For correct operation during token exchange, the two communicating 'C4xs must have CLKIN frequencies within a factor of 2 of each other (in other words, at most, one of the 'C4xs can be twice as fast as the other).

Figure 22. Communication-Port Word-Transfer-Cycle Timing [P = t_{c(H)}]

communication-port byte-cycle timing (write and read) (see Note 11 and Figure 23)

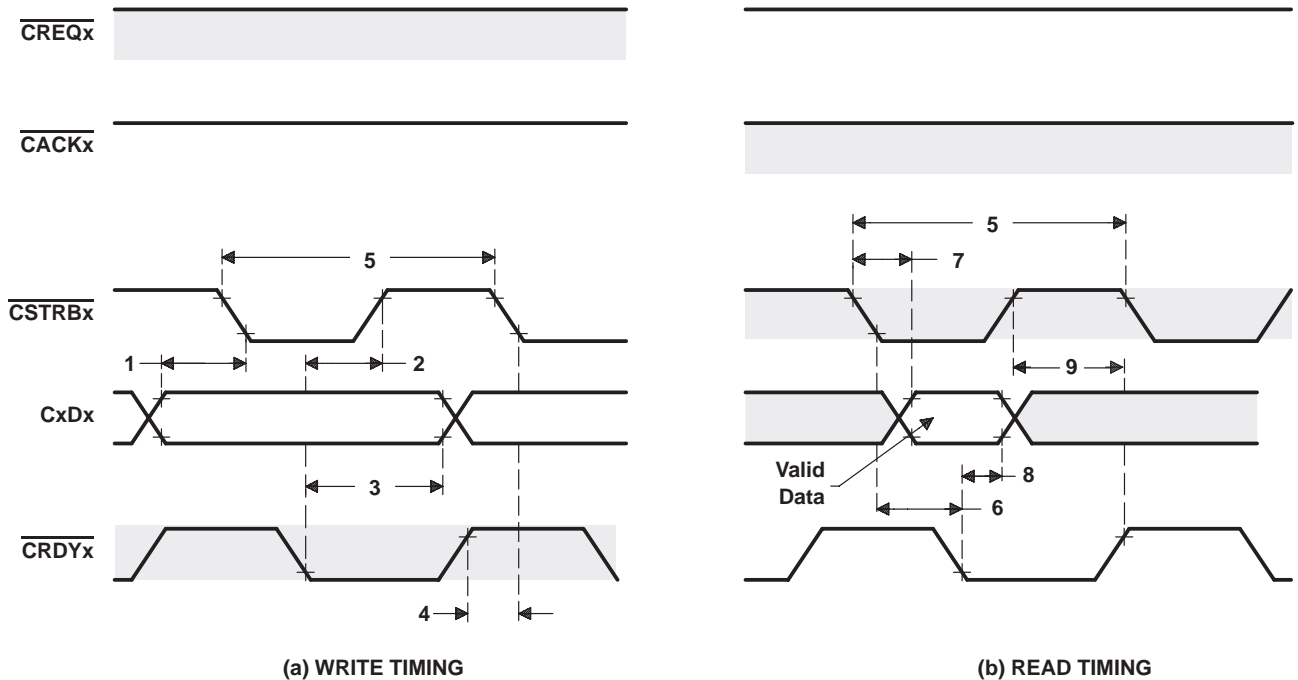
| NO. | | TMS320C40-40 TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|---|------------------------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{su}(CD-CSL)W$ Setup time, CxDx valid before \overline{CSTRBx} low (write) | 2 | | 2 | | ns |
| 2 | $t_d(CRDYL-CSH)W$ Delay time, \overline{CRDYx} low to \overline{CSTRBx} high (write) | 0† | 12 | 0† | 12 | ns |
| 3 | $t_h(CRDYL-CD)W$ Hold time, CxDx after \overline{CRDYx} low (write) | 2 | | 2 | | ns |
| 4 | $t_d(CRDYH-CSL)W$ Delay time, \overline{CRDYx} high to \overline{CSTRBx} low for subsequent bytes (write) | 0† | 12 | 0† | 12 | ns |
| 5 | $t_c(BYTE)‡$ Cycle time, byte transfer | | 44§ | | 44§ | ns |
| 6 | $t_d(CSL-CRDYL)R$ Delay time, \overline{CSTRBx} low to \overline{CRDYx} low (read) | 0† | 10 | 0† | 10 | ns |
| 7 | $t_{su}(CSH-CD)R$ Setup time, CxDx valid after \overline{CSTRBx} high (read) | 0 | | 0 | | ns |
| 8 | $t_h(CRDYL-CD)R$ Hold time, CxDx valid after \overline{CRDYx} low (read) | 2 | | 2 | | ns |
| 9 | $t_d(CSH-CRDYH)R$ Delay time, \overline{CSTRBx} high to \overline{CRDYx} high (read) | 0† | 10 | 0† | 10 | ns |

† This value is specified by design but not tested.

‡ $t_c(BYTE)$ max = summed maximum values of $t_d(CRDY-CSH)$, $t_d(CSL-CRDYL)R$, $t_d(CSH-CRDYH)R$, and $t_d(CRDYH-CSL)W$. This assumes two 'C4xs are connected.

§ This value is characterized but not tested.

NOTE 11: Communication port timing does not include line length delay.



■ = When signal is an input (clear = when signal is an output).

Figure 23. Communication-Port Byte-Cycle Timing (Write and Read)

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timing for communication-token transfer sequence, input to an output port [P = t_{c(H)}]
(see Figure 24)[†]

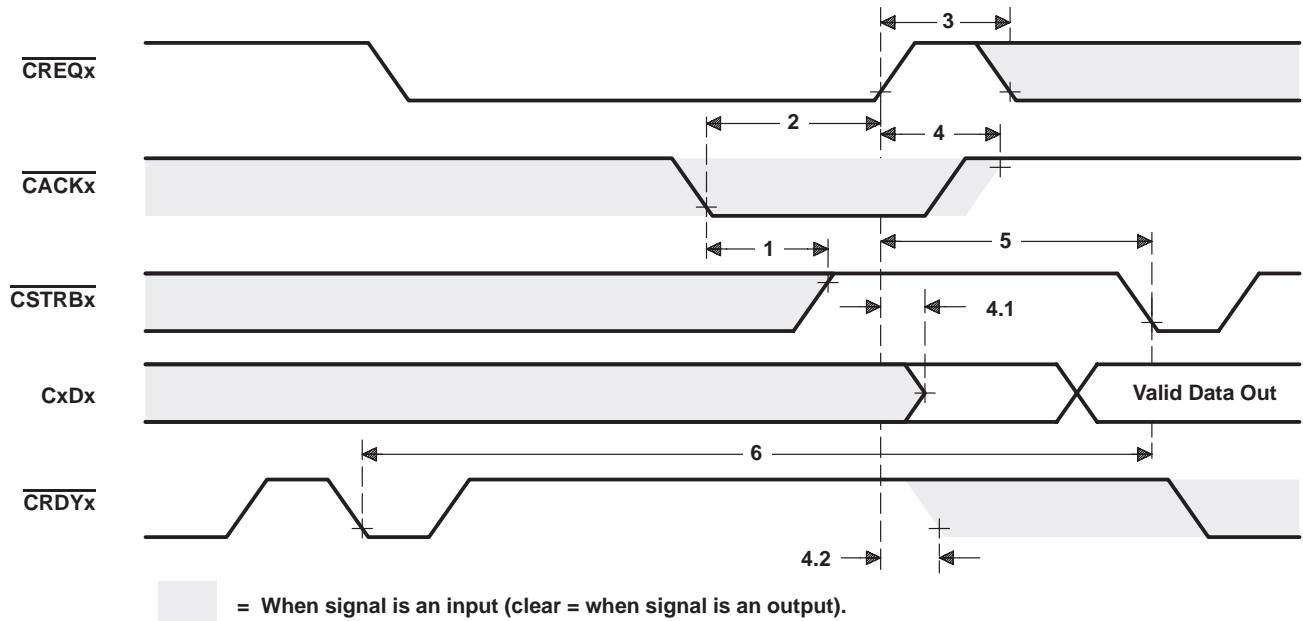
| NO. | | | TMS320C40-40 TMS320C40-50 | | TMS320C40-60 | | UNIT |
|----------------|-----------------------------|---|------------------------------|---------|--------------|---------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 [‡] | t _d (CAL-CS)T | Delay time, $\overline{\text{CACKx}}$ low to $\overline{\text{CSTRBx}}$ change from input to a high-level output | 0.5P+6 | 1.5P+22 | 0.5P+6 | 1.5P+22 | ns |
| 2 [‡] | t _d (CAL-CRQH)T | Delay time, $\overline{\text{CACKx}}$ low to start of $\overline{\text{CREQx}}$ going high for token request acknowledge | P+5 | 2P+22 | P+5 | 2P+22 | ns |
| 3 | t _d (CRQH-CRQ)T | Delay time, start of $\overline{\text{CREQx}}$ going high to $\overline{\text{CREQx}}$ change from output to an input | 0.5P-5 | 0.5P+13 | 0.5P-5 | 0.5P+13 | ns |
| 4 | t _d (CRQH-CA)T | Delay time, start of $\overline{\text{CREQx}}$ going high to $\overline{\text{CACKx}}$ change from an input to an output level high | 0.5P-5 | 0.5P+13 | 0.5P-5 | 0.5P+13 | ns |
| 4.1 | t _d (CRQH-CD)T | Delay time, start of $\overline{\text{CREQx}}$ going high to CxDx change from inputs driven to outputs driven | 0.5P-5 | 0.5P+13 | 0.5P-5 | 0.5P+13 | ns |
| 4.2 | t _d (CRQH-CRDY)T | Delay time, start of $\overline{\text{CREQx}}$ going high to $\overline{\text{CRDYx}}$ change from an output to an input | 0.5P-5 | 0.5P+13 | 0.5P-5 | 0.5P+13 | ns |
| 5 | t _d (CRQH-CSL)T | Delay time, start of $\overline{\text{CREQx}}$ going high to $\overline{\text{CSTRBx}}$ low for start of word transfer out | 1.5P-8 | 1.5P+9 | 1.5P-8 | 1.5P+9 | ns |
| 6 [‡] | t _d (CRDYL-CSL)T | Delay time, $\overline{\text{CRDYx}}$ low at end of word input to $\overline{\text{CSTRBx}}$ low for word output | 3.5P+12 | 5.5P+48 | 3.5P+12 | 5.5P+48 | ns |

[†] These values are characterized but not tested.

[‡] These timing parameters result from synchronizer delays.



timing for communication-token transfer sequence, input to an output port [$P = t_{c(H)}$] (continued)



NOTE A: Before the token exchange, \overline{CREQx} and \overline{CRDYx} are output signals asserted by the TMS320C4x that is receiving data. \overline{CACKx} , \overline{CSTRBx} , and $CxD7-CxD0$ are input signals asserted by the device sending data to the 'C4x; these are asynchronous with respect to the H1 clock of the receiving '320C4x. After token exchange, \overline{CACKx} , \overline{CSTRBx} , and $CxD7-CxD0$ become output signals, and \overline{CREQx} and \overline{CRDYx} become inputs.

Figure 24. Communication-Token Transfer Sequence, Input to an Output Port [$P = t_{c(H)}$]

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timing for communication-token transfer sequence, output to an input port [P = t_{c(H)}]
(see Figure 25)[†]

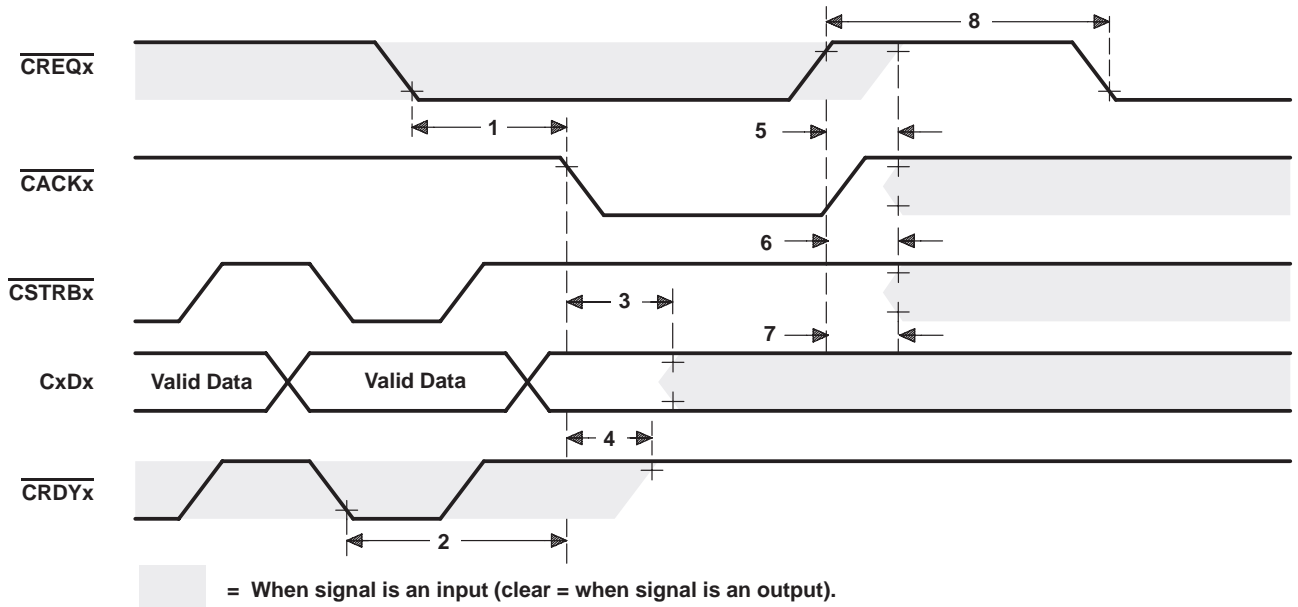
| NO. | | | TMS320C40-40 TMS320C40-50 | | TMS320C40-60 | | UNIT |
|----------------|-----------------------------|--|------------------------------|--------|--------------|--------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 [‡] | t _d (CRQL-CAL)T | Delay time, $\overline{\text{CREQx}}$ low to start of $\overline{\text{CACKx}}$ going low for token-request-acknowledge | P+5 | 2P+22 | P+5 | 2P+22 | ns |
| 2 [‡] | t _d (CRDYL-CAL)T | Delay time, $\overline{\text{CRDYx}}$ low at end of word transfer out to start of $\overline{\text{CACKx}}$ going low | P+6 | 2P+27 | P+6 | 2P+27 | ns |
| 3 | t _d (CAL-CD)I | Delay time, start of $\overline{\text{CACKx}}$ going low to CxDx change from outputs to inputs | 0.5P-8 | 0.5P+8 | 0.5P-8 | 0.5P+8 | ns |
| 4 | t _d (CAL-CRDY)T | Delay time, start of $\overline{\text{CACKx}}$ going low to $\overline{\text{CRDYx}}$ change from an input to output, high level | 0.5P-8 | 0.5P+8 | 0.5P-8 | 0.5P+8 | ns |
| 5 | t _d (CRQH-CRQ)T | Delay time, $\overline{\text{CREQx}}$ high to $\overline{\text{CREQx}}$ change from an input to output, high level | 4 | 22 | 4 | 22 | ns |
| 6 | t _d (CRQH-CA)T | Delay time, $\overline{\text{CREQx}}$ high to $\overline{\text{CACKx}}$ change from output to an input | 4 | 22 | 4 | 22 | ns |
| 7 | t _d (CRQH-CS)T | Delay time, $\overline{\text{CREQx}}$ high to $\overline{\text{CSTRBx}}$ change from output to an input | 4 | 22 | 4 | 22 | ns |
| 8 [‡] | t _d (CRQH-CRQL)T | Delay time, $\overline{\text{CREQx}}$ high to $\overline{\text{CREQx}}$ low for the next token request | P-4 | 2P+8 | P-4 | 2P+8 | ns |

[†] These values are characterized but not tested.

[‡] These timing parameters result from synchronizer delays.



timing for communication-token transfer sequence, input to an output port [$P = t_{c(H)}$] (continued)



NOTE A: Before the token exchange, \overline{CACKx} , \overline{CSTRBx} , and $CxD7-CxD0$ are asserted by the 'C4x sending data. \overline{CREQx} and \overline{CRDYx} are input signals asserted by the 'C4x receiving data and are asynchronous with respect to the H1 clock of the sending 'C4x. After token exchange, \overline{CREQx} and \overline{CRDYx} become outputs, and \overline{CSTRBx} , \overline{CACKx} , and $CxDx$ become inputs.

Figure 25. Communication-Token Transfer Sequence, Output to an Input Port [$P = t_{c(H)}$]

TMS320C40 DIGITAL SIGNAL PROCESSOR

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timer pin timing (see Note 12 and Figure 26)

| NO. | | TMS320C40-40 TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|---|------------------------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{su}(TCLK-H1L)$ Setup time, TCLKx before H1 low | 10 | | 10 | | ns |
| 2 | $t_h(H1L-TCLK)$ Hold time, TCLKx after H1 low | 0 | | 0 | | ns |
| 3 | $t_d(H1H-TCLK)$ Delay time, TCLKx valid after H1 high | | 13 | | 13 | ns |

NOTE 12: Period and polarity of valid logic level are specified by contents of internal control registers.

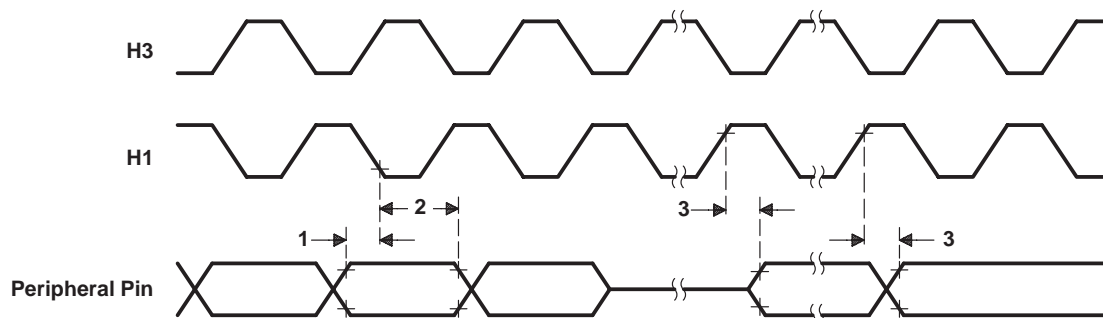


Figure 26. Timer Pin Timing Cycle

timing for IEEE-1149.1 test access port (see Figure 27)

| NO. | | TMS320C40-40 TMS320C40-50 | | TMS320C40-60 | | UNIT |
|-----|--|------------------------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | $t_{su}(TMS-TCKH)$ Setup time, TMS/TDI to TCK high | 10 | | 10 | | ns |
| 2 | $t_h(TCKH-TMS)$ Hold time, TMS/TDI from TCK high | 5 | | 5 | | ns |
| 3 | $t_d(TCKL-TDOV)$ Delay time, TCK low to TDO valid | 0 | 15 | 0 | 12 | ns |

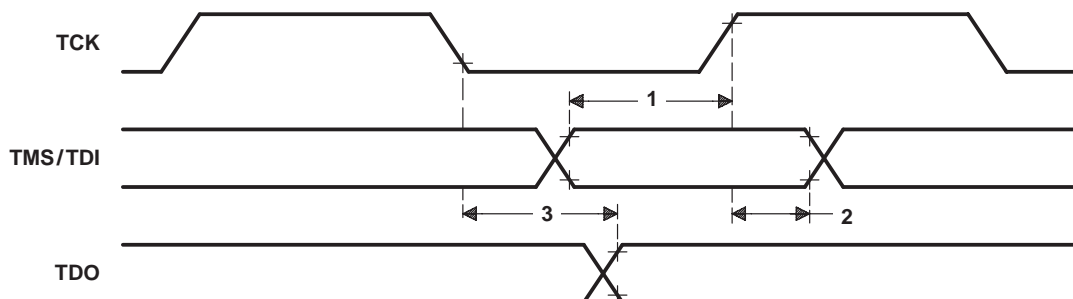


Figure 27. IEEE-1149.1 Test Access Port Timings

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|----------------------------|---------|
| TMS320C40GFL60 | NRND | CPGA | GF | 325 | 10 | Non-RoHS & Non-Green | AU | N / A for Pkg Type | | TMS320C40GFL60 @1991 TI | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TMS320C40 :

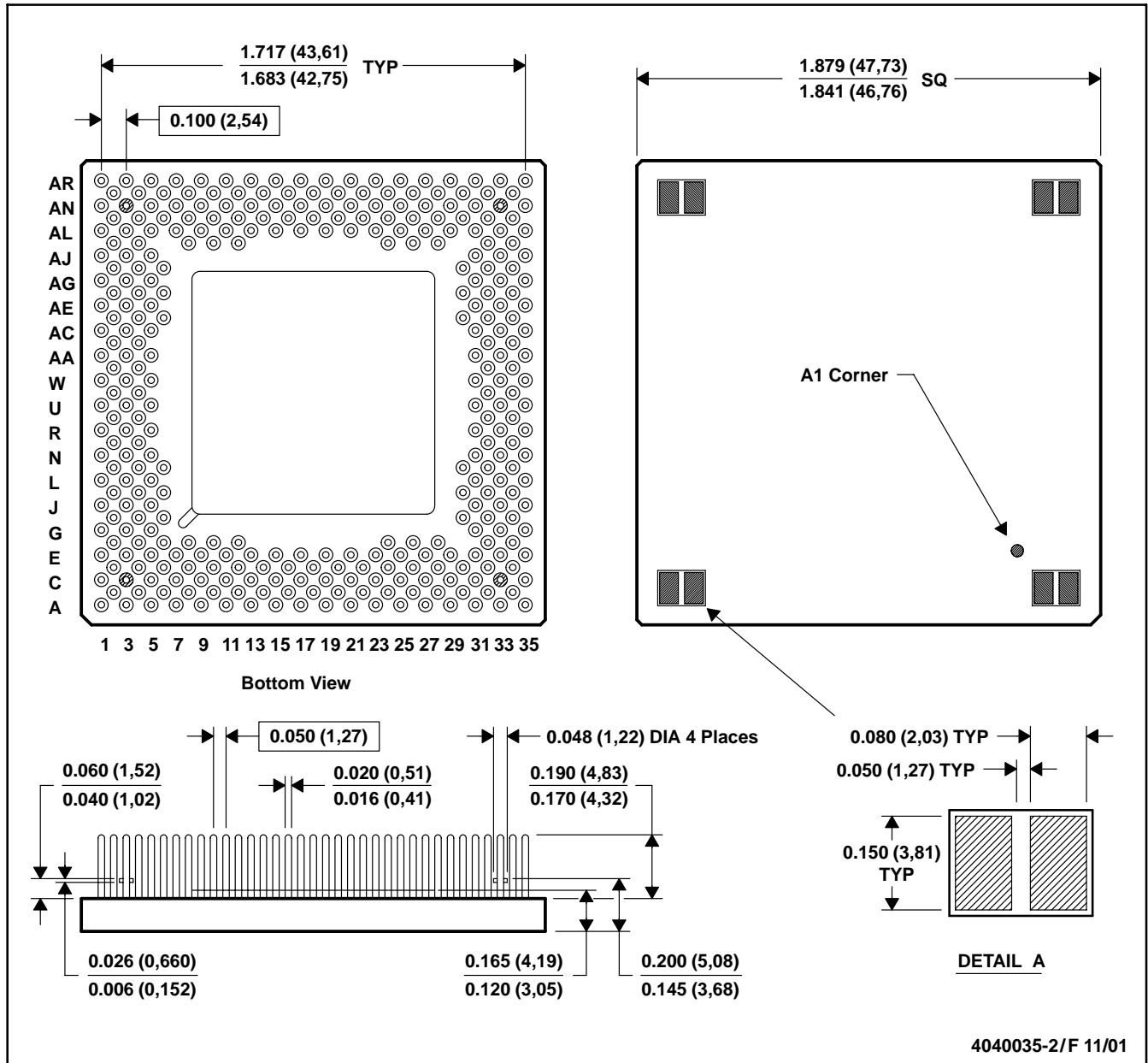
- Catalog : [SM320C40](#)
- Military : [SMJ320C40](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

GF (S-CPGA-P325)

CERAMIC PIN GRID ARRAY



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Index mark can appear on top or bottom, depending on package vendor.
 - D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edge of the ceramic.
 - E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
 - F. The pins can be gold-plated or solder-dipped.
 - G. Package thickness of 0.165 (4,19) / 0.120 (3,05) includes package body and lid.
 - H. Falls within JEDEC MO-128AK

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