TPLD801-Q1 Automotive Programmable Logic Device with 6-GPIO

1 Features

- Operating characteristics
  - Extended temperature range: -40°C to 125°C
  - Wide supply voltage range: 1.65V to 5.5V
  - Qualified for automotive applications
- Configurable macro-cells
  - 2-, 3-, and 4-bit lookup tables
  - D-type flip-flops and latches with and without reset/set option
  - 8-bit pipe delay
  - Counters and delay generator
  - Programmable deglitch filter or edge detector
  - Oscillator
- Flexible digital I/O features
  - All digital signals can be routed to any GPIO
  - Digital input modes: digital in with and without Schmitt-trigger, low-voltage digital in
  - Digital output modes: push-pull, open-drain NMOS, tri-state
- Development tools
  - InterConnect Studio
  - TPLD801-Q1 evaluation module
  - TPLD programming board

2 Applications

- Factory automation and control
- Communications equipment
- Retail automation and payment
- Test and measurement
- Pro audio, video, and signage
- Personal electronics
- Automotive

3 Description

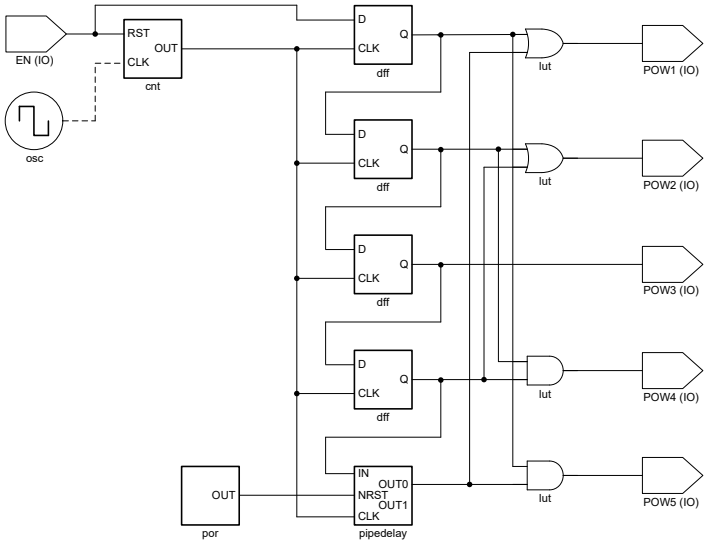
The TPLD801-Q1 is part of the TI programmable logic device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic, and analog blocks. TPLD provides a fully integrated, low power solution to implement common system functions, such as timing delays, voltage monitors, system resets, power sequencers, I/O expanders, and more. This device features configurable I/O structures that extends compatibility within mixed-signal environments, reducing the number of discrete components required.

System designers can create circuits and configure the macro-cells, I/O pins, and interconnections by temporarily emulating the non-volatile memory or by permanently programming the one-time programmable (OTP) through InterConnect Studio. The TPLD801-Q1 is supported by hardware and software ecosystem with application notes, reference designs and design examples. Visit ti.com for more information and access to design tools.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPLD801-Q1	DRL (SOT-5X3, 8)	2.1mm × 1.6mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Simplified Application

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4 Pin Configuration and Functions

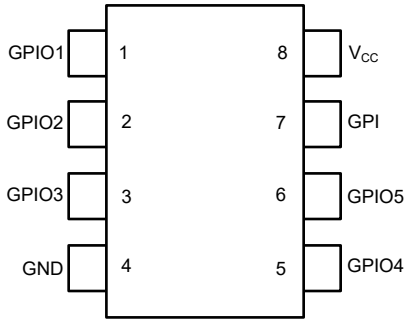

Figure 4-1. DRL Package, 8-pin SOT-5X3 (Top View)

Table 4-1. Pin Functions

PIN			DESCRIPTION	
NAME	NO.	TYPE(1)	Primary function	Secondary function (if any)
GPIO1	1	I/O	General-purpose I/O.	External OSC IN
GPIO2	2	I/O	General-purpose I/O.	
GPIO3	3	I/O	General-purpose I/O with output enable (OE). (3)	
GND	4	P	Ground.	
GPIO4	5	I/O	General-purpose I/O.	
GPIO5	6	I/O	General-purpose I/O.	
GPI	7	I	General purpose input.(2)	
VCC	8	P	Positive supply.	

(1) P = power, I/O = input/output, I = Input
(2) The general-purpose input (GPI) pin will sustain a high-voltage (VPP) during programming. Take special precaution with peripherals connected to this pin if performing in-system programming.
(3) The output enable (OE) connection is available through the connection mux and can be configured in InterConnect Studio.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage on V_{CC} relative to GND		-0.5	7	V
V_I	Input voltage		-0.5	V_{CC} + 0.5	V
V_O	Output voltage		-0.5	V_{CC} + 0.5	V
I_{IOK}	Input-output clamp current	V_{IO} < 0 or V_{IO} > V_{CC}	-50	50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	-50	50	mA
I_{DC}	Maximum average or DC current (through each pin)	Push-pull 1X		12	mA
		Push-pull 2X		17	
		Open-drain NMOS 1X		18	
		Open-drain NMOS 2X		28	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC specification JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			V_{CC}	MIN	MAX	UNIT
V_{CC}	Supply voltage			1.65	5.5	V
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
V_{IH}	High-level input voltage	Logic input	1.65V to 5.5V	0.53 × V_{CC}		V
		Low-voltage logic input	1.8V ± 0.15V	0.90		
			3.3V ± 0.3V	1.08		
			5V ± 0.5V	1.23		
V_{IL}	Low-level input voltage	Logic input	1.65V to 5.5V		0.36 × V_{CC}	V
		Low-voltage logic input	1.8V ± 0.15V		0.46	
			3.3V ± 0.3V		0.63	
			5V ± 0.5V		0.74	
T_A	Ambient temperature			–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPLD801-Q1 DRL (SOT-5X3) 8-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Supply and Power-on Reset								
V_{PORR}	Power-on reset voltage, V_{CC} rising		$V_I = V_{CC}$ or GND, $I_O = 0$	1.65V to 5.5V	1.04	1.30	1.50	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		$V_I = V_{CC}$ or GND, $I_O = 0$	1.65V to 5.5V	0.98	1.17	1.33	V
t_{SU}	Startup time		from V_{CC} rising past V_{PORR}	1.65V to 5.5V		270		µs
V_{PP}	Programming voltage			1.65V to 5.5V	7.5	8	8.5	V
Digital IO								
V_{T+}	Positive-going input threshold voltage	Logic Input with Schmitt Trigger		1.8V ± 0.15V	0.92		1.29	V
				3.3V ± 0.3V	1.55		2.17	
				5V ± 0.5V	2.21		3.19	
V_{T-}	Negative-going input threshold voltage	Logic Input with Schmitt Trigger		1.8V ± 0.15V	0.56		0.96	V
				3.3V ± 0.3V	1.10		1.79	
				5V ± 0.5V	1.63		2.70	
V_{HYS}	Schmitt trigger hysteresis ($V_{T+} - V_{T-}$)	Logic Input with Schmitt Trigger		1.8V ± 0.15V	0.23		0.49	V
				3.3V ± 0.3V	0.33		0.54	
				5V ± 0.5V	0.42		0.66	
V_{OH}	High-level output voltage	Push-pull 1X or Open-drain PMOS 1X	I_{OH} = -100µA	1.8V ± 0.15V	1.626			V
		Push-pull 2X or Open-drain PMOS 2X			1.636			
V_{OH}	High-level output voltage	Push-pull 1X or Open-drain PMOS 1X	I_{OH} = -3mA	3.3V ± 0.3V	2.710			V
		Push-pull 2X or Open-drain PMOS 2X			2.820			
V_{OH}	High-level output voltage	Push-pull 1X or Open-drain PMOS 1X	I_{OH} = -5mA	5V ± 0.5V	4.120			V
		Push-pull 2X or Open-drain PMOS 2X			4.240			
V_{OL}	Low-level output voltage	Push-pull 1X	I_{OL} = 100µA	1.8V ± 0.15V			0.009	V
		Push-pull 2X					0.005	
		Open-drain NMOS 1X					0.009	
		Open-drain NMOS 2X					0.005	

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over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	Push-pull 1X	I_{OL} = 3mA	3.3V ± 0.3V			0.118	V
		Push-pull 2X					0.076	
		Open-drain NMOS 1X					0.118	
		Open-drain NMOS 2X					0.076	
V_{OL}	Low-level output voltage	Push-pull 1X	I_{OL} = 5mA	5V ± 0.5V			0.139	V
		Push-pull 2X					0.096	
		Open-drain NMOS 1X					0.139	
		Open-drain NMOS 2X					0.096	
I_I	Input leakage current	All pins	V_I = V_{CC}	1.65V to 5.5V			±1	µA
			V_I = GND	1.65V to 5.5V			±1	
$R_{pu(int)}$	Internal pull-up resistance					1		MΩ
						100		kΩ
						10		kΩ
$R_{pd(int)}$	Internal pull-down resistance					1		MΩ
						100		kΩ
						10		kΩ
$R_{pd(int)\_GPI}$	Internal pull-down resistance - GPI/IN0					1		MΩ
						100		kΩ
						15		kΩ

5.6 Supply Current Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8V ± 0.15V			V_{CC} = 3.3V ± 0.3V			V_{CC} = 5V ± 0.5V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Standby													
I_{CC}	Quiescent current		Inputs = static, Outputs = open, I_O = 0, OSC powered off		1.04			1.10			0.95		µA
Oscillator													
I_{CC}	Quiescent current	OSC0 enabled: 25kHz	Predivide = 1		6.33			8.23			12.67		µA
			Predivide = 8		6.56			8.23			12.44		
I_{CC}	Quiescent current	OSC0 enabled: 2MHz	Predivide = 1		61.05			70.08			88.78		µA
			Predivide = 8		48.86			57.90			76.13		

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5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			V_{CC}	MIN	TYP	MAX	UNIT
Digital IO							
t_{pd}	Delay	Digital input without Schmitt trigger to Push-pull output - Rising	1.8V ± 0.15V		46.9		ns
		Digital input without Schmitt trigger to Push-pull output - Falling			39.5		
		Digital input without Schmitt trigger to Push-pull output - Rising	3.3V ± 0.3V		27.3		
		Digital input without Schmitt trigger to Push-pull output - Falling			26.4		
		Digital input without Schmitt trigger to Push-pull output - Rising	5V ± 0.5V		22.3		
		Digital input without Schmitt trigger to Push-pull output - Falling			22.5		
t_{pd}	Delay	Digital input with Schmitt trigger to Push-pull output - Rising	1.8V ± 0.15V		50.8		ns
		Digital input with Schmitt trigger to Push-pull output - Falling			42.2		
		Digital input with Schmitt trigger to Push-pull output - Rising	3.3V ± 0.3V		29.7		
		Digital input with Schmitt trigger to Push-pull output - Falling			27.2		
		Digital input with Schmitt trigger to Push-pull output - Rising	5V ± 0.5V		24.2		
		Digital input with Schmitt trigger to Push-pull output - Falling			22.8		
t_{pd}	Delay	Low-voltage digital input to Push-pull output - Rising	1.8V ± 0.15V		45.6		ns
		Low-voltage digital input to Push-pull output - Falling			49.5		
		Low-voltage digital input to Push-pull output - Rising	3.3V ± 0.3V		25.4		
		Low-voltage digital input to Push-pull output - Falling			33.0		
		Low-voltage digital input to Push-pull output - Rising	5V ± 0.5V		19.6		
		Low-voltage digital input to Push-pull output - Falling			31.5		
t_{pd}	Delay	Digital input without Schmitt trigger to Open-drain NMOS output - Rising	1.8V ± 0.15V		57.0		ns
		Digital input without Schmitt trigger to Open-drain NMOS output - Falling			39.3		
		Digital input without Schmitt trigger to Open-drain NMOS output - Rising	3.3V ± 0.3V		47.8		
		Digital input without Schmitt trigger to Open-drain NMOS output - Falling			26.2		
		Digital input without Schmitt trigger to Open-drain NMOS output - Rising	5V ± 0.5V		38.2		
		Digital input without Schmitt trigger to Open-drain NMOS output - Falling			22.3		
t_{pd}	Delay	Output enable from pin, OE, Hi-Z to 1 - Rising	1.8V ± 0.15V		45.9		ns
			3.3V ± 0.3V		27.3		
			5V ± 0.5V		22.4		
t_{pd}	Delay	Output enable from pin, OE, Hi-Z to 0 - Falling	1.8V ± 0.15V		41.1		ns
			3.3V ± 0.3V		24.5		
			5V ± 0.5V		19.6		
Configurable Use Logic							

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over operating free-air temperature range (unless otherwise noted)

PARAMETER			V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Delay	2-bit LUT - Rising	1.8V ± 0.15V		1.16		ns
		2-bit LUT - Falling			1.31		
		2-bit LUT - Rising	3.3V ± 0.3V		1.16		
		2-bit LUT - Falling			1.31		
		2-bit LUT - Rising	5V ± 0.5V		1.16		
		2-bit LUT - Falling			1.31		
t_{pd}	Delay	3-bit LUT - Rising	1.8V ± 0.15V		1.04		ns
		3-bit LUT - Falling			1.26		
		3-bit LUT - Rising	3.3V ± 0.3V		1.04		
		3-bit LUT - Falling			1.26		
		3-bit LUT - Rising	5V ± 0.5V		1.04		
		3-bit LUT - Falling			1.26		
t_{pd}	Delay	4-bit LUT - Rising	1.8V ± 0.15V		1.62		ns
		4-bit LUT - Falling			1.99		
		4-bit LUT - Rising	3.3V ± 0.3V		1.62		
		4-bit LUT - Falling			1.99		
		4-bit LUT - Rising	5V ± 0.5V		1.62		
		4-bit LUT - Falling			1.99		
t_{pd}	Delay	Latch - Rising	1.8V ± 0.15V		1.32		ns
		Latch - Falling			1.34		
		Latch - Rising	3.3V ± 0.3V		1.32		
		Latch - Falling			1.34		
		Latch - Rising	5V ± 0.5V		1.32		
		Latch - Falling			1.34		
t_{pd}	Delay	Latch nRST/nSET - Rising	1.8V ± 0.15V		1.43		ns
		Latch nRST/nSET - Falling			1.46		
		Latch nRST/nSET - Rising	3.3V ± 0.3V		1.43		
		Latch nRST/nSET - Falling			1.46		
		Latch nRST/nSET - Rising	5V ± 0.5V		1.43		
		Latch nRST/nSET - Falling			1.46		
Counter/Delay							
t_{pd}	Delay	CNT/DLY - Rising	1.8V ± 0.15V		2.61		ns
		CNT/DLY - Falling			2.59		
		CNT/DLY - Rising	3.3V ± 0.3V		2.61		
		CNT/DLY - Falling			2.59		
		CNT/DLY - Rising	5V ± 0.5V		2.61		
		CNT/DLY - Falling			2.59		
Oscillator							
f_{err}	Oscillator frequency error	OSC0 25 kHz	1.8V ± 0.15V	-5		5	%
			3.3V ± 0.3V	-5		5	
			5V ± 0.5V	-5		5	
f_{err}	Oscillator frequency error	OSC0 2 MHz	1.8V ± 0.15V	-5		5	%
			3.3V ± 0.3V	-5		5	
			5V ± 0.5V	-5		5	

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over operating free-air temperature range (unless otherwise noted)

PARAMETER			V_{CC}	MIN	TYP	MAX	UNIT
t_{d_osc}	Oscillator startup delay	OSC0 25 kHz (Auto power on)	1.8V ± 0.15V		14.3		µs
			3.3V ± 0.3V		14.2		
			5V ± 0.5V		14.1		
t_{d_osc}	Oscillator startup delay	OSC0 2 MHz (Auto power on)	1.8V ± 0.15V		6.24		µs
			3.3V ± 0.3V		6.43		
			5V ± 0.5V		6.64		
t_{set_osc}	Oscillator startup settling time	OSC0 25 kHz (Auto power on)	1.8V ± 0.15V		1		µs
			3.3V ± 0.3V		1		
			5V ± 0.5V		1		
t_{set_osc}	Oscillator startup settling time	OSC0 2 MHz (Auto power on)	1.8V ± 0.15V		7		µs
			3.3V ± 0.3V		7		
			5V ± 0.5V		7		
t_{d_err}	Delay error	OSC (Forced power on)	1.65V to 5.5V	0		1	CLK cycle
Programmable Filter							
t_{pflt_pw}	Pulse width, 1 cell	PFLT mode: (any) edge detect, edge detect output	1.8V ± 0.15V		138.0		ns
			3.3V ± 0.3V		141.3		
			5V ± 0.5V		141.7		
t_{pflt_pw}	Pulse width, 2 cells	PFLT mode: (any) edge detect, edge detect output	1.8V ± 0.15V		232.6		ns
			3.3V ± 0.3V		236.0		
			5V ± 0.5V		236.5		
t_{pflt_pw}	Pulse width, 3 cells	PFLT mode: (any) edge detect, edge detect output	1.8V ± 0.15V		326.8		ns
			3.3V ± 0.3V		330.5		
			5V ± 0.5V		330.9		
t_{pflt_pw}	Pulse width, 4 cells	PFLT mode: (any) edge detect, edge detect output	1.8V ± 0.15V		420.9		ns
			3.3V ± 0.3V		424.7		
			5V ± 0.5V		425.0		
t_{pflt_pd}	Delay, any cells	PFLT mode: (any) edge detect, edge detect output	1.8V ± 0.15V		67.4		ns
			3.3V ± 0.3V		48.7		
			5V ± 0.5V		43.7		
t_{pflt_d}	Delay, 1 cell	PFLT mode: both edge delay (shared macrocell inputs)	1.8V ± 0.15V		208.4		ns
			3.3V ± 0.3V		191.5		
			5V ± 0.5V		186.9		
t_{pflt_d}	Delay, 2 cells	PFLT mode: both edge delay (shared macrocell inputs)	1.8V ± 0.15V		303.3		ns
			3.3V ± 0.3V		286.3		
			5V ± 0.5V		281.5		
t_{pflt_d}	Delay, 3 cells	PFLT mode: both edge delay (shared macrocell inputs)	1.8V ± 0.15V		397.7		ns
			3.3V ± 0.3V		380.6		
			5V ± 0.5V		375.9		
t_{pflt_d}	Delay, 4 cells	PFLT mode: both edge delay (shared macrocell inputs)	1.8V ± 0.15V		491.9		ns
			3.3V ± 0.3V		474.6		
			5V ± 0.5V		469.8		

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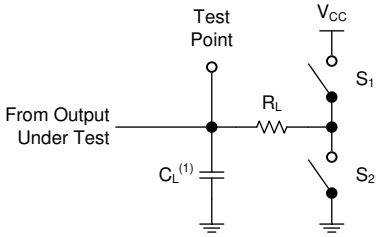
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5 ns.

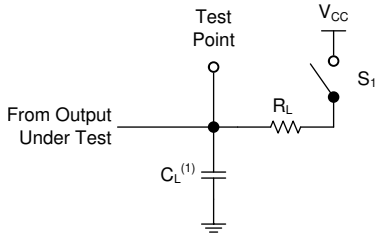
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



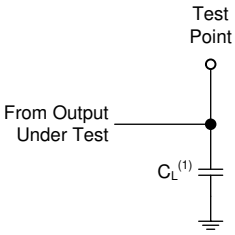
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 6-2. Load Circuit for Open-Drain Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 6-3. Load Circuit for Push-Pull Outputs

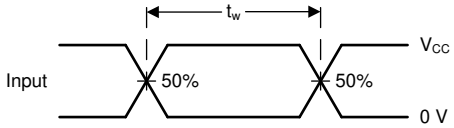


Figure 6-4. Voltage Waveforms, Pulse Duration

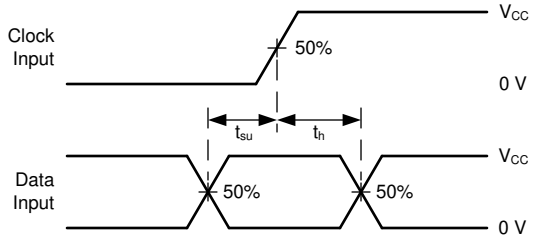
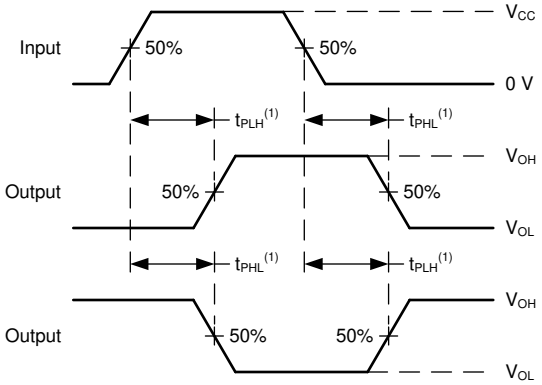


Figure 6-5. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-6. Voltage Waveforms Propagation Delays

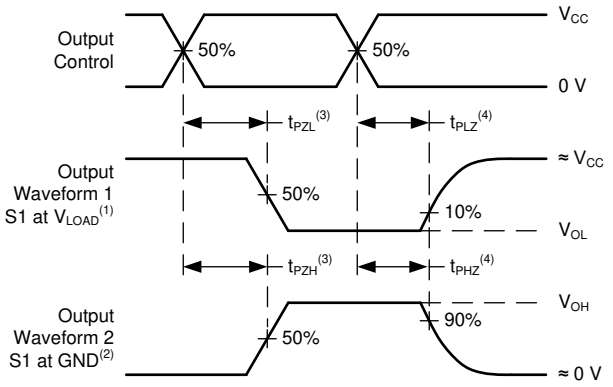
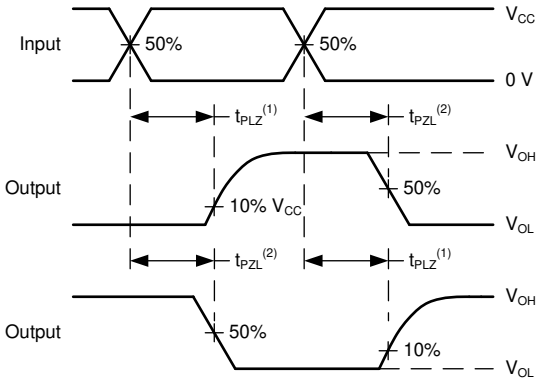
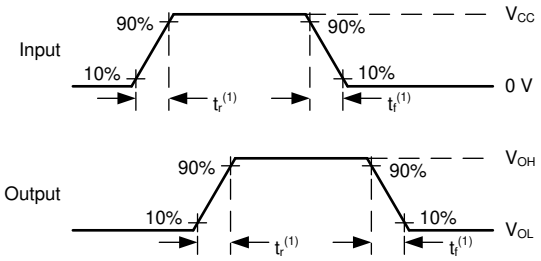


Figure 6-7. Voltage Waveforms Propagation Delays



(1) The greater between t_{PLZ} and t_{PZL} is the same as t_{pd}.

Figure 6-8. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-9. Voltage Waveforms, Input and Output Transition Times

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7 Detailed Description

7.1 Overview

The TPLD801-Q1 is part of the TI programmable logic device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic, and analog blocks to provide an integrated, compact, low power solution to implement common system functions.

The TPLD801-Q1 has one GPI and five GPIOs that can be configured as a digital input, digital output, or digital input/output.

The TPLD801-Q1 has a system of interconnects, further referred to as the connection mux, to configure the routing of internal macro-cells and I/O pins. Each connection mux input is hardwired to a specific digital macro-cell output, such as digital I/O and lookup tables. The connection mux allows each of the digital inputs to only connect to one output so that bus contention does not occur.

The TPLD801-Q1 features the following macro-cells:

- Configurable use logic blocks
  - Two 2-bit lookup tables (LUT)
  - Two 3-bit LUTs
  - Two 2-bit LUTs or D-type flip-flops (DFF)/latches
  - Two 3-bit LUTs or DFF/latches with reset/set option
  - One 3-bit LUT or pipe delay
  - One 4-bit LUT or 8-bit counter (CNT) or delay generator (DLY)
- Three 8-bit CNT/DLY
- One programmable deglitch filter (PFLT) or edge detector (EDET)
- One oscillator (OSC) to generate either a 25-kHz or 2-MHz clock

The InterConnect Studio software environment enables a simple drag-and-drop interface to build custom circuit designs and configure the macro-cells, I/O pins, and interconnections. In addition to circuit creation, InterConnect Studio has the ability to simulate digital and analog functionality to verify designs and provide a typical power consumption estimate. Once circuit designs are finalized, InterConnect Studio can temporarily emulate the design in the non-volatile memory or permanently program the one-time programmable (OTP). The OTP can be locked to prevent readback of its contents.

7.2 Functional Block Diagram

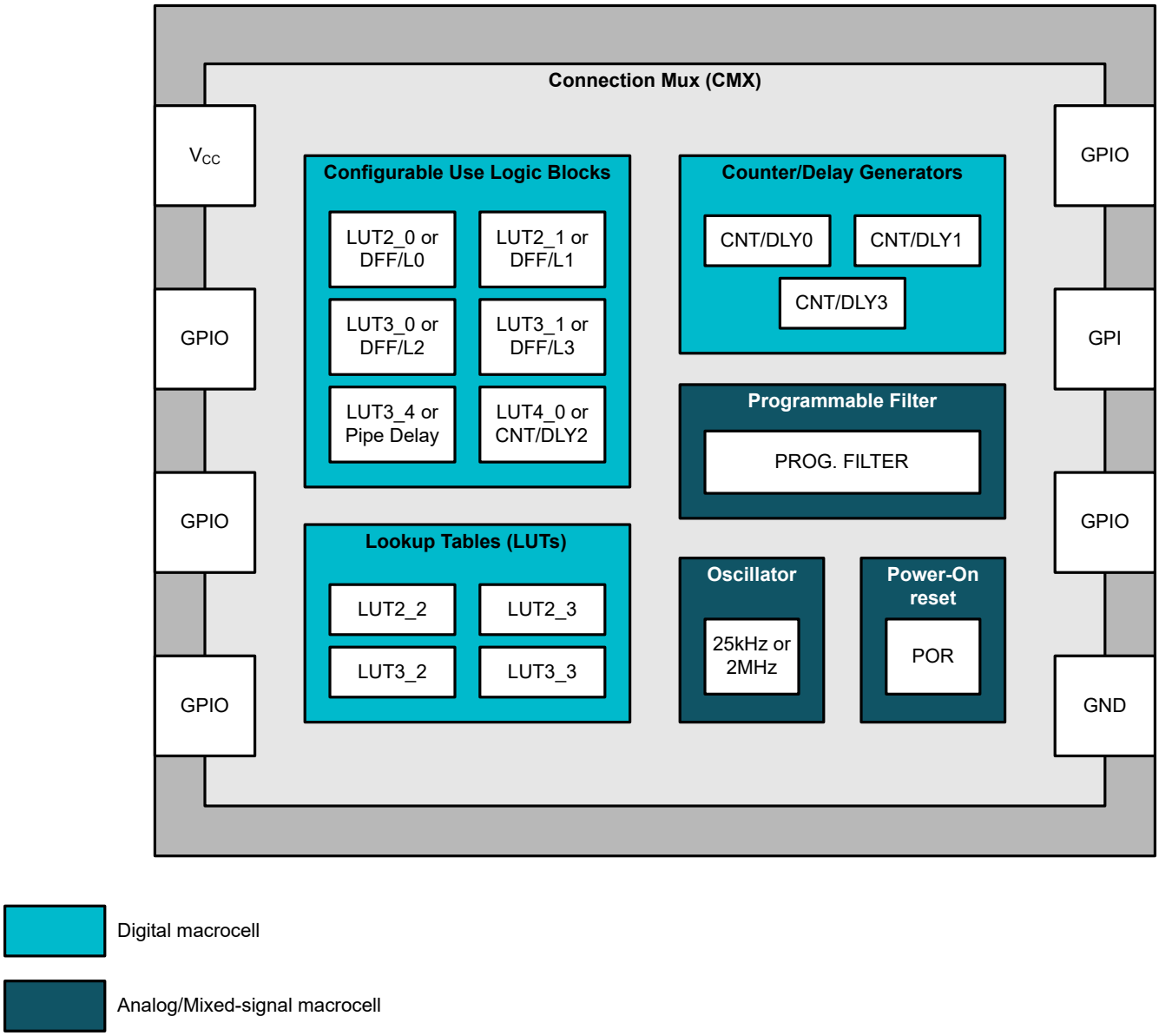

Figure 7-1. TPLD801-Q1 Functional Block Diagram

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7.3 Feature Description

7.3.1 I/O Pins

TPLD801-Q1 has one input and five multifunction I/O pins. GPIO pins can function as either a user defined input, output, or a special function.

Input modes: The following options are available when configuring pins as an input:

- Digital input without Schmitt-trigger
- Digital input with Schmitt-trigger
- Low-voltage digital input

The low-voltage digital input has lower V_{IH}/V_{IL} specifications than the digital input without Schmitt trigger. This allows for up-translation from any voltage domain lower than V_{CC} that meets the low-voltage digital input V_{IH} and V_{IL} specifications. The following pins also have the option to serve a special function:

- IO1: external clock input

Output modes: The following options are available with programmable drive strength when configuring pins as an output:

- 1x push-pull output
- 2x push-pull output
- 1x open-drain NMOS output
- 2x open-drain NMOS output
- 1x open-drain PMOS output
- 2x open-drain PMOS output

Pull-up/Pull-down Resistors: All I/O pins have the option of user-selectable resistors that can be connected to the pin structure. The selectable values on these resistors are 10kΩ, 100kΩ and 1MΩ. The internal resistors can be configured as either pull-up or pull-down. When designing in InterConnect Studio, any pin left unused in a design are configured with a 1MΩ pull-down by default. Furthermore, following a power-on event, all ports are in a Hi-Z state until the power-on reset sequence has completed.

Table 7-1. Pin Configuration Options

GPIO	IO selection	OE	IO options	Resistor	Resistor value (Ω)
IN0	PIN not used	—	—	Pull-Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Down	10k
					100k
					1M
NOTE: GPI/IN0 also has the option to reset the chip while powered on. Unlike POR, External Reset affects only GPI, LUTs, DLY, OSC, DFFs, Latches, Pipe Delay, Matrix, and GPO. NVM remains in its previous state. Users may select whether the External Reset is "Disabled", "Level sensitive", or "Edge triggered". When "Level sensitive" is selected, if the input is High, then the device is in reset mode where all internal devices are reset. When this pin goes Low, then the device will begin the reset power on sequence. When "Edge triggered" is selected, the edge detector can be configured to Rising edge or Falling edge, and an edge on GPI/IN0 resets the device and begins the reset power on sequence.					

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Table 7-1. Pin Configuration Options (continued)

GPIO	IO selection	OE	IO options	Resistor	Resistor value (Ω)
IO1, IO2, IO4, IO5	Pin not used	—	—	Pull Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Up	10k
					100k
					1M
				Pull-Down	10k
					100k
					1M
	Digital output	1	Push-pull (1X, 2X)	Floating	—
			Open-drain NMOS (1X, 2X) Open-drain PMOS (1X, 2X)	Floating	—
				Pull-Up	10k
					100k
					1M
				Pull-Down	10k
					100k
					1M
	Digital input/output	1	Open-drain NMOS (1X, 2X)	Floating	—
				Pull-Up	10k
					100k
					1M
				Pull-Down	10k
					100k
					1M

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Table 7-1. Pin Configuration Options (continued)

GPIO	IO selection	OE	IO options	Resistor	Resistor value (Ω)
IO3	Pin not used	—	—	Pull-Down	1M
	Digital input	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input	Floating	—
				Pull-Up	10k
					100k
					1M
				Pull-Down	10k
					100k
					1M
	Digital output	1/0	Push-pull (1X, 2X)	Floating	—
			Open-drain NMOS (1X, 2X) 3-state output (1X, 2X)	Floating	—
				Pull-Up	10k
					100k
					1M
				Pull-Down	10k
					100k
					1M
	Digital input/output	0	Digital in without Schmitt trigger Digital in with Schmitt trigger Low-voltage digital input)	Floating	—
				Pull-Up	10k
					100k
					1M
				Pull-Down	10k
					100k
					1M
		1	Push-pull (1X, 2X) Open-drain NMOS (1X, 2X)	Shared with above	

7.3.2 Connection Mux

The TPLD801-Q1 has a system of interconnects, referred to as the connection mux, to configure the routing of internal macro-cells and I/O pins. The connection mux has 32 inputs and 44 outputs. Each of the 32 inputs of the connection mux is hardwired to particular macro-cells, including I/O pins, LUTs, analog comparators, other digital resources, VCC, and GND. The input to a digital macro-cell uses a 5-bit register to select one of these 32 input lines.

7.3.3 Configurable Use Logic Blocks

Combinational logic is supported via lookup tables (LUTs) within the TPLD801-Q1 including two 2-bit LUTs and two 3-bit LUTs. Inputs and outputs for the combination function macro-cells are configured from the connection mux with specific logic functions being defined by the state of OTP bits.

The TPLD801-Q1 has seven combinational function blocks (macro-cells) that can serve more than one logic or timing function. In each case, they can serve as a Lookup Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these logic blocks:

- Two 2-bit LUTs
- Two 3-bit LUTs
- Two 2-bit LUTs or D-type flip-flops/latches
- Two 3-bit LUTs or D-type flip-flops/latches with reset/set option
- One 3-bit LUT or Pipe delay
- One 4-bit LUT or 8-bit Counter/delay generator

7.3.3.1 2-Bit LUT macro-cell

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection mux and produces a single output, which goes back into the connection mux.

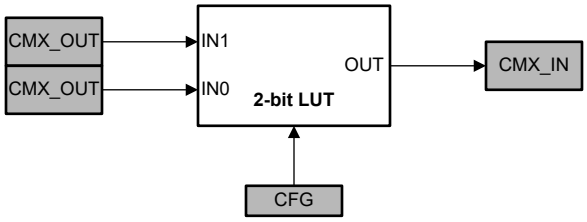

Figure 7-2. 2-bit LUT Block Diagram

These LUTs can be configured to any 2-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-2 shows the truth table for a 2-bit LUT.

Table 7-2. 2-bit LUT Truth Table

IN1	IN0	OUT
0	0	User defined
0	1	
1	0	
1	1	

Each 2-bit LUT has 4 bits in the OTP to define their output function.

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7.3.3.2 3-Bit LUT macro-cell

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection mux and produces a single output, which goes back into the connection mux.

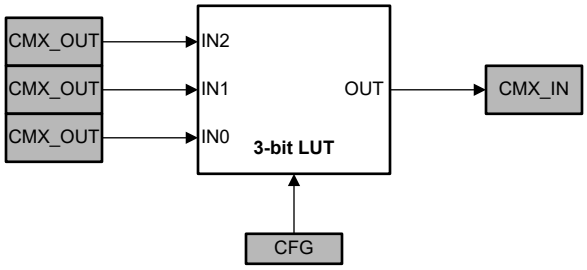

Figure 7-3. 3-bit LUT Block Diagram

These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-3 shows the truth tables for a 3-bit LUT.

Table 7-3. 3-bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	User defined
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Each 3-bit LUT has 8 bits in the OTP to define their output function.

7.3.3.3 2-Bit LUT or D Flip-Flop/Latch macro-cell

This configurable use logic block can serve as either a 2-bit LUT, or as a D flip-flop or latch.

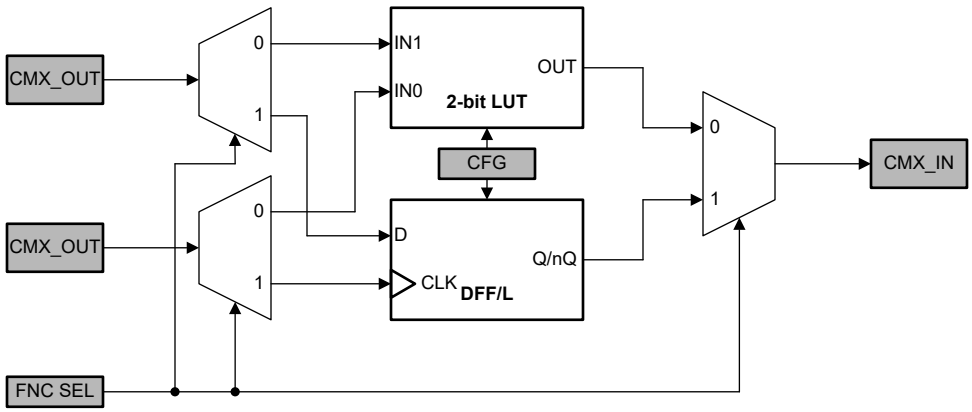

Figure 7-4. 2-bit LUT or DFF/Latch Block Diagram

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection mux and produces a single output, which goes back into the connection mux. These LUTs can be configured to any

2-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-4 shows the truth table for a 2-bit LUT.

Table 7-4. 2-bit LUT Truth Table

IN1	IN0	OUT
0	0	User defined
0	1	
1	0	
1	1	

Each 2-bit LUT has 4 bits in the OTP to define their output function.

When used to implement a sequential logic element, the two input signals from the connection mux go to the data (D) and clock (CLK) inputs of the flip-flop or latch, with the output going back to the connection mux. This macro-cell has initial state parameters, as well as clock and output polarity parameters.

The operation of the D flip-flop/latch will follow the functional descriptions below:

- The clock polarity is configurable and can be set to non-inverted (CLKPOL = 0, CLK) or inverted (CLKPOL = 1, nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q will not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is Low).
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 7-5 and Table 7-6 show the truth tables for the D flip-flop and D latch, respectively.

Table 7-5. D Flip-Flop Truth Table

CLKPOL	CLK	D	Q	nQ
0	↓	0	Q_0	nQ_0
	↑	0	0	1
	↓	1	Q_0	nQ_0
	↑	1	1	0
1	↓	0	0	1
	↑	0	Q_0	nQ_0
	↓	1	1	0
	↑	1	Q_0	nQ_0

Table 7-6. D Latch Truth Table

CLKPOL	CLK	D	Q	nQ
0	0	0	0	1
	1	0	Q_0	nQ_0
	0	1	1	0
	1	1	Q_0	nQ_0

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Table 7-6. D Latch Truth Table (continued)

CLKPOL	CLK	D	Q	nQ
1	0	0	Q_0	nQ_0
	1	0	0	1
	0	1	Q_0	nQ_0
	1	1	1	0

7.3.3.4 3-Bit LUT or D Flip-Flop/Latch with Set/Reset macro-cell

This configurable use logic blocks can serve as either a 3-bit LUT, or as a D flip-flop or latch with a reset or set.

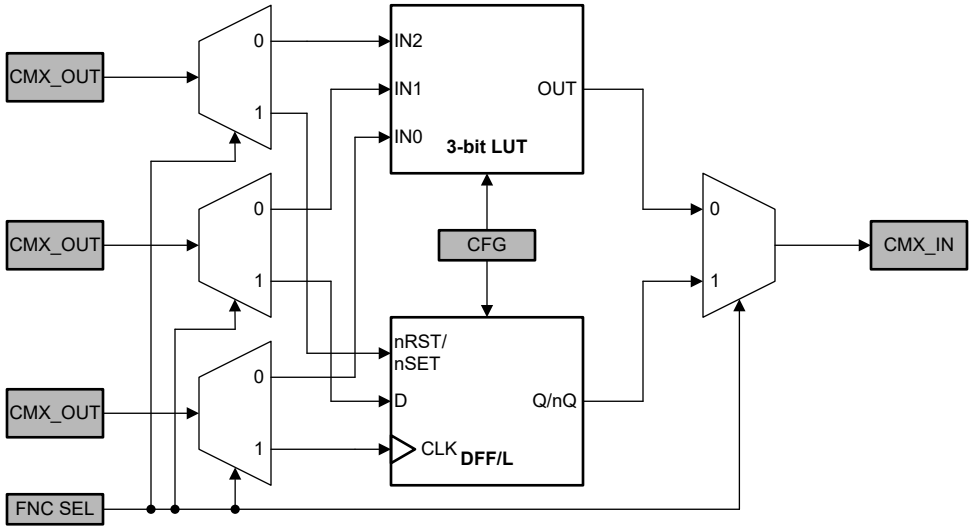

Figure 7-5. 3-bit LUT or DFF/Latch with nRST/nSET Block Diagram

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection mux and produces a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-7 shows the truth table for a 3-bit LUT.

Table 7-7. 3-bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	User defined
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Each 3-bit LUT has 8 bits in the OTP to define their output function.

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When used to implement a sequential logic element, the three input signals from the connection mux go to the data (D), clock (CLK), and reset/set (nRST/nSET) inputs for the flip-flop or latch, with the output going back to the connection mux. This macro-cell has initial state, clock polarity, reset/set polarity, and output polarity parameters.

The operation of the D flip-flop/latch will follow the function descriptions below:

- The clock polarity is configurable and can be set to non-inverted (CLKPOL = 0, CLK) or inverted (CLKPOL = 1, nCLK).
  - DFF with CLK: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
  - DFF with nCLK: CLK is falling edge triggered, then Q = D; otherwise Q will not change.
  - Latch with CLK: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).
  - Latch with nCLK: when CLK is High, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is Low).
- These DFF/latches have an option for an active-low reset or set.
  - nRST: when the input is high, the DFF/latch is in normal operation; and when low, Q is reset to 0.
  - nSET: when the input is high, the DFF/latch is in normal operation; and when low, Q is set to 1.
- If reset/set is not desired, users may tie this input to V_{CC} or another constant high source.
- The output polarity is configurable and can be set to non-inverted (Q) or inverted (nQ).

Table 7-8 and Table 7-9 show the truth tables for the D flip-flop and D latch with reset/set, respectively.

Table 7-8. D Flip-Flop with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	Q_0	nQ_0
			↑	0	0	1
			↓	1	Q_0	nQ_0
			↑	1	1	0
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		↓	0	0	1
			↑	0	Q_0	nQ_0
			↓	1	1	0
			↑	1	Q_0	nQ_0

Table 7-9. D Latch with nRST/nSET Truth Table

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	0	X	X	0	1
—	0		X	X	1	0
1	1		0	0	0	1
			1	0	Q_0	nQ_0
			0	1	1	0
			1	1	Q_0	nQ_0

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Table 7-9. D Latch with nRST/nSET Truth Table (continued)

nRST	nSET	CLKPOL	CLK	D	Q	nQ
0	—	1	X	X	0	1
—	0		X	X	1	0
1	1		0	0	Q_0	nQ_0
			1	0	0	1
			0	1	Q_0	nQ_0
			1	1	1	0

7.3.3.5 3-Bit LUT or Pipe Delay macro-cell

This macro-cell can serve as either a 3-bit LUT or as a pipe delay.

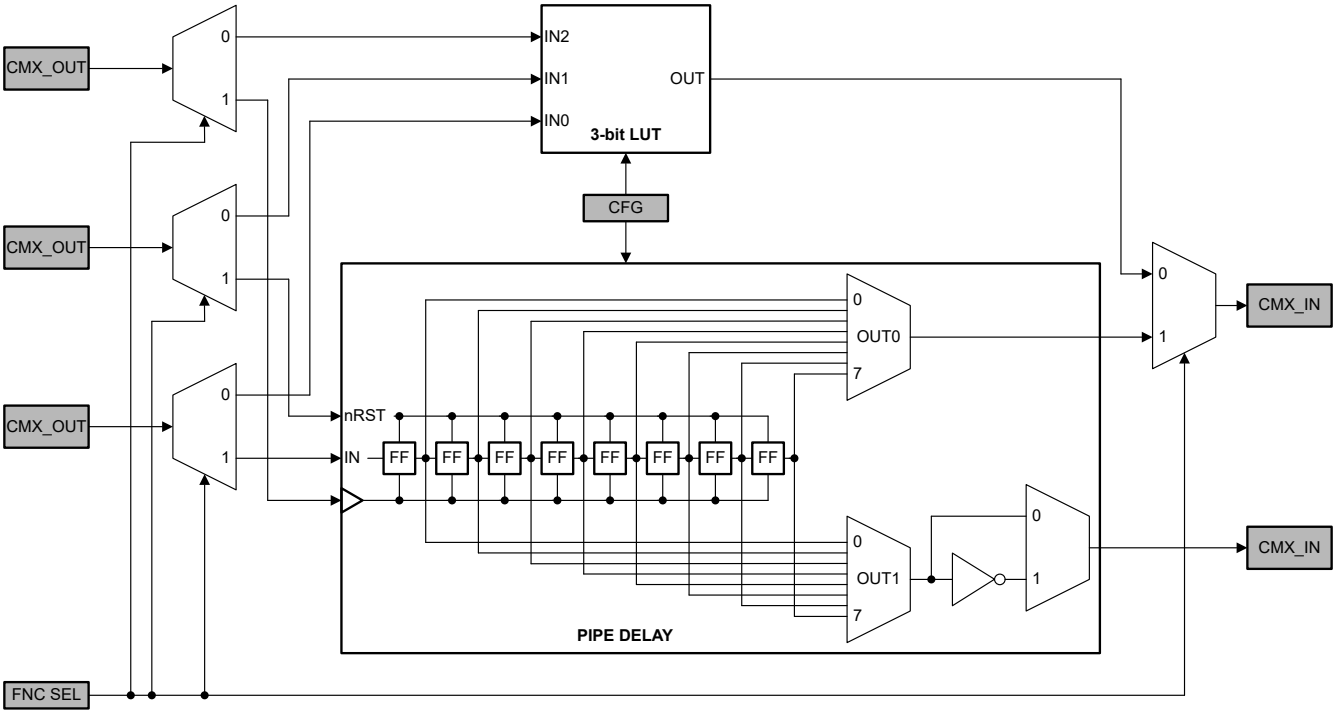

Figure 7-6. 3-bit LUT or Pipe delay block diagram

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection mux and produces a single output, which goes back into the connection mux. These LUTs can be configured to any 3-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-10 shows the truth table for a 3-bit LUT.

Table 7-10. 3-bit LUT Truth Table

IN2	IN1	IN0	OUT
0	0	0	User defined
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Each 3-bit LUT has 8 bits in the OTP to define their output function.

When used to implement a pipe delay, the three input signals from the connection mux go to the delay input (IN), clock (CLK), and reset (nRST) inputs for the flip-flop or latch, with two outputs going back to the connection mux. With this macro-cell, users can select the number of delay stages per output (from 1 to 8) and the output polarity for OUT1.

The pipe delay is an 8-stage delay composed of 8 DFFs. The DFF cells are tied in series where the output of each delay cell goes to the next DFF cell. There are delay output points for each set of the OUT0 and OUT1 outputs to a mux that is used to control the selection of the amount of delay for each pipe delay output.

For normal pipe delay functionality, the nRST input should be high. If nRST input is low, the pipe delay macro-cell is in a reset state and all outputs are low.

Figure 7-7 shows an example of the pipe delay macro-cell with 2 stages of delay selected.

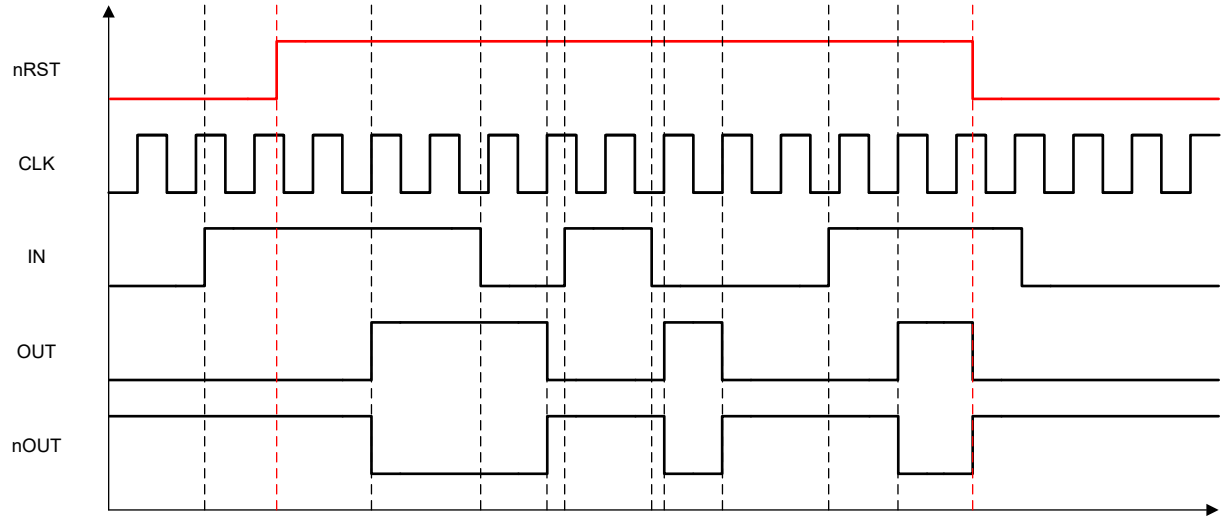

Figure 7-7. Pipe Delay Macro-Cell Timing Example (Delay = 2)

7.3.3.6 4-Bit LUT or 8-Bit Counter/Delay macro-cell

This macro-cell can serve as either a 4-bit LUT or as a counter/delay generator (CNT/DLY).

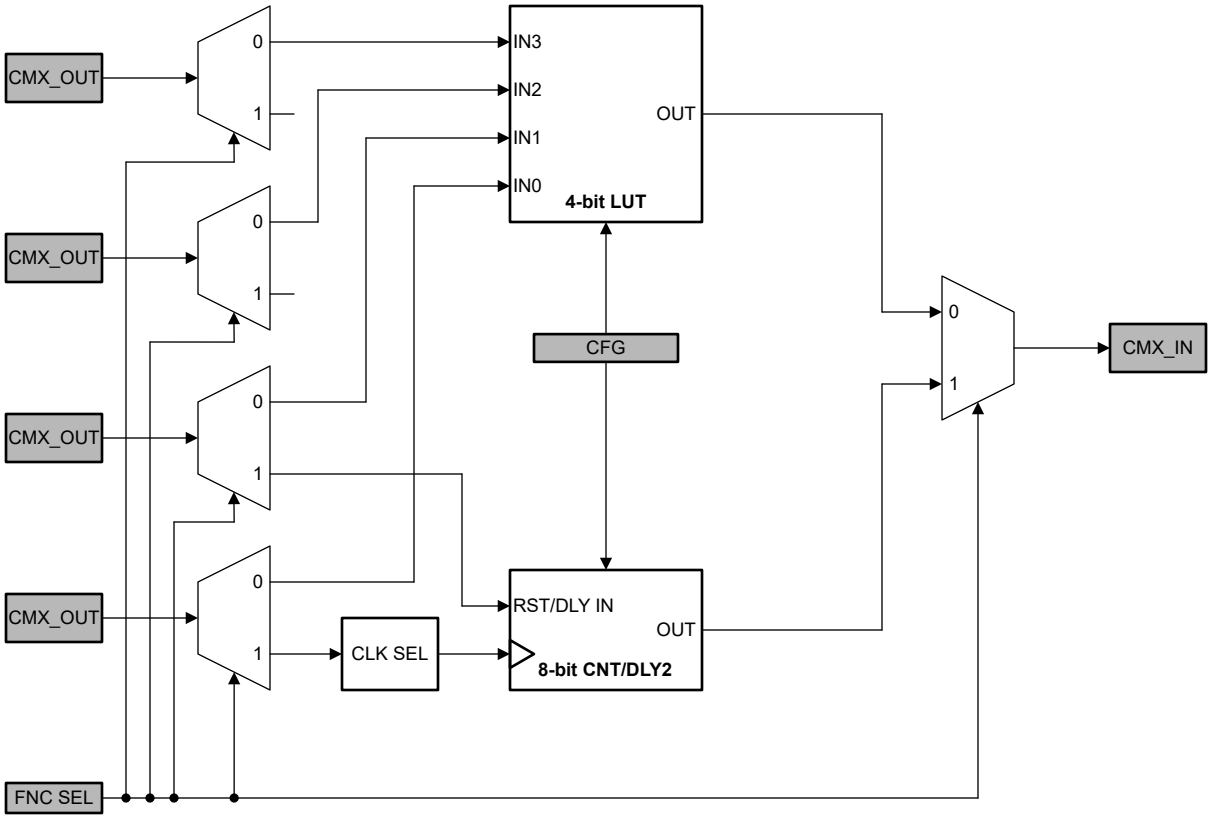

Figure 7-8. 4-bit LUT or 8-bit CNT/DLY Block Diagram

When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection mux and produces a single output, which goes back into the connection mux. This LUT can be configured to any 4-input user defined function, including the following standard digital logic functions: AND, NAND, OR, NOR, XOR, XNOR, INV.

Table 7-11 shows the truth table for a 4-bit LUT.

Table 7-11. 4-bit LUT Truth Table

IN3	IN2	IN1	IN0	OUT
0	0	0	0	User defined
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Each 4-bit LUT has 16 bits in the OTP to define their output function.

When used to implement 8-bit counter/delay function, the two input signals from the connection mux go to the clock (CLK) and reset (RST/DLY IN) for the counter/delay macro-cell, with the output going back to the connection mux. As a counter, the macro-cell counts to the given data value and generates a pulse when it reaches the set value or is reset. As a delay, it postpones rising and/or falling edges for the duration that is a function of the register value.

For more information on CNT/DLY macro-cell, see Section 7.3.4.

7.3.4 8-Bit Counters and Delay Generators (CNT/DLY)

The counters/delay generators are 8-bit, supporting counter data values from 1 to 255. For flexibility, the clock source for each of these macro-cells can be configured as the internal oscillator, a divided clock derived from an oscillator (OSC/4, /12, /24, /64, /4096), or an external clock source coming from the connection mux. There is also the option to chain from the output of the previous CNT/DLY macro-cell to implement longer counter/delay circuits. Note that the counter/delay macro-cell is rising edge triggered, that is the counter will increment/decrement on rising clock edges.

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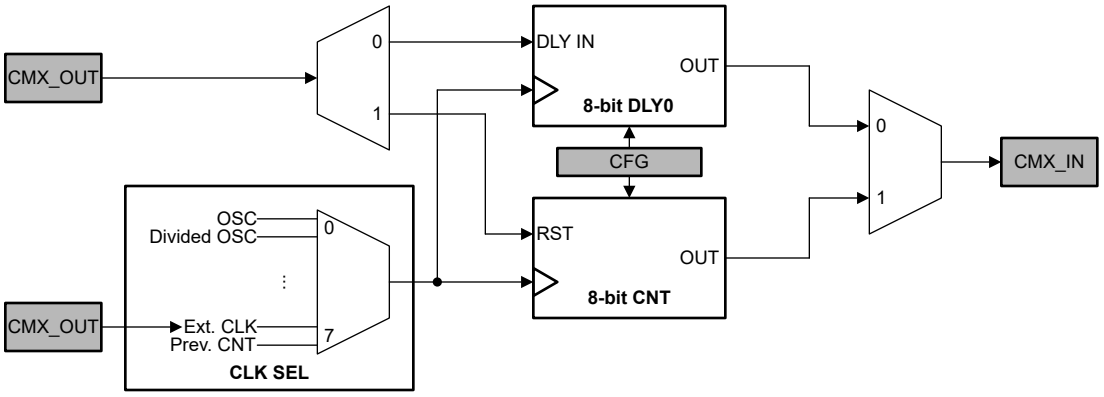


Figure 7-9. CNT/DLY Block Diagram

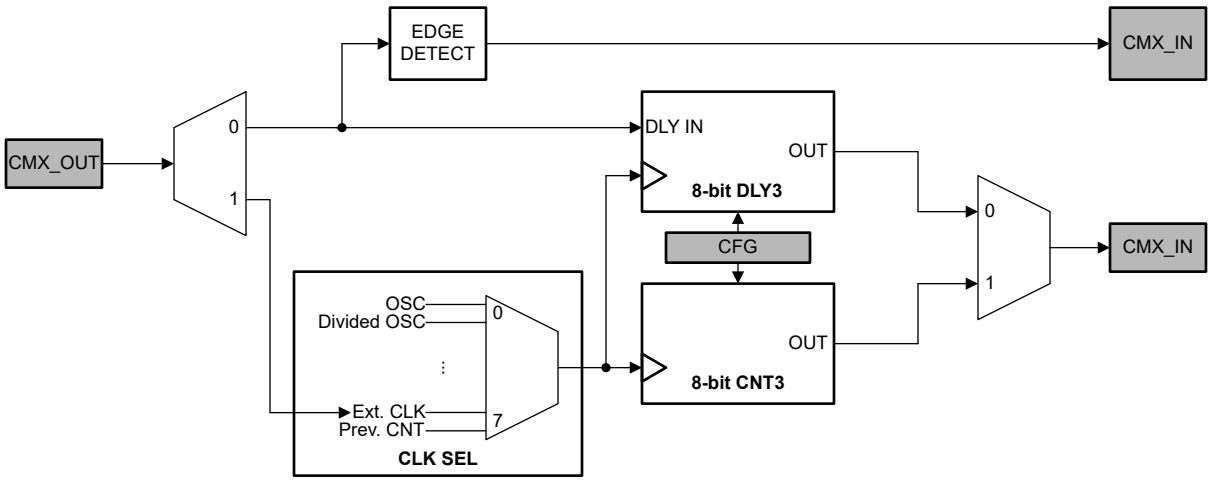


Figure 7-10. CNT/DLY3 Block Diagram

As a counter/delay (CNT/DLY) macro-cell, users may select from the following modes: delay, counter.

DLY3 also has an optional edge detector that will generate a short pulse on the specified edge in addition to the delayed output.

7.3.4.1 Delay Mode

When configured as a Delay generator (DLY), this macro-cell delays the input based on counter DATA and CLK input frequency and postpones rising and/or falling edges. The edge on which to delay is selected by the Edge select parameter and can be configured as:

- **Rising**: only delay on rising edges of IN.
- **Falling**: only delay on falling edges of IN.
- **Both**: delay on both rising and falling edges of IN.

For delay applications, it is recommended to use larger counter data values for less error. If an input pulse width is shorter than the specified delay time, the pulse will be filtered out. This feature can be useful for deglitching.

If the on-chip oscillator is used, a delay error or offset is introduced depending on whether the OSC is set to "forced power on" or "auto power on". An additional 2 clock cycles are included in the delay calculation for clock synchronization, but there is an option to bypass the clock sync.

The delay time is calculated by DELAY = (DATA + (t_{d_err} or t_{d_os}) + 2)/f_{CLK}.

When the OSC is set to "auto power on" and DLY macro-cells are triggered subsequently before the previous output is present, the OSC will continue to clock and the DLY will begin on the next rising edge. Thus, the subsequent delays can be calculated as if the OSC were set to "forced power on".

Figure 7-11 shows an example of the Delay macro-cell operation set to both edge delay and data = 1.

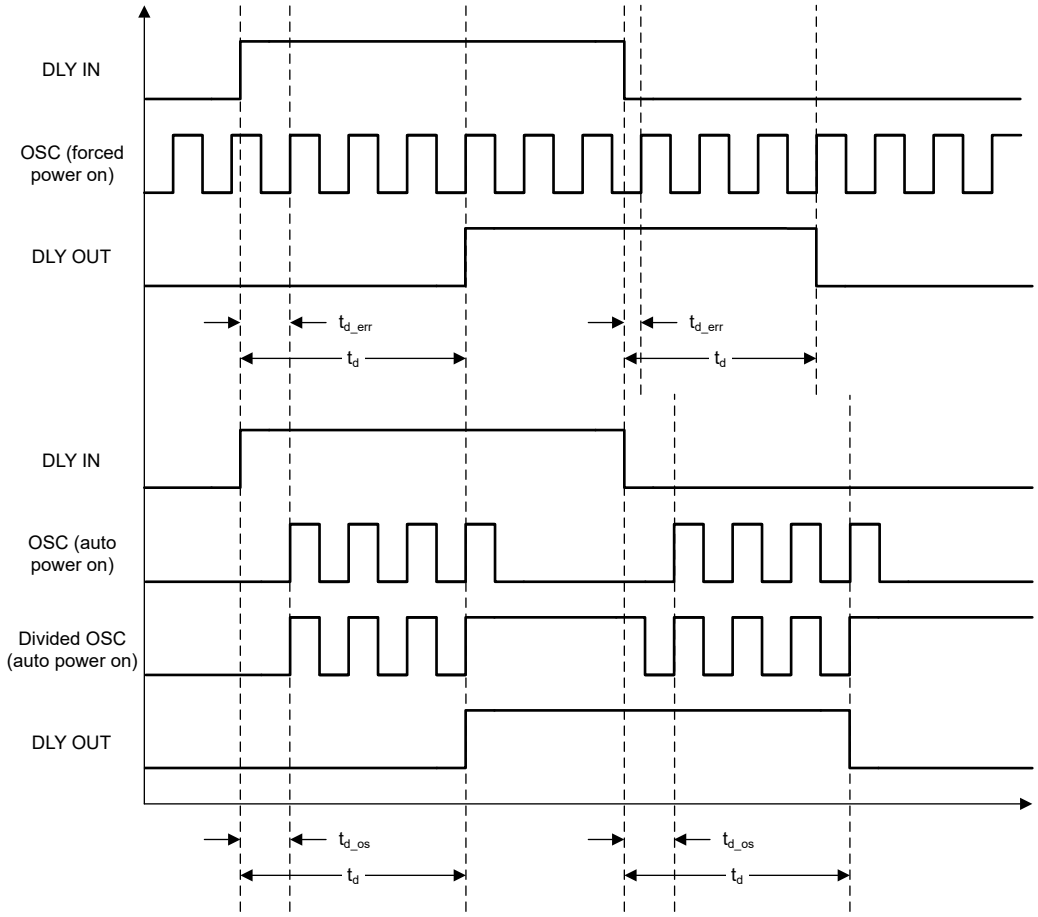


Figure 7-11. Delay output timing example (Both edge delay and DATA = 1)

Figure 7-12 shows an example timing of two different Delay macro-cells triggered consecutively with the OSC set to "auto power on".

ADVANCE INFORMATION

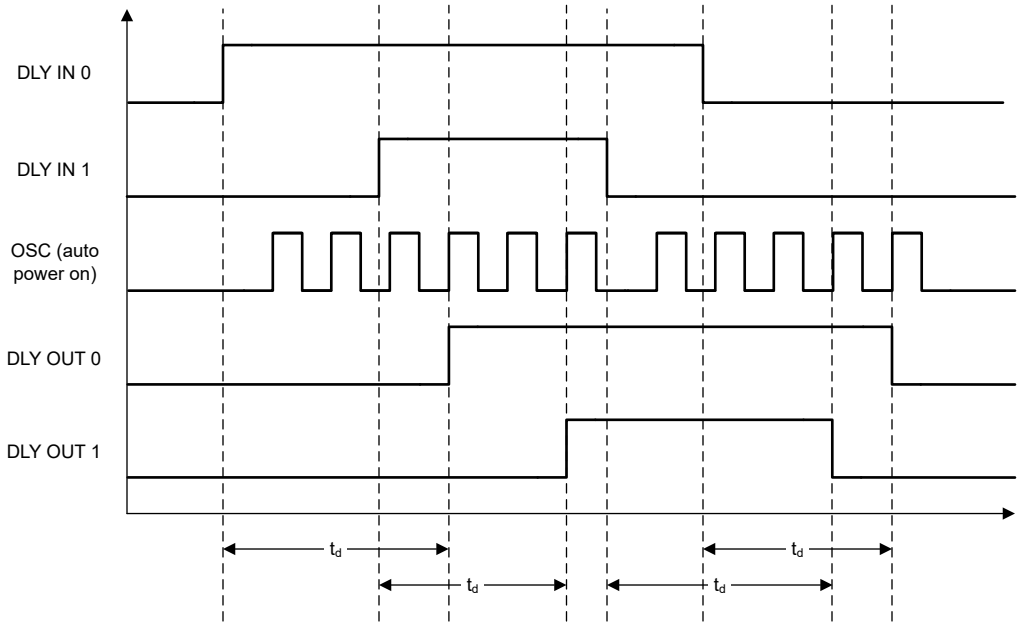


Figure 7-12. Delay output timing example (2 Delay macro-cells, Both edge delay, DATA = 1, OSC power = auto)

7.3.4.2 Reset Counter Mode

When configured as a Counter (CNT) and a valid edge appears on the IN input, this macro-cells resets the internal counter to 0 and begins counting down from DATA on the next rising clock edge. Then, the macro-cell outputs a pulse for the duration of one CLK period when the count reaches 0 and wrap around to the value in DATA. The counter will continually operate until another reset is recevied. The edge on which the Counter is reset is determined by the Edge select parameter and can be configured as:

- **Rising**: only rising edges of IN reset the counter.
- **Falling**: only falling edges of IN reset the counter.
- **Both**: both rising and falling edges of IN reset the counter.
- **High Level Reset**: the counter is reset to 0 whenever IN is High; after reset, the counter output stays Low until the next rising CLK edge, then operates normally.

The counter time is calculated by COUNT = (DATA + 1)/f_{CLK}. After a reset, an additional 2 clock cycles is added for clock synchronization, but there is an option to bypass the clock sync.

Note

Counters are initialized with DATA = 0 after POR.

Figure 7-13 and Figure 7-14 show examples of Counter output timing diagrams with respect to the Edge select parameter with DATA = 1 and DATA = 3, respectively.

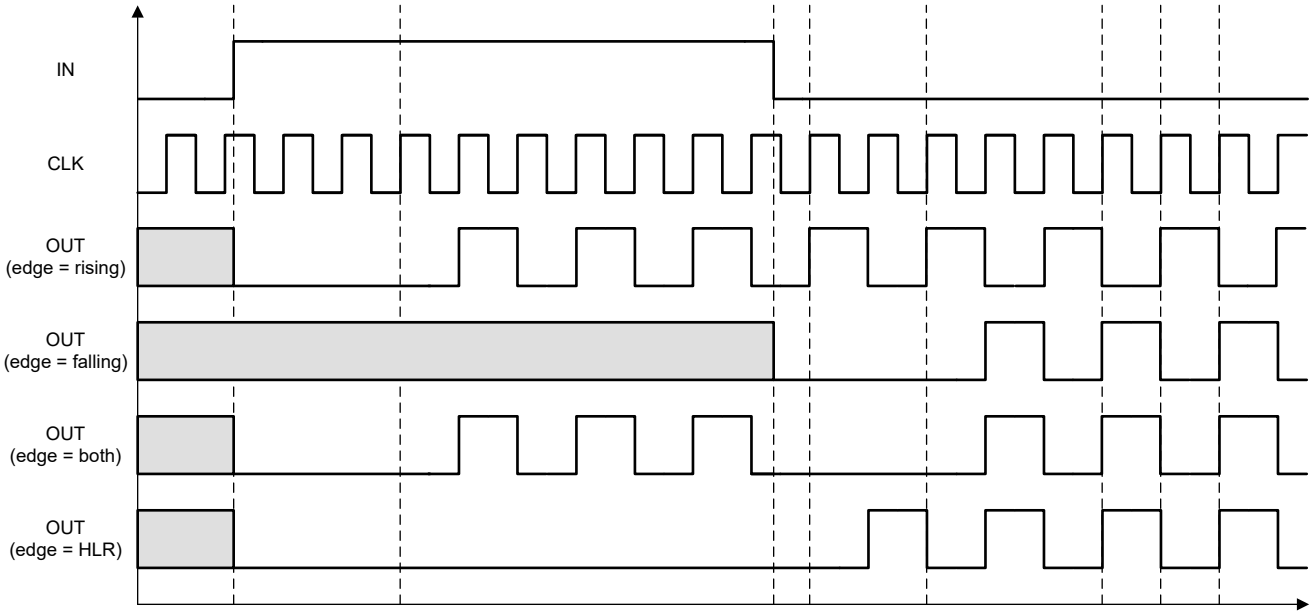


Figure 7-13. Counter output timing example (DATA = 1)

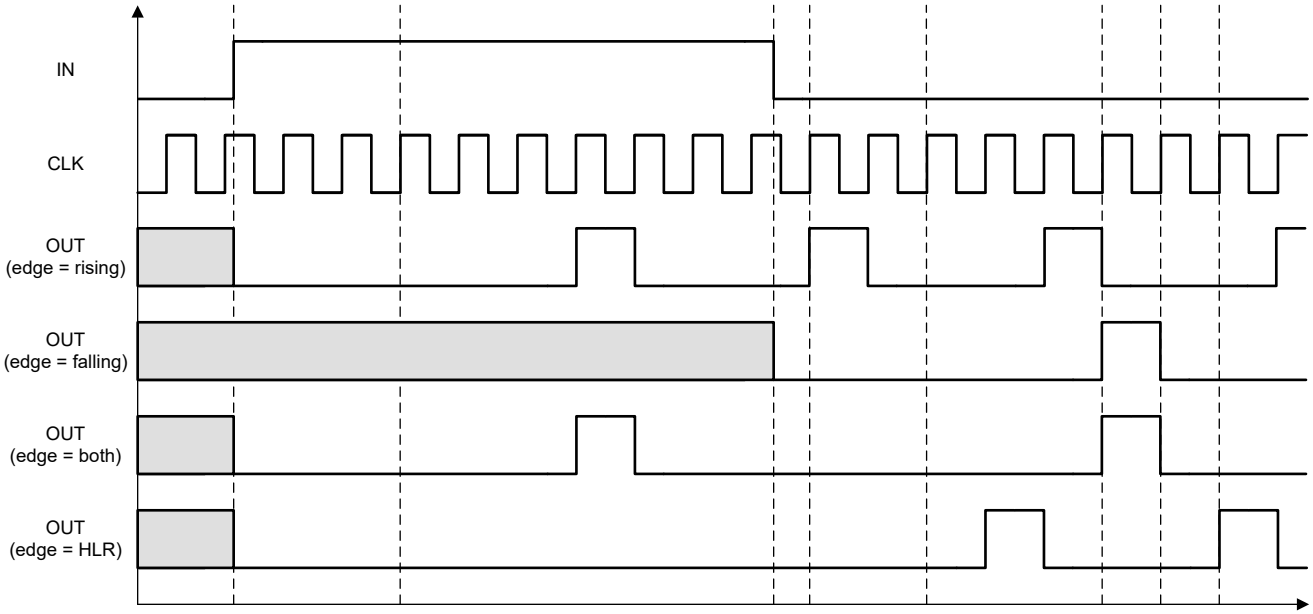


Figure 7-14. Counter output timing example (DATA = 3)

Figure 7-15 shows an example of how the Counter macro-cell operates when the IN signal is shorter than the counter length (shown when edge select parameter is set to "both").

ADVANCE INFORMATION

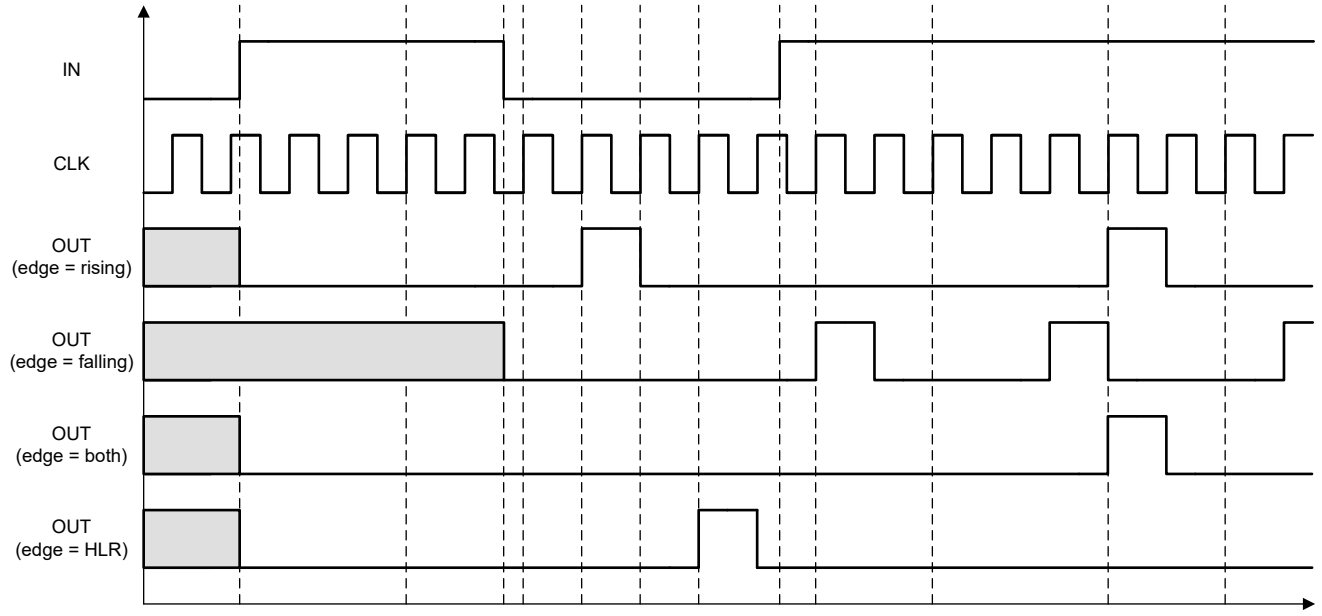


Figure 7-15. Counter output timing example with RST < DATA (DATA = 3)

7.3.5 Programmable Deglitch Filter or Edge Detector Macro-cell

The TPLD801-Q1 has one macro-cell that can be configured as a programmable filter (PFLT) or edge detector (EDET). The PFLT macro-cell can be used to generate a delay (t_{pflt_d}) characterized by t_{pflt_pw} and t_{pflt_pd}. t_{pflt_pw} can be set to 125ns, 250ns, 375ns, or 500ns and t_{pflt_pd} is a fixed value at ≅40ns. Furthermore, the output of the macro-cell can be configured to one of four options: rising edge detection, falling edge detection, both edge detection, or both edge delay. Lastly, the filter operates as a short low-pass filter and its output can be set as non-inverted or inverted.

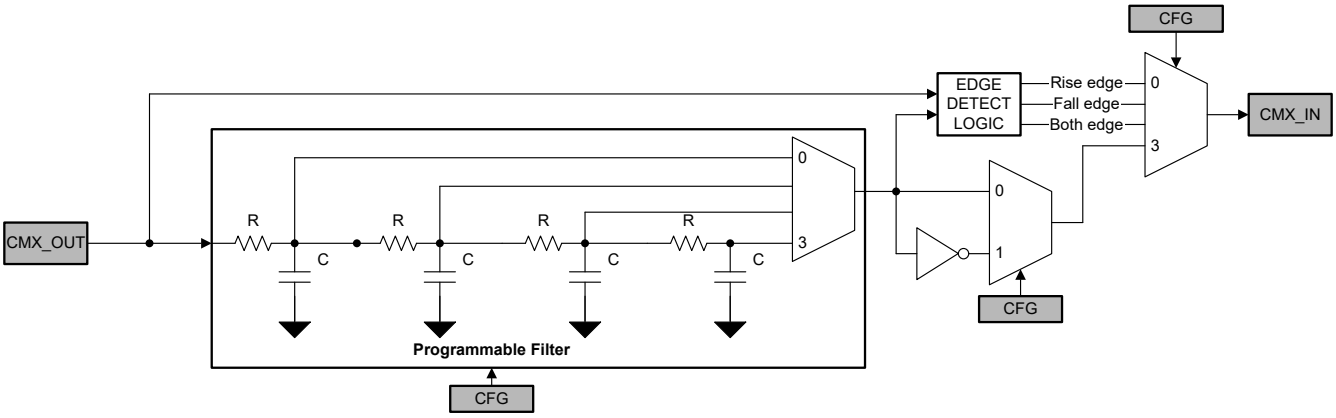


Figure 7-16. Programmable Filter and Edge Detector Block Diagram

Note

The input signal must be longer than t_{pflt_d}, otherwise it will be filtered out.

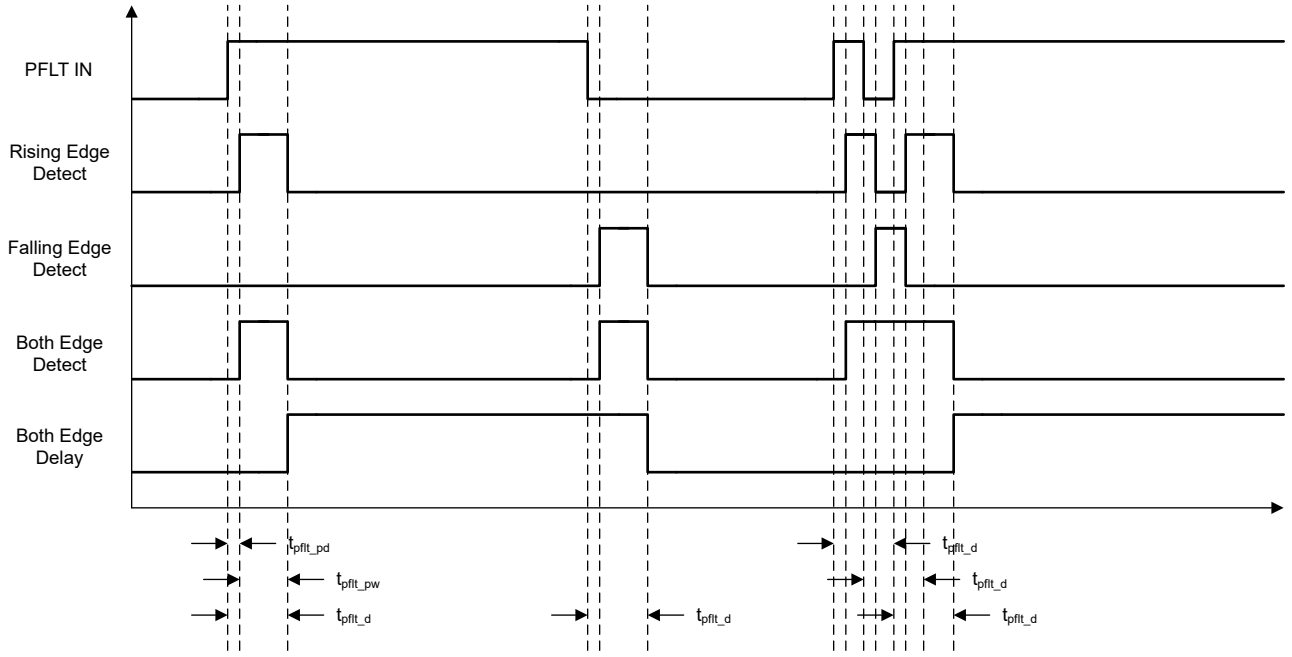


Figure 7-17. Programmable Filter and Edge Detector Output Timing Diagram Example

7.3.6 Selectable Frequency Oscillator

The TPLD801-Q1 has one internal oscillator, selectable to operate at 25kHz or at 2MHz. The user can select one of these operating frequencies for the OSC macro-cell, or the internal oscillator could be bypassed and the operating frequency can come from an external clock.

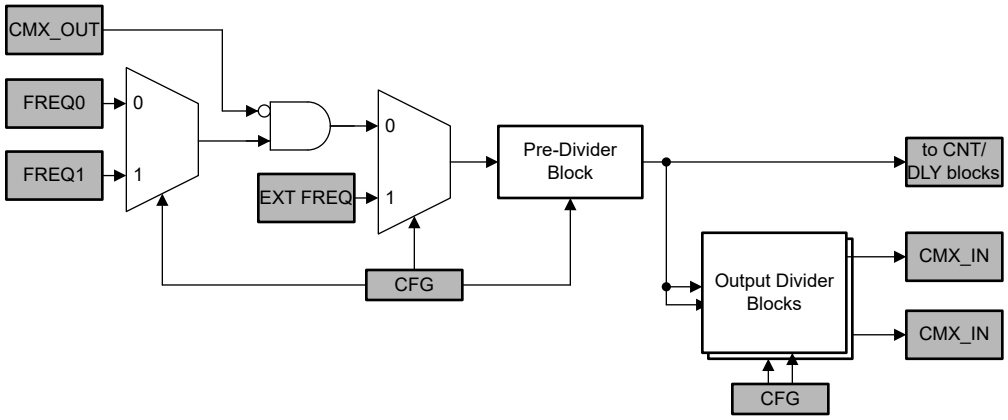


Figure 7-18. Oscillator Block Diagram

Following the operating clock input, there are two divider stages that allow users the flexibility of various clock frequencies for use throughout the device.

The first stage divider allows the selection of up to four options from the operating oscillator frequency as listed in Table 7-13. The output of the first divider stage is routed directly to the counter/delay generator macro-cell CLK inputs, where a separate second divider stage is available.

The output of the first divider stage is also routed into a second divider stage within the oscillator macro-cell. The oscillator macro-cell has two separate second stage dividers, allowing for the output of two separate clocks (OUT0 and OUT1) into the connection mux. See Table 7-14

ADVANCE INFORMATION

Oscillator power modes: When using the device's internal oscillator, there are two configuration settings available:

- **Force power on**: the internal oscillator will continuously run as long as the device is powered on.
- **Auto power on**: the internal oscillator will dynamically power on when any macro-cell requests the oscillator directly from the pre-divider block output and not through the connection mux, and then power off once the task is complete.
- **External power on/off**: the internal oscillator will be powered down when PDWN is asserted High. PDWN signal takes priority over the oscillator power modes. This is only applicable when the internal oscillator is selected and is bypassed when an external clock is used.

Table 7-12. Frequency Options and Limits

Frequency Option	MIN	TYP	MAX
FREQ0	23.75kHz	25kHz	26.25kHz
FREQ1	1.9MHz	2MHz	2.1MHz
EXT	-	-	-

Table 7-13. Oscillator Pre-dividers

Pre-Divider Option	Magnitude
P0	1
P1	2
P2	4
P3	8

Table 7-14. Oscillator Output Dividers

Output Divider Options	Magnitude
OD0	1
OD1	2
OD2	3
OD3	4
OD4	8
OD5	12
OD6	24
OD7	64

7.4 Device Functional Modes

7.4.1 Power-On Reset

The TPLD801-Q1 has a power-on reset (POR) macro-cell to ensure correct device initialization and operation of all macro-cells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{CC} power is first ramping to the device, and also while the V_{CC} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macro-cells inside the device, and finally to the state of the I/O pins.

The power-on Reset (POR) macro-cell will produce a logic High signal as an output when the device power supply (V_{CC}) rises to approximately V_{PORR} and device completely starts up. All outputs are in high impedance state and chip starts loading data from OTP. The reset signal is released for internal macro-cells and all the registers are initialized to their default states. Figure 7-19 shows POR system generates a sequence of signals that enable certain macro-cells.

ADVANCE INFORMATION

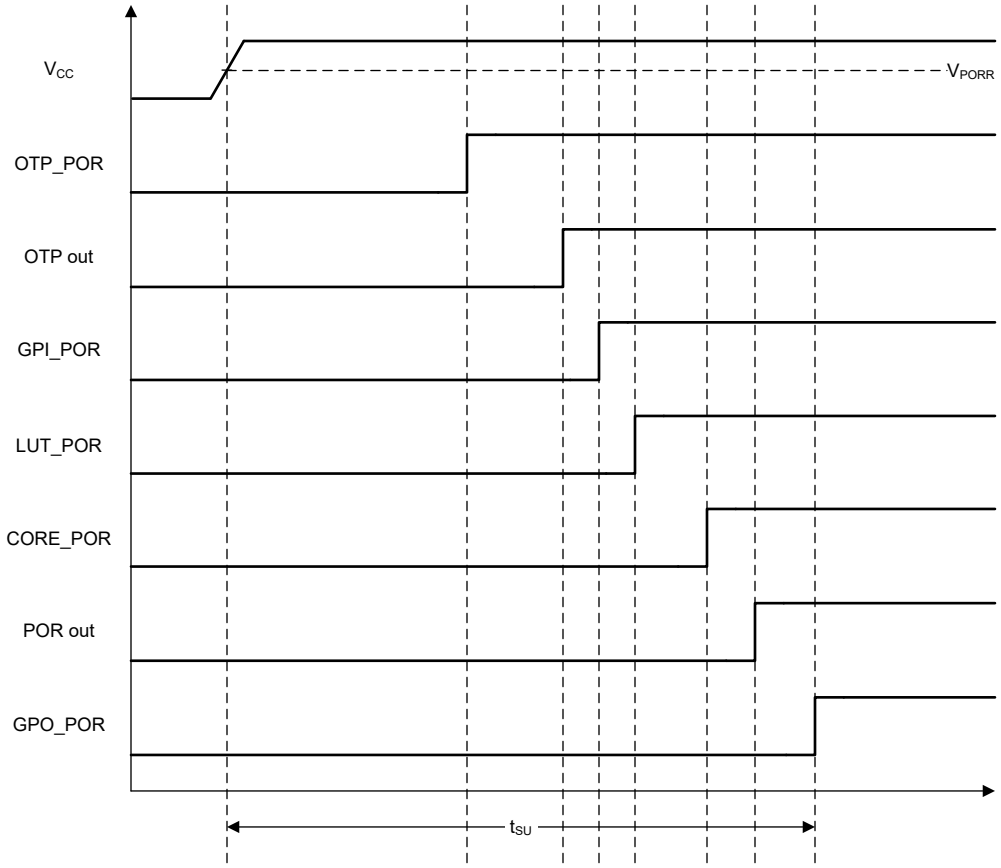


Figure 7-19. POR Sequence

As shown in Figure 7-19, after the V_{CC} has start ramping up and crosses the V_{PORR} threshold:

- First, the on-chip OTP memory is reset.
- Next, the device reads the data from OTP memory, and transfers this information to configure each macro-cell and the connection mux.
- The third stage resets the GPIOs that are configured as inputs and then enables them.
- After that, the LUTs are reset and become active. After LUTs, the delay cells, OSC, DFFs, latches and pipe delay are initialized.
- After all macro-cells are initialized, the internal POR signal generated by the POR macro-cell goes from low to high.
- The last portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point.

Delay blocks will pass their inputs through to the output during the startup sequence without delaying the signal per the configuration, so a LUT added in front of the input of a DLY that ANDs the DLY input with POR will guarantee the input signal will not appear until the device has fully powered up.

GPIO quick charge: There is an option to connect a 2-kΩ resistor in parallel to any configured pull up/pull down resistors to help inputs get to the right voltage faster, especially if there is significant capacitance. The 10 kΩ, 100 kΩ and 1 MΩ GPIO pull up/pull down resistors are not enabled until the POR sequence is completed.

Initialization: All internal macro-cells are initialized to a low level by default. Starting from when V_{CC} exceeds V_{PORR}, macro-cells in the TPLD801-Q1 are powered on and forced into a reset state.

The POR signal going high indicates the mentioned power-up sequence is complete.

ADVANCE INFORMATION

7.5 Programming

7.5.1 One-Time Programmable Memory (OTP)

The TPLD801-Q1 contains one-time programmable (OTP) non-volatile memory, which retain the device configuration in the absence of a power supply. Once a POR event is issued to the device, the OTP content is loaded into the macro-cells per the POR sequence shown in Section 7.4.1.

The TPLD801-Q1 OTP memory can be emulated for quick in-system evaluation or permanently burned using the TPLD801-Q1 EVM and InterConnect Studio software platform. While emulating the OTP, the TPLD will keep its programmed configuration as long as the supply power is provided. Once a power cycle is issued, the TPLD will revert to the configuration stored in the OTP.

8 Revision History

DATE	REVISION	NOTES
September 2024	*	Advance Information Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Packaging Option Addendum

Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
PTPLD801DRLRQ1	PREVIEW	SOT-5X3	DRL	8	3000	RoHS & Green	MATTE SN	Level-1-260C-UNLIM	-40 to 125	P801Q

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

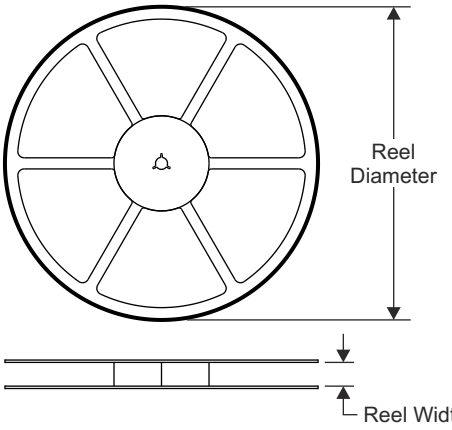
(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

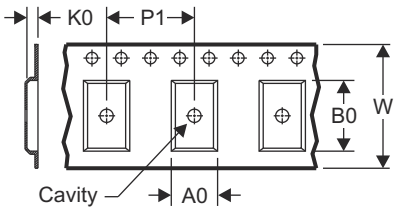
ADVANCE INFORMATION

9.2 Tape and Reel Information

REEL DIMENSIONS

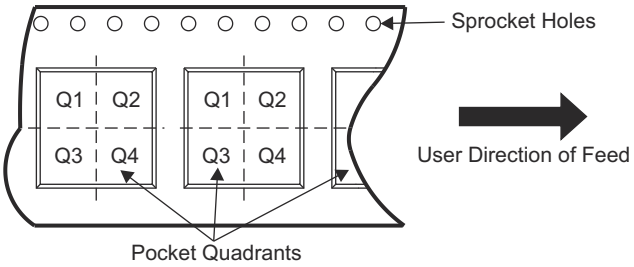


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

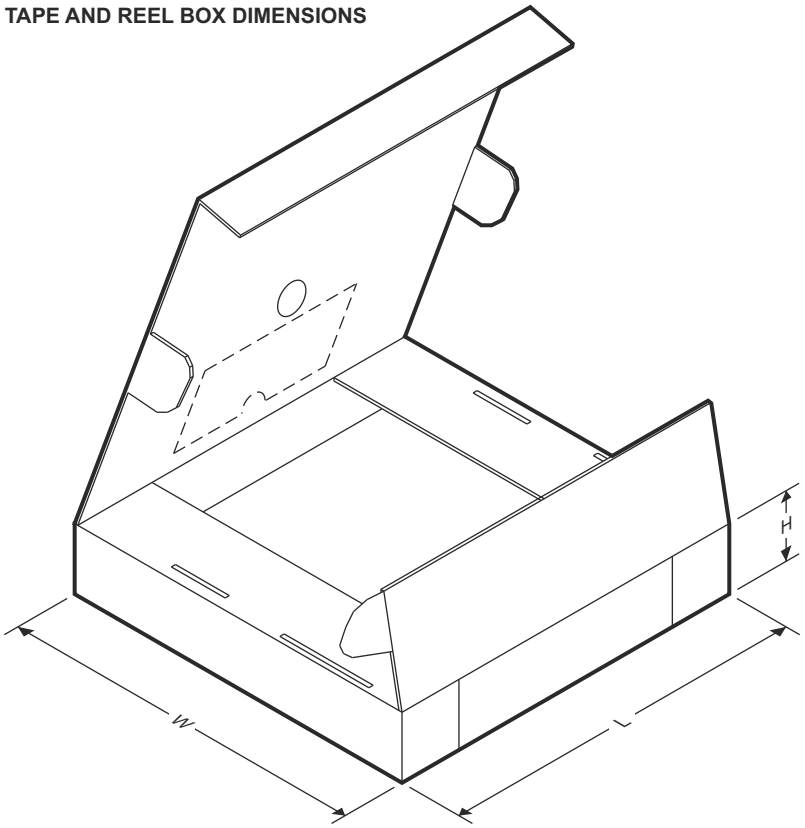
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPLD801DRLRQ1	SOT-5X3	DRL	8	3000	180	8.4	2.4	1.9	0.75	4	8	3

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPLD801DRLRQ1	SOT-5X3	DRL	8	3000	210	185	35

ADVANCE INFORMATION

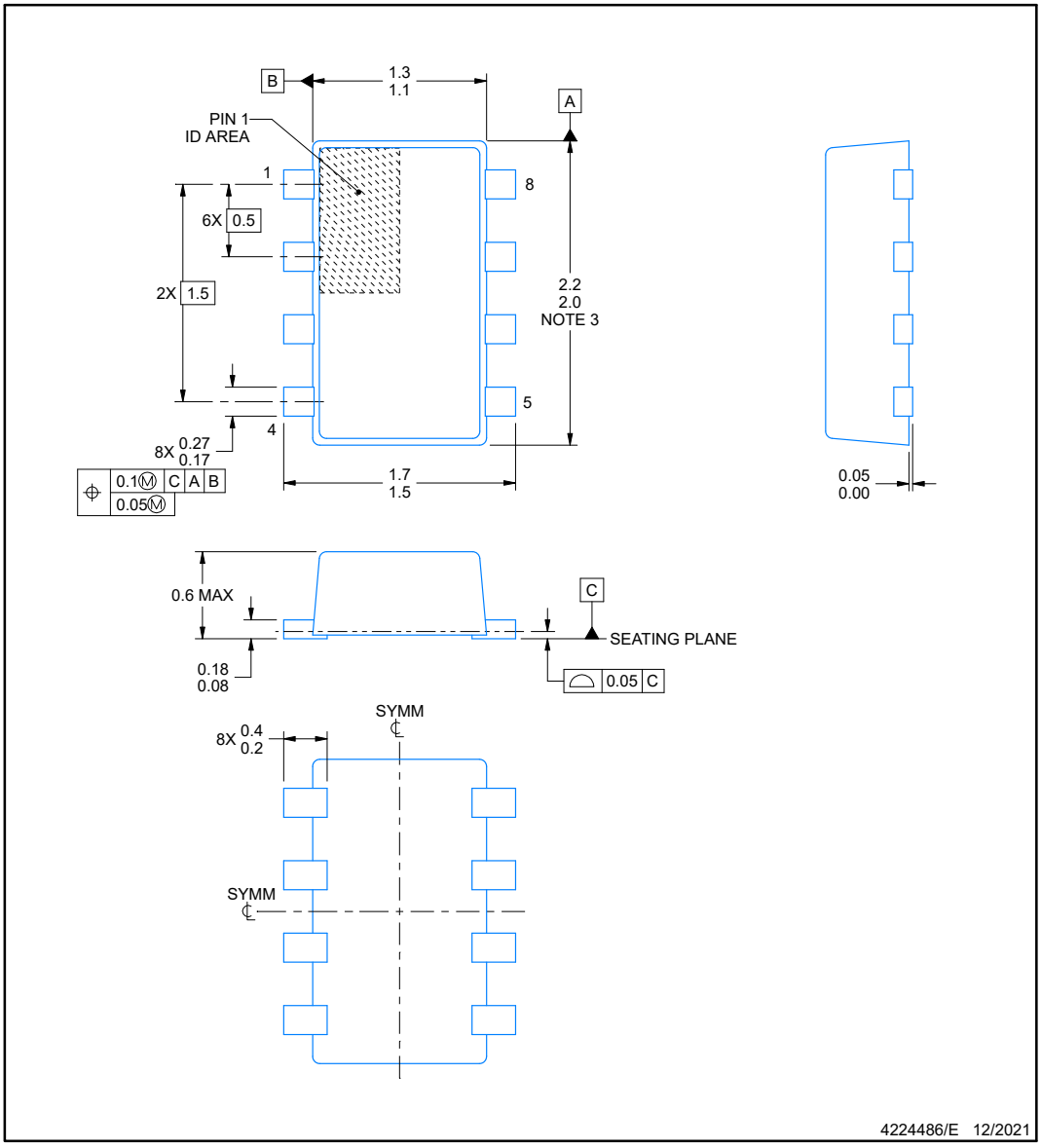
ADVANCE INFORMATION

9.3 Mechanical Data

PACKAGE OUTLINE

DRL0008A — **SOT-5X3 - 0.6 mm max height**

PLASTIC SMALL OUTLINE



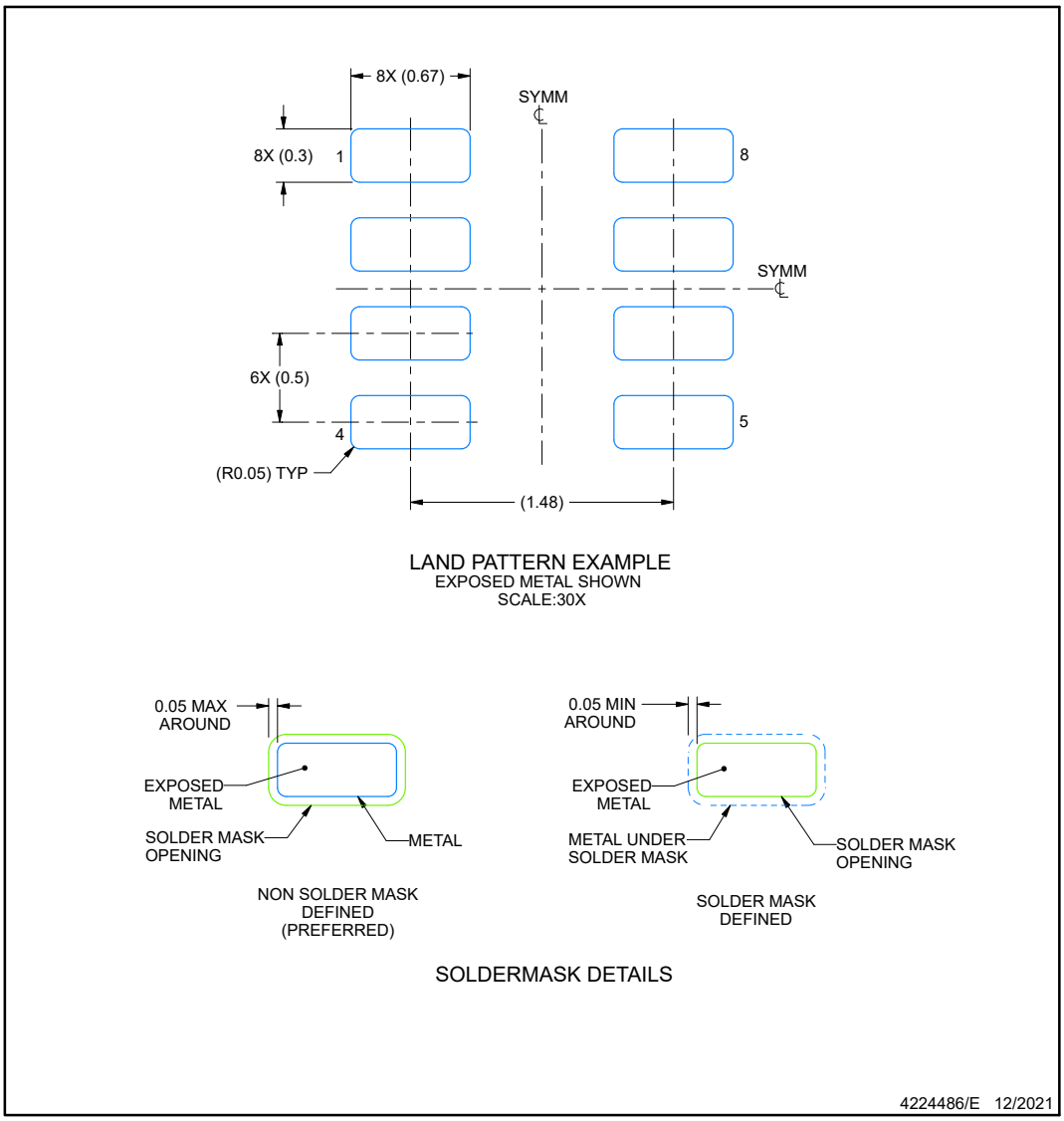
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

DRL0008A — **SOT-5X3 - 0.6 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

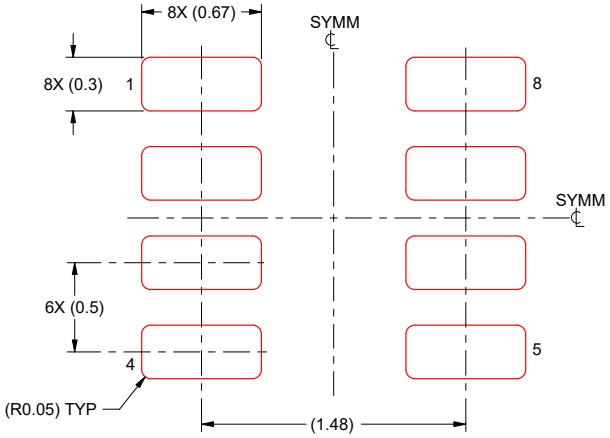
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/E 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPLD801DRLRQ1	ACTIVE	SOT-5X3	DRL	8		TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPLD801-Q1 :

- Catalog : TPLD801

NOTE: Qualified Version Definitions:

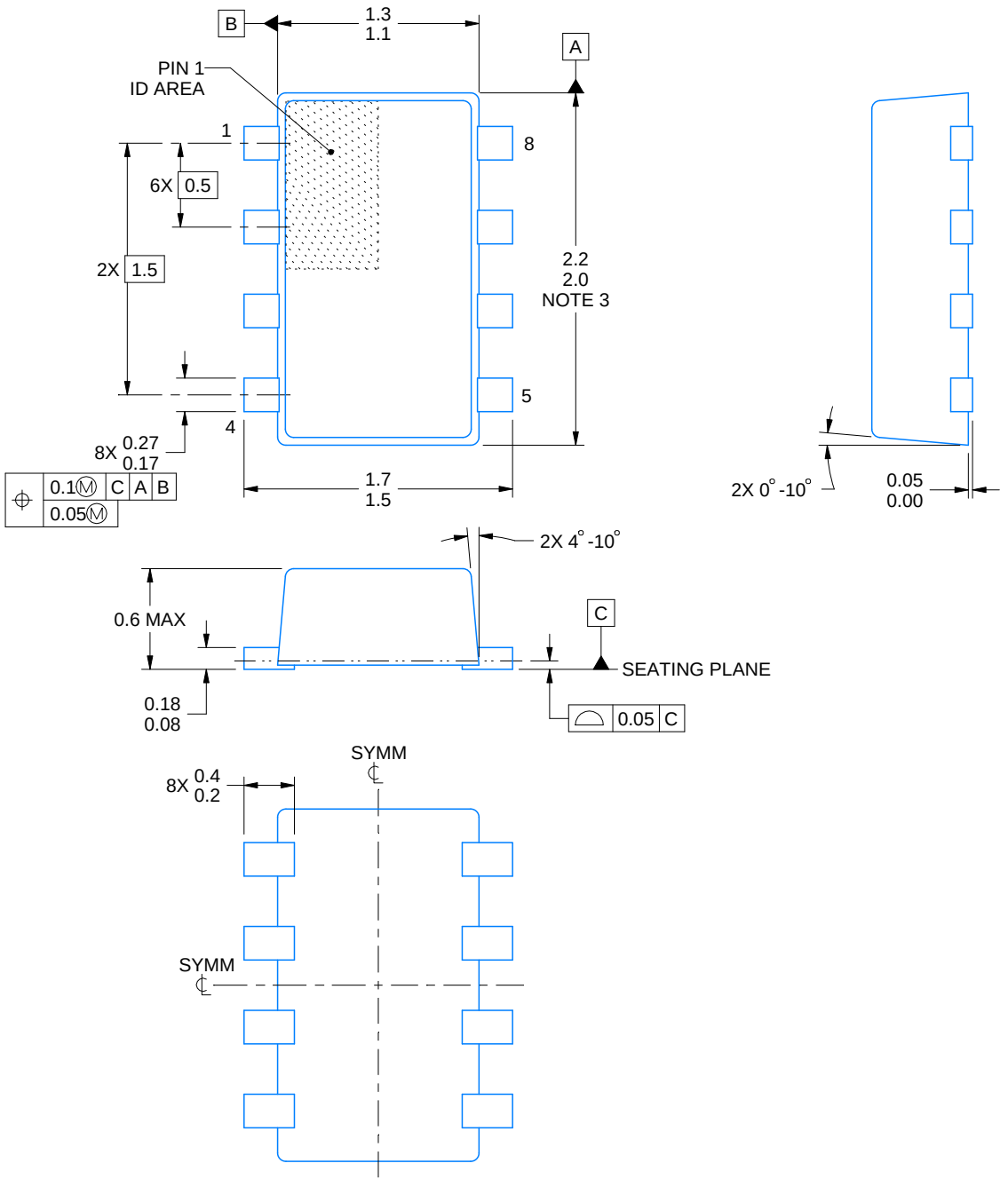
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



4224486/F 08/2024

NOTES:

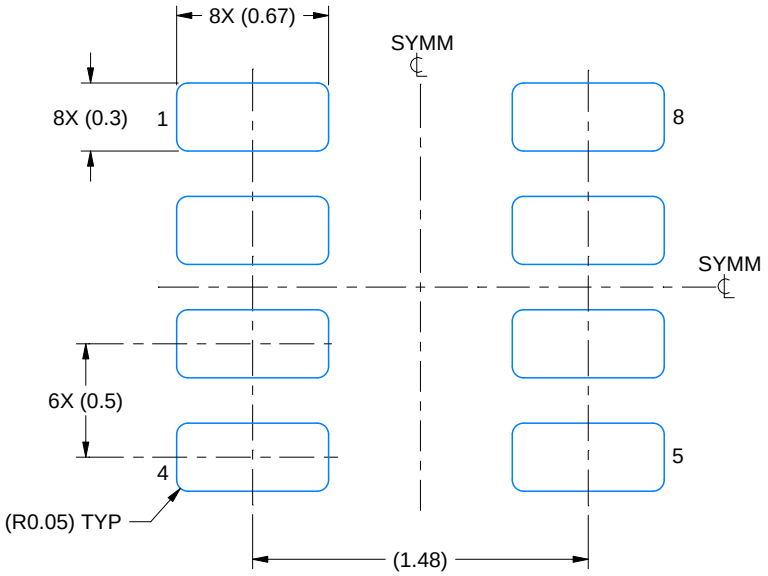
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

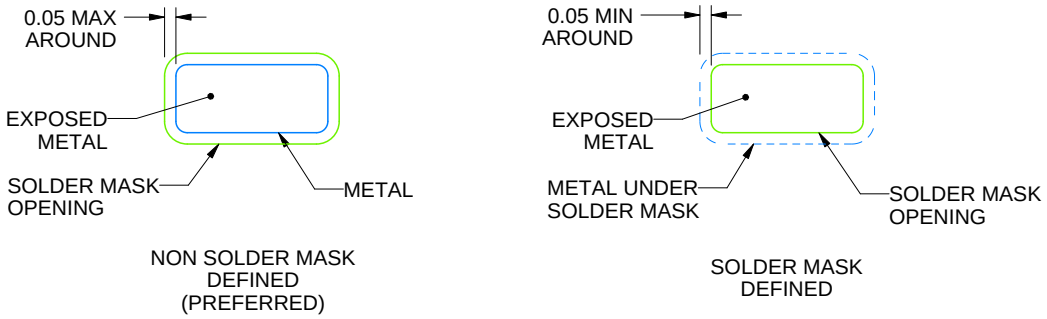
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4224486/F 08/2024

NOTES: (continued)

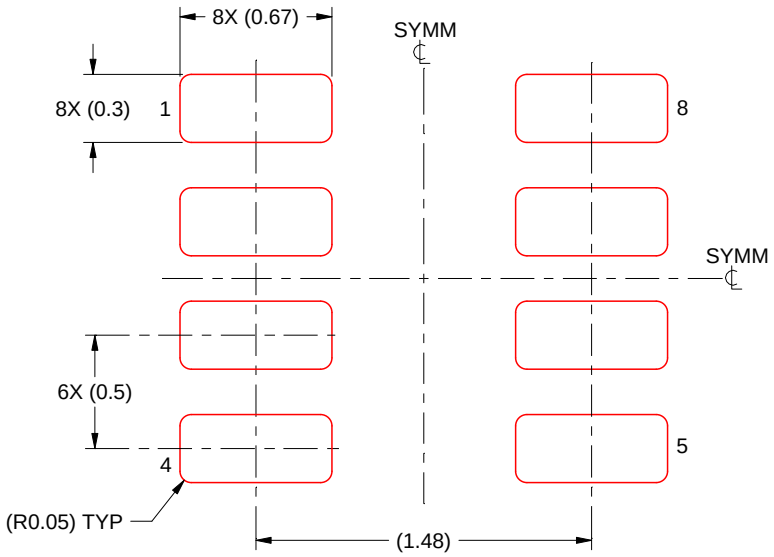
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/F 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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