TPS1213-Q1 45V Low I_Q Automotive High Side Switch Controller With Low Power Mode and Adjustable Load Wakeup Trigger

1 Features

- AEC-Q100 automotive qualified for grade 1 temperature
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 3.5V to 40V input range (45V absolute maximum)
- Reverse input protection down to –40V
- Integrated 11V charge pump
- Low quiescent current, 35μA in low power mode ($\overline{\text{LPM}}$ = Low)
- Low 1μA (typ) shutdown current (EN/UVLO = Low)
- Strong gate drive (G1PU/G1PD: 1.69A src and 2A sink)
- Adjustable short-circuit protection (ISCP) with adjustable response time (TMR) and fault flag output ($\overline{\text{FLT}}$)
- Fast transition from low power mode to active mode with WAKE indication
  - 8μs switch over time from low power path to main path by external $\overline{\text{LPM}}$ trigger (low to high)
  - Adjustable load wakeup threshold (I_{LWU}) with (6μs) switchover from low power path to main path
- Fault indication ($\overline{\text{FLT}}$) during short-circuit fault, charge pump undervoltage, and input undervoltage
- Adjustable input undervoltage lockout (UVLO)
- Short-circuit comparator diagnosis (SCP_TEST)

2 Applications

- Automotive 12V BMS
- Power distribution box

3 Description

The TPS12130-Q1 is a 45V low I_Q smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5V–40V, the device is designed for 12V system designs. The device can withstand and protect the loads from negative supply voltages down to –40V.

TPS12130-Q1 has integrated two gate drives with 1.69A source and 2A sink capacity to drive MOSFETs in the main path and 165μA source and 2A sink capacity for the low power path.

In the low power mode with $\overline{\text{LPM}}$ = Low, the low power path FET is kept ON and the main FETs are turned OFF. The device consumes low I_Q of 35μA (typ) in this mode. Auto load wakeup threshold to enter into active state can be adjusted using ISCP/LWU pin. I_Q reduces to 1μA (typ) with EN/UVLO low.

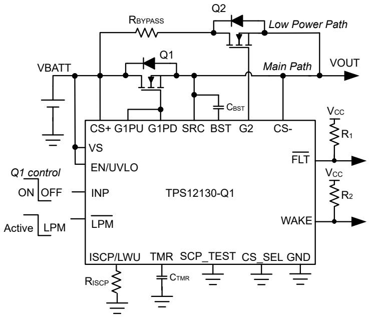
The device provides adjustable short circuit protection using MOSFET VDS sensing or by using an external R_{SNS} resistor. Auto-retry and latch-off fault behavior can be configured. The device also features diagnosis of the internal short circuit comparator using external control on SCP_TEST input.

The TPS12130-Q1 is available in a 19-pin VSSOP package.

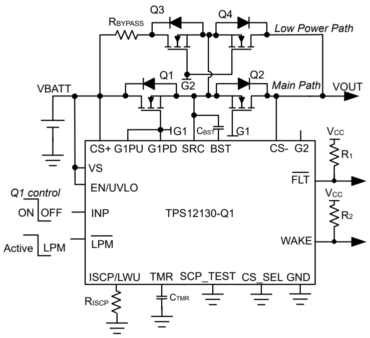
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)(2)
TPS12130-Q1	DGX (VSSOP, 19)	5.1mm × 3.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Always ON Automotive e-Fuse



Always ON Automotive e-Fuse Driving Back to Back FETs

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4 Pin Configuration and Functions

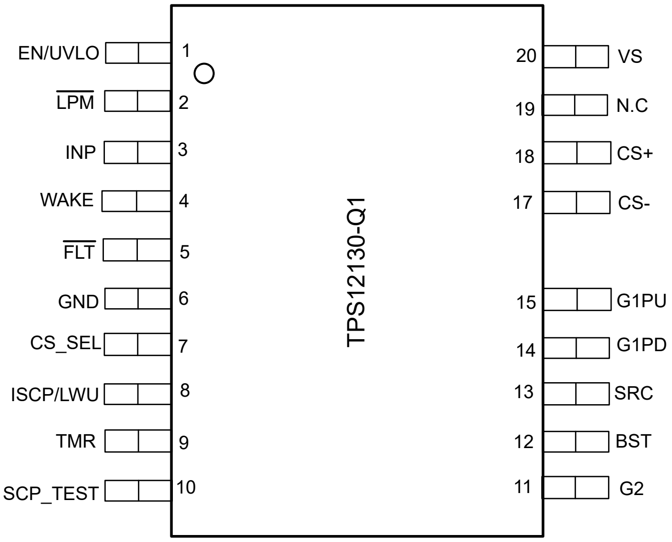


Figure 4-1. DGX Package, 19-Pin VSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
EN/UVLO	1	I	EN/UVLO input. A voltage on this pin above $V_{(ENR)}$ enables normal operation. If EN/UVLO is below $V_{(ENF)}$ then gate drives are turned OFF and $\overline{\text{FLT}}$ asserts low. Forcing this pin below $V_{(ENF)}$ (0.3V) shuts down the device reducing quiescent current. Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pulldown of 100nA pulls EN/UVLO low and keeps the device in OFF state.
$\overline{\text{LPM}}$	2	I	Low power mode input. When driven high, the devices enter into active mode. When driven low, the devices enter into low power mode. $\overline{\text{LPM}}$ has an internal weak pull down of 100nA to GND to keep G2 high when $\overline{\text{LPM}}$ is left floating.
INP	3	I	Input signal for external FET control. CMOS compatible input reference to GND that sets the state of G1PD and G1PU pins. INP has an internal weak pull down of 100nA to GND to keep G1PD pulled to SRC when INP is left floating.
WAKE	4	O	Open drain wake output. This pin asserts low when the device enters into active mode (when $\overline{\text{LPM}}$ is driven high or when a load wake up event has occurred).
$\overline{\text{FLT}}$	5	O	Open drain fault output. This pin asserts low during short circuit fault, charge pump UVLO, input UVLO and during SCP comparator diagnosis. If $\overline{\text{FLT}}$ feature is not desired then connect it to GND.
GND	6	G	Connect GND to system ground.
CS_SEL	7	—	Reserved for future use. Connect to GND.
ISCP/LWU	8	I	Short circuit detection and load wakeup threshold setting. SCP control for G1 during active mode ($\overline{\text{LPM}}$ = high) and load wakeup control on G2 during low power mode ($\overline{\text{LPM}}$ = low).
TMR	9	I	Fault timer input. A capacitor across TMR pin to GND sets the times for fault turnoff. Leave it open for fastest setting (< 10μs). Connect ISCP/LWU and TMR pin to GND to disable overcurrent protection.

Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SCP_TEST	10	I	Internal short circuit comparator (SCP) diagnosis input. When SCP_TEST is driven low to high with INP pulled high, the internal SCP comparator operation is checked. $\overline{FLT}$ goes low and G1PD gets pulled to SRC if SCP comparator is functional. Connect SCP_TEST pin to GND if this feature is not desired. SCP_TEST has an internal weak pull down of 100nA to GND.
G2	11	O	Low power mode FET gate drive output. It has 165 µA pullup and 2 A sink capacity
BST	12	O	High side bootstrapped supply. An external capacitor with a minimum value of > $Q_{g(tot)}$ of the external FET must be connected between this pin and SRC.
SRC	13	O	Source connection of the external FET.
G1PD	14	O	High current gate driver pulldown. This pin pulls down to SRC. For the fastest turnoff, tie this pin directly to the gate of the external high side MOSFET.
G1PU	15	O	High current gate driver pullup. This pin pulls up to BST. Connect this pin to G1PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the in-rush current during turnon.
CS–	17	I	Current sense negative input.
CS+	18	I	Current sense positive input.
N.C	19	—	No connect.
VS	20	P	Supply pin of the controller.

(1) I = input, O = output, I/O = input and output, P = power, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input pins	VS, CS+, CS– to GND	–40	45	V
	SRC to GND	–40	45	
	G1PU, G1PD, G2, BST to SRC	–0.3	19	
	ISCP/LWU, TMR, SCP_TEST to GND	–0.3	5.5	
	EN/UVLO, INP, $\overline{\text{LPM}}$, CS_SEL to GND, $V_{(VS)} > 0$ V	–1	45	
	EN/UVLO, INP, $\overline{\text{LPM}}$, CS_SEL to GND, $V_{(VS)} \leq 0$ V	$V_{(VS)}$	$(40 + V_{(VS)})$	
	CS+ to CS–	–1	45	
	$\overline{\text{FLT}}$, WAKE to GND	–1	20	
Sink current	$I_{(\overline{FLT})}$, $I_{(WAKE)}$		10	mA
	$I_{(CS+)}$ to $I_{(CS-)}$, 1 msec	–100	100	
Output pins	G1PU, G1PD, G2, BST to GND	–40	60	V
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN/UVLO, VS, SCP_TEST, G2)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input pins	VS to GND	3.5		40	V
	Minimum voltage on VS pin for Short Circuit Protection	4			
	EN/UVLO, INP, $\overline{\text{LPM}}$ to GND	0		40	
Output pins	$\overline{\text{FLT}}$, WAKE to GND	0		15	V
External capacitor	VS, SRC to GND	22			nF
	BST to SRC	0.1			µF
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC(1)		TPS1213-Q1	UNIT
		DGX	
		19 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

T_J = –40 ℃ to +125℃. $V_{(VS)}$ = 12 V, $V_{(BST – SRC)}$ = 11 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VS	Operating input voltage		3.5		40	V
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$ in Active mode	$V_{(EN/UVLO)} = V_{(\overline{LPM})}$ = 2 V		44		µA
	Total System Quiescent current, $I_{(GND)}$ in low power mode	$V_{(EN/UVLO)}$ = 2 V, $V_{(\overline{LPM})}$ = 0 V		35		µA
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V		1		µA
ENABLE, UNDERVOLTAGE LOCKOUT (EN/UVLO), SHORT CIRCUIT COMPARATOR TEST (SCP_TEST) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising			1.24		V
$V_{(UVLOF)}$	UVLO threshold voltage, falling			1.14		V
$V_{(ENR)}$	Enable threshold voltage for shutdown, rising				1.02	V
$V_{(ENF)}$	Enable threshold voltage for shutdown, falling		0.3			V
$V_{(SCP\_TEST)}$	SCP test mode rising threshold				2	V
$V_{(SCP\_TEST)}$	SCP test mode falling threshold		0.8			V
$I_{(EN/UVLO)}$	Enable input leakage current	$V_{(EN/UVLO)}$ = 12 V		180		nA
CHARGE PUMP (BST–SRC)						
$V_{(BST – SRC\_ON)}$	Charge Pump Turn ON voltage	$V_{(EN/UVLO)}$ = 2 V	10			V
$V_{(BST – SRC\_OFF)}$	Charge Pump Turnoff voltage	$V_{(EN/UVLO)}$ = 2 V			11.8	V
$V_{(BST\_UVLOR)}$	$V_{(BST – SRC)}$ UVLO voltage threshold, rising	$V_{(EN/UVLO)}$ = 2 V			9.5	V
$V_{(BST\_UVLOF)}$	$V_{(BST – SRC)}$ UVLO voltage threshold, falling	$V_{(EN/UVLO)}$ = 2 V	7.2			V
GATE DRIVER OUTPUTS (G1PU, G1PD, G2)						
$I_{(G1PU)}$	Peak Source Current			1.69		A
$I_{(G2)}$	G2 Source Current			165		µA
$I_{(G1PD)}$	Peak Sink Current			2		A
$I_{(G2)}$	G2 Peak Sink Current			2		A
$V_{(G1\_GOOD)}$	G1 Good rising threshold			7		V
$V_{(G2\_GOOD)}$	G2 Good rising threshold			7		V
SHORT CIRCUIT PROTECTION AND LOAD WAKE UP THRESHOLD (ISCP/LWU)						
$I_{SCP/LWU}$	SCP/LWU Input Bias current			10		µA

5.5 Electrical Characteristics (continued)

T_J = –40 ℃ to +125℃. $V_{(VS)}$ = 12 V, $V_{(BST-SRC)}$ = 11 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCP/LWU)}$	SCP/LWU threshold	$R_{(ISCP)}$ = 32.5 kΩ	60	75	90	mV
		$R_{(ISCP)}$ = 15 kΩ		40		mV
DELAY TIMER (TMR)						
$I_{(TMR\_SRC\_CB)}$	TMR source current			80		µA
$I_{(TMR\_SRC\_FLT)}$	TMR source current			2.2		µA
$I_{(TMR\_SNK)}$	TMR sink current			2.5		µA
$V_{(TMR\_SC)}$				1.1		V
$V_{(TMR\_LOW)}$				0.2		V
$N_{(A\text{-}R\ Count)}$				32		
INPUT CONTROLS (INP, $\overline{\text{LPM}}$), FAULT ($\overline{\text{FLT}}$) & WAKE FLAG (WAKE)						
$R_{(\overline{FLT})}$, $R_{(WAKE)}$	$\overline{\text{FLT}}$, WAKE switch Pull-down resistance			70		Ω
$V_{(INP\_H)}$, $V_{(\overline{LPM}\_H)}$					2	V
$V_{(INP\_L)}$, $V_{(\overline{LPM}\_L)}$			0.8			V

5.6 Switching Characteristics

T_J = –40 ℃ to +125℃. $V_{(VS)}$ = 12 V, $V_{(BST-SRC)}$ = 11 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{G1PU(INP\_H)}$	INP turn on propogation delay	INP ↑ to G1PU ↑, C_L = 47 nF		1		µs
$t_{G1PD(INP\_L)}$	INP turn off propogation delay	INP ↓ to G1PD ↓, C_L = 47 nF		5		µs
$t_{G2\_ON(\overline{LPM})}$	Active mode to LPM mode transition delay , G2 ON	$\overline{\text{LPM}}$ ↓ to G2 ↑, $C_{L(G2)}$ = Open	7			µs
$t_{G1\_OFF(\overline{LPM})}$	Active mode to LPM mode transition delay , G1 OFF	$\overline{\text{LPM}}$ ↓, G2 ↑ (above $V_{(G2\_GOOD)}$) to G1 ↓ $C_{L(G1)}$ = 47 nF	6			µs
$t_{G2(WAKE\_\overline{LPM})}$	LPM Mode to Active mode transition delay with $\overline{\text{LPM}}$ trigger	$\overline{\text{LPM}}$ ↑ , G1 ↑ (above $V_{(G1\_GOOD)}$) to G2 ↓, $C_{L(G2)}$ = 47 nF, $V_{(\overline{LPM})}$ = 0 V	6			µs
$t_{G1(WAKE\_\overline{LPM})}$	LPM Mode to Active mode transition delay with $\overline{\text{LPM}}$ trigger	$\overline{\text{LPM}}$ ↑ to G1 ↑, C_L = 47 nF			11	µs
$t_{G1(WAKE\_LWU)}$	LPM Mode to Active mode transition delay (G1 ON) during Load wakeup	$V_{(CS+–CS–)}$↑ $V_{(SCP/LWU)}$ to G1 ↑, C_L = 47 nF, $V_{(\overline{LPM})}$ = 0 V			6	µs
$t_{G1PD(UVLO\_OFF)}$	UVLO turn off propogation delay	UVLO ↓ to G1PD ↓, C_L = 47 nF, INP = 2 V		7.5		µs
t_{SC}	Hard Short-circuit protection propogation delay	$V_{(CS+–CS–)}$↑ $V_{(SCP/LWU)}$ to G1PD ↓, C_L = 47 nF, $C_{(TMR)}$ = Open, $\overline{\text{LPM}}$ = 2 V		4		µs
t_{SC_PUS}	Short-circuit protection propogation delay during power up with output short circuit	$C_{(TMR)}$ = Open			10	µs

6 Parameter Measurement Information

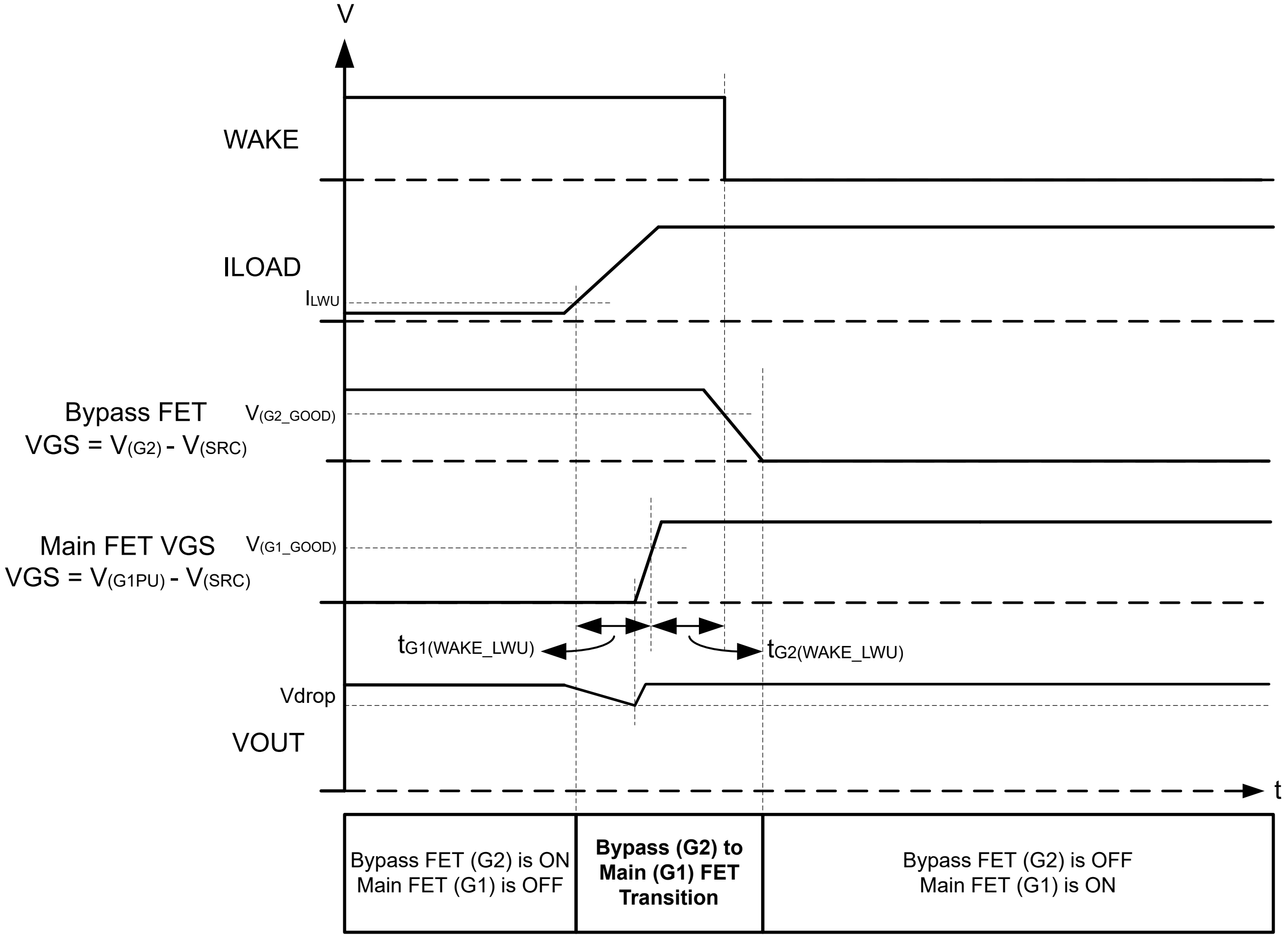


Figure 6-1. System Wake to Active Mode From Low Power Mode by Load Wakeup

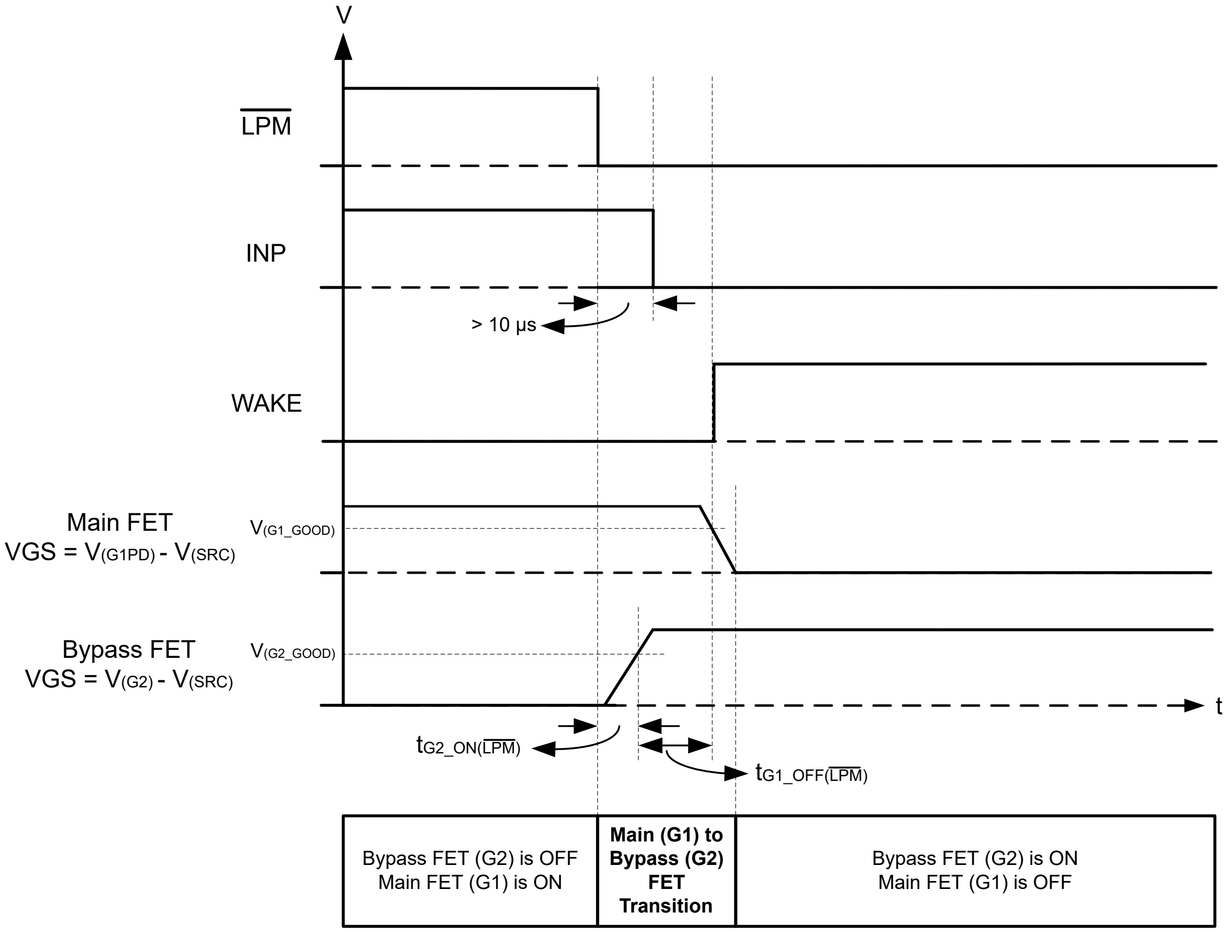


Figure 6-2. Active Mode to Low Power Mode by $\overline{\text{LPM}}$ Trigger

7 Detailed Description

7.1 Overview

The TPS12130-Q1 is a 45V low I_Q smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5V–40V, the device is designed for 12V system designs. The device can withstand and protect the loads from negative supply voltages down to –40V.

TPS12130-Q1 has integrated two gate drives with 1.69A source and 2A sink capacity to drive MOSFETs in the main path and 165µA source and 2A sink capacity for the low power path.

In the low power mode with $\overline{\text{LPM}}$ = Low, the low power path FET is kept ON and the main FETs are turned OFF. The device consumes low I_Q of 35µA (typical) in this mode. Auto load wakeup threshold to enter into active state can be adjusted using ISCP/LWU pin. I_Q reduces to 1µA (typical) with EN/UVLO low.

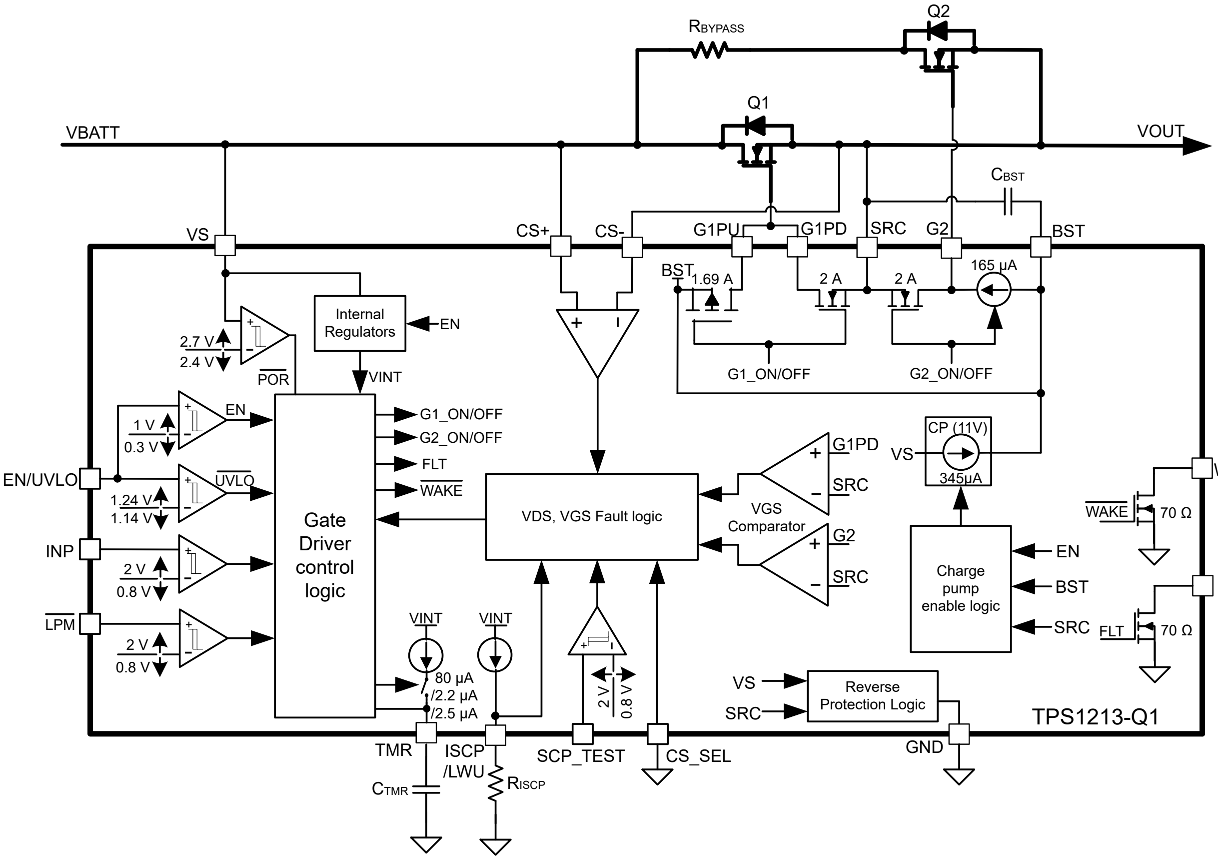
The device features WAKE output pin to indicate the mode of operation (active/low power mode).

The device provides adjustable short circuit protection using MOSFET VDS sensing or by using an external R_{SNS} resistor. Auto-retry and latch-off fault behavior can be configured. The device also features diagnosis of the internal short circuit comparator using external control on SCP_TEST input.

The device indicates fault ($\overline{\text{FLT}}$) on open drain output during short circuit, charge pump under voltage and input under voltage conditions.

The TPS12130-Q1 is available in a 19-pin VSSOP package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Charge Pump and Gate Driver Output (VS, G1PU, G1PD, BST, SRC)

Figure 7-1 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 1.69-A/2-A peak source/sink gate driver (G1) for main FET and 165-µA/2-A peak source/sink current gate driver (G2) for bypass FET. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 11-V, 345-µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, C_{BST} that is placed across the gate driver (BST and SRC).

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the C_{BST} capacitor. After the voltage across C_{BST} crosses $V_{(BST\_UVLOR)}$, the GATE driver section is activated. The device has a 1-V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Choose C_{BST} based on the external FET Q_G and allowed dip during FET turn-ON. The charge pump remains enabled until the BST to SRC voltage reaches 11.8 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 10 V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between 11.8 V and 10 V as shown in the Figure 7-2.

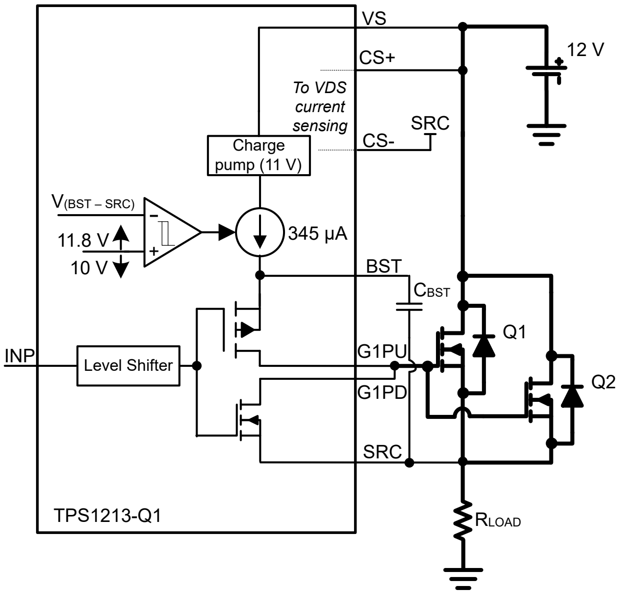


Figure 7-1. Main FET Gate Driver

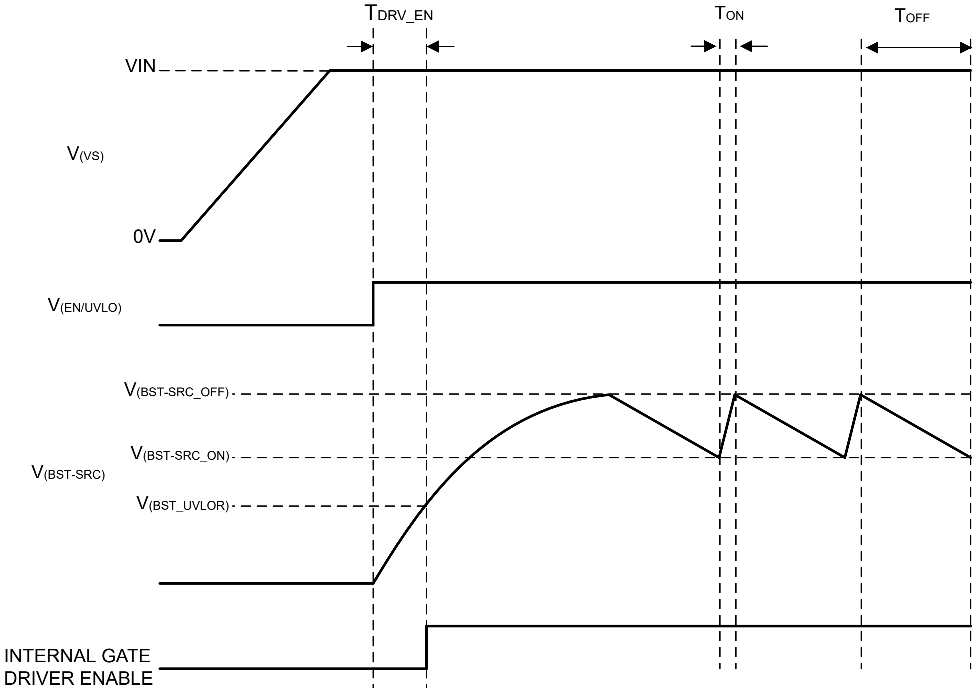


Figure 7-2. Charge Pump Operation

Use the following equation to calculate the initial gate driver enable delay:

$$T_{DRV\_EN} = \frac{C_{BST} \times V_{(BST\_UVLOR)}}{345\ \mu A} \tag{1}$$

Where,

C_{BST} is the charge pump capacitance connected across BST and SRC pins.

$V_{(BST\_UVLOR)}$ = 9.5 V (max).

7.3.2 Capacitive Load Driving

Certain end equipments like automotive power distribution unit power different loads including other ECUs. These ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur and potentially damaging the power FETs.

To limit the inrush current during capacitive load switching, the following system design techniques can be used with TPS12130-Q1 device.

7.3.2.1 Using Low Power Bypass FET (G2 drive) for Load Capacitor Charging

In high-current applications where several FETs (Q1, Q2) are connected in parallel, the gate slew rate control for bypass FET (Q3) can be used to precharge the capacitive load with inrush current limiting.

The TPS12130-Q1 integrates gate driver (G2) with a dedicated control input ($\overline{\text{LPM}}$). This feature can be used to drive a separate low power bypass FET (Q3) and precharge the capacitive load with inrush current limiting. Figure 7-3 shows the low power bypass FET implementation for capacitive load charging using TPS12130-Q1. An external capacitor C_g reduces the gate turn-ON slew rate and controls the inrush current.

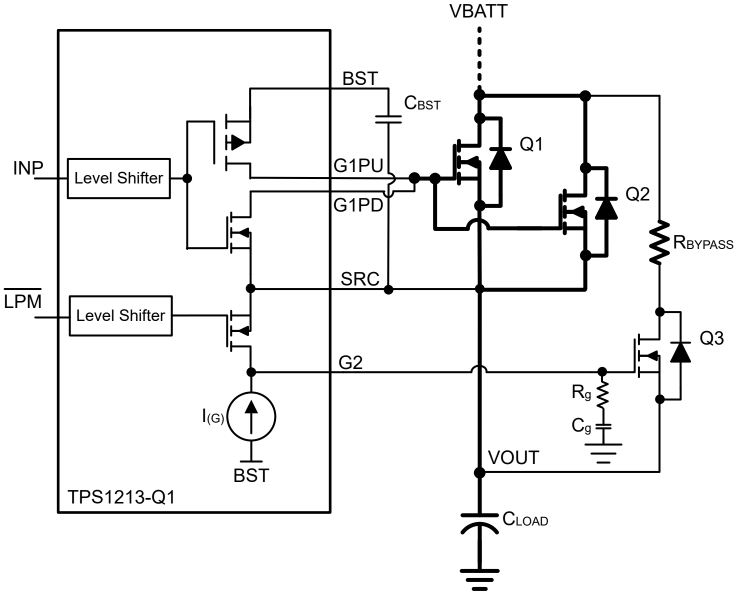


Figure 7-3. Capacitor Charging Using Gate Slew Rate Control of Low Power Bypass FET

During power up with EN/UVLO pulled high and $\overline{\text{LPM}}$ pulled low > 500µs time, the device turns ON Q3 by pulling G2 high with 165µA of source current and the main FETs (G1 gate drive) are kept OFF.

Use Equation 2 to calculate the I_{INRUSH}:

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \tag{2}$$

Where,

C_{LOAD} is the load capacitance.

VBATT is the input voltage and T_{charge} is the charge time.

Use Equation 3 to calculate the required C_g value.

$$C_g = \frac{C_{LOAD} \times I_{(G)}}{I_{INRUSH}} \tag{3}$$

Where,

$I_{(G)}$ is 165µA (typical),

A series resistor R_g must be used in conjunction with C_g to limit the discharge current from C_g during turn-off. The recommended value for Rg is between 220Ω to 470Ω.

After the output capacitor is charged, main FETs can be controlled (G1 gate drive) and bypass FET (G2 gate drive) can be turned OFF by driving $\overline{\text{LPM}}$ high externally. The main FETs (G1 gate drive) can now be turned ON by driving INP high.

Figure 7-4 shows application circuit to charge large output capacitors using low power bypass path in high current applications. This design involves a power resistor (R_{BYPASS}) in series with bypass FET as shown in Figure 7-4.

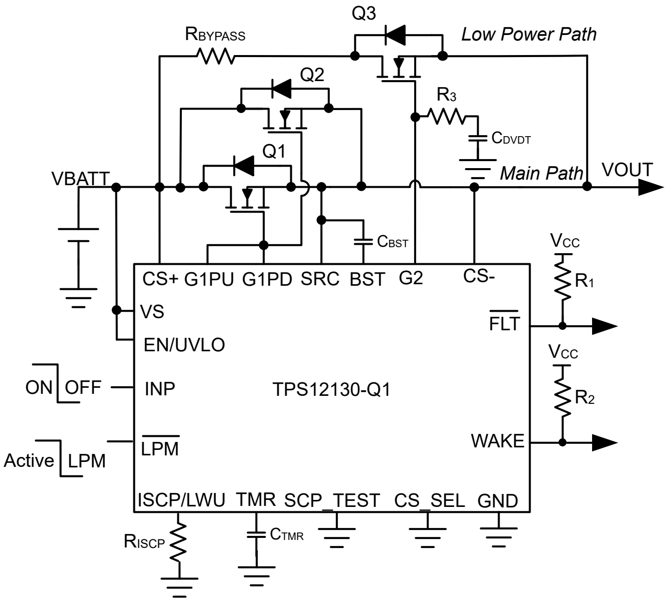


Figure 7-4. TPS12130-Q1 Application Circuit for Capacitive Load Driving Using Low Power Bypass FET and Series Power Resistor (R_{BYPASS})

Using Bypass Path for Load Capacitor Charging and Automatic Load Wakeup

TPS12130-Q1 supports load capacitor charging and automatic load wakeup functionality using a common bypass path. Use a resistor R_{BYPASS} and a FET Q3 as shown in Figure 7-4.

During the load capacitor charging, the device senses VGS of the bypass FET Q3 by monitoring the voltage across G2 and SRC. Once the sensed threshold has reached V_{G2_GOOD} threshold (7V typical) indicating the Q3 gate is enhanced (and load capacitor is charged) then the voltage across CS+ and CS– pins is monitored.

With this scheme, capacitor charging current (I_{INRUSH}) can also be set at higher than load wakeup threshold (I_{LWU}) as shown in Figure 7-5.

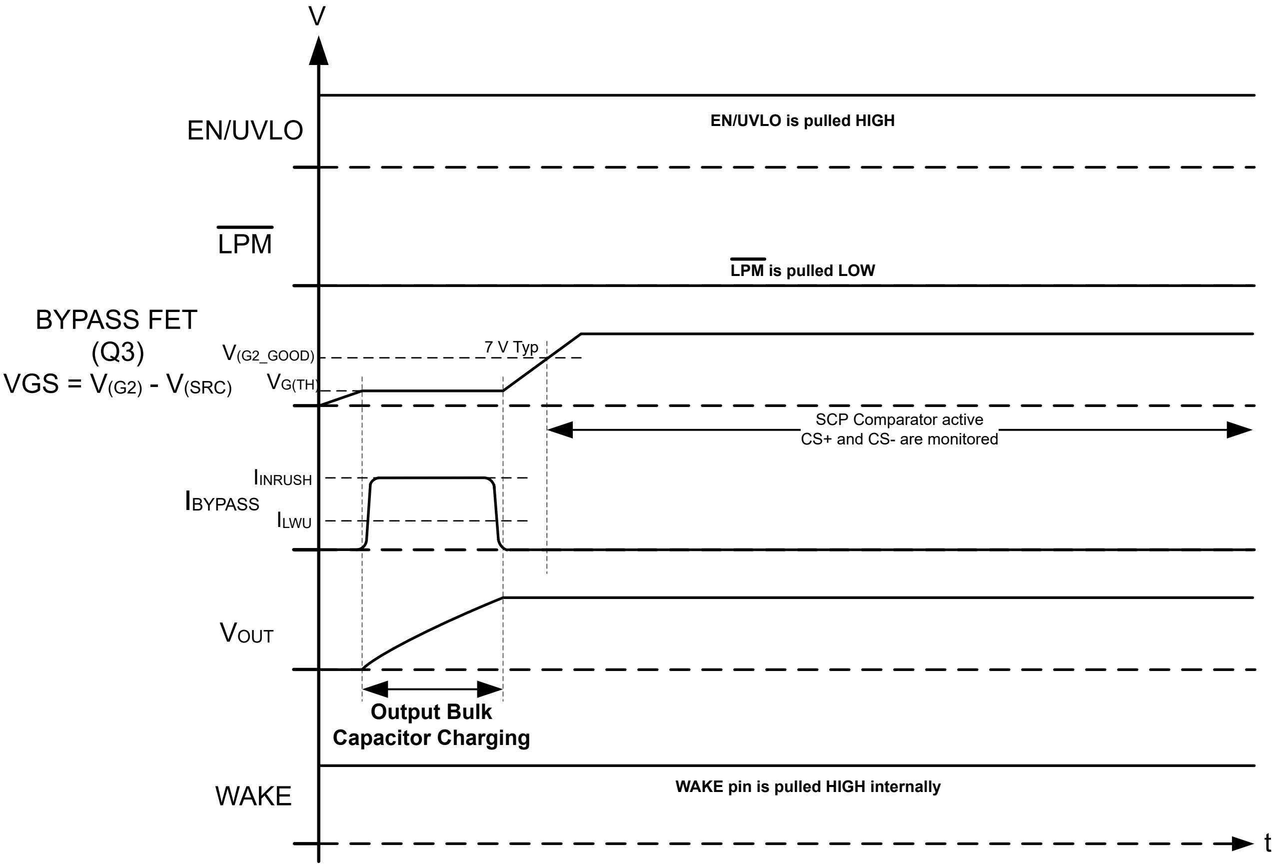


Figure 7-5. Timing Diagram for Output Bulk Capacitor Charging Using Bypass Path

Setting the load wakeup trigger threshold: During normal operation, the series power resistor R_{BYPASS} along with bypass FET R_{DSON} is used to set load wakeup current threshold. R_{BYPASS} can be selected using the following equation:

$$R_{BYPASS}\left(\Omega\right) = \frac{(2\ \mu A \times R_{ISCP} + 10\ mV)}{I_{LWU}} - R_{DSON\_BYPASS} \quad (4)$$

Refer to Equation 13 in Section 8.1.1.2 for update in equation for final revision of IC.

Where,

R_{ISCP} is the resistor selected based on set short-circuit threshold using Equation 8.

I_{LWU} is the desired load current wakeup threshold.

R_{DSON_BYPASS} is the R_{DSON} of bypass FET.

R_{BYPASS} also helps to limit the current as well as stress on Q3 during power up into short-circuit.

7.3.2.2 Using Main FET's (G1 drive) Gate Slew Rate Control

In the applications where low power bypass path is not used, the cap charging can be done using main FET gate drive control.

For limiting inrush current during turn-ON of the main FET with capacitive loads, use R_1, R_2, C_1 as shown in Figure 7-6. The R_1 and C_1 components slow down the voltage ramp rate at the gate of main FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

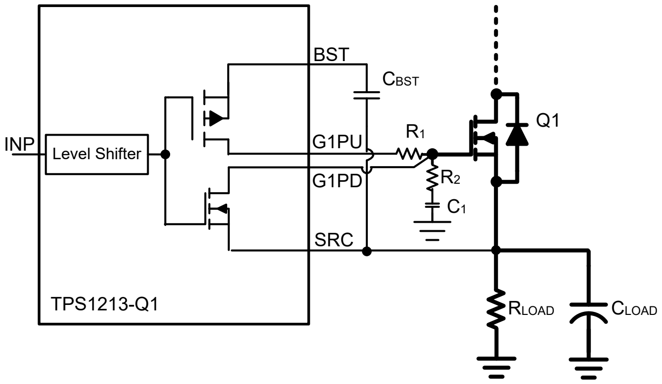


Figure 7-6. Inrush Current Limiting

Use the Equation 5 to calculate the inrush current during turn-ON of the FET.

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \tag{5}$$

$$C_1 = \frac{0.63 \times V_{(BST - SRC)} \times C_{LOAD}}{R_1 \times I_{INRUSH}} \tag{6}$$

Where,

C_{LOAD} is the load capacitance.

VBATT is the input voltage and T_{charge} is the charge time.

$V_{(BST-SRC)}$ is the charge pump voltage (11 V),

Use a damping resistor R_2 (~ 10 Ω) in series with C_1. Equation 6 can be used to compute required C_1 value for a target inrush current. A 100kΩ resistor for R_1 can be a good starting point for calculations.

Connecting G1PD pin of TPS12130-Q1 directly to the gate of the external FET ensures fast turn-OFF without any impact of R_1 and C_1 components.

C_1 results in an additional loading on C_{BST} to charge during turn-ON. Use below equation to calculate the required C_{BST} value:

$$C_{BST} = \frac{Q_{g(total)}}{\Delta V_{BST}} + 10 \times C_1 \tag{7}$$

Where,

$Q_{g(total)}$ is the total gate charge of the FET,

ΔV_{BST} (1 V typical) is the ripple voltage across BST to SRC pins.

7.3.3 Short-Circuit Protection

The TPS12130-Q1 feature adjustable short circuit protection. The threshold and response time can be adjusted using R_{ISCP} resistor and C_{TMR} capacitor respectively. The device senses the voltage across CS+ and CS– pins. These pins can be connected across the FET drain and source terminals for FET R_{DSON} sensing or across an external current sense resistor (R_{SNS}) as shown in Figure 7-7 and Figure 7-8 respectively.

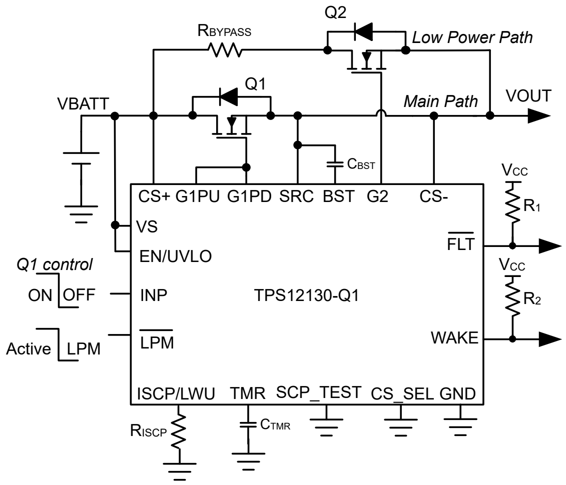


Figure 7-7. TPS12130-Q1 Application Circuit With Main FET RDSON Based Current Sensing

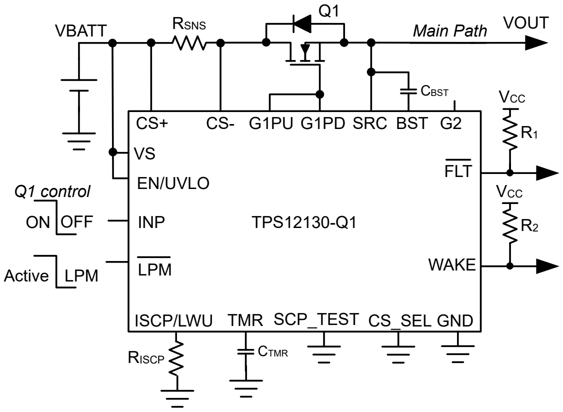


Figure 7-8. TPS12130-Q1 Application Circuit With External Sense Resistor R_{SNS} Based Current Sensing

Set the hard short-circuit detection threshold using an external R_{ISCP} resistor across ISCP/LWU and GND pins. Use Equation 8 to calculate the required R_{ISCP} value:

$$R_{ISCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{SNS} - 10\ \text{mV}\right)}{2\ \mu\text{A}} \tag{8}$$

Refer to Equation 12 in Section 8.1.1.2 section for update in equation in final revision of IC.

Where,

R_{SNS} is the current sense resistor value or the FET R_{DSON} value.

I_{SC} is the desired short circuit current level.

The hard short circuit protection response is fastest < 10µs with no C_{TMR} cap connected across TMR and GND pins.

With device powered ON and EN/UVLO, INP pulled high, during Q1 turn ON, first VGS of main FET is sensed by monitoring the voltage across G1PD to SRC. Once G1PD to SRC voltage raises above $V_{(G1\_GOOD)}$ threshold which ensures that the external FET is enhanced, then the SCP comparator output is monitored. If the sensed voltage across CS+ and CS– exceeds the short-circuit set point ($V_{SCP/LWU}$), G1PD pulls low to SRC and $\overline{\text{FLT}}$ asserts low within 10µs (with TMR pin open). Subsequent events can be set either to be auto-retry or latch off as described in following sections.

7.3.3.1 Short-Circuit Protection With Auto-Retry

The C_{TMR} programs the short-circuit protection delay (t_{SC}) and auto-retry time (t_{RETRY}). Once the voltage across CS+ and CS– exceeds the set point, the C_{TMR} starts charging with 80-µA pull-up current.

After C_{TMR} charges to $V_{(TMR\_SC)}$, G1PD pulls low to SRC and $\overline{\text{FLT}}$ asserts low providing warning on impending FET turn OFF. Post this event, the auto-retry behavior starts. The C_{TMR} capacitor starts discharging with 2.5-uA pulldown current. After the voltage reaches $V_{(TMR\_LOW)}$ level, the capacitor starts charging with 2.2-uA pullup. After 32 charging-discharging cycles of C_{TMR} the FET turns ON back and $\overline{\text{FLT}}$ de-asserts.

The device retry time (t_{RETRY}) is based on C_{TMR} for the first time as per Equation 10 and this retry time (t_{RETRY}) is < 10-µs for subsequent auto-retry events.

Use Equation 9 to calculate the C_{TMR} capacitor to be connected across TMR and GND.

$$C_{TMR} = \frac{I_{TMR} \times t_{SC}}{1.1} \tag{9}$$

Where,

I_{TMR} is internal pull-up current of 80-µA.

t_{SC} is desired short-circuit response time.

The fastest t_{SC} is < 10 µs with no C_{TMR} cap connected.

$$t_{RETRY} = 22.7 \times 10^{6} \times C_{TMR} \tag{10}$$

If the short-circuit pulse duration is below t_{SC} then the FET remains ON and C_{TMR} gets discharged using internal pull down switch.

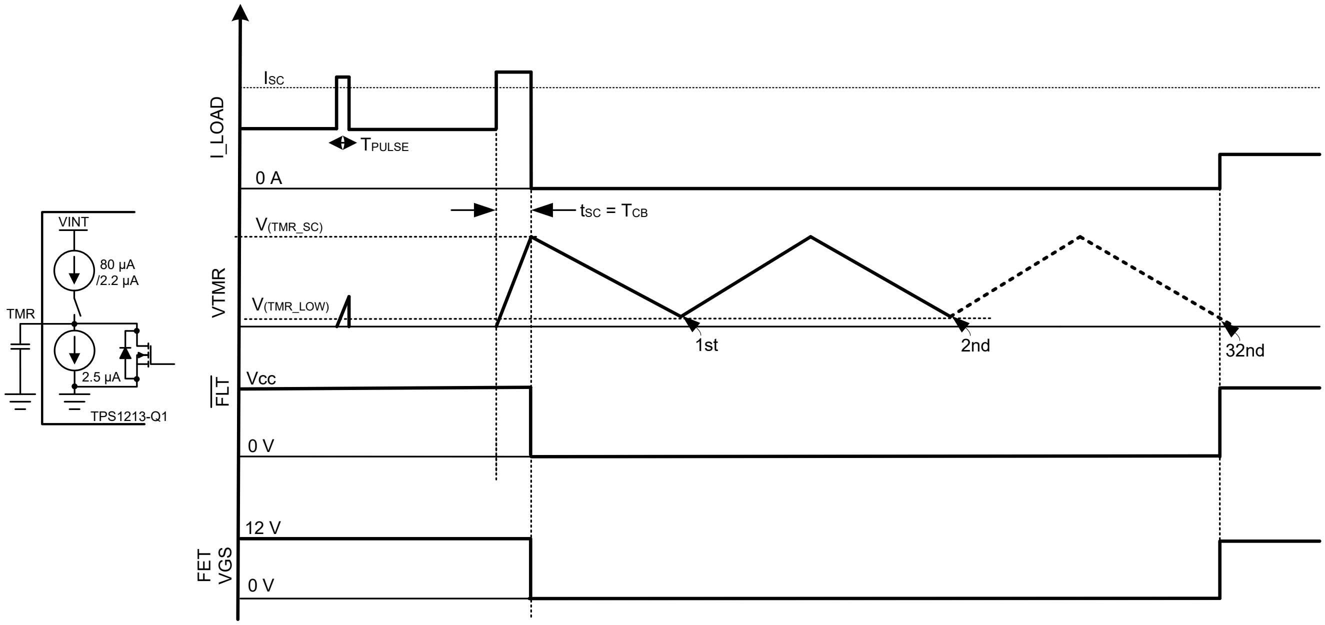


Figure 7-9. Short-Circuit Protection With Auto-Retry

7.3.3.2 Short-Circuit Protection With Latch-Off

Connect an approximately 100-kΩ resistor across C_{TMR} as shown in Figure 7-10 . With this resistor, during the charging cycle, the voltage across C_{TMR} gets clamped to a level below $V_{(TMR\_SC)}$ resulting in a latch-off behavior and $\overline{FLT}$ asserts low at same time.

Use Equation 11 to calculate C_{TMR} capacitor to be connected between TMR and GND for R_{TMR} = 100-kΩ.

$$C_{TMR} = \frac{t_{SC}}{R_{TMR} \times \ln\left(\frac{1}{1 - \frac{1.1}{R_{TMR} \times 80\ \mu A}}\right)} \tag{11}$$

Where,

I_{TMR} is internal pull-up current of 80-µA.

t_{SC} is desired short-circuit response time.

Pull down INP or $\overline{\text{LPM}}$ low or EN/UVLO (below $V_{(ENF)}$) or power cycle VS below $V_{(VS\_PORF)}$ to reset the latch. At low edge, the timer counter is reset and C_{TMR} is discharged. G1PU pulls up to BST when INP is pulled high.

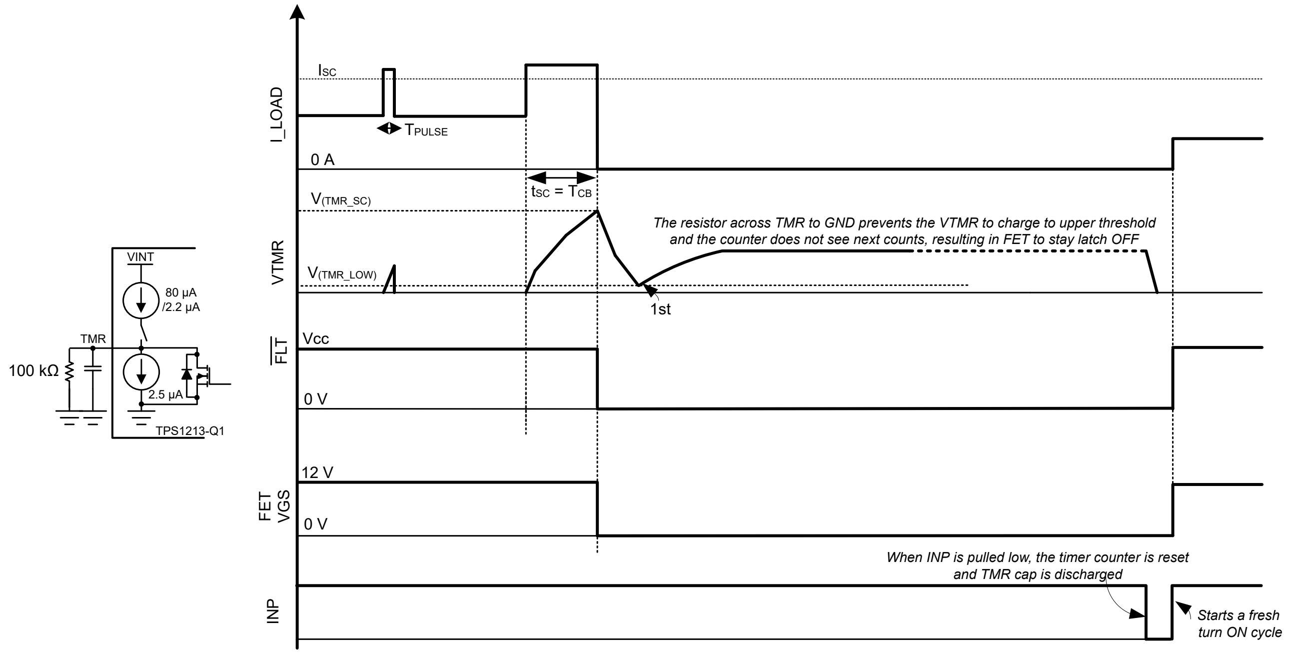


Figure 7-10. Short-Circuit Protection With Latch-Off

7.3.4 Device Functional Modes

7.3.4.1 State Diagram

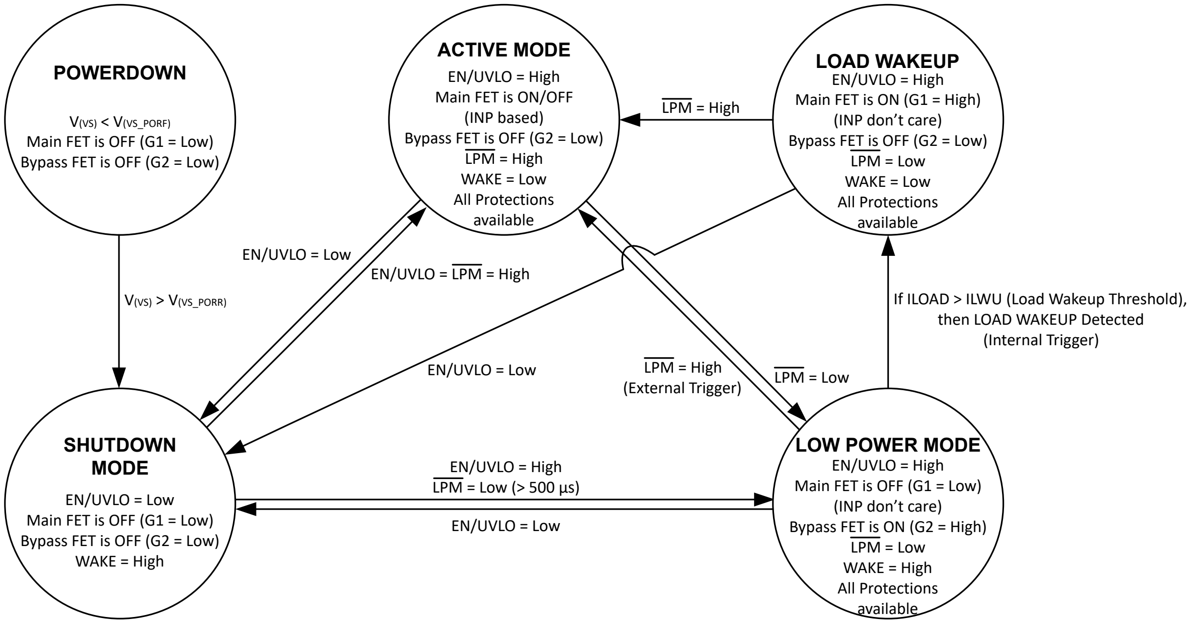


Figure 7-11. TPS12130-Q1 State Diagram

7.3.4.2 State Transition Timing Diagram

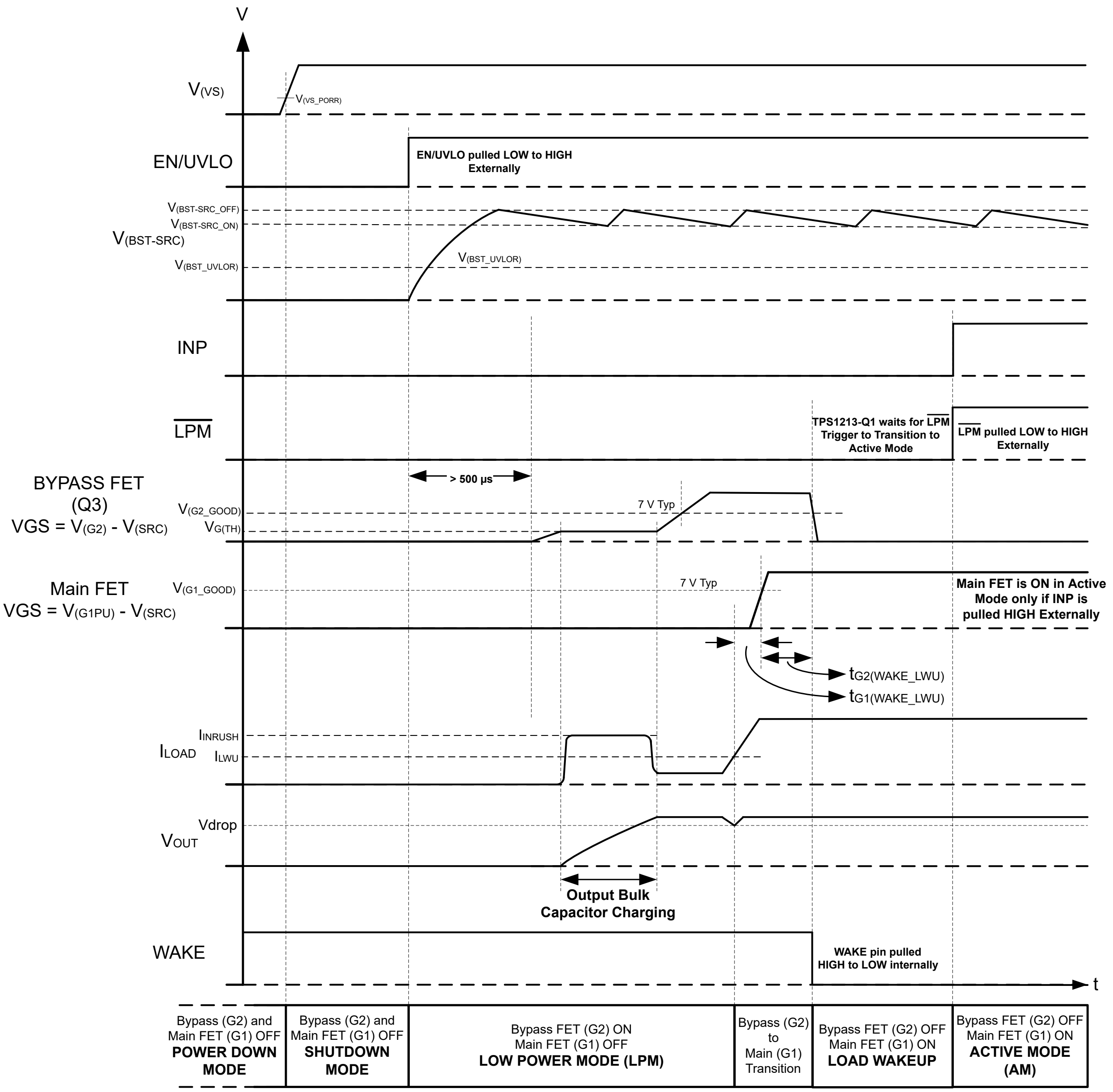


Figure 7-12. State Transition Timing Diagram With Load Wakeup Event

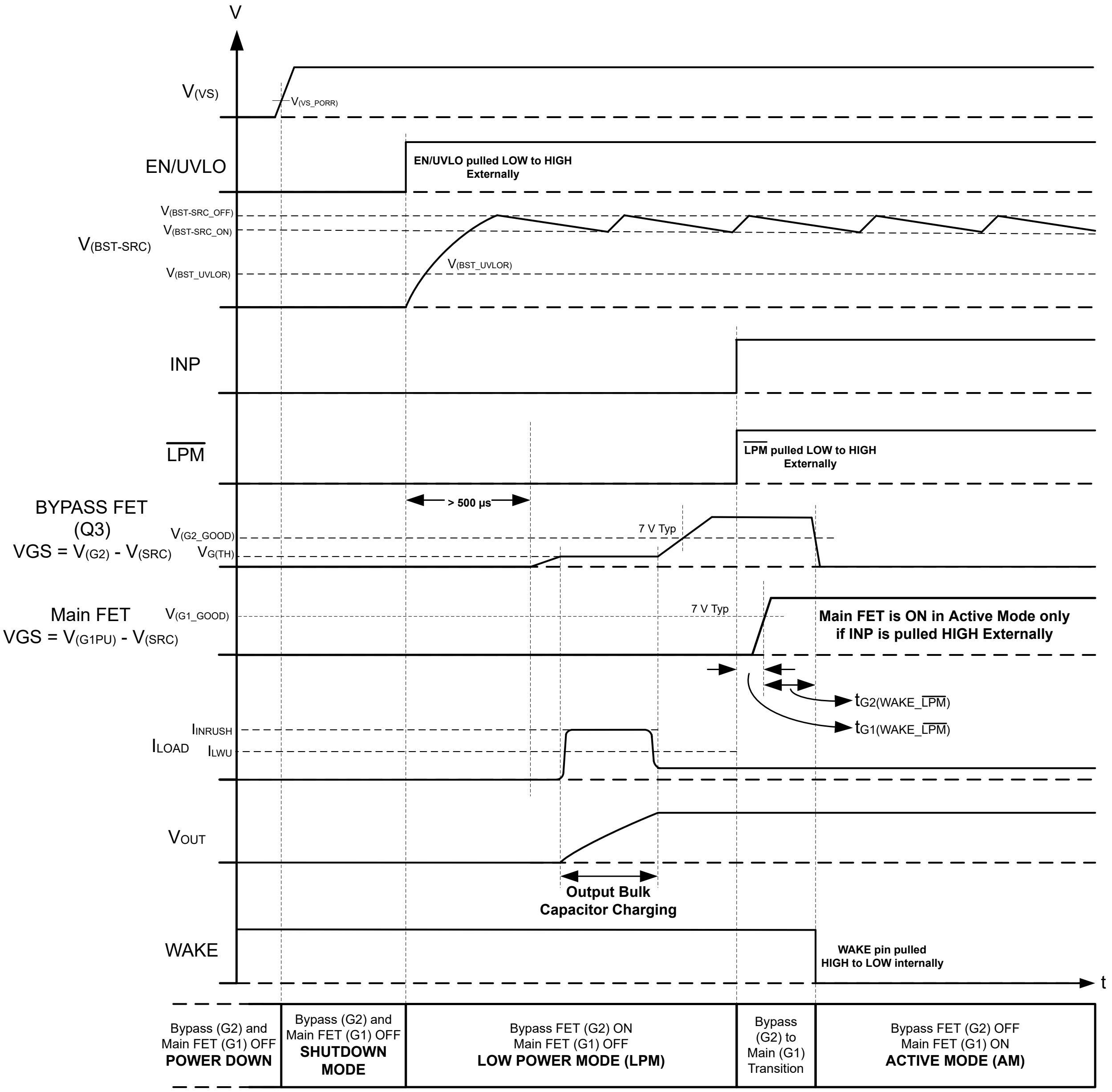


Figure 7-13. State Transition Timing Diagram With $\overline{\text{LPM}}$ Trigger

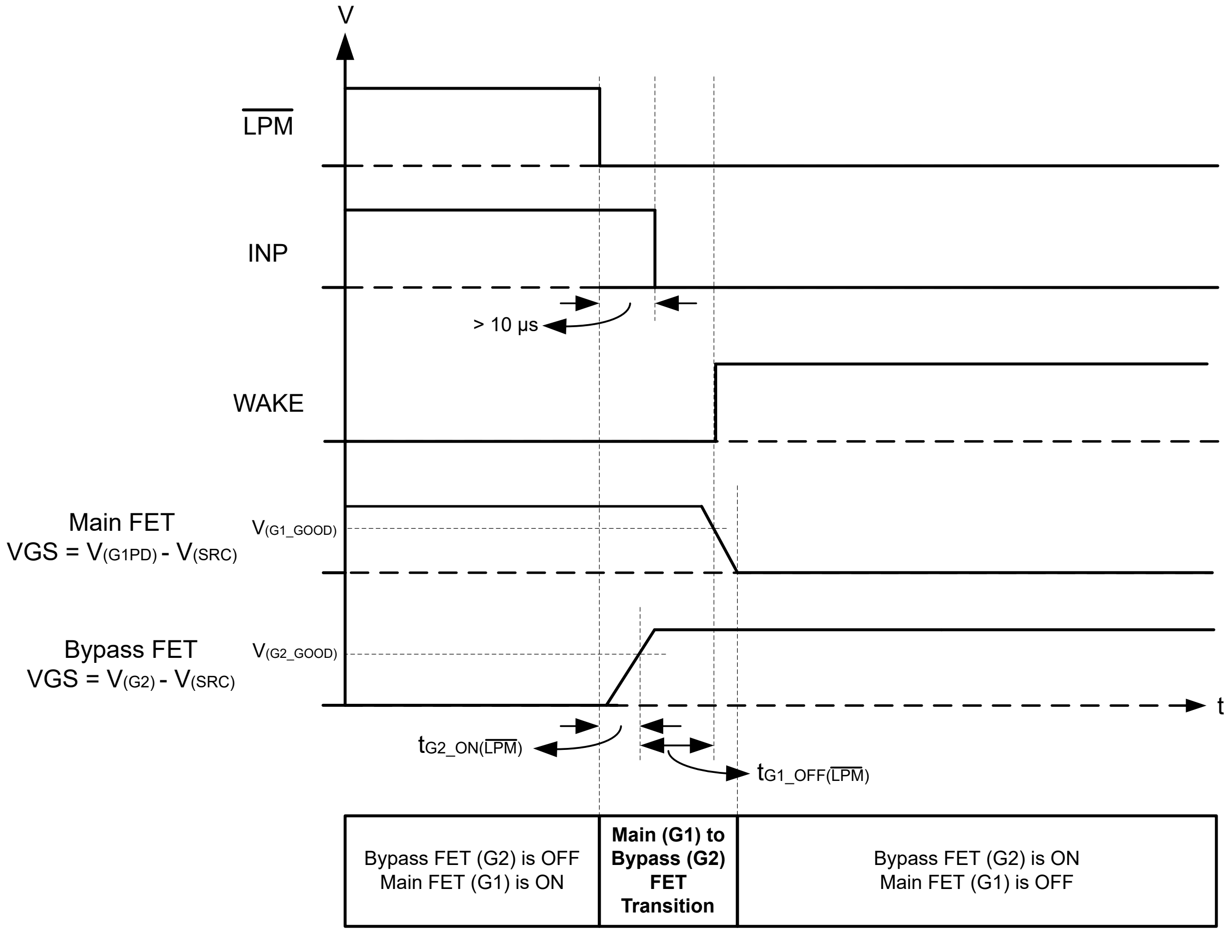


Figure 7-14. $\overline{\text{LPM}}$ and INP Signal Sequencing Consideration to Enter Into Low Power Mode From Active Mode

7.3.4.3 Power Down

If applied VS voltage is below $V_{(VS\_PORF)}$ then the device is in disabled state. In this mode, the charge pump and all the protection features are disabled. Both the gate drive outputs (G1PD and G2) are low.

7.3.4.4 Shutdown Mode

With VS > $V_{(VS\_PORR)}$ and EN/UVLO pulled < $V_{(ENF)}$, the device transitions to low I_Q shutdown mode. In this mode, the charge pump and all the protection features are disabled. Both the gate drive outputs (G1PD and G2) are low. The device consumes low I_Q of 1µA (typical) in this mode.

- **Shutdown to Low Power Mode:**

  To transition from shutdown to low power mode, drive EN/UVLO high (> $V_{(ENR)}$) and simultaneously drive $\overline{\text{LPM}}$ low for > 500µs.
- **Shutdown to Active Mode:**

  To transition from shutdown to active mode directly, drive EN/UVLO and $\overline{\text{LPM}}$ together high at same time.

7.3.4.5 Low Power Mode

The device transitions from shutdown to low power mode when EN/UVLO is driven high (> $V_{(ENR)}$) and $\overline{\text{LPM}}$ is driven low for > 500µs simultaneously.

The device can also transition from active mode to low power mode when $\overline{\text{LPM}}$ is pulled low. When entering from active mode to low power mode, $\overline{\text{LPM}}$ and INP signal sequencing consideration can be followed as per Figure 7-14. Pulling INP low before $\overline{\text{LPM}}$ results in main FET (G1 gate drive) turning OFF which can cause output voltage droop momentarily before bypass FET (G2 gate drive) turns ON. Pulling INP low after at least 10µs of $\overline{\text{LPM}}$ is pulled low makes a seamless transition from active to low power mode without any output voltage dip.

In this mode, charge pump and gate drivers are enabled. The main FET (G1 gate drive) is OFF and bypass FET (G2 gate drive) is turned ON and WAKE pin asserts high in this state. TPS12130-Q1 consumes low I_Q of 35µA (typical) in low power mode.

The device transitions from low power mode to active mode when:

- **External Trigger:** $\overline{\text{LPM}}$ is pulled high externally
- **Internal Trigger:** Load current exceeds load wakeup trigger threshold (I_{LWU}) set by Equation 4

After load current exceeds load wakeup threshold (I_{LWU}), the device automatically turns OFF the bypass FET (G2 gate drive) and turns ON main FET (G1 gate drive) and WAKE asserts low indicating the exit from the low power mode.

The device waits for external $\overline{\text{LPM}}$ signal to go high to transition into Active mode.

Protections available in low power mode are:

- Input UVLO: Bypass FET (G2 gate drive) is turned OFF when voltage on EN/UVLO falls below $V_{(UVLOF)}$ and $\overline{\text{FLT}}$ asserts low.
- Charge pump UVLO: Bypass FET (G2 gate drive) is turned OFF when voltage between BST to SRC falls below $V_{(BST\_UVLOF)}$ and $\overline{\text{FLT}}$ asserts low.
- Short-circuit protection: If output short-circuit event occurs in low power mode then, the device automatically exits low power mode by turning OFF the bypass FET (G2 gate drive) and turning ON main FET (G1 gate drive) via the load wakeup functionality. In load wakeup state, if the voltage across CS+ and CS– exceeds the set short-circuit threshold ($V_{SCP/LWU}$), main FET (G1 gate drive) is turned OFF and $\overline{\text{FLT}}$ asserts low. The subsequent operation is based on auto-retry or latch off as per the configuration.

7.3.4.6 Active Mode

The device transitions from shutdown mode to active mode directly when EN/UVLO and $\overline{\text{LPM}}$ are driven high together at same time.

TPS12130-Q1 transitions from low power mode into active mode by:

- **External Trigger:** Drive $\overline{\text{LPM}}$ high externally.
- **Internal Trigger:** After load current exceeds load wakeup threshold (I_{LWU}), TPS12130-Q1 automatically turns OFF the bypass FET (G2 gate drive). Drive $\overline{\text{LPM}}$ high after load wakeup event to switch to active mode.

In this mode, charge pump, gate drivers and all protections are enabled. The main FET (G1 gate drive) can be tuned ON or OFF by driving INP high or low respectively and bypass FET (G2 gate drive) is turned OFF and WAKE pin asserts low in this state.

The device exits active mode and enters low power mode when $\overline{\text{LPM}}$ is pulled low.

Protections available in active state are:

- Input UVLO: Main FET (G1 gate drive) is turned OFF when voltage on EN/UVLO falls below $V_{(UVLOF)}$ and $\overline{\text{FLT}}$ asserts low.
- Charge pump UVLO: Main FET (G1 gate drive) is turned OFF when voltage between BST to SRC falls below $V_{(BST\_UVLOF)}$ and $\overline{\text{FLT}}$ asserts low.

- Short-circuit protection: Main FET (G1 gate drive) is turned OFF when voltage across CS+ and CS– exceeds the set short-circuit threshold ($V_{SCP/LWU}$). The device goes in auto-retry or latch-off based on the selected configuration and $\overline{\text{FLT}}$ asserts low.

7.3.5 Undervoltage Protection (UVLO)

TPS12130-Q1 has an accurate undervoltage protection (< ±2%) using EN/UVLO pin providing robust protection. Connect a resistor ladder as shown in Figure 7-15 for undervoltage protection threshold programming.

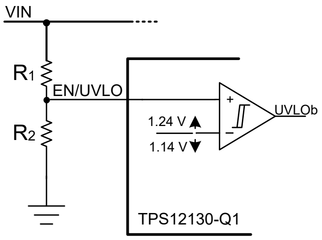


Figure 7-15. Programming Undervoltage Protection Threshold

7.3.6 Reverse Polarity Protection

The TPS12130-Q1 devices features integrated reverse polarity protection to protect the device from failing during input and output reverse polarity faults. Reverse polarity faults occur during installation and maintenance of the end equipment's. The device is tolerant to reverse polarity voltages down to -40 V both on input and on the output.

On the output side, the device can see transient negative voltages during regular operation due to output cable harness inductance kickbacks when the switches are turned OFF. In such systems the output negative voltage level is limited by the output side TVS or a diode.

7.3.7 Short-Circuit Protection Diagnosis (SCP_TEST)

In the safety critical designs, short-circuit protection (SCP) feature and its diagnosis is important.

The TPS12130-Q1 features the diagnosis of the internal short circuit protection. When SCP_TEST is driven low to high then, a voltage is applied internally across the SCP comparator inputs to simulate a short circuit event. The comparator output controls the gate drive (G1PU/G1PD) and also the $\overline{\text{FLT}}$. If the gate drive goes low (with initially being high) and $\overline{\text{FLT}}$ also goes low then it indicates that the SCP is good otherwise it is to be treated as SCP feature is not functional.

If the SCP_TEST feature is not used, then connect SCP_TEST pin to GND.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS12130-Q1 is a 45V low I_Q smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5V–40V and features such as low power mode with automatic load wakeup functionality, short circuit protection the device is suitable for 12V power distribution system designs. The device can also withstand and protect the loads from negative supply voltages down to –40V.

The following design procedure can be used to select the supporting component values based on the application requirement.

8.1.1 Application Limitations

8.1.1.1 Short-Circuit Protection Delay

In application designs with current sense configurations as shown in Figure 7-7 and Figure 7-8 with C_{TMR} = Open, the short-circuit protection delay during power up with output short circuited does not match the specified maximum value of 10μs.

Testing has shown that the actual short-circuit protection delay during power up by EN/UVLO signal is approximately 70 μs. This increase in protection delay still allows for the TPS12130-Q1 to operate as designed, but results in larger power dissipation in the external MOSFET during output short-circuit scenario.

A design fix must be included in the final version of the IC.

8.1.1.2 Short-Circuit Protection and Load wakeup Threshold

The minimum short-circuit protection threshold is limited to 30mV.

A design update is planned in the final revision of the IC to extend the minimum threshold down to 20mV. Due to the design update there will be a change of R_{ISCP} resistor formula and the revised formula will be as per the Equation 12:

$$R_{ISCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{SNS}\ -\ 19\ \text{mV}\right)}{2\ \mu\text{A}} \tag{12}$$

$$R_{BYPASS}\left(\Omega\right) = \frac{\left(2\ \mu\text{A}\ \times\ R_{ISCP}\ +19\ \text{mV}\right)}{I_{LWU}} - R_{DSON\_BYPASS} \tag{13}$$

Lowest SCP threshold setting will be limited to 20mV.

8.2 Typical Application 1: Driving Power at all times (PAAT) Loads With Automatic Load Wakeup

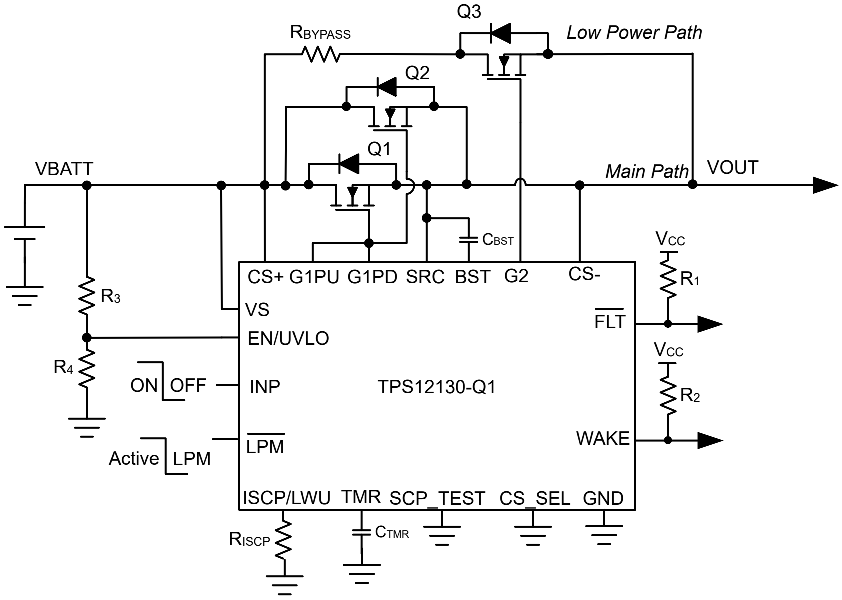


Figure 8-1. TPS12130-Q1 Application circuit for driving power at all times (PAAT) loads with automatic load wakeup

8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{BATT_MIN} to V_{BATT_MAX}	8 to 16 V
Undervoltage lockout set point, V_{INUVLO}	6.5 V
Maximum load current, I_{OUT}	40 A
Short-circuit protection threshold, I_{SC}	100 A
Fault timer period (t_{SC})	50 µs
Fault response	Auto-retry
Load wakeup threshold, I_{LWU}	50 mA

8.2.2 Detailed Design Procedure

Selection of MOSFET, Q_1 and Q_2

For selecting the MOSFET Q_1 and Q_2, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application. Considering 35 V as the maximum application voltage due to load dump, MOSFETs with V_{DS} voltage rating of 40 V is chosen for this application.

The maximum V_{GS} TPS12130-Q1 can drive is 11 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected.

To reduce the MOSFET conduction losses, an appropriate $R_{DS(ON)}$ is preferred.

Based on the design requirements, two of BUK7J1R4-40H are selected and its ratings are:

- 40-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 1.06-mΩ typical at 10-V V_{GS}
- MOSFET $Q_{g(total)}$ is 73 nC typical

TI recommends to make sure that the short-circuit conditions such max V_{IN} and I_{SC} are within SOA of selected FETs (Q_1 and Q_2) for > t_{SC} timing.

Selection of Bootstrap Capacitor, C_{BST}

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 345 µA. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving two parallel BUK7J1R4-40H MOSFETs

$$C_{BST} = \frac{Q_{g(total)}}{1\ \text{V}} = 2 \times 73\ \text{nF} = 146\ \text{nF} \tag{14}$$

Choose closest available standard value: 150 nF, 10 %.

Programming the Short-Circuit Protection Threshold – R_{ISCP} Selection

The R_{ISCP} sets the short-circuit protection threshold, whose value can be calculated using

$$R_{ISCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{DS\_ON} - 10\ \text{mV}\right)}{2\ \mu\text{A}} \tag{15}$$

Refer to Equation 12 in Section 8.1.1.2 section for update in equation in final revision of IC.

To set 100 A as short-circuit protection threshold, R_{ISCP} value is calculated to be 20 kΩ for two FETs in parallel.

Choose the closest available standard value: 20.2 kΩ, 1%.

Programming the Fault timer Period – C_{TMR} Selection

For the design example under discussion, overcurrent transients are allowed for 50-µs duration. This blanking interval, t_{SC} (or circuit breaker interval, T_{CB}) can be set by selecting appropriate capacitor C_{TMR} from TMR pin to ground. The value of C_{TMR} to set 50 µs for t_{SC} can be calculated using following equation:

$$C_{TMR} = \frac{80\ \mu\text{A} \times t_{SC}}{1.1} \tag{16}$$

Choose closest available standard value: 3.3 nF, 10%.

TMR pin can be left floating for fast reponse of t_{SC} < 10 µs.

Programming the Load Wakeup Threshold – R_{BYPASS} and Q_3 Selection

During normal operation, the resistor R_{BYPASS} along with bypass FET R_{DSON} is used to set load wakeup current threshold.

For selecting the MOSFET Q_3, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance R_{DSON}.

Based on the design requirements, BUK6D23-40E is selected and its ratings are:

- 40-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 17-mΩ typical at 10-V V_{GS}
- MOSFET $Q_{g(total)}$ is 11 nC typical
- MOSET $V_{GS(th)}$ is 1.3 V min
- MOSFET C_{ISS} is 582 pF typical

The recommended range of the short-circuit threshold voltage which is same as load wakeup threshold, $V_{(SCP/LWU)}$, extends from 30 mV to 500 mV. Values near the low threshold of 30 mV can be affected by the system noise. Values near the upper threshold of 500 mV would result in high short-circuit current threshold. To minimize both the concerns, 50 mV is selected as the short-circuit or load wakeup threshold voltage.

The $V_{(SCP/LWU)}$ value can also be calculated based on selected R_{ISCP} resistor by following equation:

$$V_{(SCP/LWU)}\left(\text{mV}\right) = 2\ \mu\text{A} \times R_{ISCP} + 10\ \text{mV} \quad (17)$$

R_{BYPASS} resistor value can be selected using below equation:

$$R_{BYPASS} = \frac{V_{(SCP/LWU)}}{I_{LWU}} - R_{DSON\_BYPASS} \quad (18)$$

Refer to Equation 13 in Section 8.1.1.2 section for update in equation in final revision of IC.

To set 50 mA as load wakeup threshold, R_{BYPASS} value is calculated to be ~ 1 Ω.

The average power rating of the bypass resistor can be calculated by following equation:

$$P_{AVG} = I_{LWU}^{2} \times R_{BYPASS} \quad (19)$$

The average power dissipation of R_{BYPASS} is calculated to be ~ 0.0025 W

The peak power dissipation in the bypass resistor is given by following equation:

$$P_{PEAK} = \frac{V_{BATT\_MAX}^{2}}{R_{BYPASS}} \quad (20)$$

The peak power dissipation of R_{BYPASS} is calculated to be ~ 256 W

The peak power dissipation time for power-up with short into LPM can be calculated based on following equation:

$$T_{PULSE} = C_{ISS} \times \frac{\left(V_{(G2\_GOOD)} - V_{GS(th)}\right)}{I_{(G2)}} + 10\ \mu\text{s} \quad (21)$$

where,

$V_{(G2\_GOOD)}$ is internal threshold with 7 V (typical) value,

$I_{(G2)}$ is 165 µA (typical),

$V_{GS(th)}$ is gate to source voltage and C_{ISS} is effective input capacitance of selected bypass FET.

Based on Equation 21, T_{PULSE} is calculated to be ~ 32 µs.

One 1-Ω, 1.5-W, 1% CRCW25121R00JNEGHP resistor is used to support both average and peak power dissipation for > T_{PULSE} time calculated in Equation 21.

TI suggests the designer to share the entire power dissipation profile of bypass resistor with the resistor manufacturer and get their recommendation.

ADVANCE INFORMATION

The peak short-circuit current in bypass path can be calculated based on following equation:

$$I_{PEAK\_BYPASS} = \frac{V_{IN\_MAX}}{R_{BYPASS}} \tag{22}$$

I_{PEAK_BYPASS} is calculated to be 16-A based on R_{BYPASS} selected in Equation 18.

Setting the Undervoltage Lockout Set Point, R_3 and R_4

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider network of R_3 and R_4 connected between VS, EN/UVLO and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving below equation:

$$V_{(UVLOR)} = V_{INUVLO} \times \frac{R_4}{R_3 + R_4} \tag{23}$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for R_3 and R_4. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I_{(R34)}$ must be chosen to be 20 times greater than the leakage current of UVLO pin.

From the device electrical specifications, $V_{(UVLOR)}$ = 1.24 V. From the design requirements, V_{INUVLO} is 6.5 V. To solve the equation, first choose the value of R_3 = 470 kΩ and use Equation 23 to solve for R_4 = 107.5 kΩ.

Choose the closest standard 1% resistor values: R_3 = 470 kΩ, and R_4 = 107 kΩ.

8.2.3 Application Curves

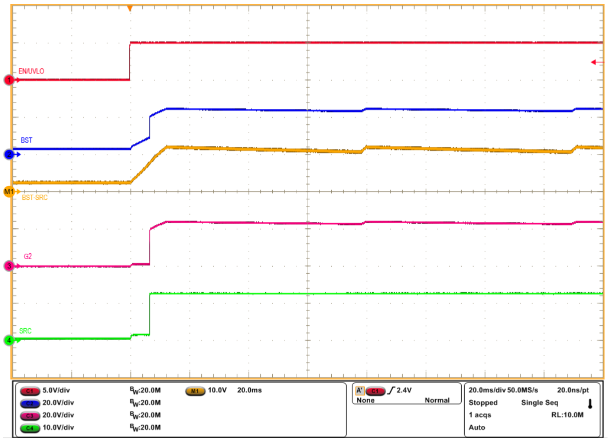


Figure 8-2. Start-Up Profile of Low Power Path ($\overline{\text{LPM}}$ = Low, VIN = 12V, No Load, CBST = 470nF)

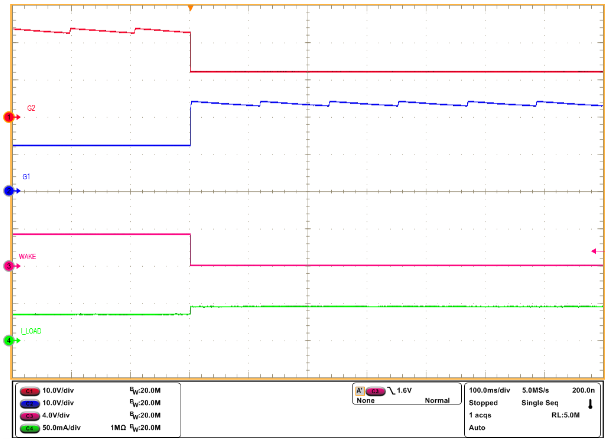


Figure 8-3. State Transition From LPM to Active Mode ($\overline{\text{LPM}}$ = Low, VIN = 12V, EN/UVLO = High)

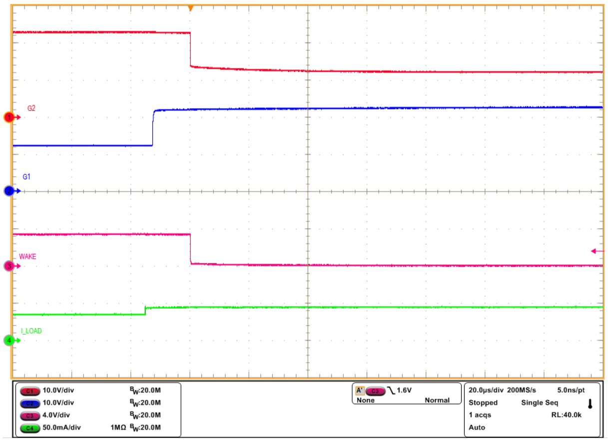


Figure 8-4. Zoom-In View of State Transition From LPM to Active Mode ($\overline{\text{LPM}}$ = Low, VIN = 12V, EN/UVLO = High)

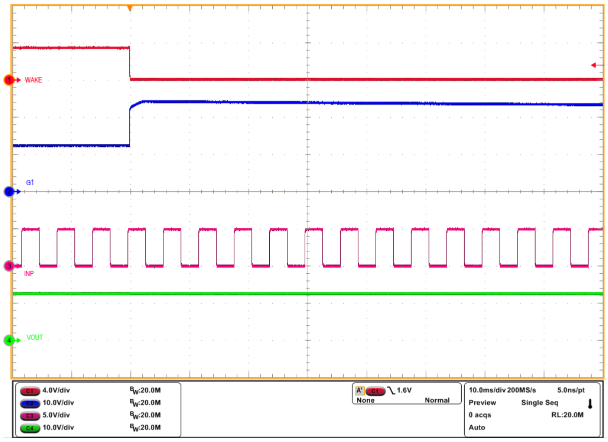


Figure 8-5. As $\overline{\text{LPM}}$ = Low, INP Has No Control on G1 Even After WAKEUP

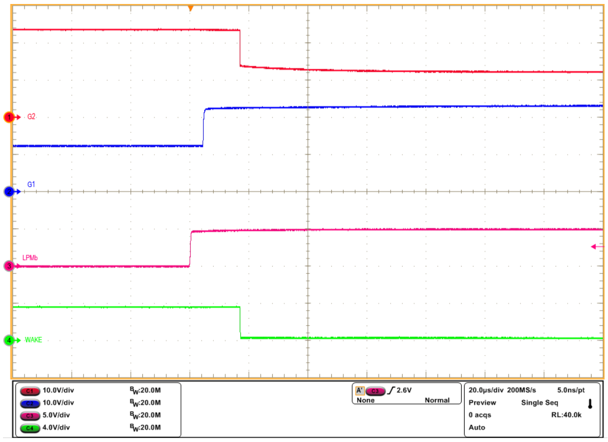


Figure 8-6. State Transition From LPM to Active Mode ($\overline{\text{LPM}}$ = Low to High, VIN = 12V, No Load)

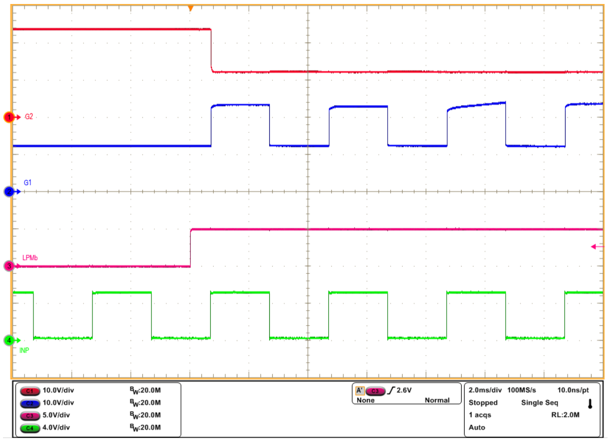


Figure 8-7. With $\overline{\text{LPM}}$ = Low to High, INP Gained Control on G1 (VIN = 12V, No Load)

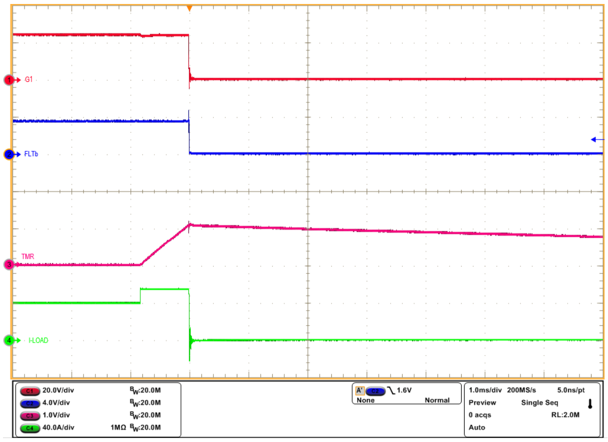


Figure 8-8. Overcurrent Response of TPS1213-Q1 EVM for 40A to 55A Load Step

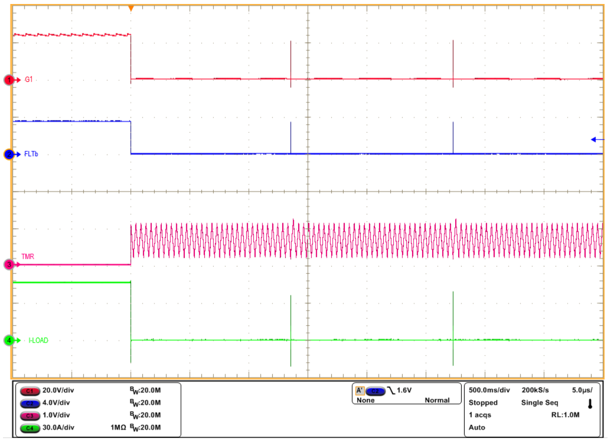


Figure 8-9. Auto-Retry Response of TPS12130-Q1 for an Overcurrent Fault

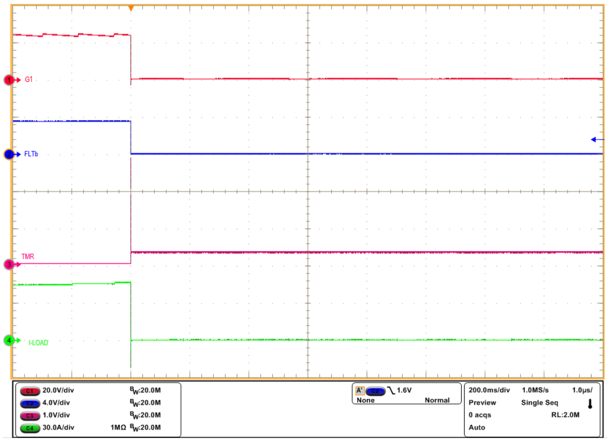


Figure 8-10. Latch-Off Response of TPS12130-Q1 for an Overcurrent Fault

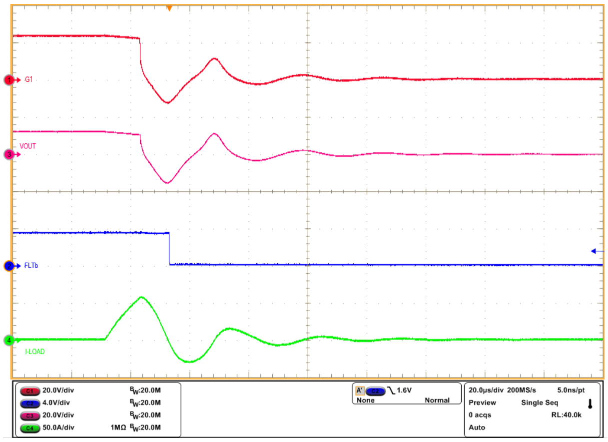


Figure 8-11. Output Short-Circuit Response of TPS12130-Q1

8.3 Typical Application 2: Driving Power at all times (PAAT) Loads With Automatic Load Wakeup and Output Bulk Capacitor Charging

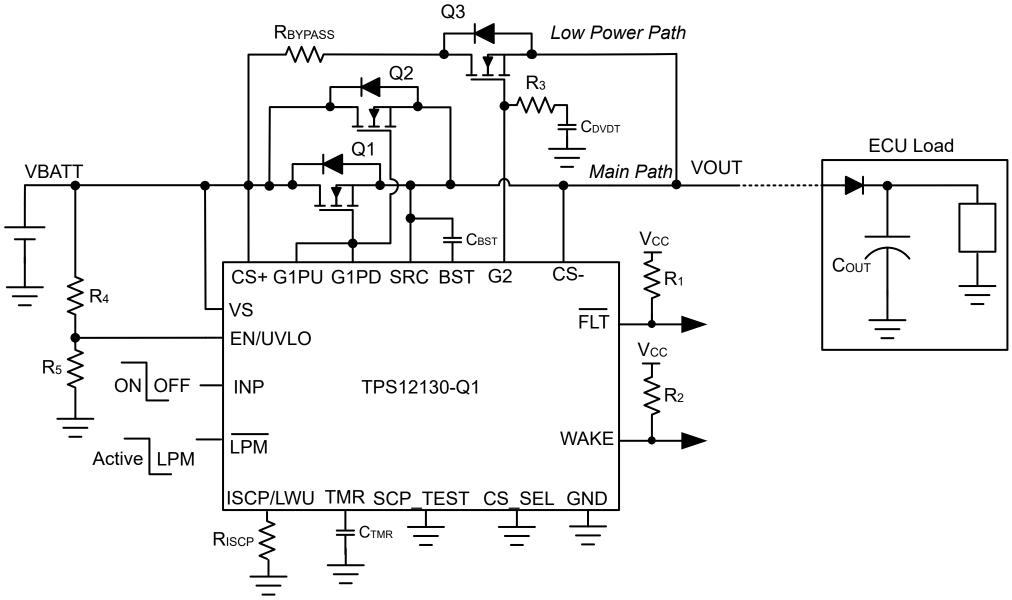


Figure 8-12. TPS12130-Q1 Application circuit for driving power at all times (PAAT) loads with automatic load wakeup and output bulk capacitor charging

8.3.1 Design Requirements

Table 8-2. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{BATT_MIN} to V_{BATT_MAX}	8 to 16 V
Undervoltage lockout set point, V_{INUVLO}	6.5 V
Maximum load current, I_{OUT}	40 A
Output bulk capacitor, C_{OUT}	220 µF
C_{OUT} charging time, T_{charge}	2 ms
Short-circuit protection threshold, I_{SC}	100 A
Fault timer period (t_{SC})	50 µs
Fault response	Auto-retry
Load wakeup threshold, I_{LWU}	50 mA

8.3.2 External Component Selection

By following similar design procedure as outlined in Section 8.2.2, the external component values are calculated as below:

- C_{BST} = 150 nF
- R_{ISCP} = 20.2 kΩ to set 100 A as short-circuit protection threshold
- C_{TMR} = 3.3 nF to set 50 µs short-circuit protection delay
- R4 and R5 are selected as 470 kΩ and 107 kΩ respectively to set VIN undervoltage lockout threshold at 6.5 V

Programming the Inrush current – R_3 and C_{DVDT} Selection

Use following equation to calculate the I_{INRUSH}:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{BATT\_MAX}}{T_{charge}} \quad (24)$$

Use following equation to calculate the required C_g based on I_{INRUSH} calculated in Equation 24.

$$C_g = \frac{C_{LOAD} \times I_{(G)}}{I_{INRUSH}} \quad (25)$$

Where,

$I_{(G)}$ is 165 µA (typical),

To set I_{INRUSH} at 1.76 A, C_g value is calculated to be ~ 20.6 nF.

A series resistor R_g must be used in conjunction with C_g to limit the discharge current from C_g during turn-off . The chosen value of R_3 is 100 Ω and C_g is 22 nF.

Programming the Load Wakeup Threshold – R_{BYPASS} and Q_3 Selection

During normal operation, the resistor R_{BYPASS} along with bypass FET R_{DSON} is used to set load wakeup current threshold.

For selecting the MOSFET Q_3, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance R_{DSON}.

Based on the design requirements, BUK7J1R4-40H is selected and its ratings are:

- 40-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 1.06-mΩ typical at 10-V V_{GS}
- MOSFET $Q_{g(total)}$ is 73 nC typical
- MOSET $V_{GS(th)}$ is 2.4 V min
- MOSFET C_{ISS} is 5.4 nF typical

The recommended range of the short-circuit threshold voltage which is same as load wakeup threshold, $V_{(SCP/LWU)}$, extends from 30 mV to 500 mV. Values near the low threshold of 30 mV can be affected by the system noise. Values near the upper threshold of 500 mV would result in high short-circuit current threshold. To minimize both the concerns, 50 mV is selected as the short-circuit or load wakeup threshold voltage.

The $V_{(SCP/LWU)}$ value can also be calculated based on selected R_{ISCP} resistor by following equation:

$$V_{(SCP/LWU)}\left(mV\right) = 2\ \mu A \times R_{ISCP} + 10\ mV \quad (26)$$

R_{BYPASS} resistor value can be selected using below equation:

$$R_{BYPASS} = \frac{V_{(SCP/LWU)}}{I_{LWU}} - R_{DSON\_BYPASS} \quad (27)$$

Refer to Equation 13 in Section 8.1.1.2 section for update in equation in final revision of IC.

To set 50 mA as load wakeup threshold, R_{BYPASS} value is calculated to be ~ 1 Ω.

The average power rating of the bypass resistor can be calculated by following equation:

$$P_{AVG} = I_{LWU}{}^2 \times R_{BYPASS} \quad (28)$$

The average power dissipation of R_{BYPASS} is calculated to be ~ 0.0025 W

The peak power dissipation in the bypass resistor is given by following equation:

$$P_{PEAK} = \frac{V_{BATT\_MAX}^{\ 2}}{R_{BYPASS}} \quad (29)$$

The peak power dissipation of R_{BYPASS} is calculated to be ~ 256 W

The peak power dissipation time for power-up with short into LPM can be calculated based on following equation:

$$T_{PULSE} = C_{ISS} \times \frac{\left(V_{(G2\_GOOD)} - V_{GS(th)}\right)}{I_{(G2)}} + 10\ \mu s \quad (30)$$

where,

$V_{(G2\_GOOD)}$ is internal threshold with 7 V (typical) value,

$I_{(G2)}$ is 165 µA (typical),

$V_{GS(th)}$ is gate to source voltage and C_{ISS} is effective input capacitance of selected bypass FET.

Based on Equation 30, T_{PULSE} is calculated to be ~ 769 µs.

One 1-Ω, 1.5-W, 1% CRCW25121R00FKEGHP resistor is used to support both average and peak power dissipation for > T_{PULSE} time calculated in Equation 30.

TI suggests the designer to share the entire power dissipation profile of bypass resistor with the resistor manufacturer and get their recommendation.

The peak short-circuit current in bypass path can be calculated based on following equation:

$$I_{PEAK\_BYPASS} = \frac{V_{IN\_MAX}}{R_{BYPASS}} \quad (31)$$

I_{PEAK_BYPASS} is calculated to be 16-A based on R_{BYPASS} selected in Equation 27.

TI suggest the designer to ensure that operating point (V_{BATT_MAX}, I_{PEAK_BYPASS}) for bypass path (Q_3) is within the SOA curve for > T_{PULSE} time calculated in Equation 30.

8.3.3 Application Curves

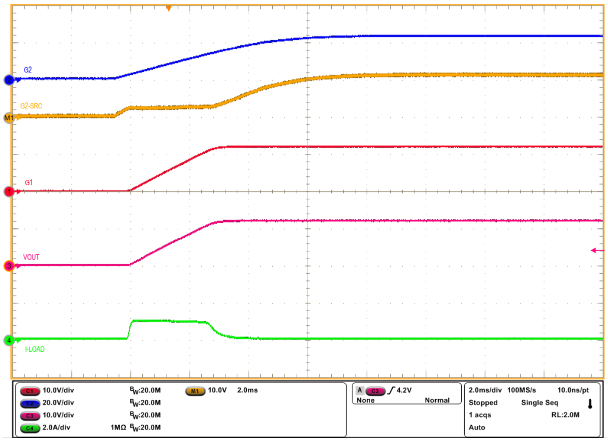


Figure 8-13. Inrush Current Profile with 220 µF at the Output ($\overline{\text{LPM}}$ = Low)

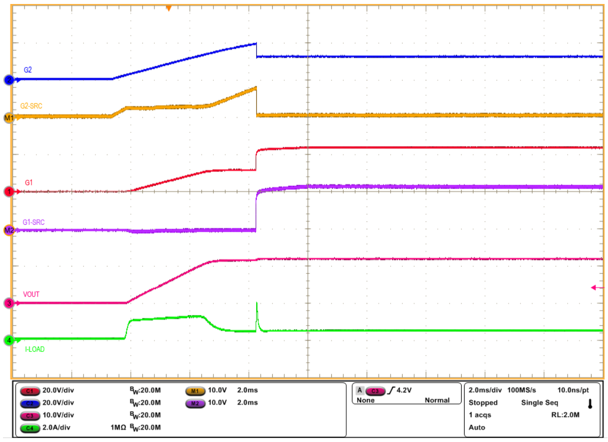


Figure 8-14. Inrush Current Profile with 220 µF at the Output and 0.5 A Load ($\overline{\text{LPM}}$ = Low)

8.4 TIDA-020065: Automotive Smart Fuse Reference Design driving Power at all times (PAAT) Loads With Automatic Load Wakeup, Output Bulk Capacitor Charging, Bi-directional Current Sensing and Software I2t

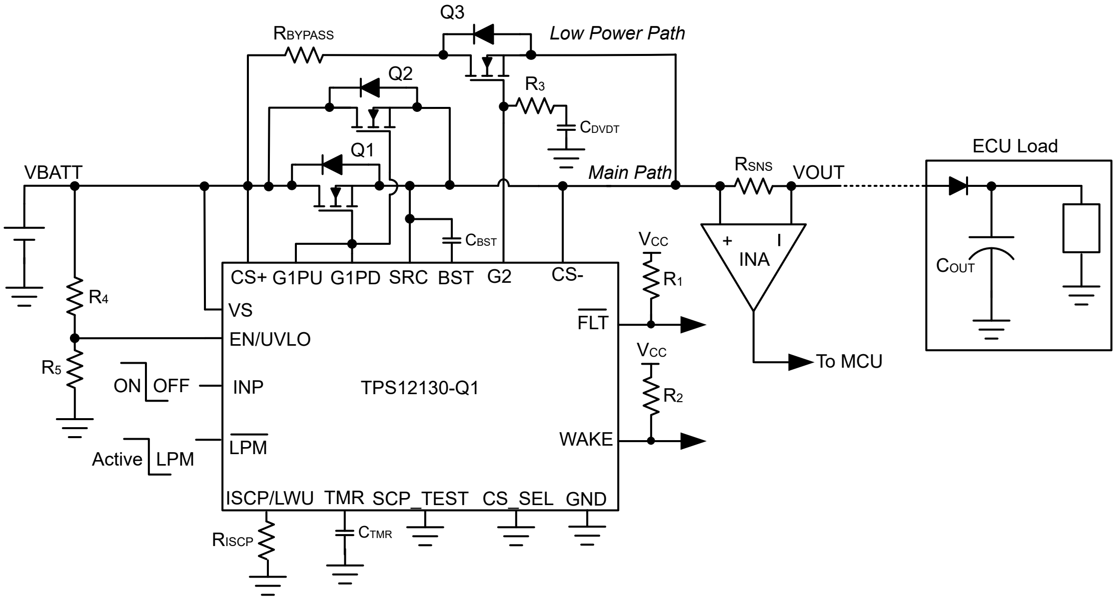


Figure 8-15. Always ON Automotive E-fuse with Bi-directional current sensing and Software I2t

The TIDA-020065 automotive smart fuse design is targeted for power-distribution box and zone-control module systems. As vehicles shift from domain-based architecture to zone-based architecture, these systems aim to replace the standard melting fuse with a semiconductor design to allow for the following:

1. Resettable fuses, which allow for optimized cable wiring as fuses no longer need to be in an easily-accesible location.
2. Improved time-current characteristics across temperature, which allows for optimized harness cable diameter and reduced cost due to less variability between devices compared to standard melting fuses.

Nevertheless, replacing the melting fuse introduces the following challenges:

1. Wire harness protection during overload and short-circuit events while avoiding tripping during peak load transient events
2. Protect the FETs from uncontrolled inrush currents while charging load bulk capacitors
3. Reducing semiconductor power consumption in key-off state for powered-at-all-times loads

The TIDA-020065 aims to demonstrate how these challenges can be addressed at a system level for highcurrent loads. This design features the TPS12130-Q1 device for driving a main power path in the drive state, and a low power path for the key-off state. This design also features the INA296B3-Q1 device which is used to sense the load current so the MSPM0L1306-Q1 can run a software-based I2t algorithm to replicate fuse behavior.

8.5 Power Supply Recommendations

When the external MOSFETs turn-OFF during the conditions such as INP control, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS12130-Q1 gets powered from the VS pin. Voltage at this pin must be maintained above $V_{(VS\_PORR)}$ level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place a R_{VS} – C_{VS} filter between the input supply line and VS pin to filter out the supply noise. TI recommends an R_{VS} value around 100Ω.

In a case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS+ and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add a placeholder for RC filter components across the sense resistor (R_{SNS}) and tweak the values during test in the real system. The RC filter components must not be used in current sense designs by MOSFET VDS sensing to avoid impact on the short-circuit protection response.

Figure 8-16 shows the circuit implementation with optional protection components.

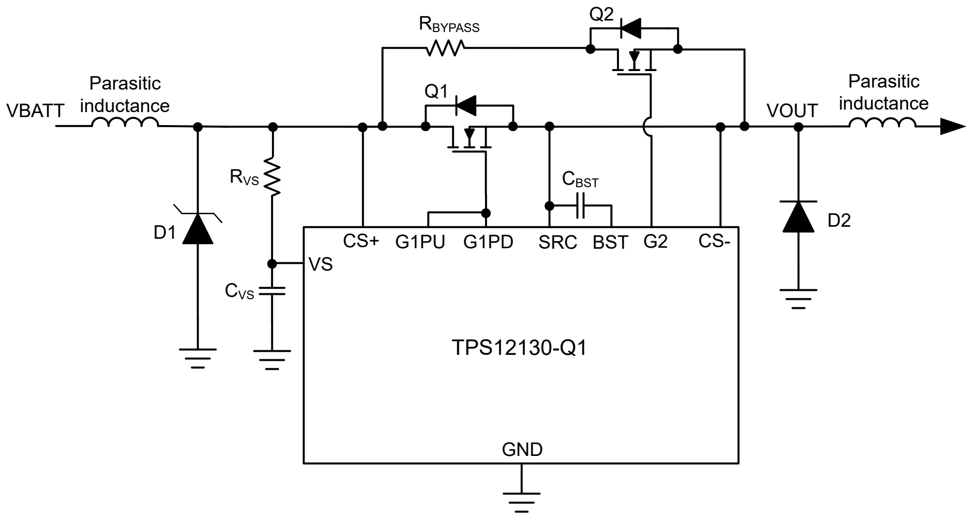


Figure 8-16. Circuit Implementation With Optional Protection Components For TPS12130-Q1

8.6 Layout

8.6.1 Layout Guidelines

- Place the sense resistor (R_{SNS}) close to the TPS12130-Q1 and then connect R_{SNS} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.

  For VDS based Current Sensing, follow the same kevlin techniques across the MOSFET.
- Choose a 0.1 µF or higher value ceramic decoupling capacitor between VS terminal and GND for all the applications. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.

- Make the high-current path from the board input to the load, and the return path, parallel and close to each other to minimize loop inductance.
- Place the external MOSFETs close to the controller GATE drive pins (G1PU/G1PD) such that the GATE of the MOSFETs are close to the controller GATE drive pins and forms a shorter GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- Place the external boot-strap capacitor close to BST and SRC pins to form very short loop.
- Connect the ground connections for the various components around the TPS12130-Q1 directly to each other, and to the TPS12130-Q1 GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.

8.6.2 Layout Example

▨ Top Layer

🟥 Inner Layer GND plane

🟦 Inner Layer PGND plane

◎ Via to GND plane

◎ Via to PGND plane

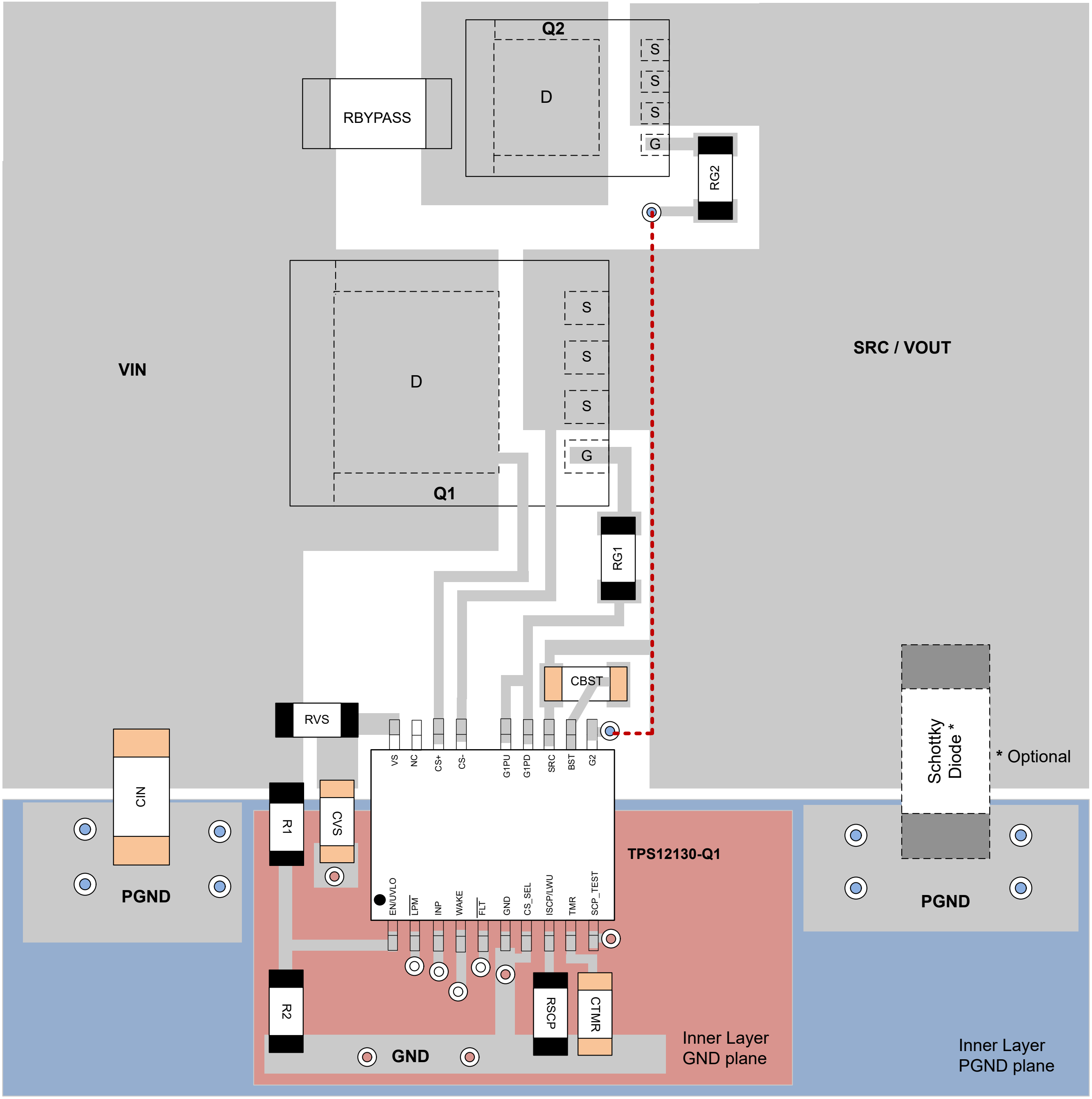


Figure 8-17. Typical PCB Layout Example for TPS12130-Q1 With Low-Power Path

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

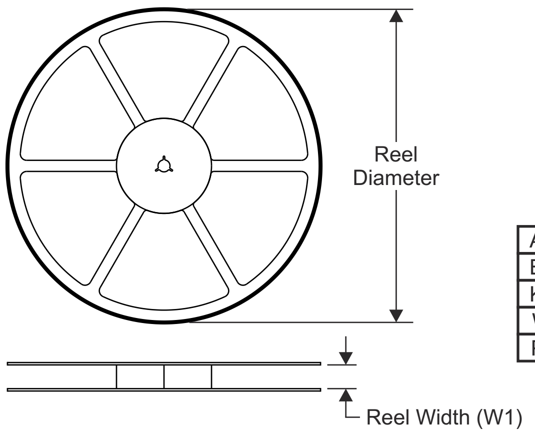
DATE	REVISION	NOTES
March 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

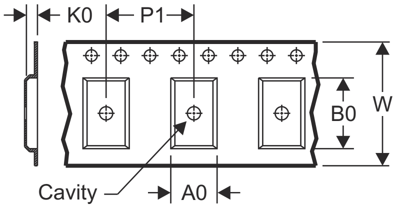
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

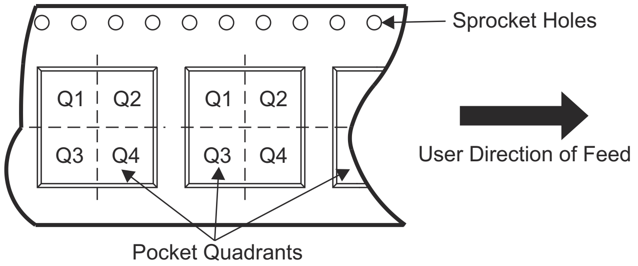


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

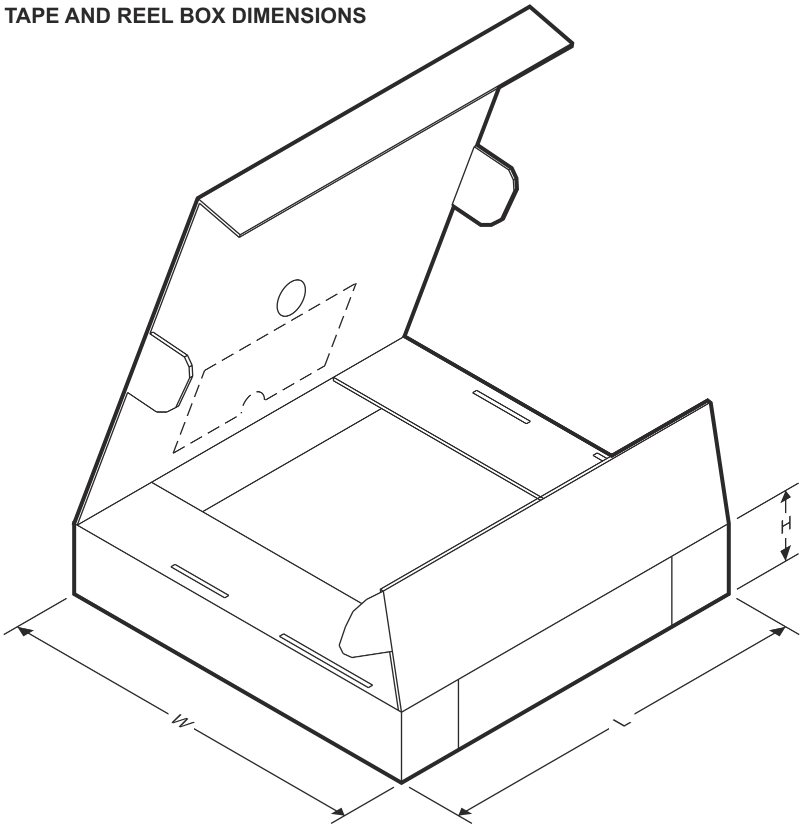
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS12130QDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS12130QDGXRQ1	VSSOP	DGX	19	5000	356.0	356.0	35.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS12130QDGXRQ1	ACTIVE	VSSOP	DGX	19	5000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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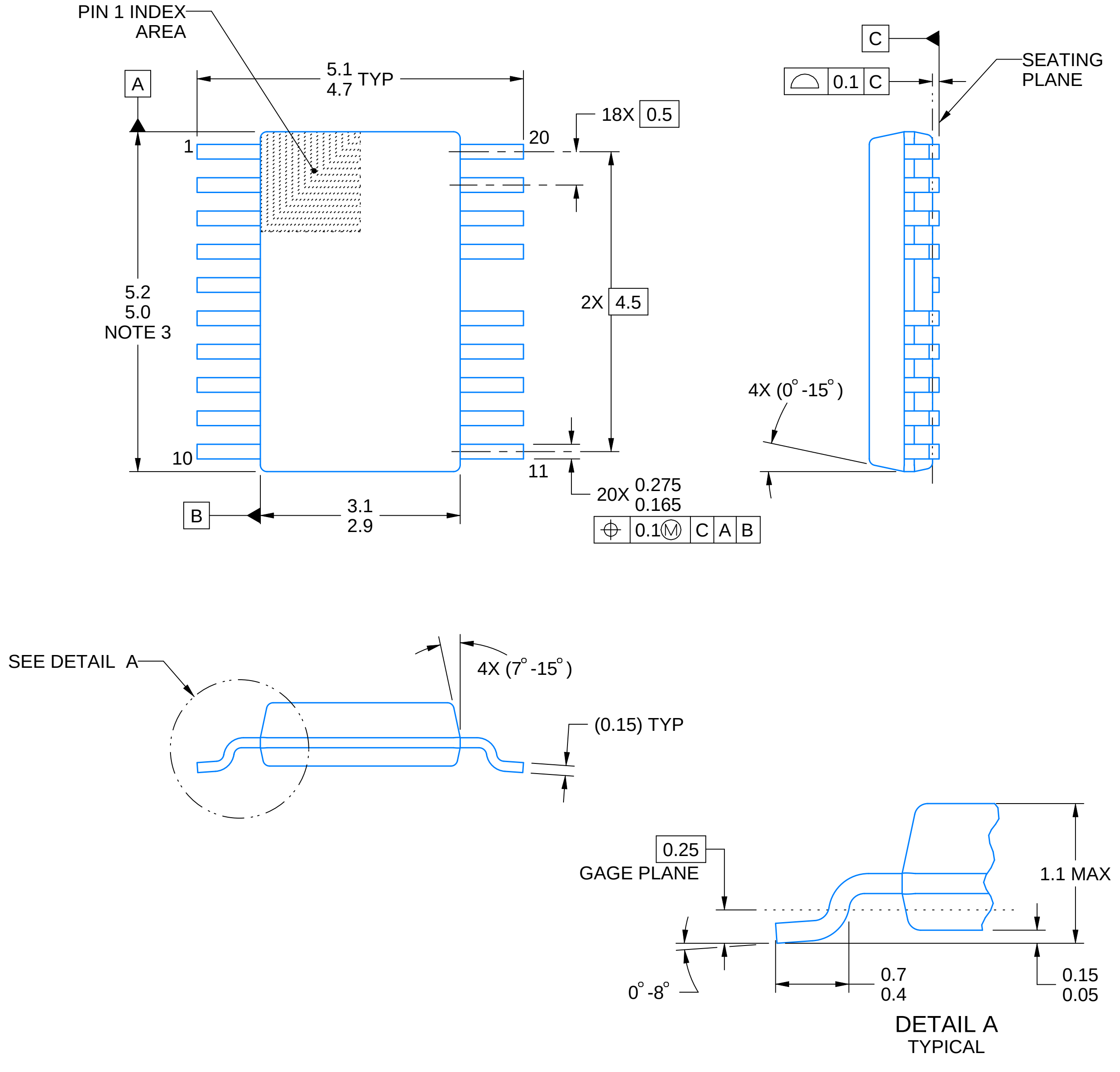
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

DGX0019A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

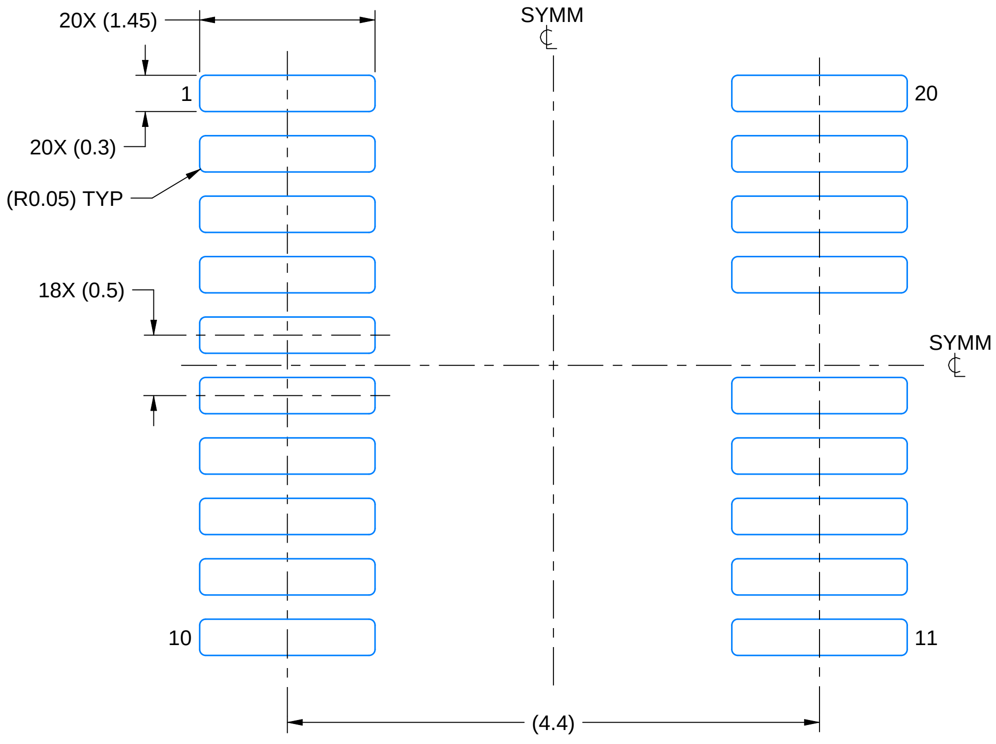


4226944/A 07/2021

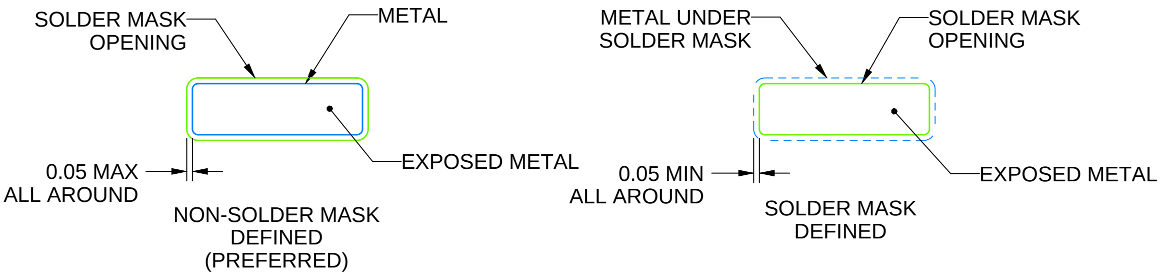
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X



SOLDER MASK DETAILS

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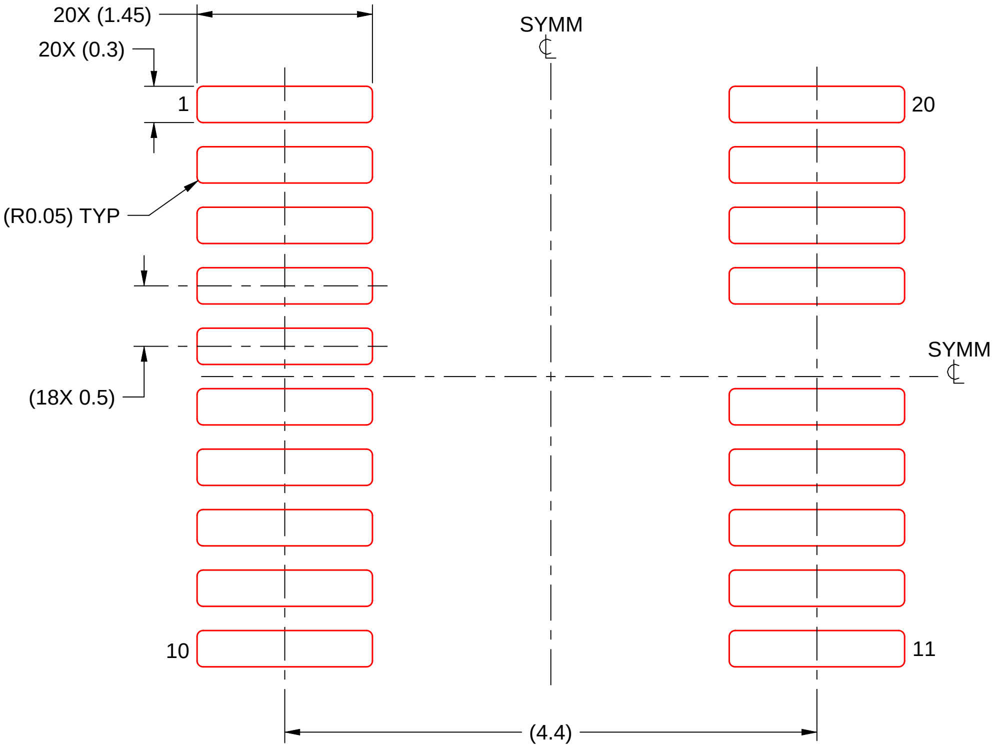
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226944/A 07/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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