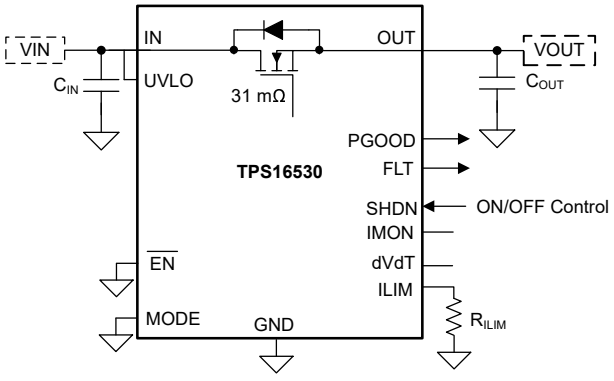
TPS16530 58-V, 4.5-A eFuse With Pulse Current Support for Load Transients

1 Features

- 4.5-V to 58-V operating voltage, 67-V absolute maximum
- Integrated 58-V, 31-mΩ R_{ON} Hot-Swap FET
- 0.6-A to 4.5-A adjustable current limit (± 7%)
- IPC9592B clearance for 56-V operation (20-pin HTSSOP)
- 2x pulse current support for load transients
- Low quiescent current, 21-µA in shutdown
- Adjustable UVLO cut off with ± 2% accuracy
- Adjustable output slew rate control for inrush current limiting
  - Charges large and unknown capacitive loads through thermal regulation during device power up
- Power Good Output (PGOOD)
- Selectable overcurrent fault response options between Auto-Retry and Latch Off (MODE)
- Analog current monitor (IMON) output (± 6%)
- Available in easy-to-use 20-pin HTSSOP and 24-pin VQFN packages

2 Applications

- Power amplifier protection in telecom radios
- Medical equipment
- Fire alarm control panels
- Industrial printers



Simplified Schematic

3 Description

The TPS16530 is an easy to use, positive 58-V, 4.5-A eFuse with a 31-mΩ integrated FET. Protection for the load, source and eFuse itself are provided along with adjustable features such as accurate overcurrent protection, fast short circuit protection, output slew rate control and undervoltage lockout. PGOOD can be used for enable and disable control of the downstream DC-DC converters.

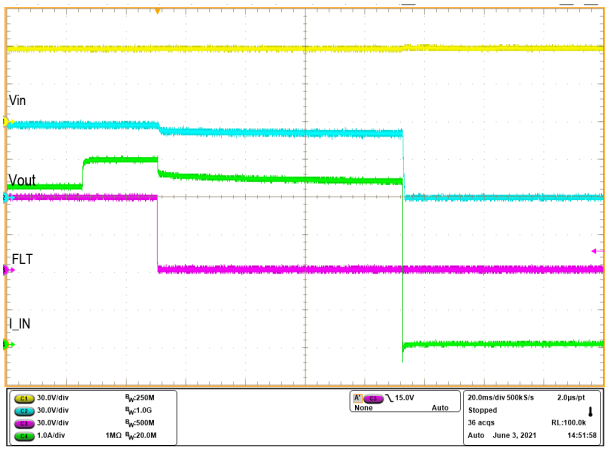
The enable pin provides external control for enabling and disabling the internal FET. The shutdown pin can be used for putting the device in low power shutdown mode. For system status monitoring and downstream load control, the device provides fault and a precise current monitor output. The MODE pin allows flexibility to configure the device between the two current-limiting fault responses (latch off and auto-retry).

The devices are available in 20-pin HTSSOP and 24-pin VQFN packages and are specified over a –40°C to +125°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS16530	VQFN (24)	4.00 mm × 4.00 mm
TPS16530	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pulse Current Support

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2021	*	Initial Release

5 Pin Configuration and Functions

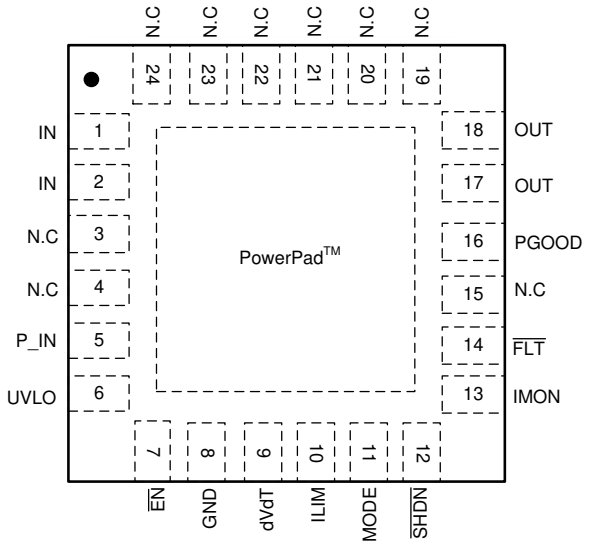


Figure 5-1. TPS16530 RGE Package 24-Pin VQFN Top View

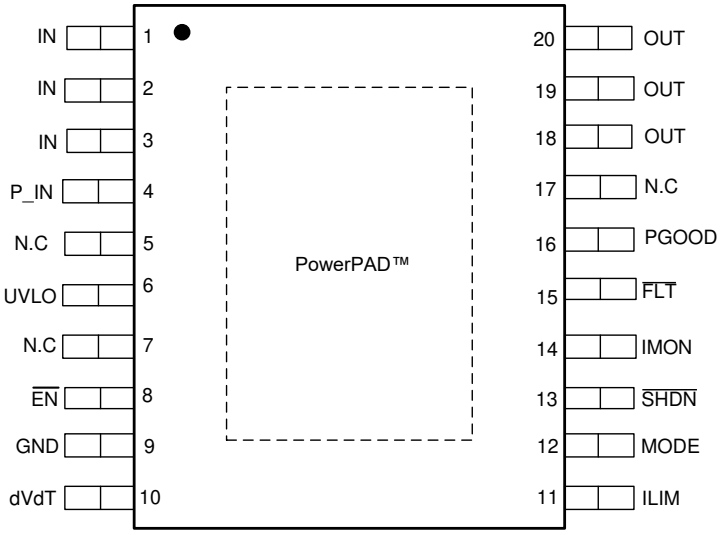


Figure 5-2. TPS16530 PWP Package 20-Pin HTSSOP Top View

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TPS16530			
	VQFN	HTSSOP		
IN	1	1	P	Power Input. Connects to the DRAIN of the internal FET.
	2	2		
	—	3		
P_IN	5	4	P	Supply voltage of the device. Always connect P_IN to IN directly.
UVLO	6	6	I	Input for setting the programmable undervoltage lockout threshold. An undervoltage event turns off the internal FET and asserts $\overline{FLT}$ to indicate the power-failure. If not used, this pin can be connected to IN or P_IN.
$\overline{EN}$	7	8	I	Active low enable pin. If not used, this pin can be connected to GND. Do not leave this pin open or floating.
GND	8	9	—	Connect GND to system ground
dVdT	9	10	I/O	A capacitor from this pin to GND sets output voltage slew rate. Leaving this pin floating enables device power up in thermal regulation resulting in fast output charge. See the *Hot Pug-In and In-Rush Current Control* section.
ILIM	10	11	I/O	A resistor from this pin to GND sets the overload limit. See *Overload and Short Circuit Protection* section.
MODE	11	12	I	Mode selection pin for Overload fault response. See the *Device Functional Modes* section.
$\overline{SHDN}$	12	13	I	Shutdown pin. Pulling $\overline{SHDN}$ low makes the device to enter into low power shutdown mode. Cycling $\overline{SHDN}$ pin voltage resets the device that has latched off due to a fault condition.
IMON	13	14	O	Analog current monitor output. This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage. If unused, leave this pin floating.
$\overline{FLT}$	14	15	O	Fault event indicator. It is an open drain output. If unused, leave floating or connect to GND.

Table 5-1. Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	TPS16530			
	VQFN	HTSSOP		
PGOOD	16	16	O	Active High. A high indicates that the internal FET is enhanced. PGOOD goes low when the internal FET is turned OFF during a fault or when $\overline{\text{SHDN}}$ is pulled low. If PGOOD is unused then connect to GND or leave it floating.
OUT	17	18	P	Power Output of the device
	18	19		
	—	20		
N.C	3	5	—	Internally Not connected. Can be connected to other pins (P_IN, OUT, GND) for enhanced thermal performance.
	4	7		
	15	17		
	19	—		
	20	—		
	21	—		
	22	—		
	23	—		
	24	—		
PowerPAD™			—	Connect the PowerPAD to GND plane for heat sinking. Do not use the PowerPAD as the only electrical connection to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN, P_IN, OUT, UVLO, $\overline{FLT}$, PGOOD	Input Voltage	–0.3	67	V
$\overline{EN}$, dVdT, IMON, MODE, $\overline{SHDN}$, ILIM	Input Voltage	–0.3	5.5	
$I_{\overline{FLT}}$, I_{dVdT}, I_{PGOOD}	Sink current		10	mA
I_{dVdT}, I_{ILIM} , I_{MODE}, $I_{\overline{SHDN}}$	Source current	Internally limited		
T_J	Operating Junction temperature	–40	150	°C
	Transient junction temperature	–40	$T_{(TSD)}$	
T_{stg}	Storage temperature	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN, P_IN	Input Voltage	4.5		58	V
OUT, UVLO, PGOOD, $\overline{FLT}$		0		58	
$\overline{EN}$, dVdT, IMON, MODE		0		4	
$\overline{SHDN}$		0		5	
ILIM	Resistance	4		30	kΩ
IMON	Resistance	1			
IN, P_IN, OUT	External Capacitance	0.1			µF
dVdT		10			nF
T_J	Operating Junction temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS16530		UNIT
		RGE (VQFN)	PWP (HTSSOP)	
		24 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.1	31.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	22.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	8.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.7	8.8	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC(1)		TPS16530		UNIT
		RGE (VQFN)	PWP (HTSSOP)	
		24 PINS	20 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN)}$ = $V_{(P\_IN)}$ < 58 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(IN)}$, $V_{(P\_IN)}$	Operating input voltage		4.5		58	V
$IQ_{(ON)}$	Supply current	Enabled: $V_{(\overline{SHDN})}$ = 2 V		1.38	1.7	mA
$IQ_{(OFF)}$		$V_{(\overline{SHDN})}$ = 0 V		21	60	µA
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.176	1.2	1.224	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.09	1.122	1.15	V
$I_{(UVLO)}$	UVLO Input leakage current	0 V ≤ $V_{(UVLO)}$ ≤ 58 V	–150	30	150	nA
Enable ($\overline{EN}$) INPUT						
$V_{(\overline{ENR})}$	Enable threshold voltage, rising				1.25	V
$V_{(\overline{ENF})}$	Enable threshold voltage, falling		0.65			V
$I_{(\overline{EN})}$	Enable Input leakage current	0 V ≤ $V_{(\overline{EN})}$ ≤ 4 V	–150	13.5	150	nA
CURRENT LIMIT PROGRAMMING (ILIM)						
$I_{(OL)}$	Over Load current limit	$R_{(ILIM)}$ = 30 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.54	0.6	0.66	A
$I_{(OL)}$	Over Load current limit	$R_{(ILIM)}$ = 9 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	1.84	2	2.16	A
$I_{(OL)}$	Over Load current limit	$R_{(ILIM)}$ = 4.02 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	4.185	4.5	4.815	A
$I_{(OL\_Pulse)}$	Transient Pulse Over current limit	4 kΩ < $R_{(ILIM)}$ < 30 kΩ		2 × $I_{(OL)}$		A
$I_{(FASTRIP)}$	Fast-trip comparator threshold			3 × $I_{(OL)}$		A
$I_{(SCP)}$	Short Circuit Protect current			45		A
PASS FET OUTPUT (OUT)						
R_{ON}	IN to OUT total ON resistance	0.6 A ≤ $I_{(OUT)}$ ≤ 4.5 A, T_J = 25°C	26	30.44	34.5	mΩ
R_{ON}	IN to OUT total ON resistance	0.6 A ≤ $I_{(OUT)}$ ≤ 4.5 A, T_J = 85°C	33		45	mΩ
R_{ON}	IN to OUT total ON resistance	0.6 A ≤ $I_{(OUT)}$ ≤ 4.5 A, –40°C ≤ T_J ≤ +125°C	19	30.44	53	mΩ
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT charging current	$V_{(dVdT)}$ = 0 V	1.775	2	2.225	µA
$GAIN_{(dVdT)}$	dVdT to OUT gain	$V_{(OUT)}$ /$V_{(dVdT)}$	23.5	25	26	V/V
$V_{(dVdTmax)}$	dVdT maximum capacitor voltage		3.8	4.17	4.75	V
$R_{(dVdT)}$	dVdT discharging resistance		10	16.6	26.6	Ω
LOW IQ SHUTDOWN ($\overline{SHDN}$) INPUT						
$V_{(\overline{SHDN})}$	Open circuit voltage	$I_{(\overline{SHDN})}$ = 0.1 µA	2.48	2.7	3.3	V
$V_{(SHUTF)}$	$\overline{SHDN}$ threshold voltage for low IQ shutdown, falling		0.8			V
$V_{(SHUTR)}$	$\overline{SHDN}$ threshold rising				2	V
$I_{(\overline{SHDN})}$	Leakage current	$V_{(\overline{SHDN})}$ = 0 V	–10			µA
CURRENT MONITOR OUTPUT (IMON)						

6.5 Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN)}$ = $V_{(P\_IN)}$ < 58 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$GAIN_{(IMON)}$	Gain factor $I_{(IMON)}$:$I_{(OUT)}$	0.6 A ≤ $I_{(OUT)}$ ≤ 2 A	25.66	27.9	30.14	µA/A
		2 A ≤ $I_{(OUT)}$ ≤ 4.5 A	26.22	27.9	29.58	µA/A
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-down resistance		36	74	130	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 58 V	–150	30	150	nA
POWER GOOD (PGOOD)						
$R_{(PGOOD)}$	PGOOD Pull-down resistance		36	74	130	Ω
$I_{(PGOOD)}$	PGOOD Input leakage current	0 V ≤ $V_{(PGOOD)}$ ≤ 58 V	–150		150	nA
THERMAL PROTECTION						
$T_{(J\_REG)}$	Thermal regulation set point		136	145	154	ºC
$T_{(TSD)}$	Thermal shutdown (TSD) threshold, rising			165		ºC
$T_{(TSDhyst)}$	TSD hysteresis			11		ºC
MODE						
MODE_SEL	Mode selection	MODE = Open		Latch		
		MODE = Short to GND		Auto – Retry		

6.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN)}$ = $V_{(P\_IN)}$ < 58 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
UVLO INPUT (UVLO)						
UVLO_$t_{on(dly)}$	UVLO switch turnon delay	UVLO↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ ≥ 10 nF, [$C_{(dVdT)}$ in nF]		742 + 49.5 x $C_{(dVdT)}$		µs
UVLO_$t_{off(dly)}$	UVLO switch turnoff delay	UVLO↓(20 mV below $V_{(UVLOF)}$) to $\overline{FLT}$↓	9	11	16	µs
$t_{UVLO\_FLTdly)}$	UVLO to fault de-assertion delay	UVLO↑ to $\overline{FLT}$ ↑ delay	500	617	700	µs
ENABLE INPUT ($\overline{EN}$)						
$\overline{EN}$_$t_{OFF(dly)}$	Enable turn-off delay	$\overline{EN}$↑ (20 mV above $V_{(OVPR)}$) to $\overline{FLT}$↓	8.5	11	14	µs
$\overline{EN}$_$t_{on(dly)}$	Enable turn-on delay	$\overline{EN}$↓ (100 mV below $V_{(OVPF)}$) to FET ON $C_{(dVdT)}$ ≥ 10 nF, [$C_{(dVdT)}$ in nF]		150 + 49.5 x $C_{(dVdT)}$		µs
SHUTDOWN CONTROL INPUT ($\overline{SHDN}$)						
$t_{SD(dly)}$	SHUTDOWN entry delay	$\overline{SHDN}$↓ (below $V_{(SHUTF)}$) to FET OFF	0.8	1	1.5	µs
CURRENT LIMIT						
$t_{FASTTRIP(dly)}$	Hot-short response time	$I_{(OUT)}$ > $I_{(SCP)}$		1		µs
$t_{FASTTRIP(dly)}$	Soft short response	$I_{(FASTTRIP)}$ < $I_{(OUT)}$ < $I_{(SCP)}$	2.2	3.2	4.5	µs
$t_{CL\_ILIM(dly)}$	Maximum duration in current limit		129	162	202	ms
$t_{CB(dly)}$	Maximum duration in 2x Pulse current limiting	$I_{(OL)}$ < $I_{(OUT)}$ ≤ $I_{(2xOL)}$	20	25.5	31	ms
$t_{CL\_ILIM\_FLT(dly)}$	$\overline{FLT}$ delay in current limit		1.09	1.3	1.6	ms
OUTPUT RAMP CONTROL (dVdT)						
$t_{(FASTCHARGE)}$	Output ramp time in fast charging	$C_{(dVdT)}$ = Open, 10% to 90% $V_{(OUT)}$, $C_{(OUT)}$ = 1 µF; $V_{(IN)}$ = 24V	350	495	700	µs

6.6 Timing Requirements (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN)}$ = $V_{(P\_IN)}$ < 58 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(dVdT)}$	Output ramp time	$C_{(dVdT)}$ = 22 nF, 10% to 90% $V_{(OUT)}$, $V_{(IN)}$ = 24V		8.35		ms
POWER GOOD (PGOOD)						
t_{PGOODR}	PGOOD delay (deglitch) time	Rising edge	8	11.5	13	ms
t_{PGOODF}	PGOOD delay (deglitch) time	Falling edge	8	10	13	ms
FAULT FLAG ($\overline{FLT}$)						
$t_{CB\_FLT(dly)}$	$\overline{FLT}$ assertion delay in Pulse over current limiting	Delay from $I_{(OUT)}$ > $I_{(OL)}$ to $\overline{FLT}$↓.	22	25.5	30	ms
THERMAL PROTECTION						
$t_{(TSD\_retry)}$	Retry delay in TSD	MODE = GND	500	648	800	ms
$t_{(Treg\_timeout)}$	Thermal Regulation timeout		1	1.3	1.6	s

6.7 Typical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = $V_{(P\_IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)

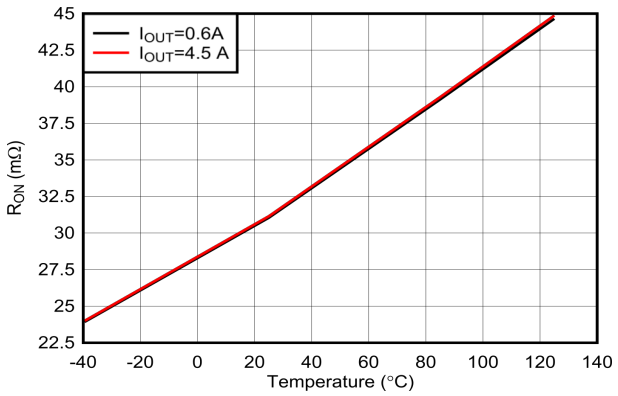


Figure 6-1. On-Resistance vs Temperature Across Load Current

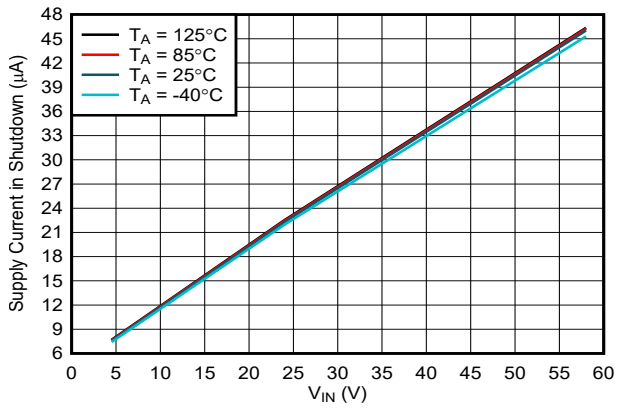


Figure 6-2. Input Supply Current vs Supply Voltage in Shutdown

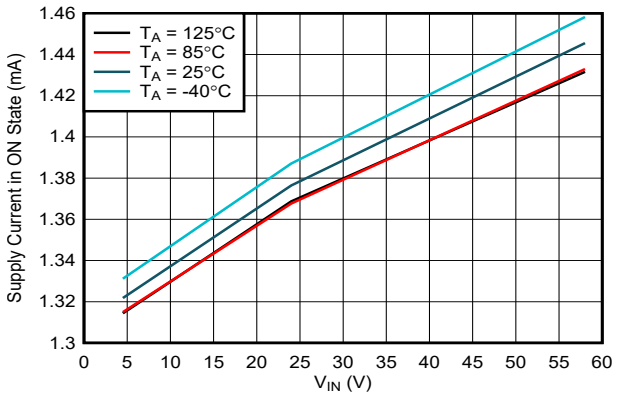


Figure 6-3. Input Supply Current vs Supply Voltage During Normal Operation

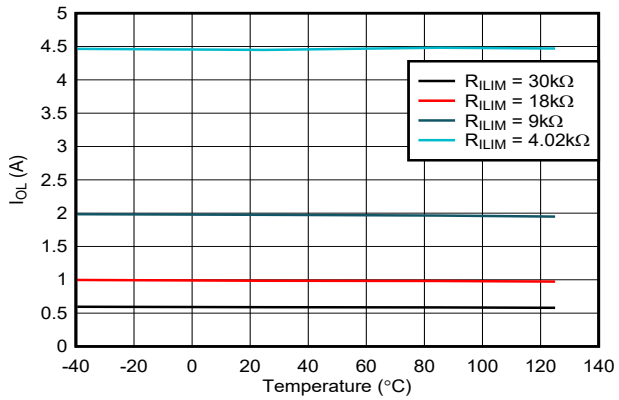


Figure 6-4. Overload Current Limit vs Temperature

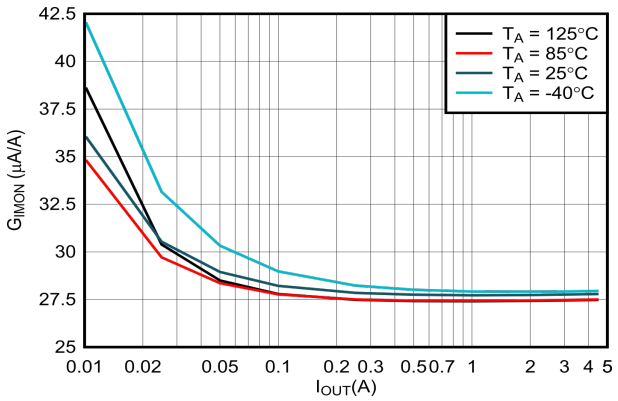
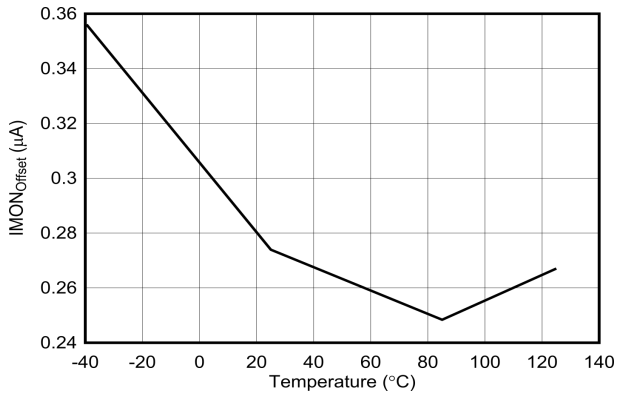


Figure 6-5. Current Monitor Gain vs Output Current

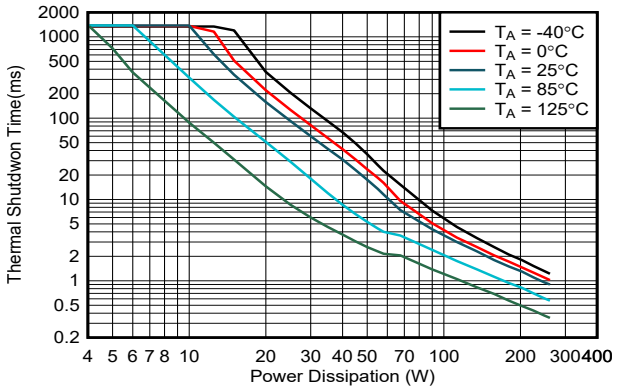


I_{OUT} = 4.5 A

Figure 6-6. IMON Offset vs Temperature

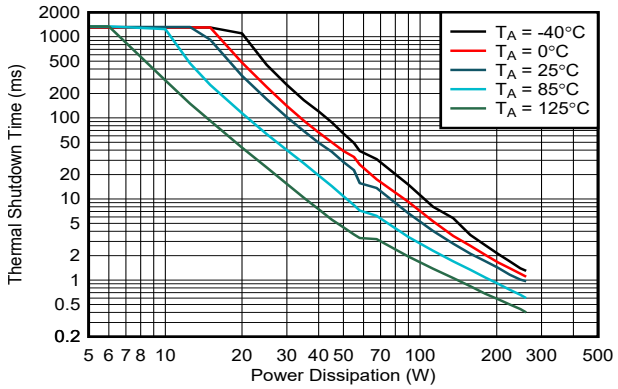
6.7 Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = $V_{(P\_IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)



Taken on VQFN device with 95 cm^2 copper connected to Exposed PAD

Figure 6-7. Thermal Shutdown Time vs Power Dissipation for RGE Package



Taken on HTSSOP with 110 cm^2 copper connected to Exposed PAD

Figure 6-8. Thermal Shutdown Time vs Power Dissipation for PWP Package

7 Parameter Measurement Information

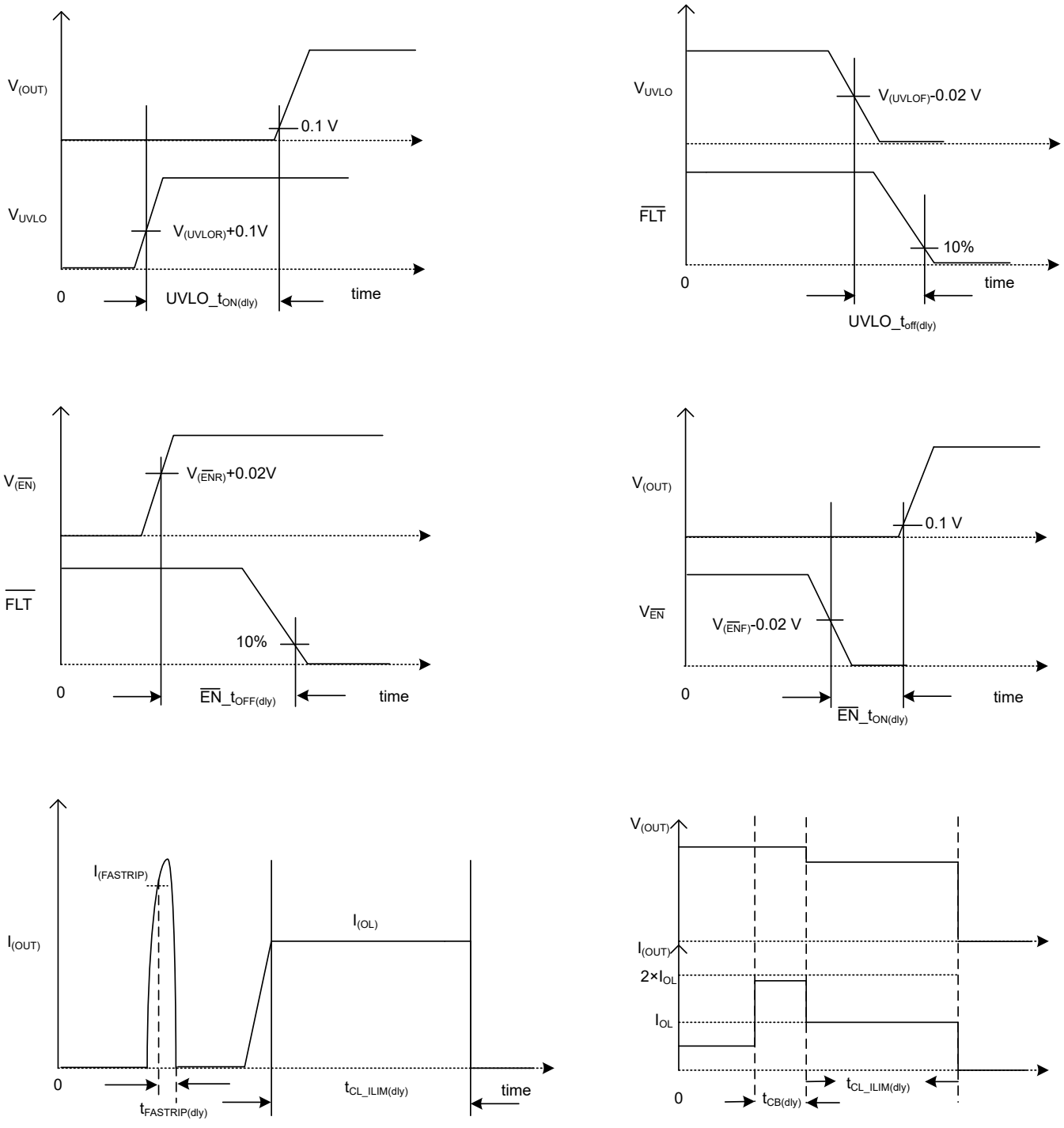


Figure 7-1. Timing Waveforms

8 Detailed Description

8.1 Overview

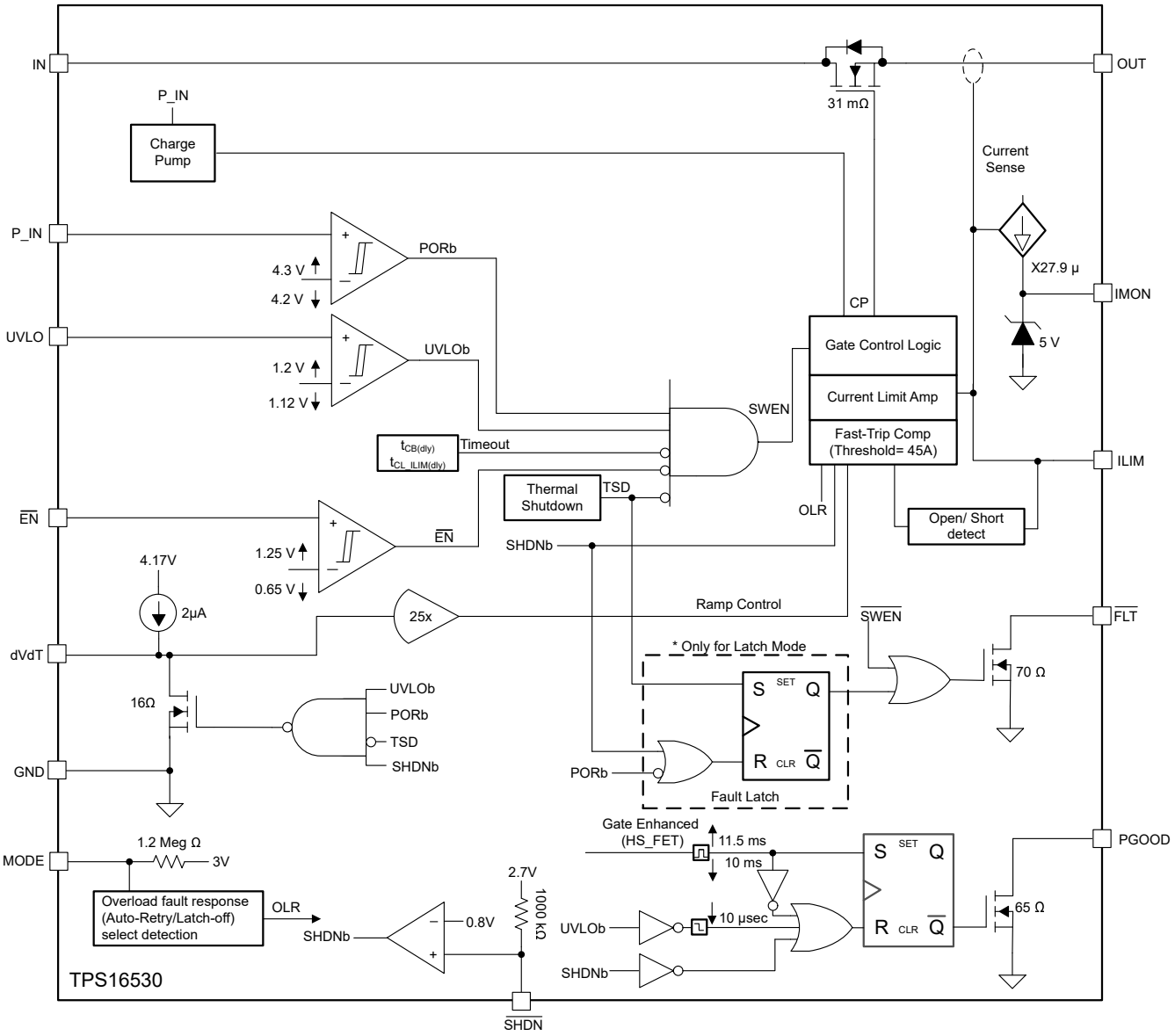
The TPS16530 is a 58-V industrial eFuse. The device provides robust protection for all systems and applications powered from 4.5 V to 58 V. For hot-pluggable boards, the device provides hot-swap power management with in-rush current control and programmable output voltage slew rate features using the dVdT pin. Load, source and device protections are provided with many programmable features including overcurrent and undervoltage. The precision overcurrent limit (±7% at 6 A) helps to minimize over design of the input power supply, while the fast response short circuit protection 1 µs (typical) immediately isolates the faulty load from the input supply when a short circuit is detected.

The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault signal for the downstream system. The device's overall threshold accuracy of 2% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip.

Additional features of the TPS16530 include:

- ±6% current monitor output (IMON) for health monitoring of the system
- A choice of latch off or automatic restart mode response during current limit and thermal fault using MODE pin
- PGOOD indicator output
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for faults
- Enable and Disable control from an MCU using $\overline{\text{EN}}$ pin
- Low power shutdown using $\overline{\text{SHDN}}$ pin

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Hot Plug-In and In-Rush Current Control

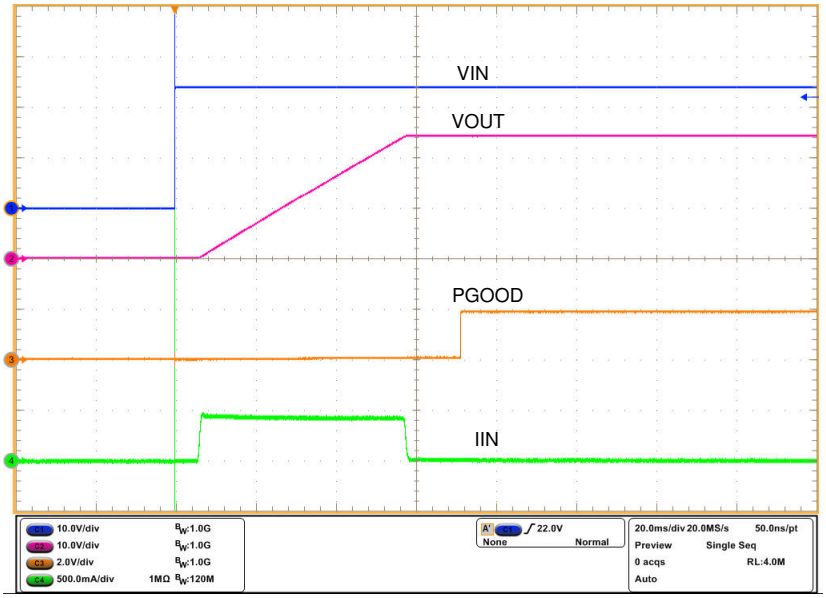
The devices are designed to control the inrush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on. The fastest output slew rate of 24V/500 µs can be achieved by leaving dVdT pin floating. The inrush current can be calculated using Equation 1.

$$I = C \times \frac{dV}{dT} \geq I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \quad (1)$$

where

$$t_{dVdT} = 20.8 \times 10^3 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

Figure 8-1 illustrates in-rush current control performance of the device during Hot Plug-In.



C_{dVdT} = 100 nF C_{OUT} = 1000 µF R_{ILIM} = 4.02 kΩ

Figure 8-1. Hot Plug In and Inrush Current Control at 24-V Input

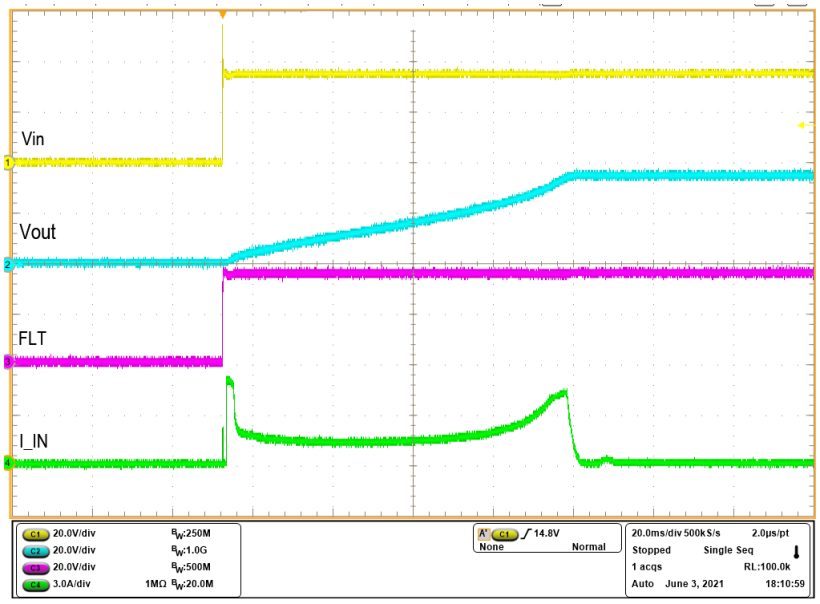
8.3.1.1 Thermal Regulation Loop

The average power dissipation within the eFuse during power up with a capacitive load can be calculated using Equation 3.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (3)$$

System designs requiring to charge large output capacitors rapidly may result in an operating point that exceeds the power dissipation versus time boundary limits of the device defined by Figure 6-7 characteristic curve. This may result in increase in junction temperature beyond the device's maximum allowed junction temperature. To keep the junction temperature within the operating range, the thermal regulation control loop regulates the junction temperature at $T_{(J\_REG)}$, 145°C (typical) by controlling the inrush current profile and thereby limiting the power dissipation within the device automatically. An internal 1.3 sec (typical), $t_{(Treg\_timeout)}$ timer starts from the instance the thermal regulation operation kicks in. If the output does not power up within this time then the internal FET is turned OFF. Subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF) setting as per the Table 8-2. The maximum time-out of 1.3 sec (typical) in thermal regulation loop operation ensures that the device and the system board does not heat up during steady fault conditions such as wake up with output short-circuit. This scheme ensures reliable power up operation.

Thermal regulation control loop is internally enabled during power up by $V_{(IN)}$, UVLO cycling and turn ON using $\overline{SHDN}$ control. Figure 8-2 illustrates performance of the device operating in thermal regulation loop during power up by $V_{(IN)}$ with a large output capacitor. The Thermal regulation loop gets disabled internally after the power up sequence when the internal FET's gate gets fully enhanced or when the $t_{(Treg\_timeout)}$ of 1.3 sec (typical) time is elapsed.



C_{dVdT} = Open V_{IN} = 35 V R_{ILIM} = 4.02 kΩ

Figure 8-2. Thermal Regulation Loop Response During Power Up With 4.7-mF Capacitive Load

8.3.2 Undervoltage Lockout (UVLO)

The TPS16530 device features an accurate ± 2% adjustable undervoltage lockout functionality. When the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input undervoltage fault, the internal FET quickly turns off and $\overline{FLT}$ is asserted. The UVLO comparator has a hysteresis of 78 mV (typical). To set the input UVLO threshold, connect a resistor divider network from IN supply to UVLO terminal to GND as shown in Figure 8-3. If the Under-Voltage Lock-Out function is not needed, the UVLO terminal must be connected to the IN terminal. UVLO terminal must not be left floating.

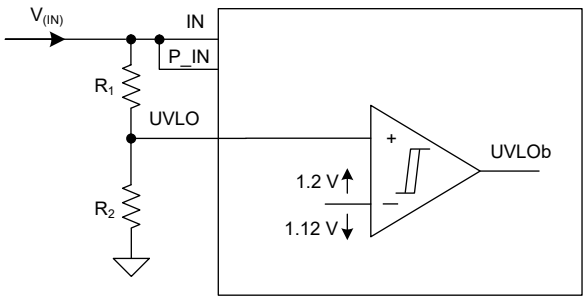


Figure 8-3. UVLO Thresholds Set by R_1 and R_2

8.3.3 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

8.3.3.1 Overload Protection

The TPS16530 device features accurate overload current limiting and fast short circuit protection feature. The device supports a pulse current up to 9A (2 × I_{OL}) for transient loads. Table 8-1 describes the overload response of TPS16530 device.

Table 8-1. Overload Response of TPS16530 Device

Output Current	Overload or Over-Current Response
$I_{OUT} < I_{OL}$	No action. Device provides current up-to I_{OL}.
$I_{OL} \le I_{OUT} < 2 \times I_{OL}$	Device provides current up to $2 \times I_{OL}$ for a duration of $t_{CB(dly)}$ and then limits current to I_{OL} for a maximum duration of $t_{CL\_ILIM(dly)}$.
$2 \times I_{OL} \le I_{OUT} < 3 \times I_{OL}$	Device limits current to $2 \times I_{OL}$ for a maximum duration of $t_{CB(dly)}$ and then limits current to I_{OL} for a maximum duration of $t_{CL\_ILIM(dly)}$.
$3 \times I_{OL} \le I_{OUT}$	Device provides fast trip protection or short circuit protection and turns off the internal FET. See the *Short Circuit Protection* section.

The power dissipation across the device during this operation will be $[(V_{IN} – V_{OUT}) \times I_{OL}]$ for $I_{OUT} < 2 \times I_{OL}$ or $[(V_{IN} – V_{OUT}) \times 2 \times I_{OL}]$ for $2 \times I_{OL} < I_{OUT} < 3 \times I_{OL}$and this could heat up the device and eventually enter into thermal shutdown.

For current limit of $I_{OL,}$ the maximum duration for current limiting is $t_{CL\_ILIM(dly)}$, 162 msec (typical). For current limit of $2 \times I_{OL,}$ the maximum duration for current limiting is $t_{CB(dly)}$, 25 msec (typical) .

If the thermal shutdown occurs before this time the internal FET turns OFF and the device operates either in auto-retry or latch off mode based on MODE pin configuration in Table 8-2. Set the current limit using Equation 4.

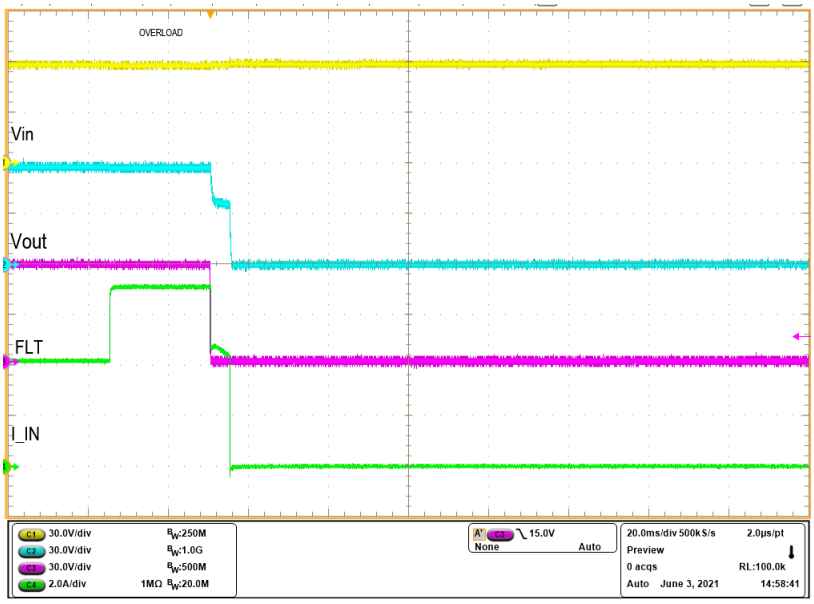
$$I_{OL} = \frac{18}{R_{(ILIM)}} \tag{4}$$

where

- $I_{(OL)}$ is the overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ

During the overload current limiting, if the overload condition exists for more than $t_{CL\_ILIM\_FLT(dly)}$, 1.3 msec (typical), the $\overline{FLT}$ asserts to warn of impending turnoff of the internal FETs due to the subsequent thermal shutdown event or due to $t_{CL\_ILIM(dly)}$ timer expiry. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. Figure 8-4 shows the device behavior in case of overload event. The device provides a pulse current of 7 A for a duration of 25 ms and then turns off the internal FET due to thermal shutdown before the expiry of $t_{CL\_ILIM(dly)}$.

The $2 \times I_{(OL)}$ pulse current support is activated only after PGOOD goes high. If PGOOD is in low state such as during start-up operation or during auto-retry cycles, the $2 \times I_{(OL)}$ pulse current support is not activated and the device limits the current at $I_{(OL)}$ level.



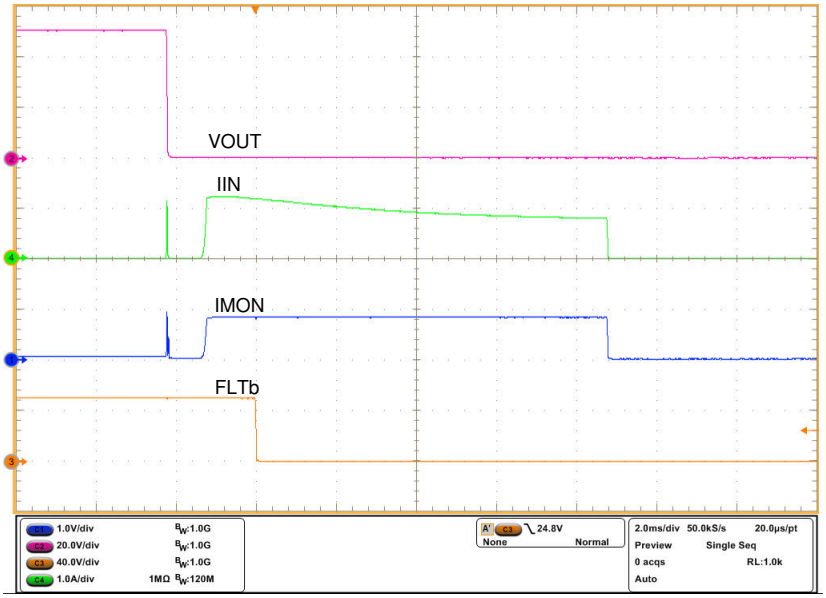
V_{IN} = 58 V ILIM = 4.5 A I_{OUT} = 4 A to 7 A

Figure 8-4. Pulse Current Support

The TPS16530 device feature ILIM pin short and open fault detection and protection. The internal FET is turned OFF when ILIM pin is detected short or open to GND and it remains OFF till the ILIM pin fault is removed.

8.3.3.2 Short Circuit Protection

During a transient output short circuit event, the current through the device increases rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator. The fast-trip comparator architecture is designed for fast turn OFF $t_{FASTTRIP(dly)}$ = 1 µs (typical) with $I_{(SCP)}$ = 45 A of the internal FET during an output short circuit event. The fast-trip threshold is internally set to $I_{(FASTTRIP)}$. The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then the device functions similar to the overload condition. Figure 8-5 illustrates output hot-short performance of the device.



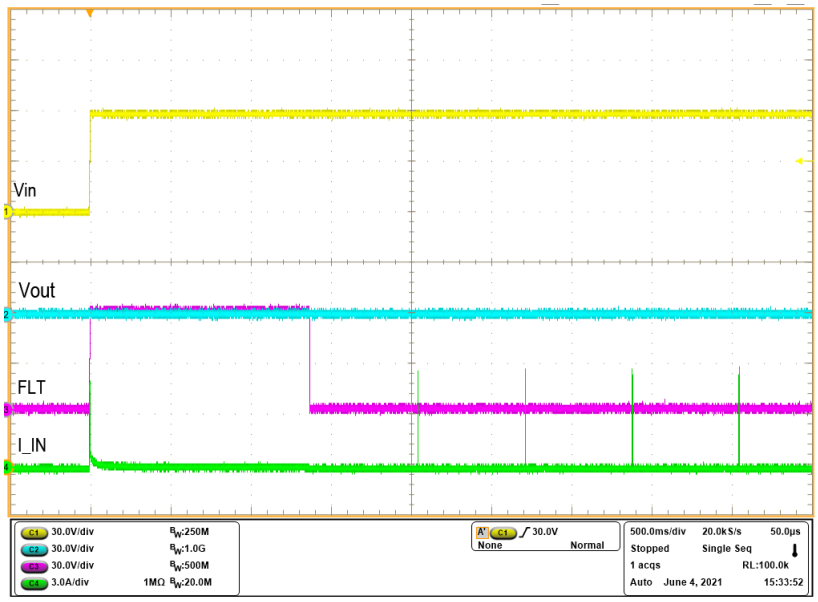
V_{IN} = 50 V R_{ILIM} = 18 kΩ

Figure 8-5. Output Hot-Short Response

The fast-trip comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This performance is achieved by controlling the turn OFF time of the internal FET based on the overcurrent level, $I_{(FASTTRIP)}$, through the device. The higher the overcurrent, the faster the turn OFF time, $t_{FASTTRIP(dly)}$. At Overload current level in the range of $I_{FASTTRIP} < I_{OUT} < I_{SCP}$, the fast-trip comparator response is 3.2 µs (typical).

8.3.3.2.1 Start-Up With Short-Circuit On Output

When the device is started with short-circuit on the output, the current begins to limit at $I_{(OL)}$. Due to high power dissipation of VIN × $I_{(OL)}$ within the device the junction temperature increases. Subsequently, the thermal regulation control loop limits the load current to regulate the junction temperature at $T_{(J\_REG)}$, 145°C (typical) for a duration off $t_{(Treg\_timeout)}$, 1.25 sec (typical). Subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF) setting as per Table 8-2. $\overline{FLT}$ gets asserted after $t_{(Treg\_timeout)}$ and remains asserted till the output short-circuit is removed. Figure 8-6 illustrates the behavior of the device in this condition.



V_{IN} = 58 V ILIM = 4.5 A

Figure 8-6. Start-Up With Short on Output

8.3.4 Current Monitoring Output (IMON)

The TPS16530 device features an accurate analog current monitoring output. A current source at IMON terminal is internally configured to be proportional to the current flowing from IN to OUT. This current can be converted into a voltage using a resistor $R_{(IMON)}$ from IMON terminal to GND terminal. The IMON voltage can be used as a means of monitoring current flow through the system. The maximum voltage ($V_{(IMONmax)}$) for monitoring the current is limited to 4 V. This limit puts a limitation on maximum value of $R_{(IMON)}$ resistor and is determined by Equation 5.

$$V(IMON) = \left[I(OUT) \times GAIN(IMON)\right] \times R(IMON) \quad (5)$$

Where,

- $GAIN_{(IMON)}$ is the gain factor $I_{(IMON)}$:$I_{(OUT)}$ = 27.9 µA/A (typical)
- $I_{(OUT)}$ is the load current

See Figure 6-5 for IMON gain versus load current (0.01 to 4.5 A) and Figure 6-6 for IMON Offset versus Temperature plots. Figure 6-6 illustrates IMON performance.

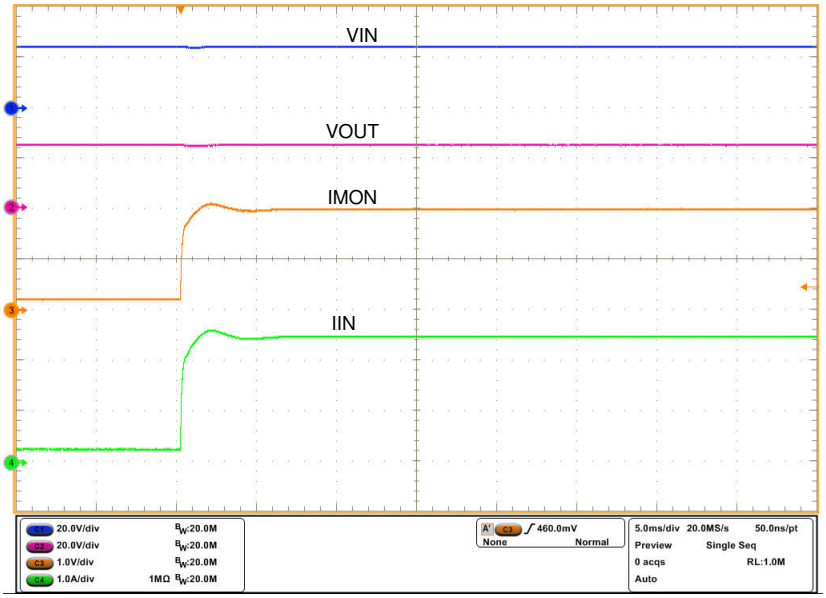


Figure 8-7. IMON Response During a Load Step

The IMON pin must not have a bypass capacitor to avoid delay in the current monitoring information.

8.3.5 FAULT Response ($\overline{\text{FLT}}$)

The $\overline{\text{FLT}}$ open-drain output asserts (active low) under the faults events such as undervoltage, overload, current limiting, ILIM pin short and thermal shutdown conditions. The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry. $\overline{\text{FLT}}$ can be left open or connected to GND when not used.

8.3.6 Power Good Output (PGOOD)

The devices feature an open drain Power good (PGOOD) indicator output. PGOOD can be used for enable and disable control of the downstream loads like DC/DC converters. PGOOD goes high when the internal FET's gate is enhanced. It goes low when the internal FET turns OFF during a fault event or when $\overline{\text{SHDN}}$ is pulled low or when $\overline{\text{EN}}$ is pulled high. There is a deglitch of 11.5 msec (typical), t_{PGOODR}, at the rising edge and 10 msec (typical), t_{PGOODF}, on falling edge. PGOOD is a rated for 58 V and can be pulled to IN or OUT through a resistor.

8.3.7 IN, P_IN, OUT and GND Pins

Connect a minimum of 0.1-µF capacitor across IN and GND. Connect P_IN and IN together. Do not leave any of the IN and OUT pins unconnected.

8.3.8 Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FET if the junction temperature exceeds $T_{(TSD)}$, 165°C (typical). After the thermal shutdown event, depending upon the mode of fault response configured as shown in Table 8-2, the device either latches off or commences an auto-retry cycle of 648 msec (typical), $t_{(TSD\_retry)}$ after $T_J < [T_{(TSD)} – 11°C]$. During the thermal shutdown, the fault pin $\overline{\text{FLT}}$ pulls low to indicate a fault condition.

8.3.9 Low Current Shutdown Control ($\overline{\text{SHDN}}$)

The internal and the external FET and hence the load current can be switched off by pulling the $\overline{\text{SHDN}}$ pin below a 0.8-V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device. The device quiescent current reduces to 21 µA (typical) in shutdown state. To assert $\overline{\text{SHDN}}$ low, the pull down must have sinking capability of at least 10 µA. To enable the device, $\overline{\text{SHDN}}$ must be pulled up to at least 2 V. Once the device is enabled, the internal FET turns on with dVdT mode.

8.3.10 Enable Input ($\overline{EN}$)

The $\overline{EN}$ pin can be used to turn-on or turn-off the internal FET. $\overline{EN}$ can be used with a 1.8-V Digital IO of FPGA or MCU. For rising and falling thresholds of $\overline{EN}$ pin. See $V_{\overline{ENR}}$ and $V_{\overline{ENF}}$ in *Electrical Characteristics*. After the $\overline{EN}$ is made low, the output ramps with slew rate configured by dVdT pin.

$\overline{EN}$ pin does not reset the latch in latch mode (MODE = Open) and making $\overline{EN}$ pin high asserts the $\overline{FLT}$ pin. See the *Parameter Measurement Information* for the behavior of $\overline{FLT}$ with $\overline{EN}$ pin.

8.4 Device Functional Modes

The TPS16530 device respond differently to overload with MODE pin configurations. Table 8-2 lists the operational differences.

Table 8-2. Device Operational Differences Under Different MODE Configurations

MODE Pin Configuration	Current Limiting, Over Current Fault and Thermal Shutdown Operation
Open	Active Current limiting for a maximum duration of $t_{CL\_ILIM(dly)}$. There after Latches OFF. Latch reset by toggling $\overline{SHDN}$ or UVLO low to high or power cycling IN.
Shorted to GND	Active Current limiting for a maximum duration of $t_{CL\_ILIM(dly)}$. There after auto-retries after a delay of $t_{(TSD\_retry)}$.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS16530 is a 58-V eFuse, typically used for Hot-Swap and Power rail protection applications. The device operates from 4.5 V to 58 V with programmable current limit, undervoltage protections. The device aids in controlling in-rush current and provides current limiting for systems such as telecom radios and industrial printers. The device also provides robust protection for multiple faults on the system rail.

The *Detailed Design Procedure* section can be used to select component values for the device.

9.2 Typical Application

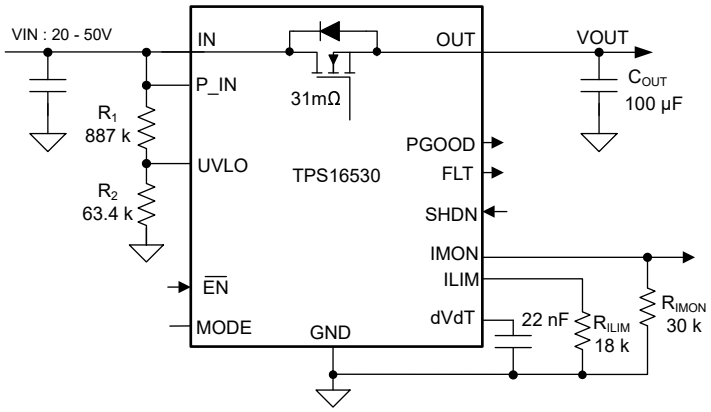


Figure 9-1. 20 V–50 V, 1-A eFuse Protection Circuit for Telecom Radios

9.2.1 Design Requirements

Table 9-1 shows the Design Requirements for TPS16530.

Table 9-1. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$V_{(IN)}$	Input voltage range	20 V–50 V
$V_{(UV)}$	Undervoltage lockout set point	18 V
$I_{(LIM)}$	Overload Current limit	1 A
C_{OUT}	Output capacitor	100 µF
$I_{(INRUSH)}$	Inrush Current limit	300 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Programming the Current-Limit Threshold $R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the overload current limit, which can be set using Equation 6.

$$R_{(ILIM)} = \frac{18}{I_{OL}} = 18k\Omega \quad (6)$$

where

- I_{LIM} = 1 A

Choose the closest standard 1% resistor value: $R_{(ILIM)}$ = 18 kΩ

9.2.2.2 Undervoltage Lockout and Overvoltage Set Point

The Undervoltage Lockout (UVLO) trip point are adjusted using an external voltage divider network of R_1 and R_2 connected between IN, UVLO, and GND pins of the device. The values required for setting the undervoltage are calculated by solving $V_{(UVLOR)} = R_2 / (R_1+R_2) \times V_{(UV\_IN)}$.

For minimizing the input current drawn from the power supply, {$I_{(R12)} = V_{(IN)} / (R_1 + R_2)$}, TI recommends to use higher value resistance for R_1 and R_2.

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, $I(R_{12})$ must be chosen to be 20 times greater than the leakage current of UVLO pin.

Choose the closest standard 1% resistor values: R_1 = 887 kΩ, R_2 = 63.4 kΩ.

9.2.2.3 Setting Output Voltage Ramp Time (t_{dVdT})

Use Equation 1 and Equation 2 to calculate required $C_{(dVdT)}$ for achieving an inrush current of 300 mA. $C_{(dVdT)}$ = 22 nF. Figure 9-2 and Figure 9-3 illustrate the inrush current limiting performance during 50-V hot-plug in condition.

9.2.2.3.1 Support Component Selections R_{PGOOD} and $C_{(IN)}$

The R_{PGOOD} serves as pull-up for the open-drain output. The current sink by this pin must not exceed 10 mA (see the *Absolute Maximum Ratings* table). TI recommends typical resistance value in the range of 10 kΩ to 100 kΩ for R_{PGOOD}. Figure 9-6 illustrates the power up performance of the system. The C_{IN} is a local bypass capacitor to suppress noise at the input. TI recommends a minimum of 0.1 µF for $C_{(IN)}$.

9.2.3 Application Curves

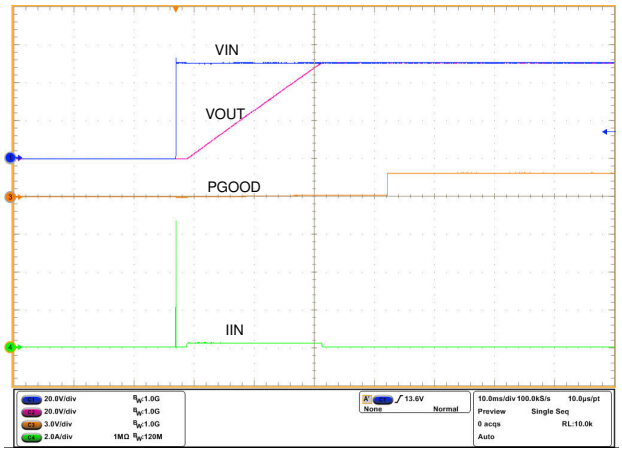


Figure 9-2. Hot-Plug In at 50-V Supply with No Load

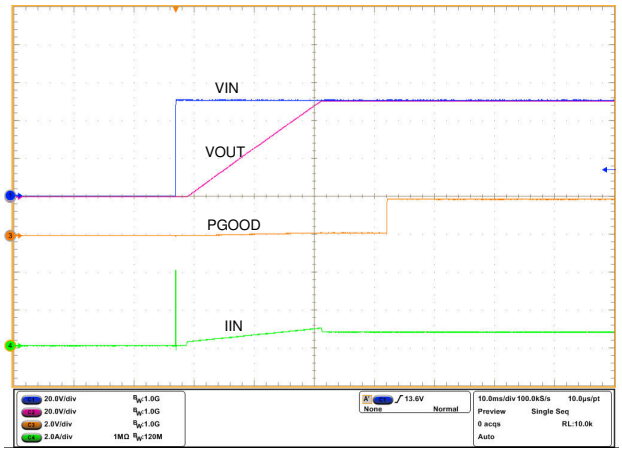
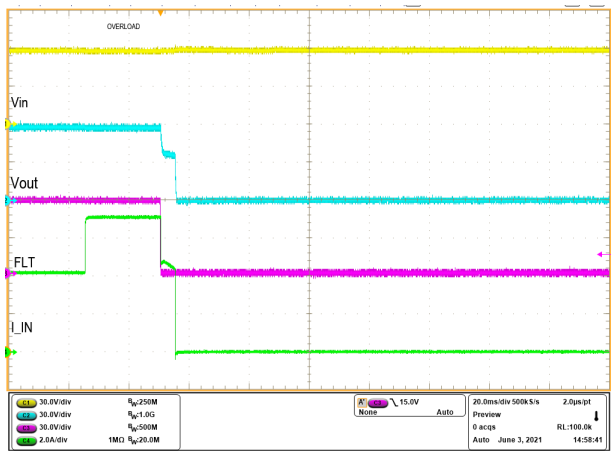


Figure 9-3. Hot-Plug In at 50-V Supply with 60-Ω Load



ILIM = 4.5 A

Figure 9-4. Overload Performance During Load Step from 4 A to 7 A

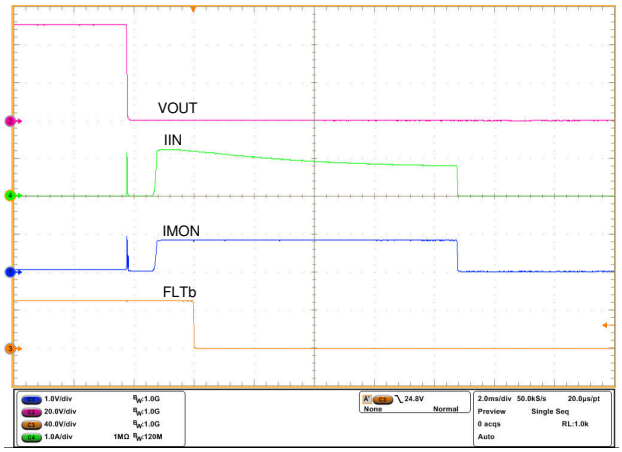


Figure 9-5. Output Hot-short Performance with 50-V Input Supply

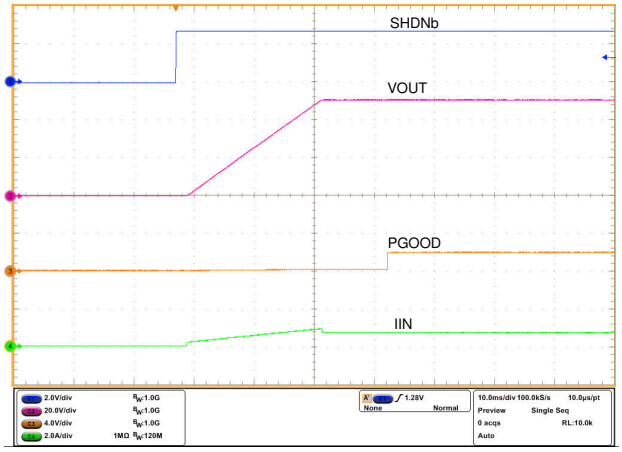


Figure 9-6. Turn ON Using $\overline{\text{SHDN}}$ Control

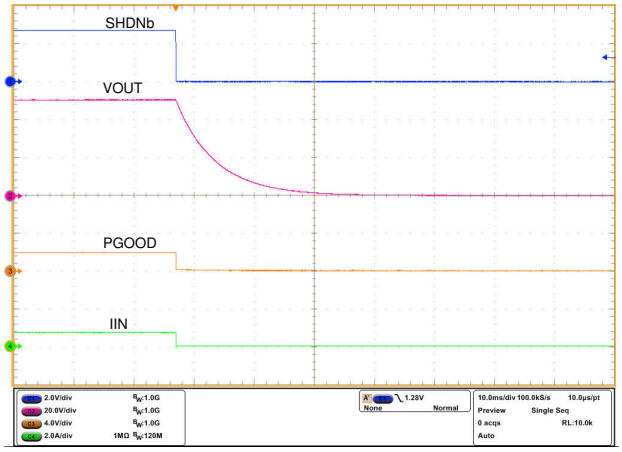


Figure 9-7. Turn OFF Using $\overline{\text{SHDN}}$ Control

9.3 System Examples

9.3.1 48-V Power Amplifier Protection for Telecom Radios

With the TPS16530, a simple 48-V power supply path protection can be realized for telecom radios. Figure 9-8 shows the simplified schematic for this. For start-up with negative gate voltage drive at GaN FETs, TI recommends to use appropriate resistors for biasing the gate of GaN FETs to keep V_{OUT} > –0.2 V and I_{OUT} < 70 µA from TPS16530.

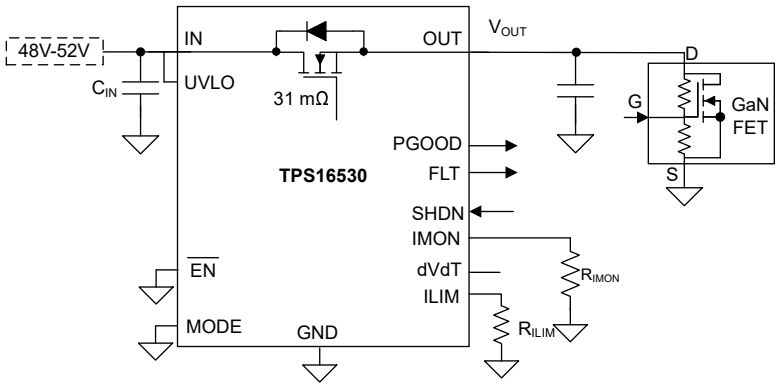


Figure 9-8. TPS16530 Configured for 48-V Power Amplifier Protection

Protection features with this configuration include:

- Accurate current limiting with pulse current support
- Inrush current control with 24-V/500-µs output voltage slew rate

10 Power Supply Recommendations

The TPS16530 eFuse is designed for the supply voltage range of 4.5 V ≤ V_{IN} ≤ 58 V. If the input supply is located more than a few inches from the device, TI recommends an input ceramic bypass capacitor higher than 0.1 µF. Power supply must be rated higher than the current limit set to avoid voltage droops during overcurrent and short circuit conditions.

10.1 Transient Protection

In case of short circuit and overload current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 7.

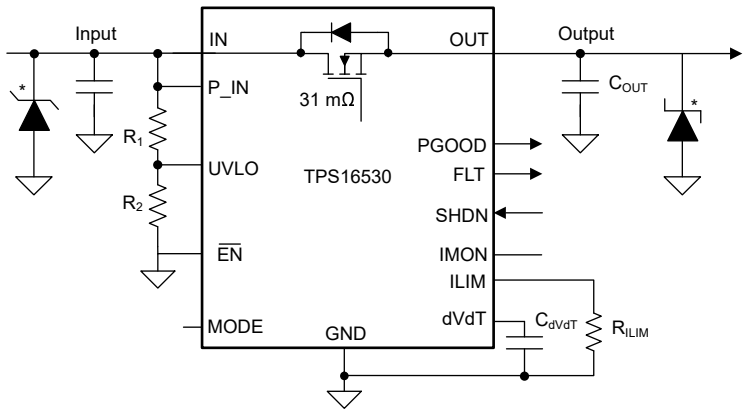
$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (7)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during positive and negative surge tests on the supply lines. In such applications, TI recommends to place at least 1 µF of input capacitor.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 10-1.



* Optional components needed for suppression of transients

Figure 10-1. Circuit Implementation with Optional Protection Components for TPS16530

11 Layout

11.1 Layout Guidelines

- For all the applications, a 0.1 µF or higher value ceramic decoupling capacitor is recommended between IN terminal and GND.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current. See Figure 11-1 and Figure 11-2 for a typical PCB layout example.
- Locate all the TPS16530 device support components $R_{(ILIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, UVLO resistors close to the device pin. Connect the other end of the component to the GND with shortest trace length.
- The trace routing for the $R_{(ILIM)}$ component to the device must be as short as possible to reduce parasitic effects on the current limit accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: When properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board GND plane directly under the device. Other planes, such as the bottom side of the circuit board, can be used to increase heat sinking in higher current applications.

11.2 Layout Example

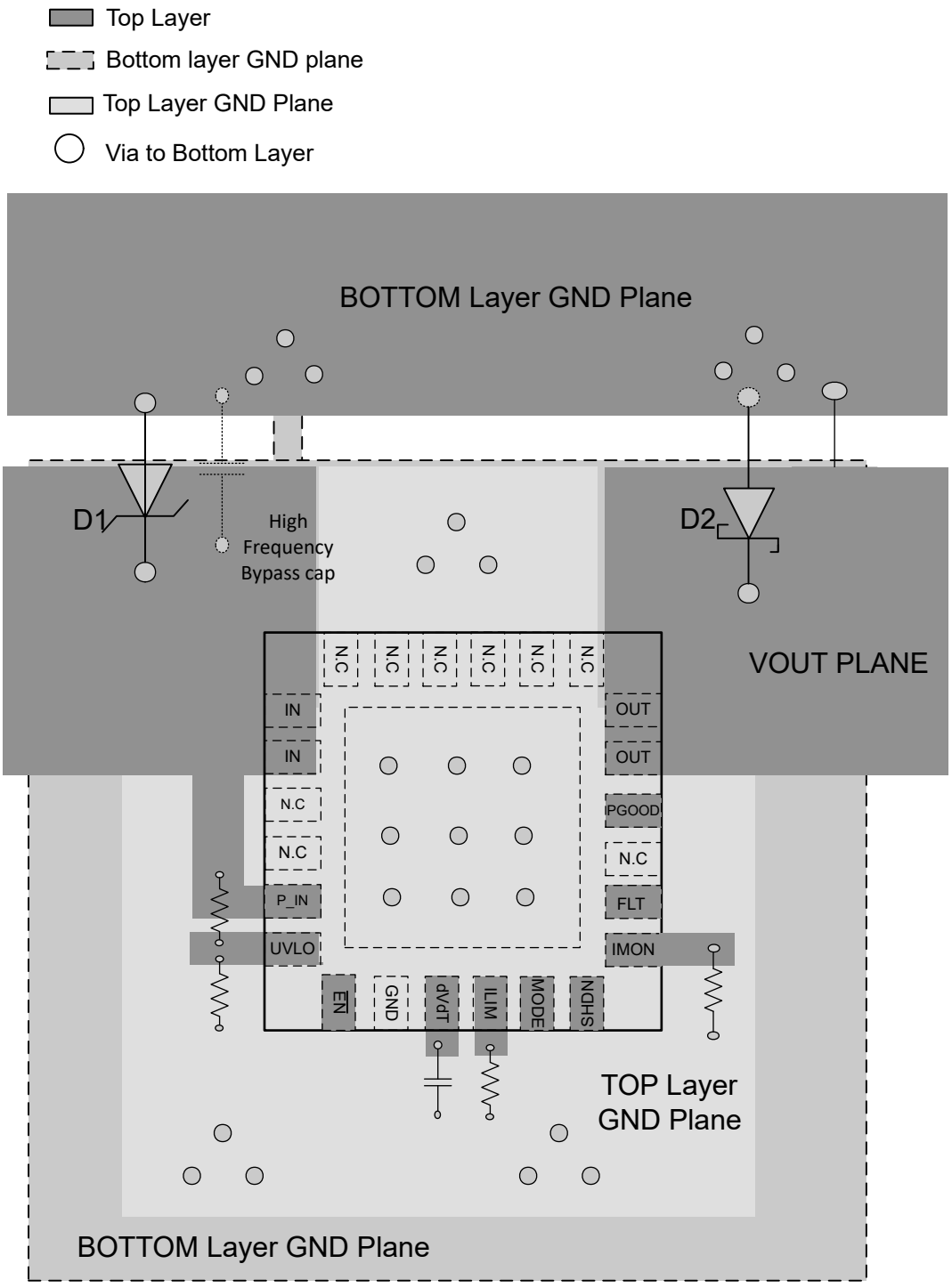


Figure 11-1. PCB Layout Example With QFN Package With a 2-Layer PCB

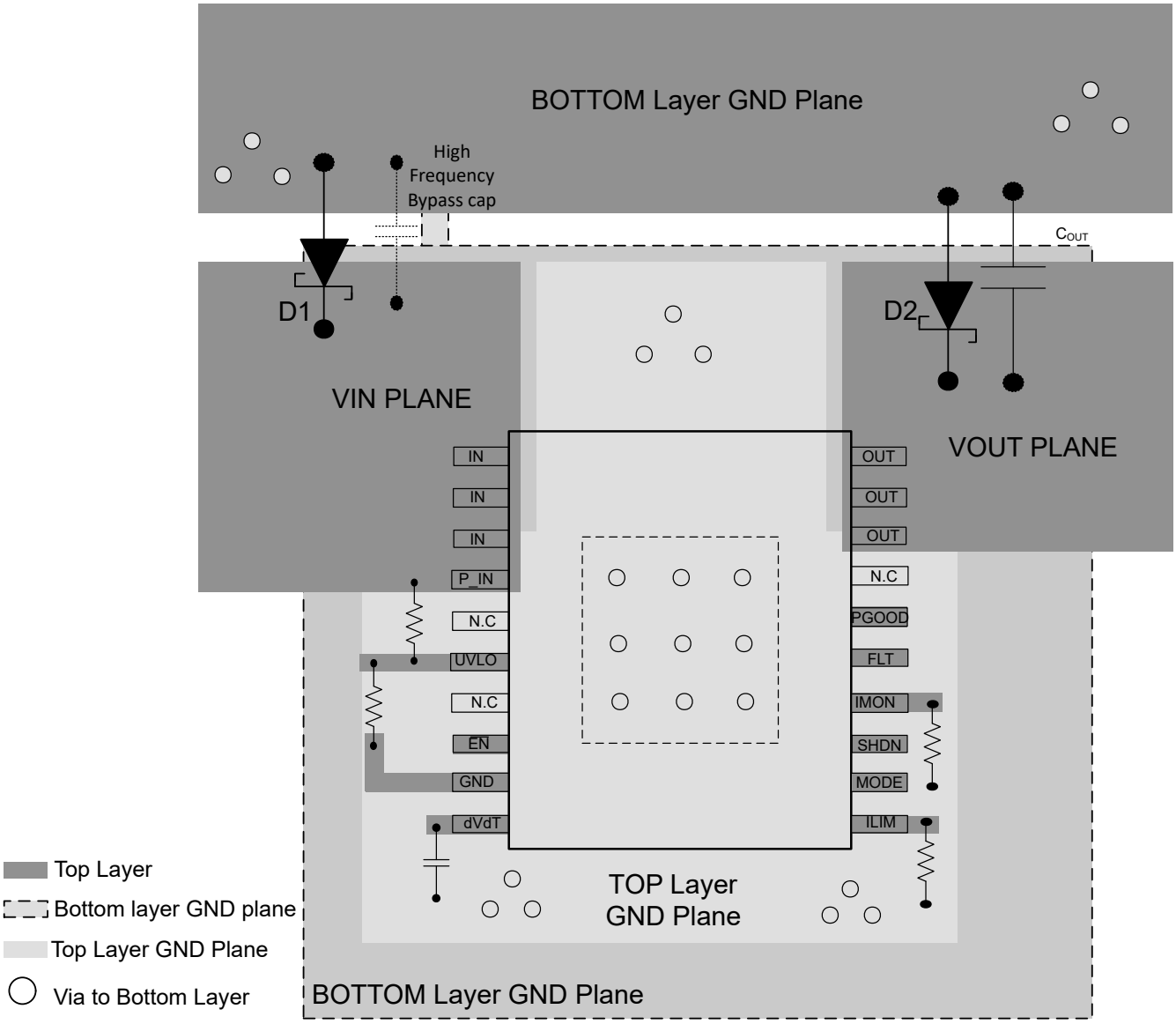


Figure 11-2. Typical PCB Layout Example With HTSSOP Package With a 2-Layer PCB

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *TPS1653 Design Calculator*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS16530PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS16530	Samples
TPS16530RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16530	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

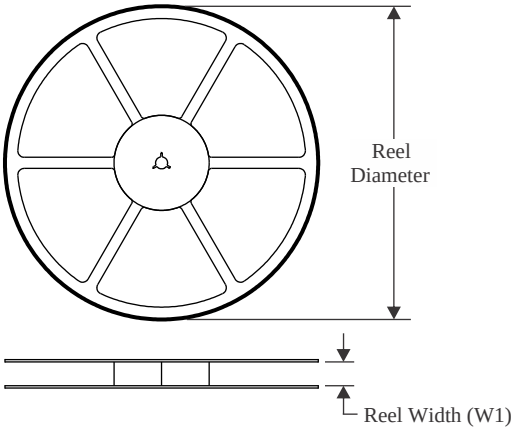
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

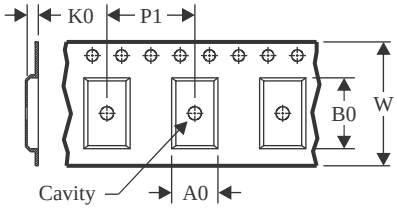
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

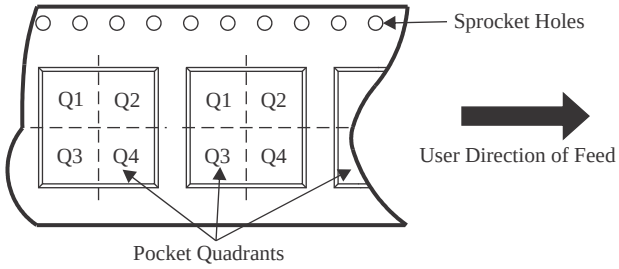


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

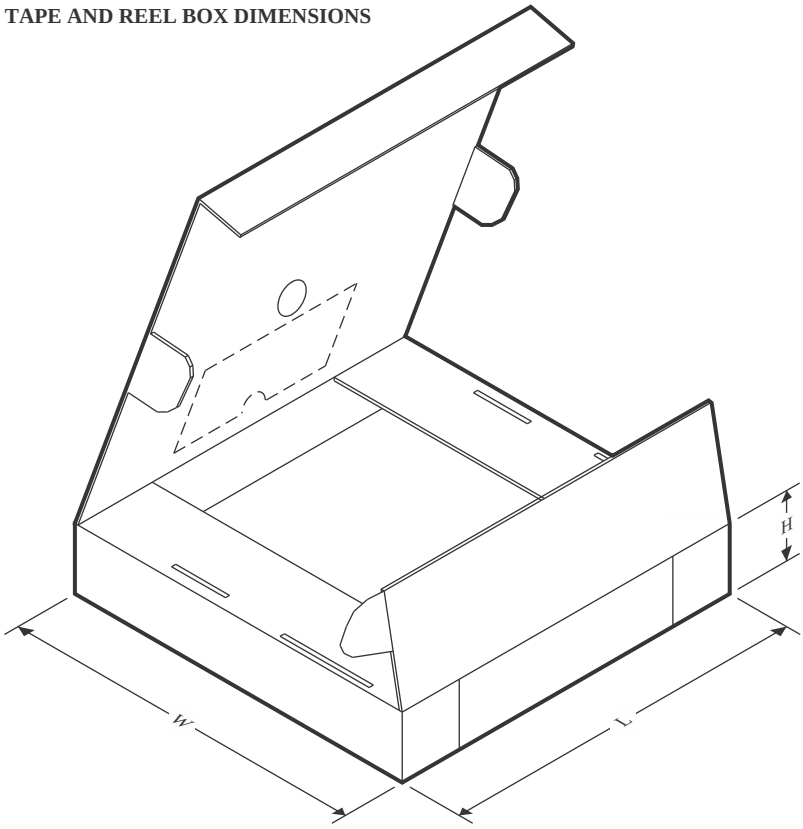
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS16530PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS16530RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

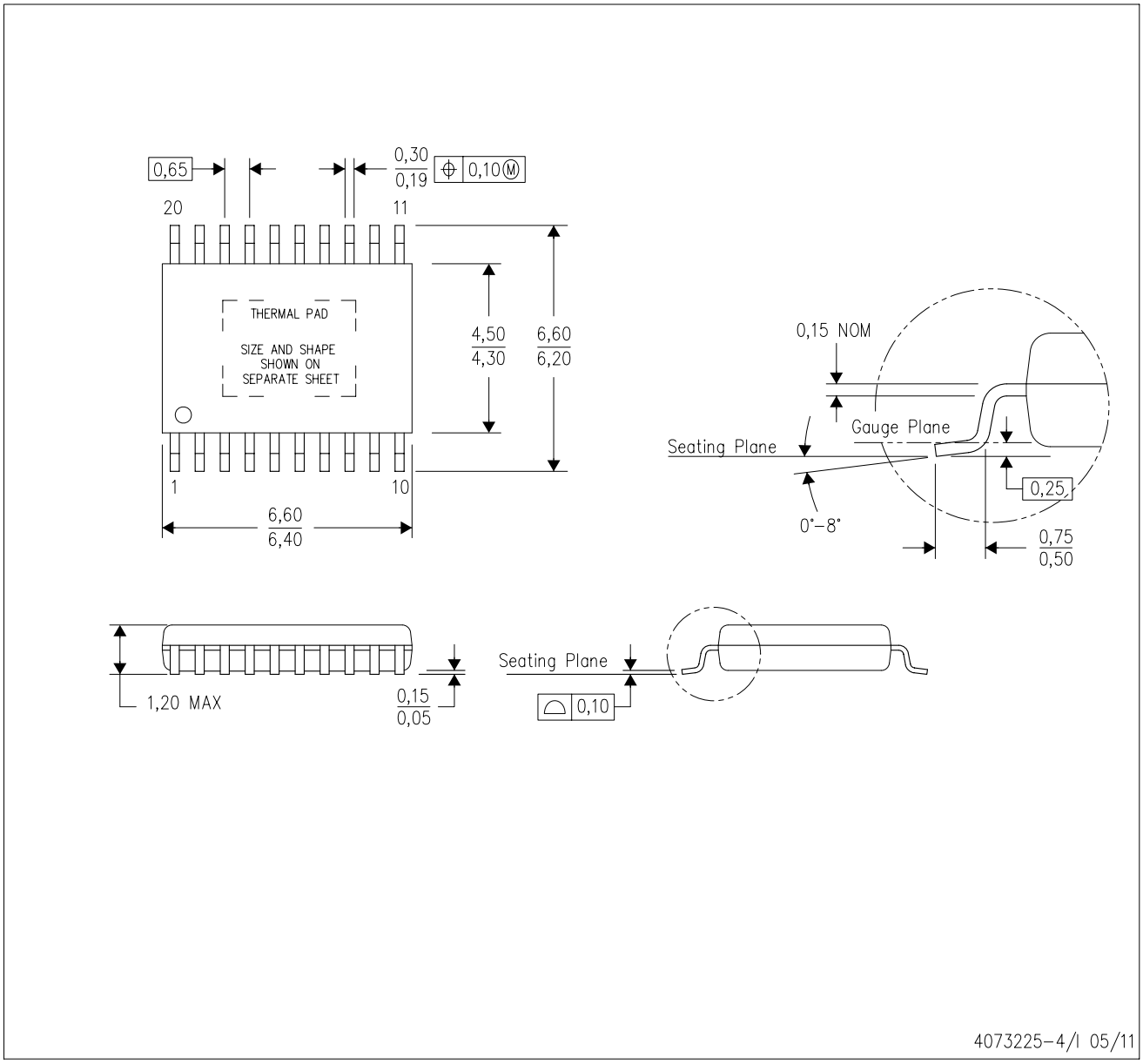
TAPE AND REEL BOX DIMENSIONS



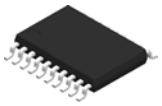
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS16530PWPR	HTSSOP	PWP	20	2000	356.0	356.0	35.0
TPS16530RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

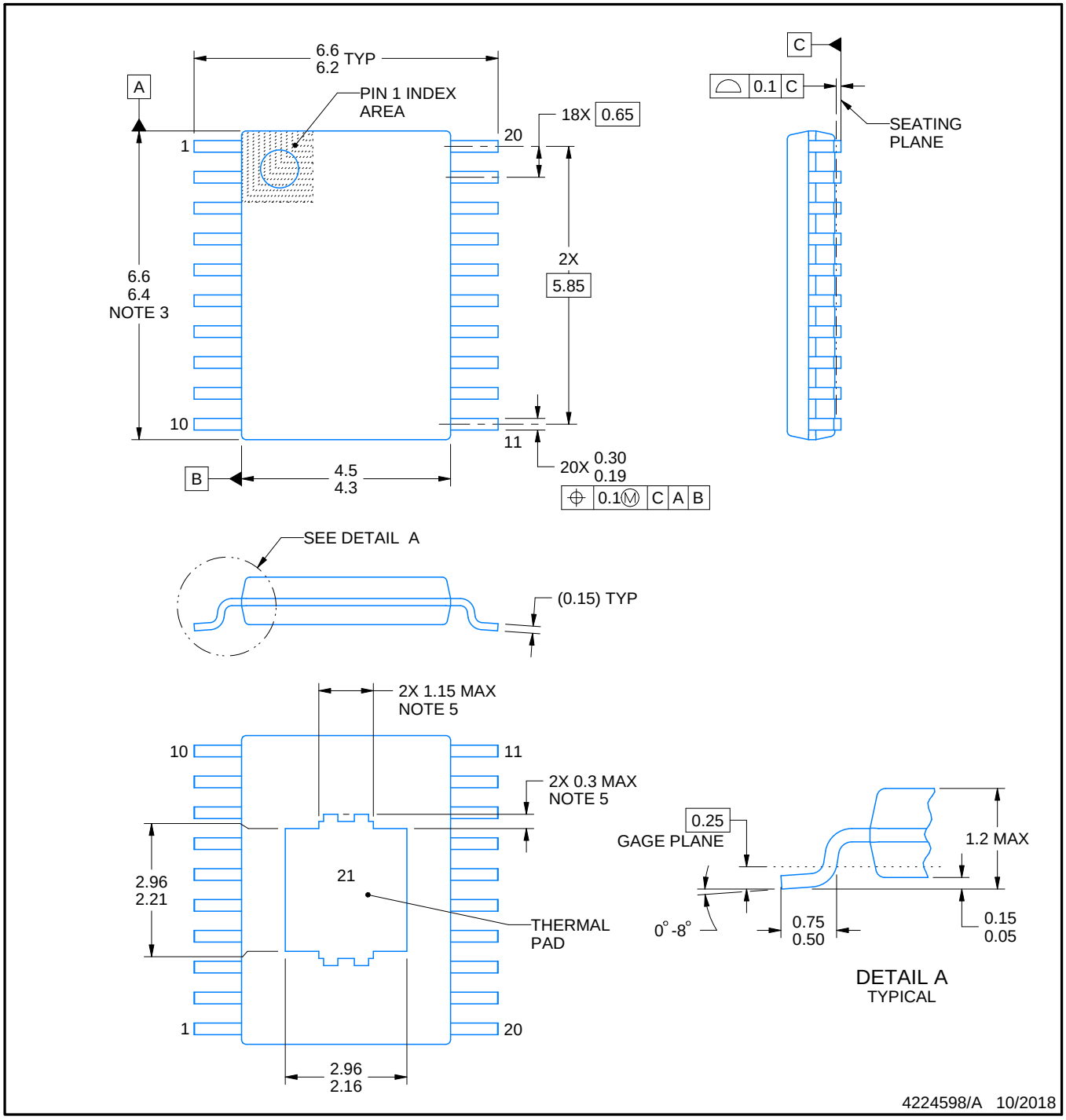


PACKAGE OUTLINE

PWP0020T

PowerPAD™ TSSOP - 1.2 mm max height

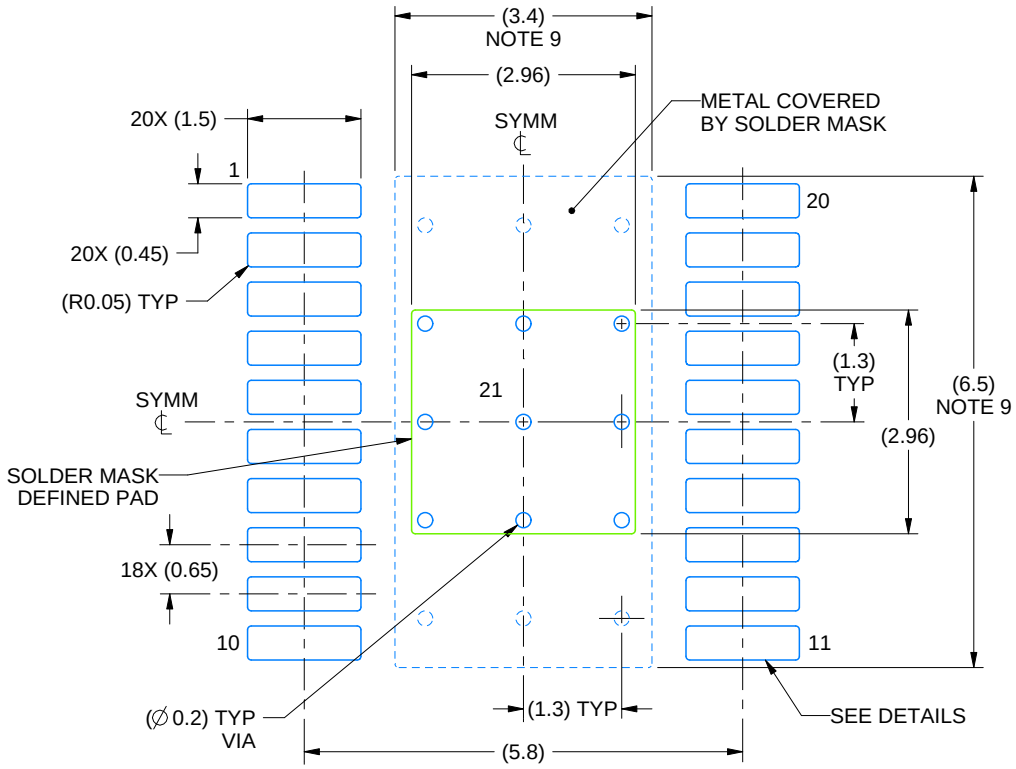
SMALL OUTLINE PACKAGE



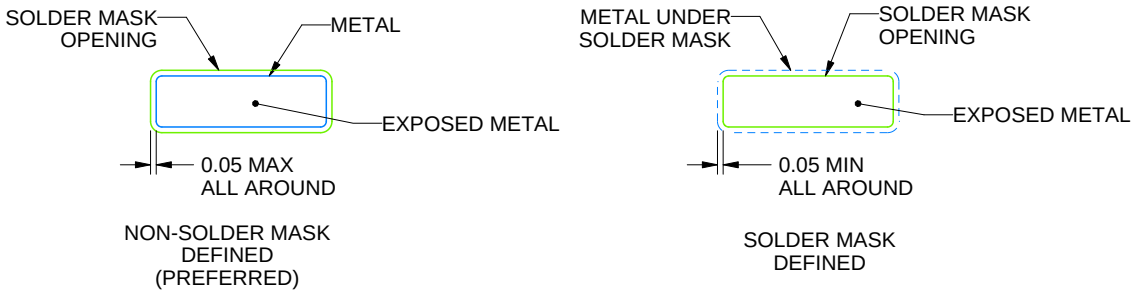
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

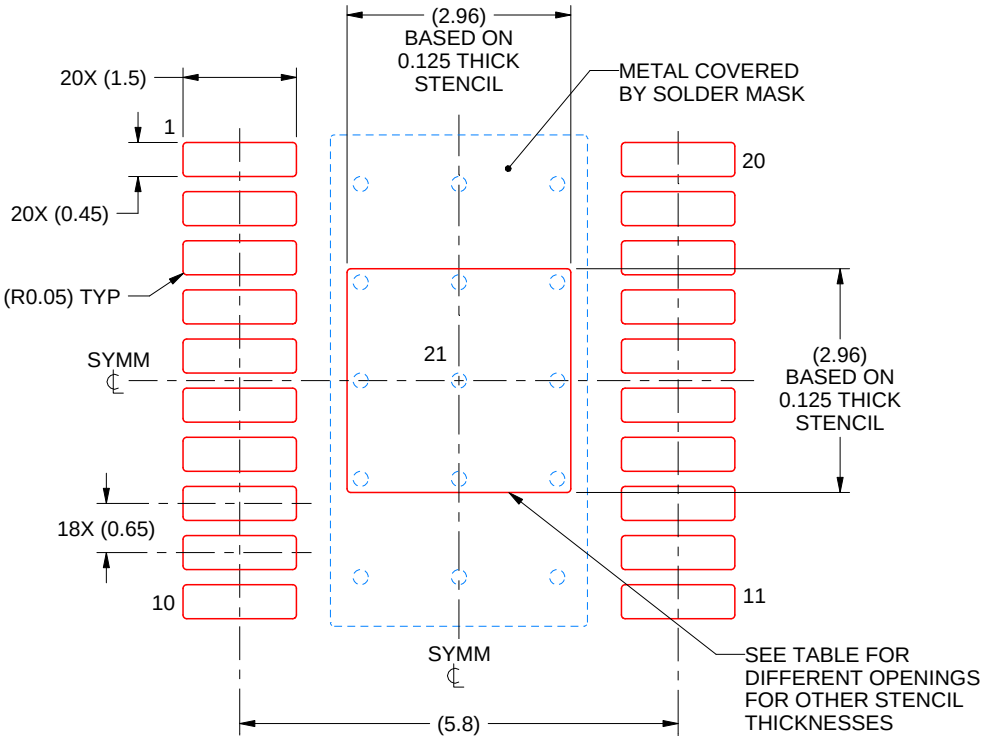


SOLDER MASK DETAILS

4224598/A 10/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.31 X 3.31
0.125	2.96 X 2.96 (SHOWN)
0.15	2.70 X 2.70
0.175	2.50 X 2.50

4224598/A 10/2018

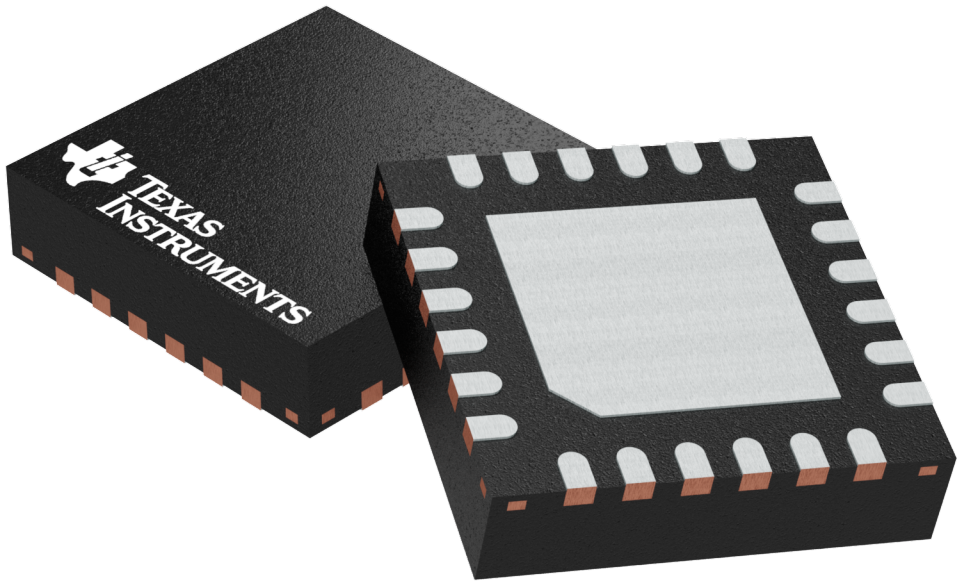
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

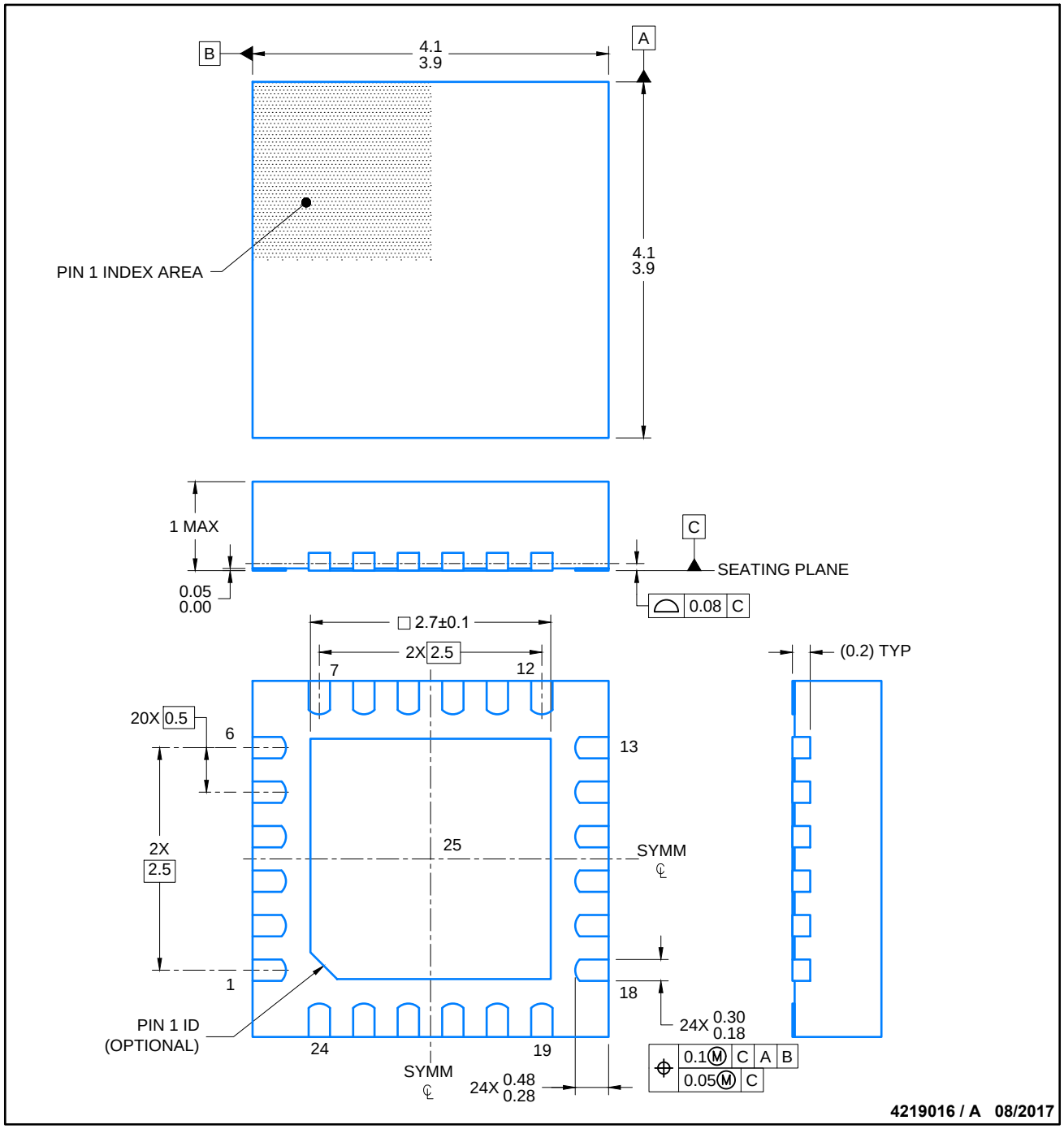
4204104/H

PACKAGE OUTLINE

RGE0024H

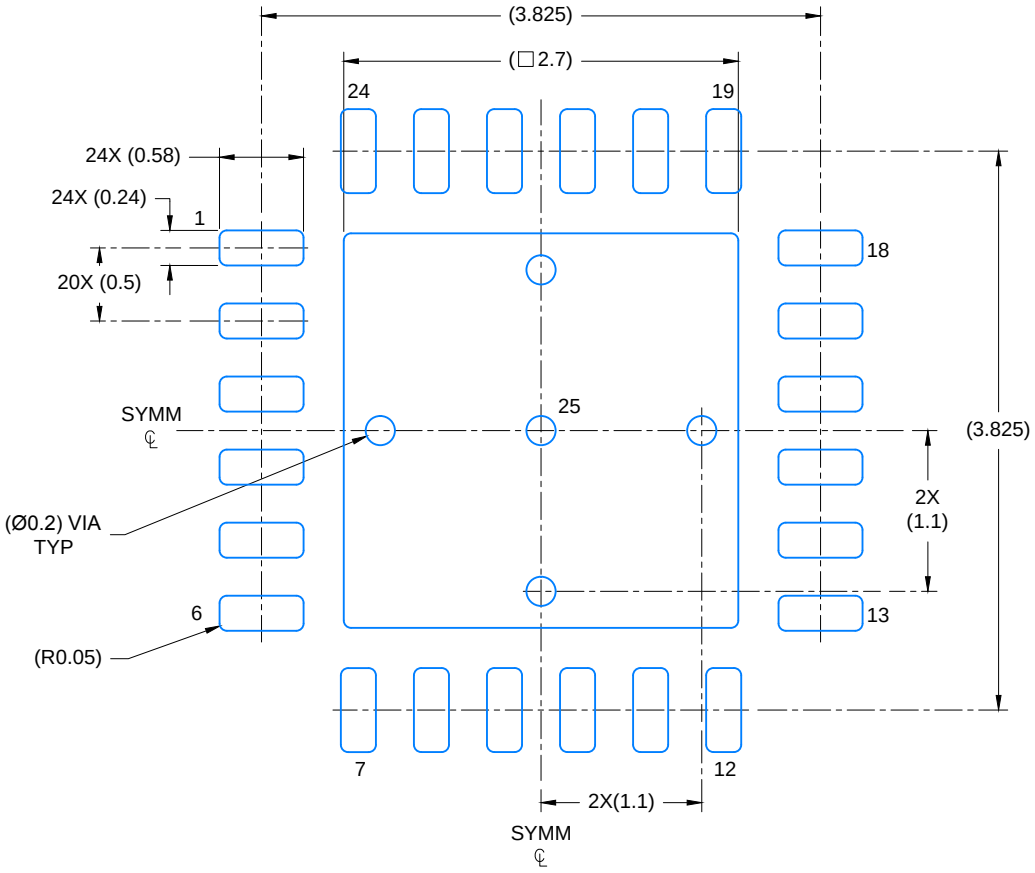
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



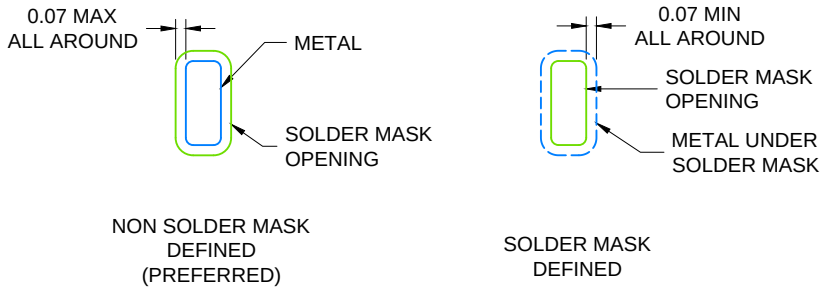
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

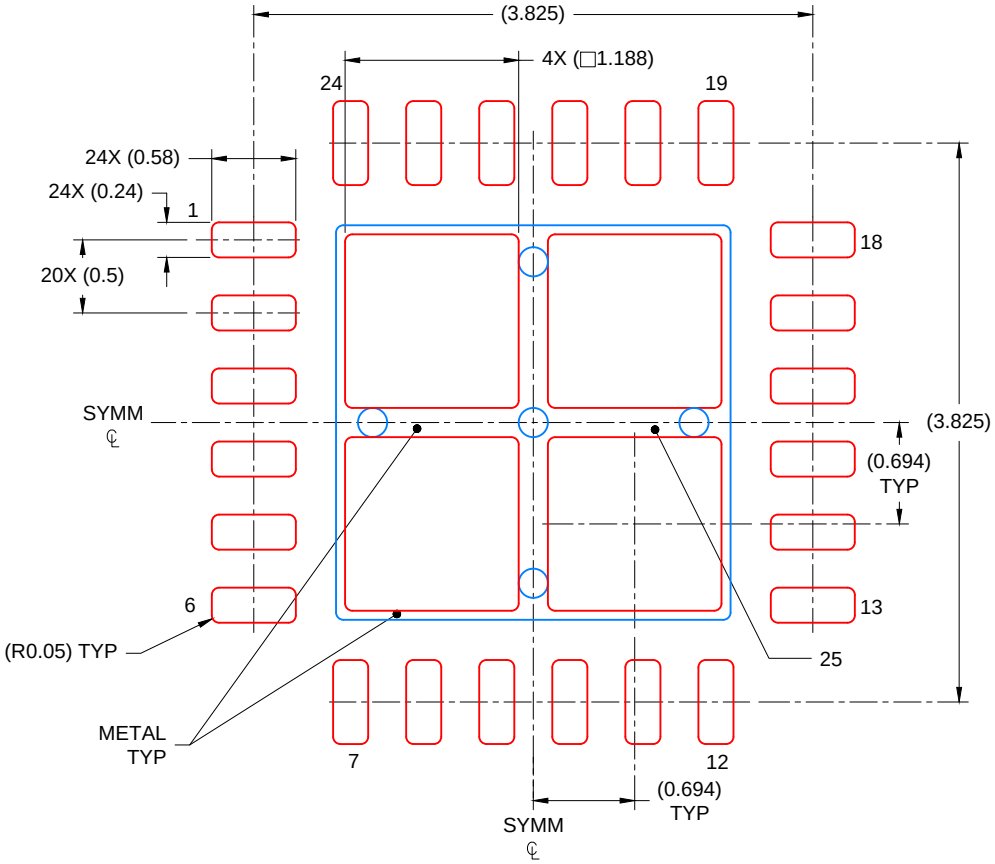


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265