TPS22919 5.5 V, 1.5 A, 90-mΩ Self-Protected Load Switch with Controlled Rise Time

1 Features

- Input operating voltage range (V_{IN}): 1.6 V to 5.5 V
- Maximum continuous current (I_{MAX}): 1.5 A
- On-Resistance (R_{ON}):
  - 5-V V_{IN}: 89 mΩ (typical)
  - 3.6-V V_{IN}: 90 mΩ (typical)
  - 1.8-V V_{IN}: 105 mΩ (typical)
- Output short protection (I_{SC}): 3 A (typical)
- Low power consumption:
  - ON state (I_Q): 8 µA (typical)
  - OFF state (I_{SD}): 2 nA (typical)
- Smart ON pin pull down (R_{PD}):
  - ON ≥ V_{IH} (I_{ON}): 100 nA (maximum)
  - ON ≤ V_{IL} (R_{PD}): 530 kΩ (typical)
- Slow Turn ON timing to limit inrush current (t_{ON}):
  - 5.0 V Turn ON time (t_{ON}): 1.95 ms at 3.2 mV/µs
  - 3.6 V Turn ON time (t_{ON}): 1.75 ms at 2.7 mV/µs
  - 1.8 V Turn ON time (t_{ON}): 1.5 ms at 1.8 mV/µs
- Adjustable output discharge and fall time:
  - Internal QOD resistance = 24 Ω (typical)

2 Applications

- Personal electronics
- Set top box
- HDTV
- Multi function printer

3 Description

The TPS22919 device is a small, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.6 V to 5.5 V and can support a maximum continuous current of 1.5 A.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. When power is first applied, a Smart Pull Down is used to keep the ON pin from floating until system sequencing is complete. Once the pin is deliberately driven High (>V_{IH}), the Smart Pull Down will be disconnected to prevent unnecessary power loss.

The TPS22919 load switch is also self-protected, meaning that it will protect itself from short circuit events on the output of the device. It also has thermal shutdown to prevent any damage from overheating.

TPS22919 is available in a standard SC-70 package characterized for operation over a junction temperature range of –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22919DCK	SC-70 (6)	2.1 mm × 2.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

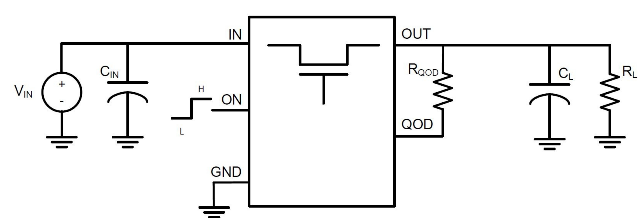


Table of Contents

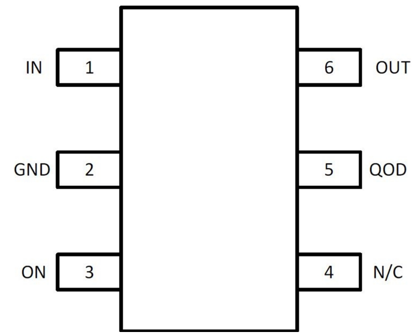
4 Revision History

Changes from Revision A (February 2019) to Revision B	Page

Changes from Original (October 2018) to Revision A	Page
• Changed Advanced Information to Production Data	1

5 Pin Configuration and Functions

DCK Package
6-Pin SC-70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input.
2	GND	—	Device ground.
3	ON	I	Active high switch control input. Do not leave floating.
4	NC	—	No connect pin, leave floating.
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways. • Placing an external resistor between VOUT and QOD • Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin floating See the *Fall Time (t_{FALL}) and Quick Output Discharge (QOD)* section for more information.
6	VOUT	O	Switch output.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	–0.3	6	V
V_{OUT}	Maximum Output Voltage Range	–0.3	6	V
V_{ON}	Maximum ON Pin Voltage Range	–0.3	6	V
V_{QOD}	Maximum QOD Pin Voltage Range	–0.3	6	V
I_{MAX}	Maximum Continuous Current		1.5	A
I_{PLS}	Maximum Pulsed Current (2 ms, 2% Duty Cycle)		2.5	A
T_J	Junction temperature	Internally Limited		°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	1.6		5.5	V
V_{OUT}	Output Voltage Range	0		5.5	V
V_{IH}	ON Pin High Voltage Range	1		5.5	V
V_{IL}	ON Pin Low Voltage Range	0		0.35	V
T_A	Ambient Temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS22919	UNIT
		DCK (SC-70)	
		PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	142.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	52.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	68.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Typical values at VIN = 3.6V unless otherwise specified

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
Input Supply (VIN)								
$I_{Q,\ VIN}$	VIN Quiescent Current	$V_{ON} \geq V_{IH}$, VOUT = Open		25°C		8	15	µA
				-40°C to 125°C			20	µA
$I_{SD,\ VIN}$	VIN Shutdown Current	$V_{ON} \leq V_{IL}$, VOUT = GND		25°C		2	20	nA
				-40°C to 125°C			800	nA
ON-Resistance (RON)								
R_{ON}	ON-State Resistance	I_{OUT} = -200 mA	V_{IN} = 5 V	25°C		89	125	mΩ
				-40°C to 85°C			150	mΩ
				-40°C to 105°C			175	mΩ
				-40°C to 125°C			200	mΩ
			V_{IN} = 3.6 V	25°C		90	150	mΩ
				-40°C to 85°C			200	mΩ
				-40°C to 105°C			225	mΩ
				-40°C to 125°C			250	mΩ
			V_{IN} = 1.8 V	25°C		105	300	mΩ
				-40°C to 85°C			400	mΩ
				-40°C to 105°C			450	mΩ
				-40°C to 125°C			500	mΩ
Output Short Protection (ISC)								
I_{SC}	Short Circuit Current Limit	$V_{OUT} \leq V_{IN}$ - 1.5 V		-40°C to 125°C		3		A
		$V_{OUT} \leq V_{SC}$		-40°C to 125°C	30	500	900	mA
V_{SC}	Output Short Detection Threshold	V_{IN} - V_{OUT}		-40°C to 125°C	0.3	0.36	0.46	V
t_{SC}	Output Short Reponse Time	V_{IN} = 1.6V to 5.5V, 10mΩ short applied		-40°C to 125°C		2		µs
T_{SD}	Thermal Shutdown			Rising		180		℃
				Falling		145		℃
Enable Pin (ON)								
I_{ON}	ON Pin Leakage	$V_{ON} \geq V_{IH}$		-40°C to 125°C			100	nA
$R_{PD,\ ON}$	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$		-40°C to 125°C		530		kΩ
Quick-output Discharge (QOD)								
$R_{PD,\ QOD}$	QOD Pin Internal Discharge Resistance	$V_{ON} \leq V_{IL}$		-40°C to 125°C		24		Ω

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of CL = 0.1 µF, RL = 100 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	VIN = 5.0 V			1950		µs
		VIN = 3.6 V			1750		µs
		VIN = 1.8 V			1500		µs
t_R	Output Rise Time	VIN = 5.0 V			1280		µs
		VIN = 3.6 V			1100		µs
		VIN = 1.8 V			750		µs
SR_{ON}	Turn ON Slew Rate	VIN = 5.0 V			3.2		mV/µs
		VIN = 3.6 V			2.7		mV/µs
		VIN = 1.8 V			1.8		mV/µs
t_{OFF}	Turn OFF Time	VIN = 1.8 V to 5.0V	R_L = 100Ω, C_L = 0.1uF		6		µs

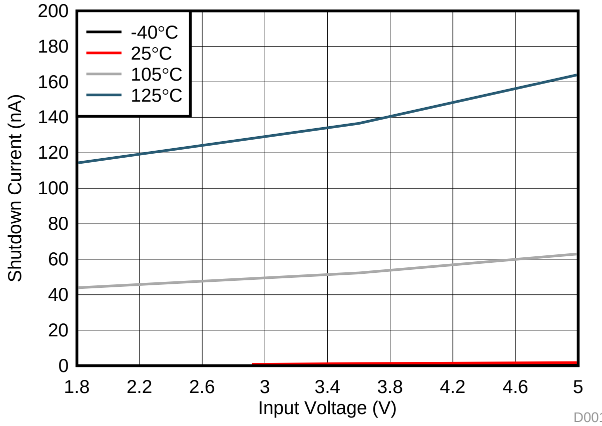
Switching Characteristics (continued)

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of CL = 0.1 µF, RL = 100 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{FALL}	Output Fall Time (1)	R_L = 100Ω	C_L = 0.1uF, R_{QOD} = Short		10		µs
		R_L = Open (2)	C_L = 10uF, R_{QOD} = Short		0.4		ms
			C_L = 10uF, R_{QOD} = 100 Ω		3.5		ms
			C_L = 100uF, R_{QOD} = Short		4		ms

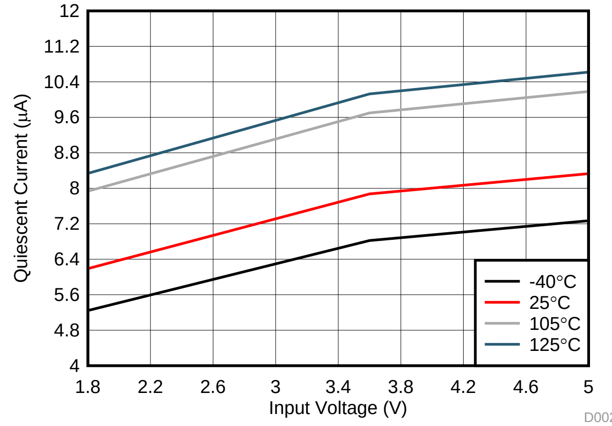
(1) Output may not discharge completely if QOD is not connected to VOUT
(2) See the *Timing Application* section for information on how R_L and C_L affect Fall Time.

6.7 Typical Characteristics



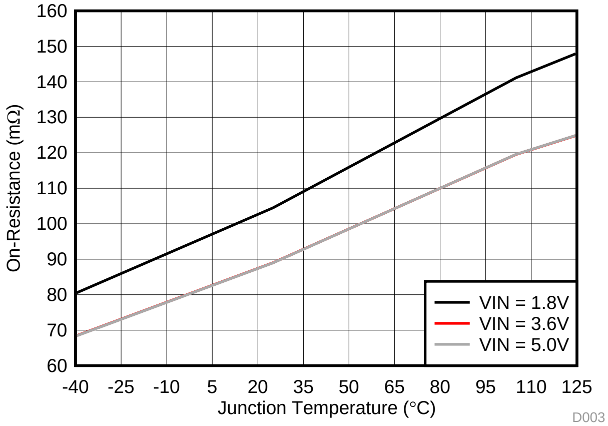
$V_{ON} \leq V_{IL}$

Figure 1. Shutdown Current vs Input Voltage



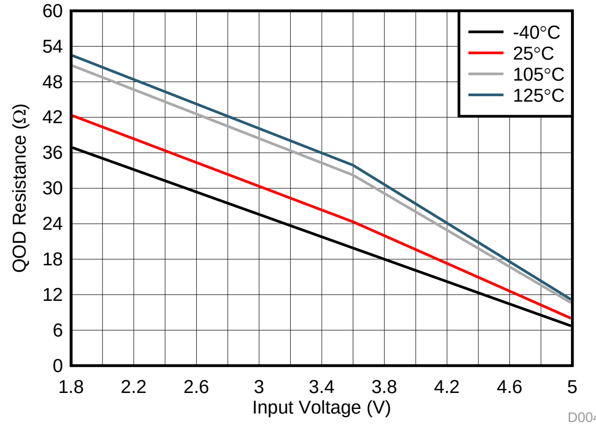
$V_{ON} \geq V_{IH}$

Figure 2. Quiescent Current vs Input Voltage



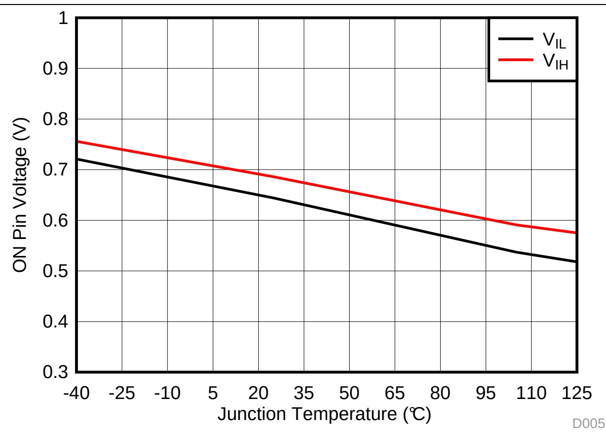
I_{LOAD} = –200 mA

Figure 3. On-Resistance vs Junction Temperature



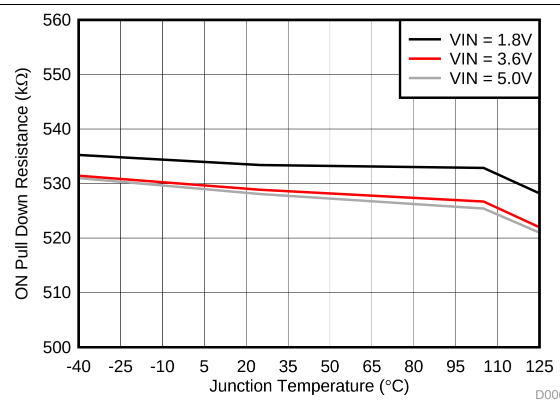
$V_{ON} \leq V_{IL}$

Figure 4. QOD Resistance vs Input Voltage



$V_{ON} \leq V_{IL}$

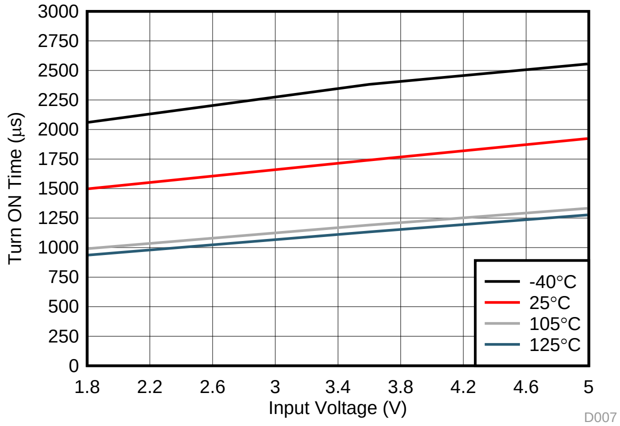
Figure 5. V_{IH}/V_{IL} vs Junction Temperature



$V_{ON} \leq V_{IL}$

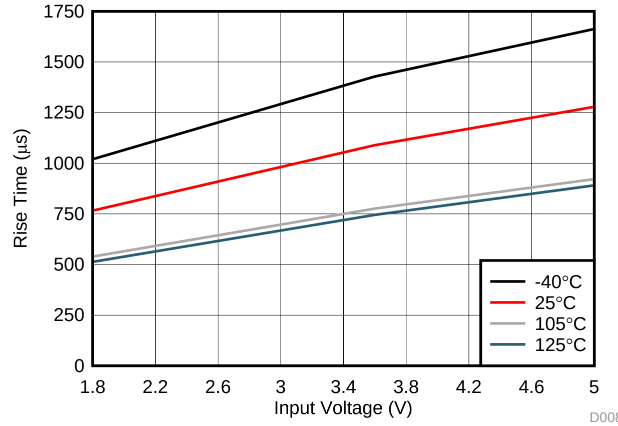
Figure 6. ON Pull Down Resistance vs Junction Temperature

Typical Characteristics (continued)



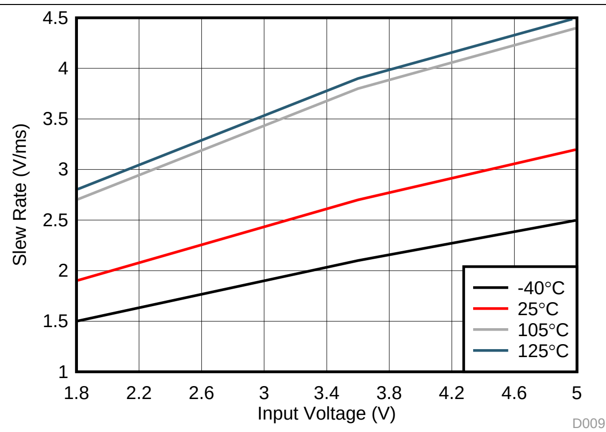
C_L = 0.1 µF R_L = 100 Ω

Figure 7. Turn ON Time vs Input Voltage



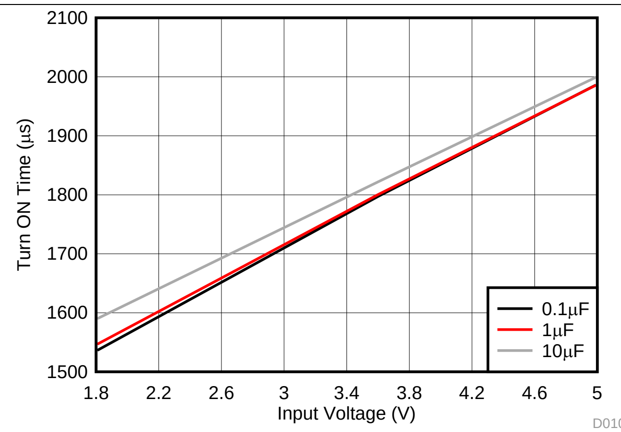
C_L = 0.1 µF R_L = 100 Ω

Figure 8. Rise Time vs Input Voltage



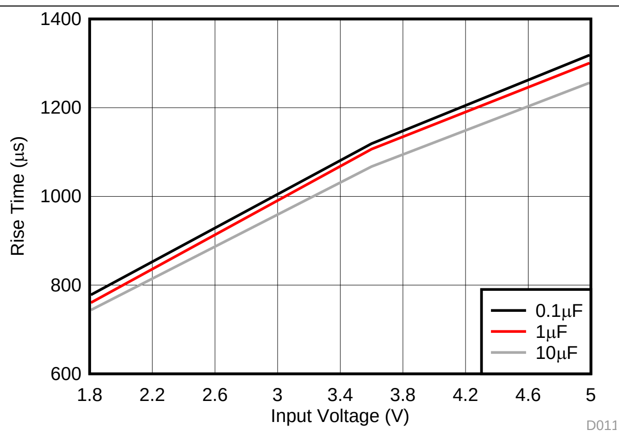
C_L = 0.1 µF R_L = 100 Ω

Figure 9. Output Slew Rate vs Input Voltage



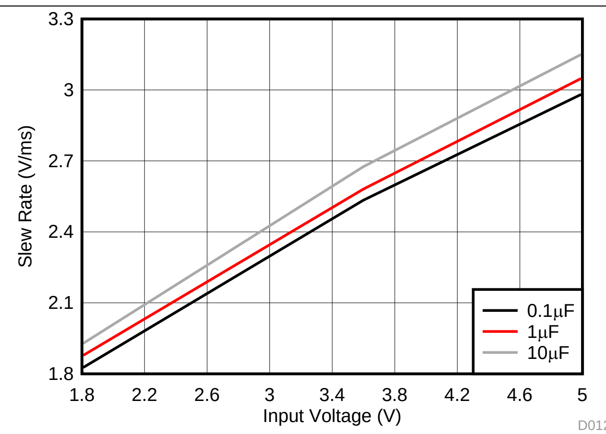
R_L = 100 Ω T_J = 25°C

Figure 10. Turn ON Time vs Input Voltage Across Load Capacitance



R_L = 100 Ω T_J = 25°C

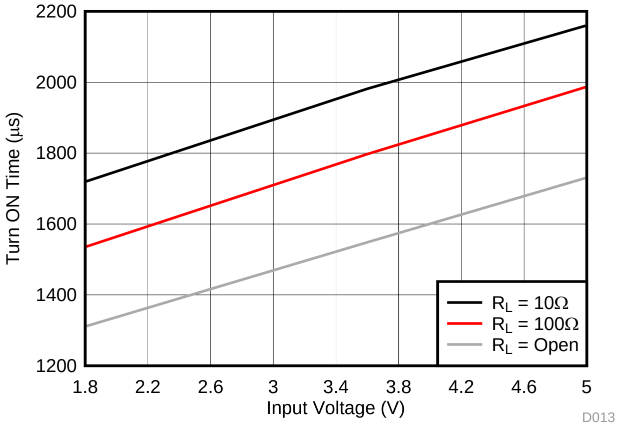
Figure 11. Rise Time vs Input Voltage Across Load Capacitance



R_L = 100 Ω T_J = 25°C

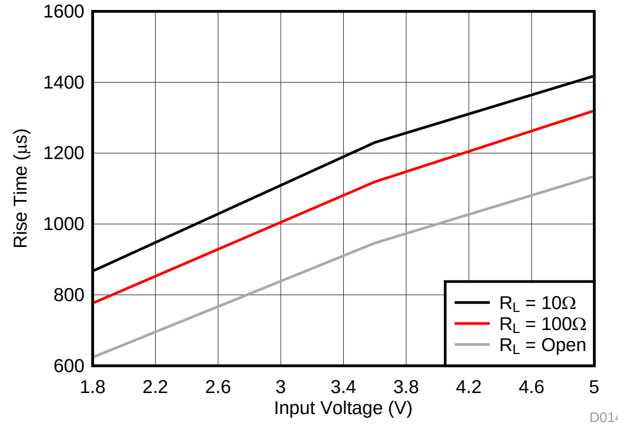
Figure 12. Slew Rate vs Input Voltage Across Load Capacitance

Typical Characteristics (continued)



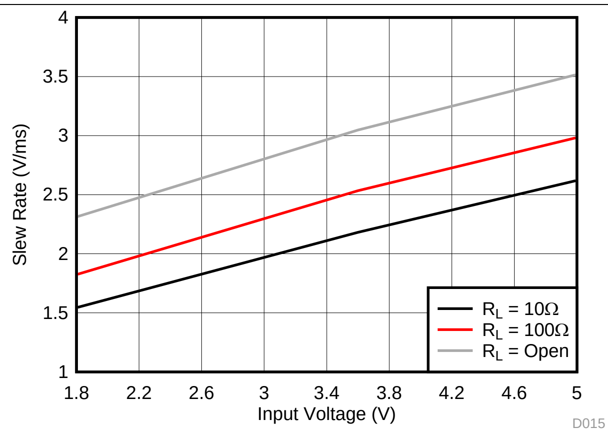
C_L = 0.1 µF T_J = 25°C

Figure 13. Turn ON Time vs Input Voltage Across Load Resistance



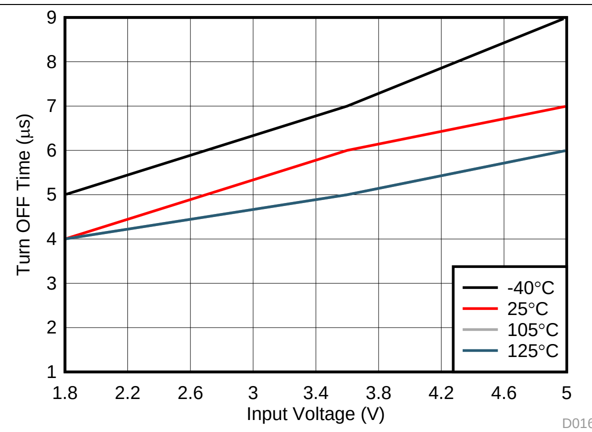
C_L = 0.1 µF T_J = 25°C

Figure 14. Rise Time vs Input Voltage Across Load Resistance



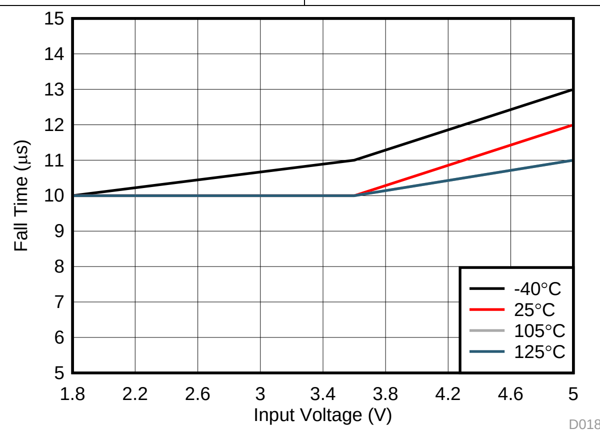
C_L = 0.1 µF T_J = 25°C

Figure 15. Output Slew Rate vs Input Voltage Across Load Resistance



C_L = 0.1 µF R_L = 100 Ω

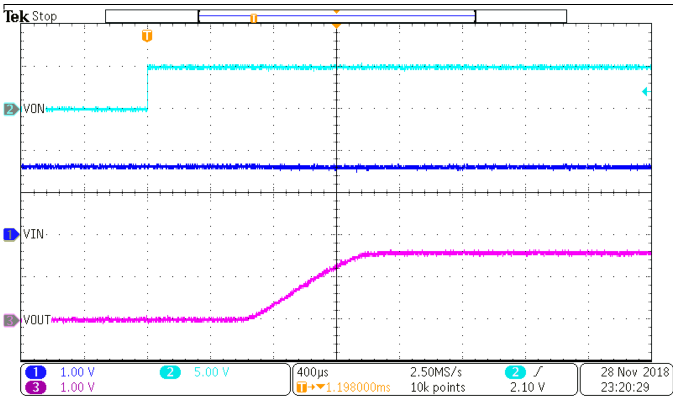
Figure 16. Turn OFF Time vs Input Voltage



C_L = 0.1 µF R_L = 100 Ω $R_{PD,QOD}$ = Short

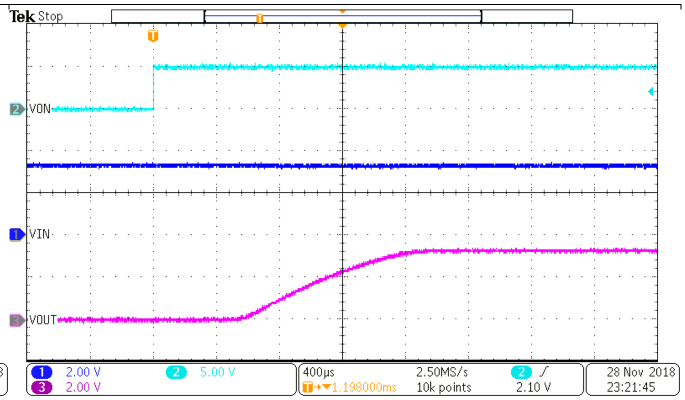
Figure 17. Fall Time vs Input Voltage

Typical Characteristics (continued)



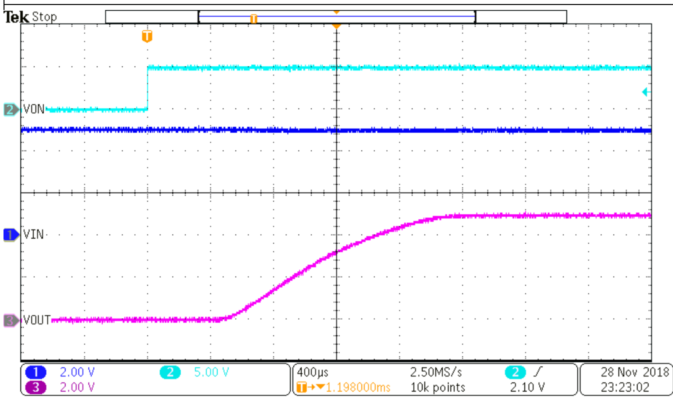
C_L = 0.1 µF R_L = 100 Ω

Figure 18. Rise Time with VIN = 1.8 V



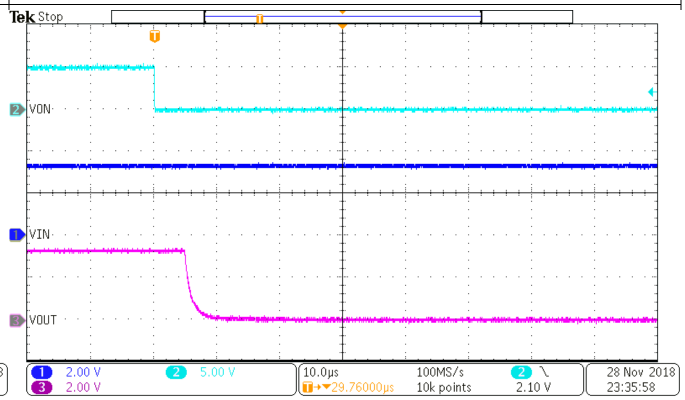
C_L = 0.1 µF R_L = 100 Ω

Figure 19. Rise Time with VIN = 3.3 V



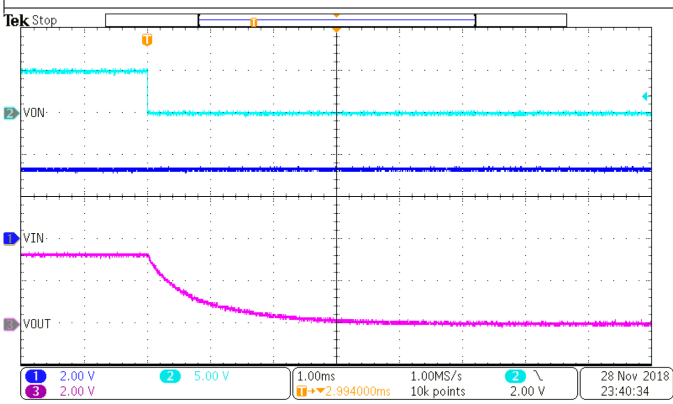
C_L = 0.1 µF R_L = 100 Ω

Figure 20. Rise Time with VIN = 5 V



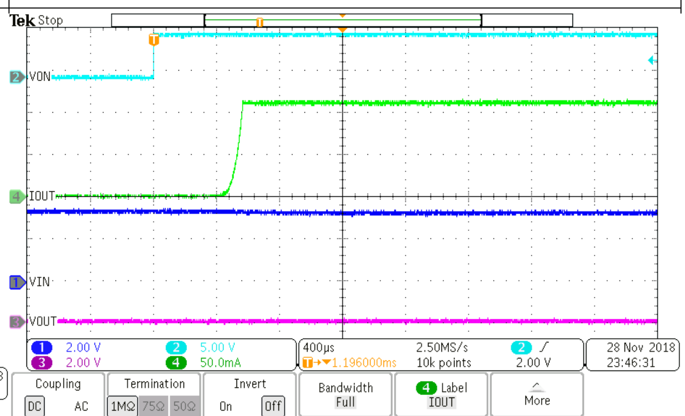
C_L = Open R_L = 100 Ω

Figure 21. Turn off with a small load capacitance



C_L = 10 µF R_L = 100 Ω

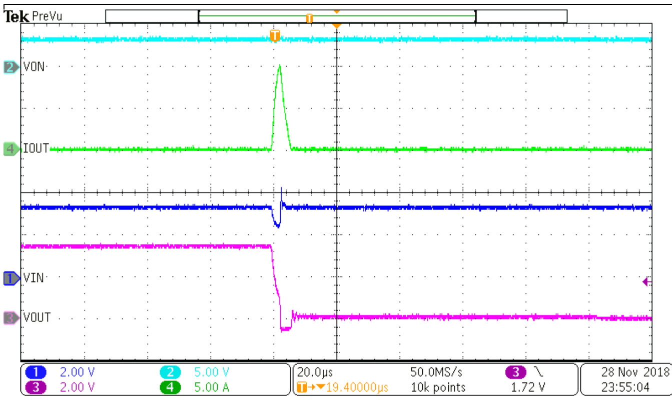
Figure 22. Turn off with a large load capacitance



V_{IN} = 3.3 V

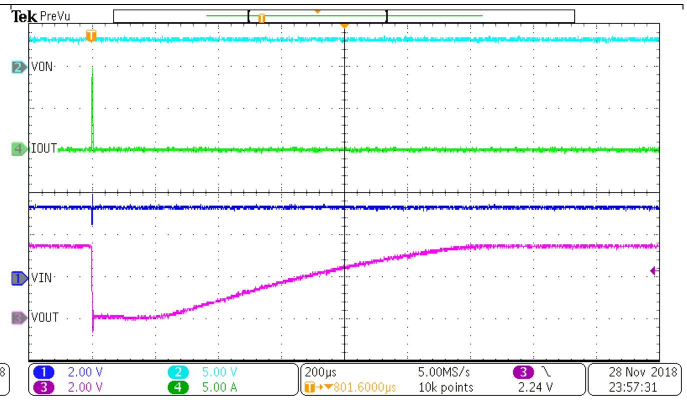
Figure 23. Turn on into an output short

Typical Characteristics (continued)



V_{IN} = 3.3 V

Figure 24. Hot short event when ON

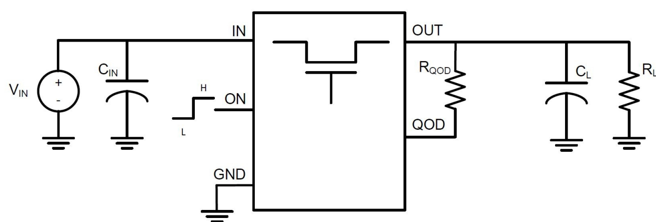


V_{IN} = 3.3 V

Figure 25. Hot short event when ON and recovery

7 Parameter Measurement Information

7.1 Test Circuit and Timing Waveforms Diagrams



(1) Rise and fall times of the control signal are 100 ns

(2) Turn-off times and fall times are dependent on the time constant at the load. For the TPS22919 devices, the internal pull-down resistance QOD is enabled when the switch is disabled. The time constant is (R_{QOD} + $R_{PD,QOD}$ || R_L) × C_L.

Figure 26. Test Circuit

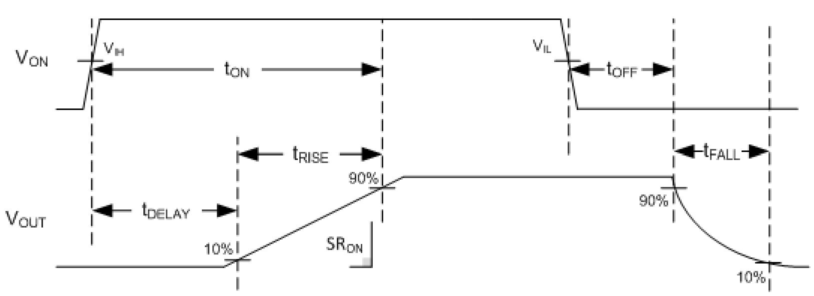


Figure 27. Timing Waveforms

8 Detailed Description

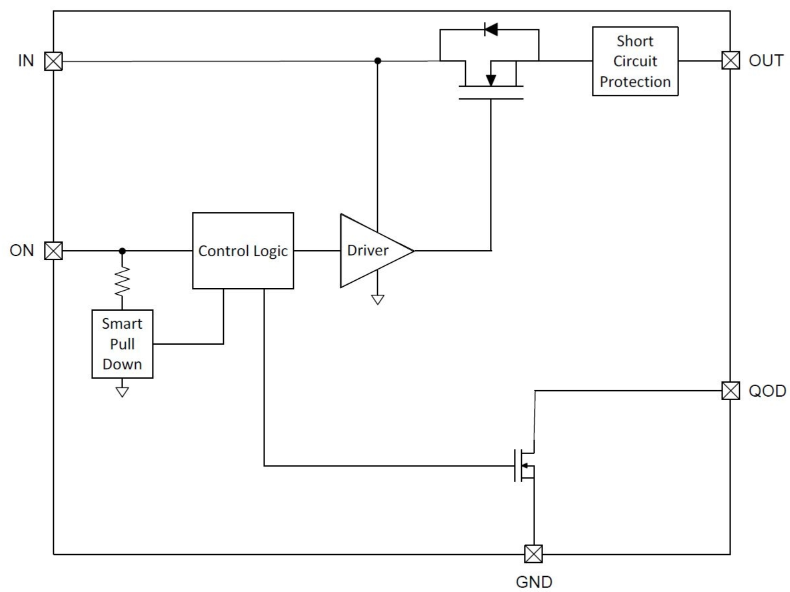
8.1 Overview

The TPS22919 device is a 5.5-V, 1.5-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device.

The TPS22919 device has a slow slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The TPS22919 load switch is also self-protected, meaning that it will protect itself from short circuit events on the output of the device. It also has thermal shutdown to prevent any damage from overheating.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to VIN, a Smart Pull Down is used to keep the ON pin from floating until the system sequencing is complete. Once the ON pin is deliberately driven high ($\geq V_{IH}$), the Smart Pull Down is disconnected to prevent unnecessary power loss. See Table 1 when the ON Pin Smart Pull Down is active.

Table 1. Smart-ON Pull Down

VON	Pull Down
$\leq V_{IL}$	Connected
$\geq V_{IH}$	Disconnected

8.3.2 Output Short Circuit Protection (I_{SC})

The device will limit current to the output in case of output shorts. When a short occurs, the large VIN to VOUT voltage drop causes the switch to limit the output current (I_{SC}) within (t_{SC}). When the output is below the hard short threshold (V_{SC}), a lower limit is used to minimize the power dissipation while the fault is present. The device will continue to limit the current until it reaches its thermal shutdown temperature. At this time, the device will turn off until its temperature has lowered by the thermal hysteresis (35°C typical) before turning on again.

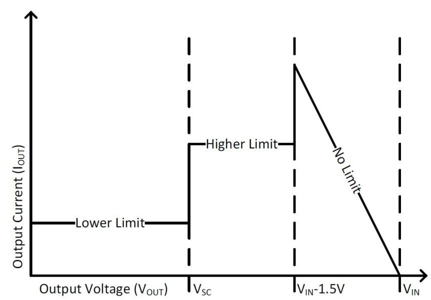


Figure 28. Output Short Circuit Current Limit

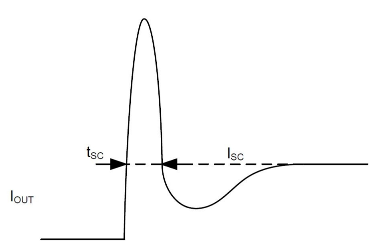


Figure 29. Output Short Circuit Response

8.3.3 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22919 device includes a QOD pin that can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance QOD ($R_{PD,QOD}$).
- QOD pin connected to VOUT pin using an external resistor R_{QOD}. After the switch becomes disabled, the discharge rate is controlled by the value of the total discharge resistance. To adjust the total discharge resistance, Equation 1 can be used:

  $$R_{DIS} = R_{PD,QOD} + R_{QOD}$$

  Where:

  - R_{DIS} = Total output discharge resistance (Ω)

  - $R_{PD,QOD}$ = Internal pulldown resistance (Ω)
  - R_{QOD} = External resistance placed between the VOUT and QOD pins (Ω) (1)
- QOD pin is unused and left floating. Using this method, there will be no quick output discharge functionality, and the output will remain floating after the switch is disabled.

The fall times of the device depend on many factors including the total discharge resistance (R_{DIS}) and the output capacitance (C_L). To calculate the approximate fall time of V_{OUT} use Equation 2.

$$t_{FALL} = 2.2 \times (R_{DIS} \parallel R_L) \times C_L$$

Where:

- t_{FALL} = Output Fall Time from 90% to 10% (µs)
- R_{DIS} = Total QOD + R_{QOD} Resistance (Ω)
- R_L = Output Load Resistance (Ω)
- C_L = Output Load Capacitance (µF) (2)

8.3.3.1 QOD When System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN}. Past a certain V_{IN} level, the strength of the R_{PD} will be reduced. If there is still remaining charge on the output capacitor, this will result in longer fall times. For further information regarding this condition, see the *Setting Fall Time for Shutdown Power Sequencing* section.

8.4 Device Functional Modes

Table 2 describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

Table 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22919 VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND ($R_{PD, QOD}$ + R_{QOD})
L	QOD pin tied to VOUT directly	GND ($R_{PD, QOD}$)
L	QOD pin left open	Floating
H	N/A	VIN

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22919 devices can be used to power downstream modules.

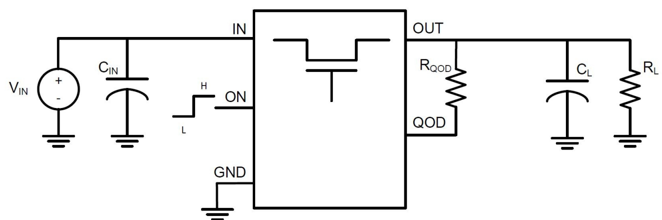


Figure 30. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in Table 3 as the design parameters:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	3.6 V
Load Current / Resistance (R_L)	1 kΩ
Load Capacitance (C_L)	47 µF
Minimum Fall Time (t_F)	40 ms
Maximum Inrush Current (I_{RUSH})	150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use Equation 3 to find the maximum slew rate value to limit inrush current for a given capacitance:

$$(\text{Slew Rate}) = I_{RUSH} \div C_L$$

where

- I_{INRUSH} = maximum acceptable inrush current (mA)
- C_L = capacitance on VOUT (µF)
- Slew Rate = Output Slew Rate during turn on (mV/µs) (3)

Based on Equation 3, the required slew rate to limit the inrush current to 150 mA is 3.2 mV/µs. The TPS22919 has a slew rate of 2.3 mV/µs, so the inrush current will be below 150 mA.

9.2.2.2 Setting Fall Time for Shutdown Power Sequencing

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS22919 device, adding a load switch to each power rail can be used to manage the power down sequencing. To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down.

Once the required fall time is determined, the maximum external discharge resistance (R_{DIS}) value can be found using Equation 2:

$$t_{FALL} = 2.2 \times (R_{DIS} \parallel R_L) \times C_L \quad (4)$$

$$R_{DIS} = 630\ \Omega \quad (5)$$

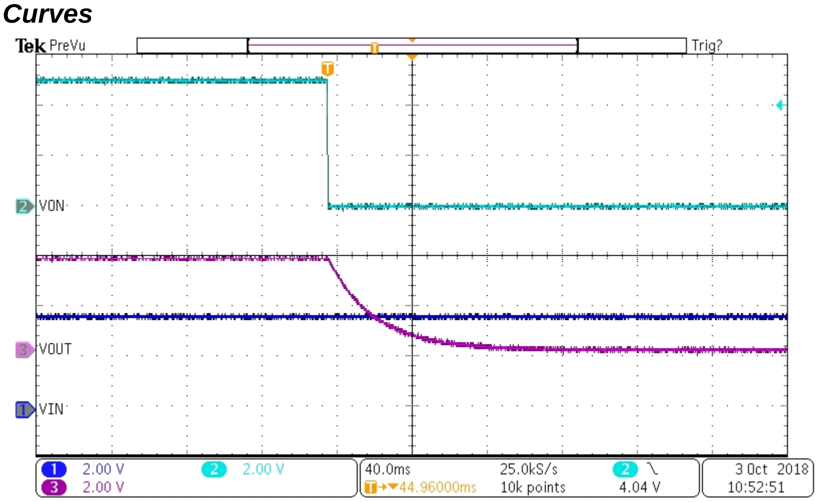
Equation 1 can then be used to calculate the R_{QOD} resistance needed to achieve a particular discharge value:

$$R_{DIS} = QOD + R_{QOD} \quad (6)$$

$$R_{QOD} = 600\ \Omega \quad (7)$$

To ensure a fall time greater than, choose an R_{QOD} value greater than 600 Ω.

9.2.2.3 Application Curves



A.

C_L = 47µF

Figure 31. Fall Time (R_{QOD} = 1 kΩ)

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

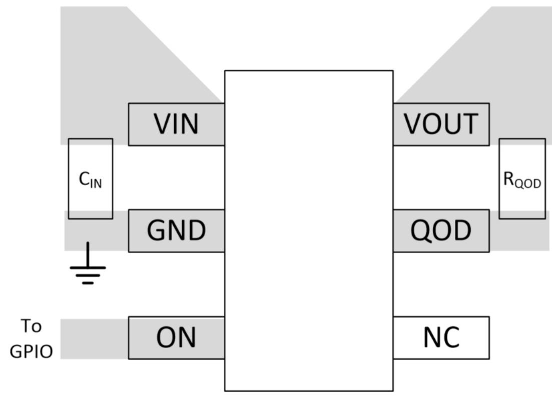


Figure 32. Recommended Board Layout

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 8:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \tag{8}$$

where

- $P_{D(MAX)}$ = maximum allowable power dissipation
- $T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the TPS22919 devices)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. Refer to the Thermal Parameters table. This parameter is highly dependent upon board layout. (8)

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS22919DCKR	OBSOLETE	SC70	DCK	6		TBD	Call TI	Call TI			
TPS22919DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	1CS	Samples
TPS22919DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	1CS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

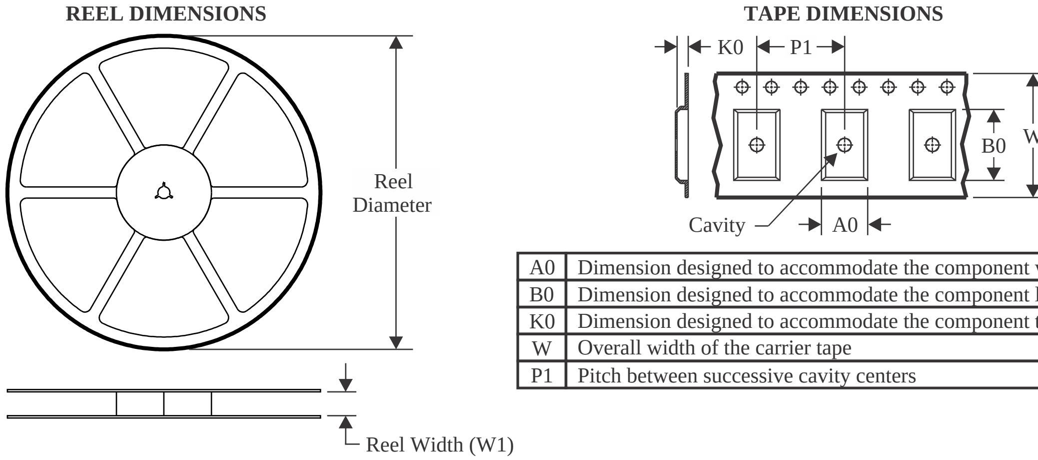
OTHER QUALIFIED VERSIONS OF TPS22919 :

- Automotive : TPS22919-Q1

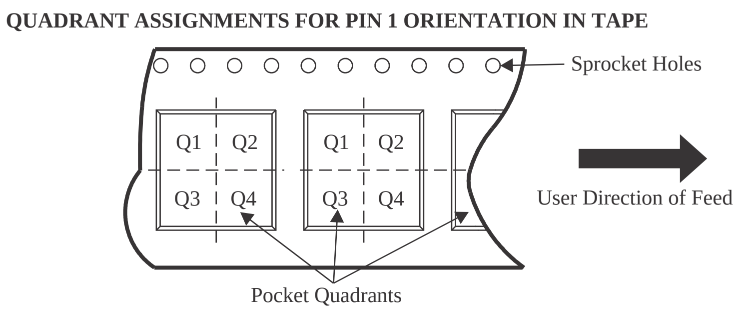
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



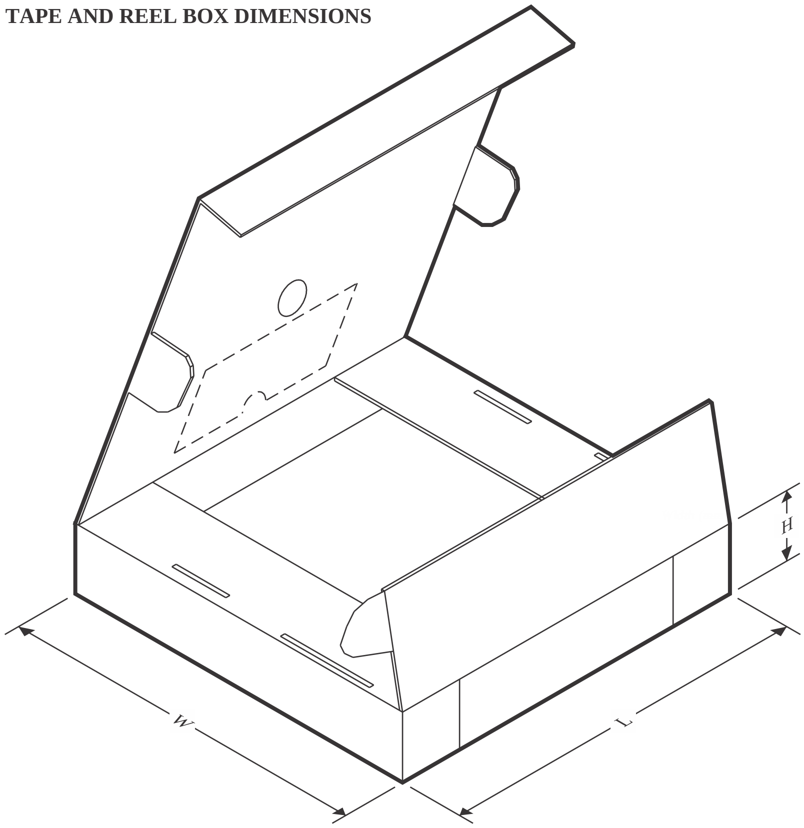
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

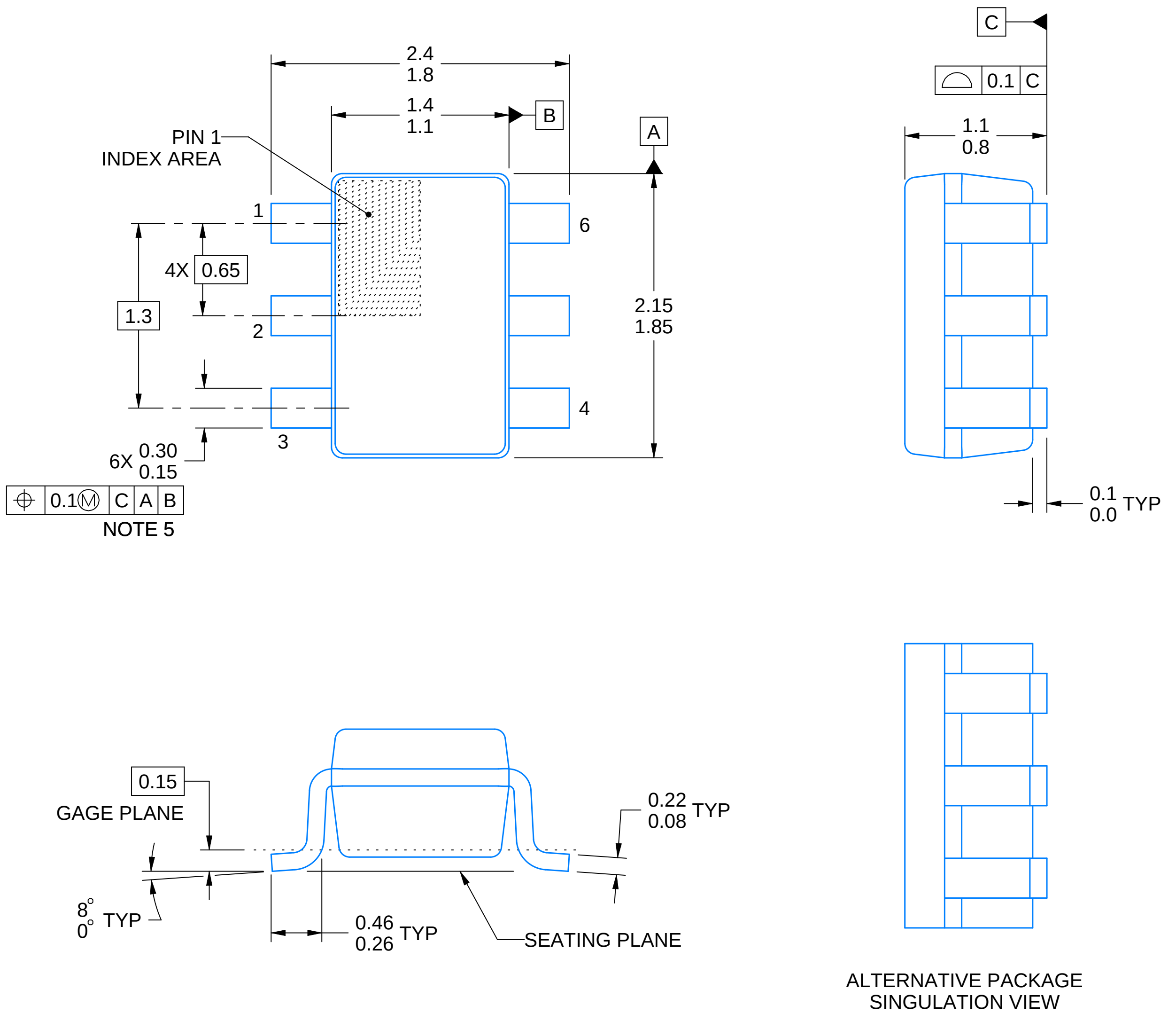
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22919DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TPS22919DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

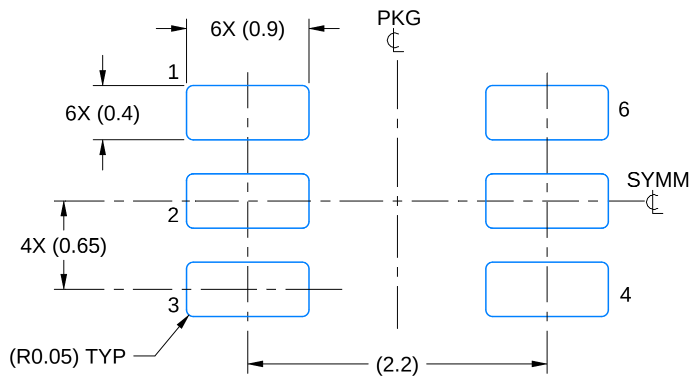
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22919DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
TPS22919DCKT	SC70	DCK	6	250	210.0	185.0	35.0



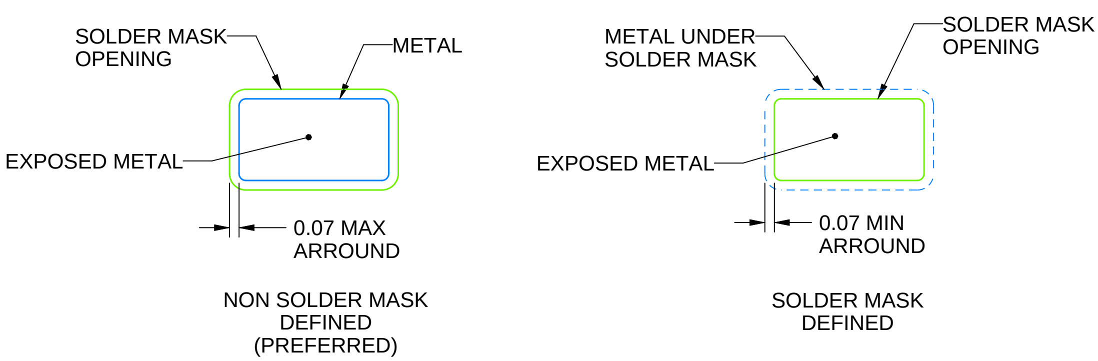
4214835/B 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

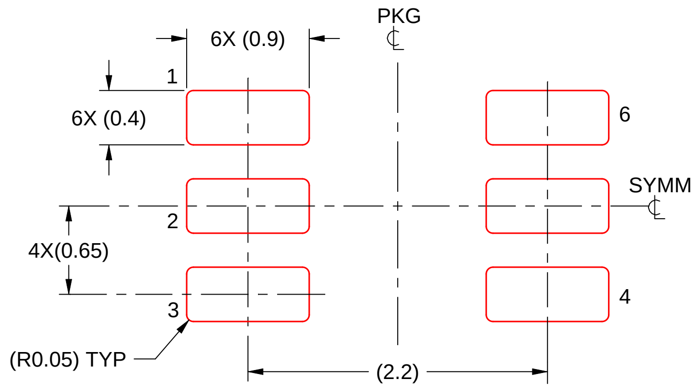


SOLDER MASK DETAILS

4214835/B 04/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/B 04/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.