–48-V Hot Swap Power Manager

Check for Samples: TPS2394

FEATURES

- **Operating Supply Range of –12 V to –80 V**
- **Withstands Transients to –100 V**
- **Programmable Current Limit**
- **Programmable Linear Inrush Slew Rate**
- **Programmable UV/OV Thresholds**
- **Programmable UV and OV Hysteresis**
- **Fault Timer to Eliminate Nuisance Trips**
- **Power Good and Fault Outputs**
- **14-Pin TSSOP Package**

APPLICATIONS

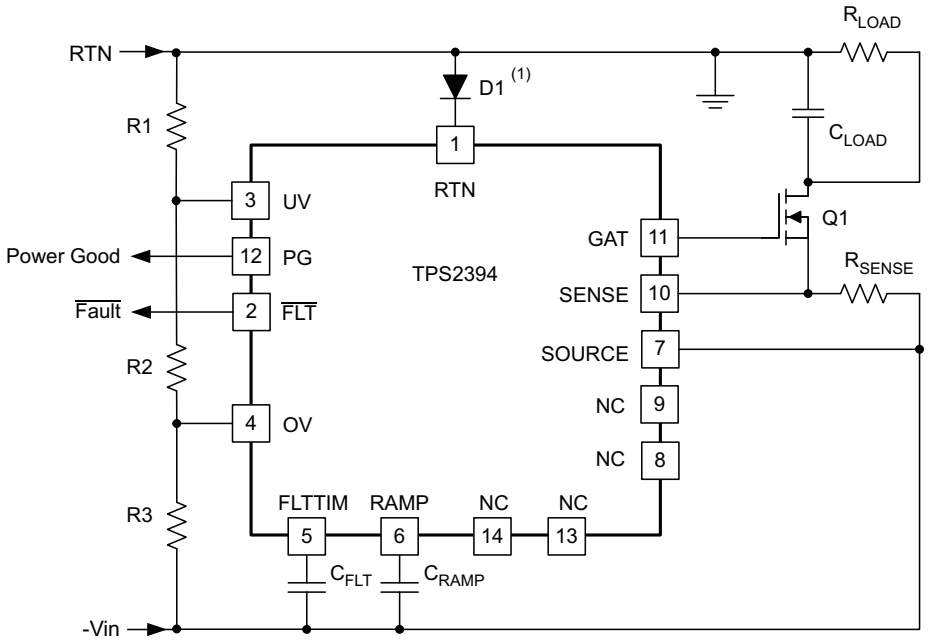
- **–48-V Distributed Power Systems**
- **Central Office Switching**
- **ATCA Systems**
- **Base Stations**

DESCRIPTION

The TPS2394 is a hot swap power manager which can provide inrush limit, over current protection, short circuit protection. The TPS2394 operates with supply voltages from −12 V to −80 V, and withstands input transient to −100 V.

The TPS2394 uses a power FET to provide load current slew rate control and peak current limiting that is programmed by one resistor and one capacitor. The device also provides a power good output to enable down-stream power converters and a fault output to indicate load problems.

TYPICAL APPLICATION DIAGRAM



(1) D1 optional per application requirements.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)(2)

PARAMETERS		VALUE	UNIT
Input voltage range	RTN	–0.3 to 100	V
	FLTTIM, RAMP, SENSE, OV, UV	–0.3 to 15	
Output voltage range	$\overline{FLT}$, PG (3)	–0.3 to 100	
Continuous output current	$\overline{FLT}$, PG	10	mA
Operating junction temperature range, T_J		–55 to 125	°C
ESD - Human body model (HBM)		2	kV
ESD - Charged device model (CDM)		1.5	

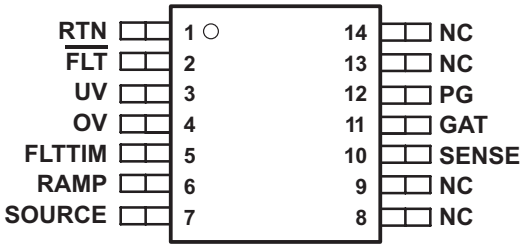
(1) All voltages are with respect to SOURCE (unless otherwise noted).
(2) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) With 10 kΩ minimum series resistance. Range limited to –0.3V to 80V from low impedance source.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input supply, SOURCE to RTN	–80	–48	–12	V
Operating junction temperature range	–40		85	°C

TSSOP-14 PACKAGE
(TOP VIEW)



PRODUCT INFORMATIONS(1)

T_A	PACKAGE	PART NUMBER
−40°C to 85°C	TSSOP-14	TPS2394PW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at wwww.ti.com.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS2394 PW (14 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	120.8	°C/W
θ_{JB}	Junction-to-board thermal resistance	62.8	
ψ_{JT}	Junction-to-top characterization parameter	1	
ψ_{JB}	Junction-to-board characterization parameter	56.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

SOURCE = -48 V, UV = 2.5 V, OV = 0.5 V, SENSE = 0 V, RAMP = 0 V, T_A = −40°C to 85°C (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
I_{CC1}	Supply current	SOURCE = -48 V		1000	1500	µA
I_{CC2}	Supply current	SOURCE = -80 V			2000	
V_{UVLO_I}	Internal UVLO threshold voltage	To GAT pull up	–11.8	–10	–8	V
V_{HYST}	Internal UVLO hysteresis voltage		50	240	500	mV
OVERVOLTAGE AND UNDERVOLTAGE INPUTS (OV AND UV)						
V_{THUV}	UV threshold voltage, UV rising, to SOURCE	To GAT pull up, 25°C	1.391	1.400	1.409	V
		To GAT pull up, 0 to 70°C	1.387	1.400	1.413	
		To GAT pull up, –40 to 85°C	1.384	1.400	1.419	
I_{HYSUV}	UV hysteresis	UV = −45.5 V	–11	–10	–9	µA
I_{ILUV}	UV low−level input current	UV = −47 V	–1		1	
V_{THOV}	OV threshold voltage, OV rising, to SOURCE	To GAT pull up	1.376	1.400	1.426	V
I_{HYSOV}	OV hysteresis	OV = −45.5 V	–11.1	–10	–8.6	µA
I_{ILOV}	OV low−level input current	OV = −47 V	–1		1	
LINEAR CURENT AMPLIFIER (LCA)						
V_{OH}	High level output, GAT−SOURCE	SENSE = SOURCE	11	14	17	V
I_{SINK_f}	GAT sink current in fault	SENSE – SOURCE = 80 mV, GAT = –43 V, FLTTIME = 5 V	30	75		mA
I_{SINK_I}	GAT sink current in linear mode	SENSE – SOURCE = 80 mV, GAT = –43 V, FLTTIME = 2 V		5	10	
I_{IN}	SENSE input current	0 V < SENSE – SOURCE < 0.2 V	–1		1	µA
V_{REF_K}	Reference clamp voltage, SENSE – SOURCE	RAMP – SOURCE = 6 V	34	42	50	mV
V_{IO}	Input offset voltage, SENSE – SOURCE	RAMP – SOURCE = 0 V	–7		9	

(1) All voltages are with respect to RTN unless otherwise stated.
(2) Currents are positive into and negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS (continued)

SOURCE = -48 V, UV = 2.5 V, OV = 0.5 V, SENSE = 0 V, RAMP = 0 V, T_A = −40°C to 85°C (unless otherwise noted)[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RAMP GENERATOR						
I_{SRC1}	RAMP source current, slow turn-on rate	RAMP – SOURCE = 0.25 V	–800	–550	–300	nA
I_{SRC2}	RAMP source current, normal rate	RAMP – SOURCE = 1 V and 3 V	–11.3	–10	–8.5	µA
V_{OL}	Low-level output voltage	UV = SOURCE			5	mV
A_V	Voltage gain, relative to SENSE	0 V < RAMP – SOURCE < 5 V	9.5	10	10.7	mV/V
OVERLOAD COMPARATOR						
V_{TH_OL}	SENSE current overload threshold		100	120	140	mV
t_{RSP}	Response time	SENSE – SOURCE = 200 mV	2	4	7	µs
FAULT TIMER						
V_{OL}	FLTTIM low−level output voltage, to SOURCE	UV = –48 V			5	mV
I_{CHG}	FLTTIM charging current, current limit mode	FLTTIM – SOURCE = 2 V	–54	–50	–41	µA
V_{FLT}	FLTTIM fault threshold voltage to SOURCE		3.75	4.00	4.25	V
V_{RST}	Fault reset threshold to SOURCE			0.5		
I_{DSG}	FLTTIM Discharge current, retry mode	FLTTIM – SOURCE = 2 V		0.38	0.75	µA
D	Output duty cycle during retry cycles	SENSE − SOURCE = 80 mV, FLTTIM – SOURCE = 2 V		1%	1.5%	
I_{RST}	FLTTIM discharge current, timer reset mode	FLTTIM – SOURCE = 2 V, SENSE = V		1		mA
LOGIC OUTPUTS ($\overline{FLT}$, PG)						
I_{OHFLT}	$\overline{FLT}$ high-level output leakage current	UV = –48 V, $\overline{FLT}$ – SOURCE = 80 V	–10		10	µA
I_{OHPG}	PG high-level output leakage current	UV = –45 V, PG – SOURCE = 80 V	–10		10	
$R_{DS(on)}$	$\overline{FLT}$ ON resistance	SENSE–SOURCE = 80 mV, FLTTIM–SOURCE = 5 V, $I_{(\overline{FLT})}$ = 1 mA		50	80	Ω
	PG ON resistance	UV = –48 V, I_O(PG) = 1 mA		50	80	Ω

DEVICE INFORMATION

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{FLT}$	2	O	Open-drain, active-low indication that the part is in fault.
FLTTIM	5	I/O	Connection for user programming of the fault timeout period.
GAT	11	O	Gate drive for external N-channel MOSFET that ramps load current and disconnects in the event of a fault.
NC	9		Not connected, leave floating
NC	8		Not connected, leave floating
NC	14		Not connected, leave floating
NC	13		Not connected, leave floating
OV	4	I	Over voltage sense input.
PG	12	O	Open-drain, active-high indication that the power MOSFET is fully enhanced.
RAMP	6	I/O	Programming input for setting the inrush current slew rate.
RTN	1	I	Supply return (for positive grounded system).
SENSE	10	I	Positive current sense input.
SOURCE	7	I/O	Negative current sense input.
UV	3	I	Under voltage sense input.

PIN DESCRIPTIONS

$\overline{FLT}$: Open-drain, active-low indication that TPS2394 has shut down due to a faulted load. This happens if the load current stays limited by the linear current amplifier (LCA) for more than the fault time (time to charge the FLTTIM capacitor). $\overline{FLT}$ is cleared when input supply drops below the UV-comparator threshold or exceeds the OV-comparator threshold. The $\overline{FLT}$ output is pulled to SOURCE. The $\overline{FLT}$ output is able to sink 10 mA when in fault, withstand 80 V without leakage when not faulted, and withstand transients as high as 100 V when limited by a series resistor of at least 10 kΩ.

FLTTIM: Connection for user programming of the fault timeout period. An external capacitor connected from FLTTIM to SOURCE establishes the timeout period to declare a fault condition. This timeout protects against indefinite current sourcing into a faulted load, and also provides a filter against nuisance trips from momentary current spikes or surges. TPS2394 defines a fault condition as voltage at the SENSE pin at or greater than the 42-mV fault threshold. When a fault condition exists, the timer is active. The devices manage fault timing by charging the external capacitor to the 4-V fault threshold, then subsequently discharging it at approximately 1% the charge rate to establish the duty cycle for retrying the load. Whenever the fault latch is set (timer expired), GAT and $\overline{FLT}$ are pulled low.

GAT: Gate drive for an external N-channel protection power MOSFET. When input supply is above the UV threshold and below the OV threshold, gate drive is enabled and the device begins charging the external capacitor connected to RAMP. RAMP develops the reference voltage at the non-inverting input of the internal LCA. The inverting input is connected to the current sense node, SENSE. The LCA acts to slew the pass MOSFET gate to force the SENSE voltage to track the reference. The reference is internally clamped to 42 mV, so the maximum current that can be sourced to the load is determined by the sense resistor value as $I_{MAX} \leq 42\ mV/R_{SENSE}$. Once the load voltage has ramped up to the input dc potential and current demand drops off, the LCA drives GAT 14 V above SOURCE to fully enhance the pass MOSFET, completing the low-impedance supply return path for the load.

PG: Open-drain, active-high indication that load current is below the current limit and the power MOSFET is fully enhanced. When commanded load current is more than the actual load current, the linear current amplifier (LCA) will raise the power MOSFET gate voltage to fully enhance the power MOSFET. At this time, the PG output will go high. This output can be used to enable a down-stream dc-to-dc converter. The PG output is pulled to SOURCE and is able to sink 10 mA when in fault, withstand 80 V without leakage when power is not good, and withstand transients as high as 100 V when limited by a series resistor of at least 10 kΩ.

OV: Over voltage comparator input. This input is typically connected to a voltage divider between RTN and SOURCE to sense the magnitude of the input supply. If OV is less than 1.4 V above SOURCE, and UV is more than 1.4 V above SOURCE, and there is no fault, the linear current amp will be enabled. In the event of a fault, pulling OV high or UV low will reset the fault latch and allow the IC to restart. OV can also be used as an active-low logic enable input. The over-voltage comparator hysteresis is programmed by the equivalent resistance seen looking into the divider at the OV input.

RAMP: Programming input for setting inrush current and current slew rate. An external capacitor connected between RAMP and SOURCE establishes turn-on current slew rate. During turn-on, TPS2394 charges this capacitor to establish the reference input to the LCA at 1% of the voltage from RAMP to SOURCE. The closed-loop control of the LCA and the pass MOSFET maintains the V(SENSE - SOURCE) at the reference potential, so the load current slew rate is directly set by the voltage ramp rate at the RAMP pin. When fully charged, RAMP can exceed SOURCE by 6 V, but the reference is internally clamped to 42 mV, limiting load current to 42 mV/R_{SENSE}. When the output is disabled via OV, UV, or due to a load fault, the RAMP capacitor is discharged and held low to initialize for the next turn on.

The TPS2394 initiates ramp capacitor charging, and consequently load current slewing, at a reduced rate. This reduced rate applies until the voltage on the RAMP pin is about 0.5 V. The maximum di/dt rate, as set by Equation 2, is effective once the device switches to a 10-mA charging source.

RTN: Positive supply input. For negative voltage systems, this pin connects directly to the return node of the input power bus.

SENSE: Current sense input. An external low-value resistor connected between SENSE and SOURCE is used to monitor current magnitude. There are two internal device thresholds associated with the voltage at the SENSE pin. During ramp-up of the load capacitance or during other periods of excessive demand, the linear current amp (LCA) will regulate this voltage to 42 mV. Whenever the LCA is in current regulation mode, the FLTTIM capacitor charges. If the LCA output is at its maximum, GAT is pulled 14 V above SOURCE. At this time, a fast fault such as a short circuit can cause the SENSE voltage to rapidly exceed 120 mV (the overload threshold). In this case, the GAT pin is pulled low rapidly, bypassing the fault timer.

SOURCE: Connection to the input supply negative rail.

UV: Under Voltage Comparator input. This input is typically connected to a voltage divider between RTN and SOURCE to sense the magnitude of the input supply. If UV is more than 1.4 V above SOURCE, OV is less than 1.4 V above SOURCE, and there is no fault, the LCA will be enabled. In the event of a fault, pulling UV low or OV high will reset the fault latch and allow restarting. UV can also be used as an active high logic enable input. The under-voltage comparator hysteresis is programmed by the equivalent resistance seen looking into the divider at the UV input.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs AMBIENT TEMPERATURE

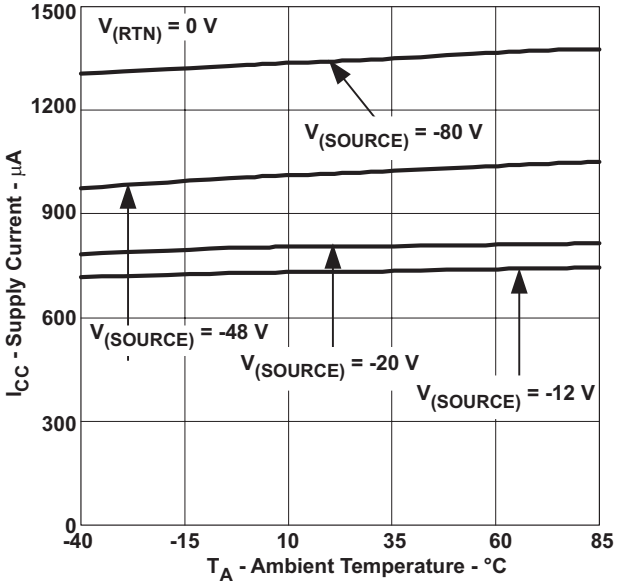


Figure 1.

UNDERVOLTAGE PULL-UP CURRENT vs AMBIENT TEMPERATURE

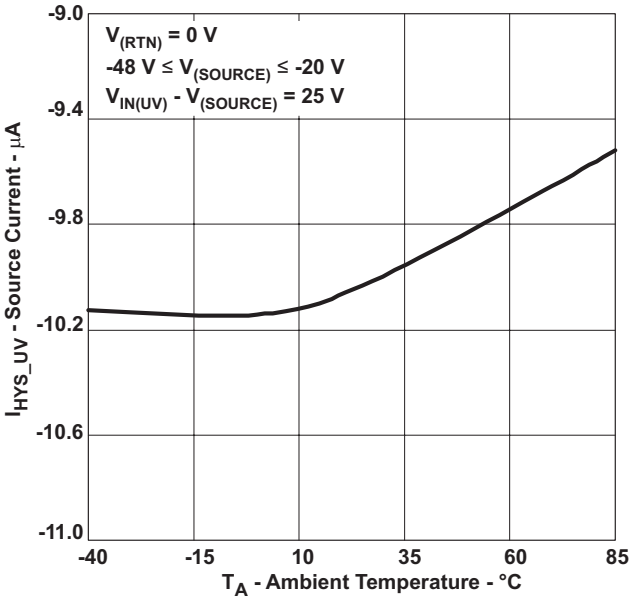


Figure 2.

GAT HIGH-LEVEL OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

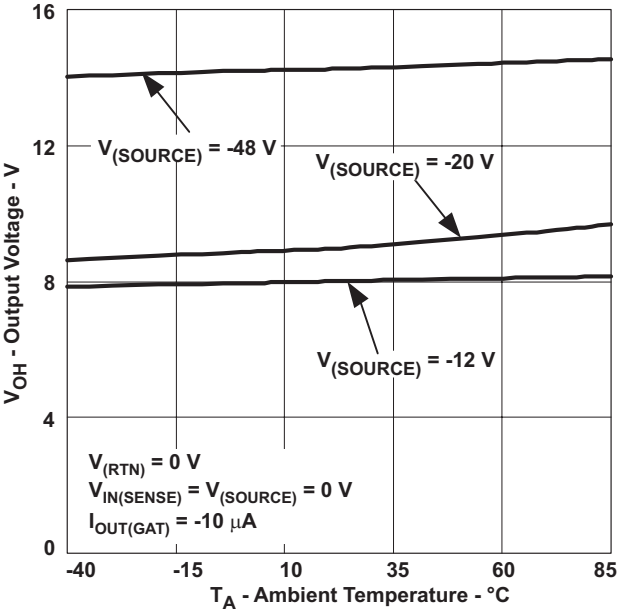


Figure 3.

RAMP OUTPUT CURRENT vs AMBIENT TEMPERATURE, REDUCED RATE MODE

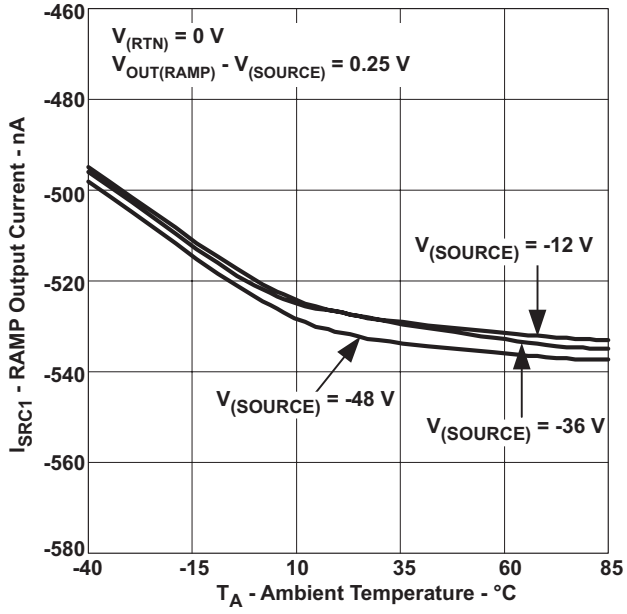


Figure 4.

TYPICAL CHARACTERISTICS (continued)

RAMP OUTPUT CURRENT vs AMBIENT TEMPERATURE, NORMAL RATE MODE

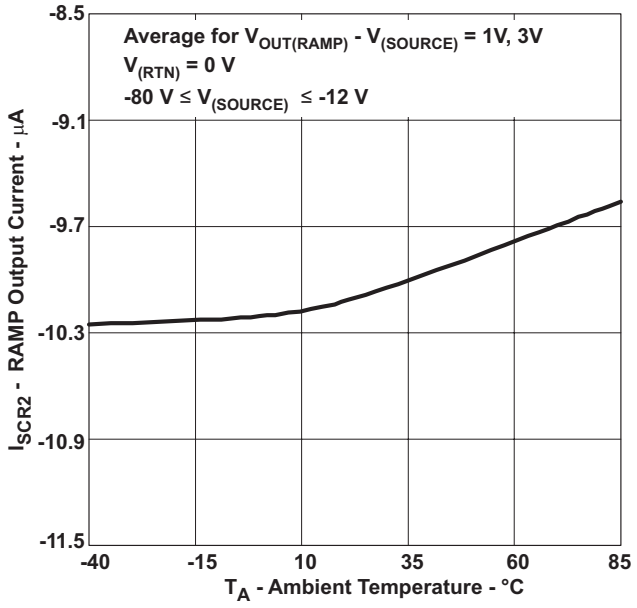


Figure 5.

TIMER CHARGING CURRENT vs AMBIENT TEMPERATURE

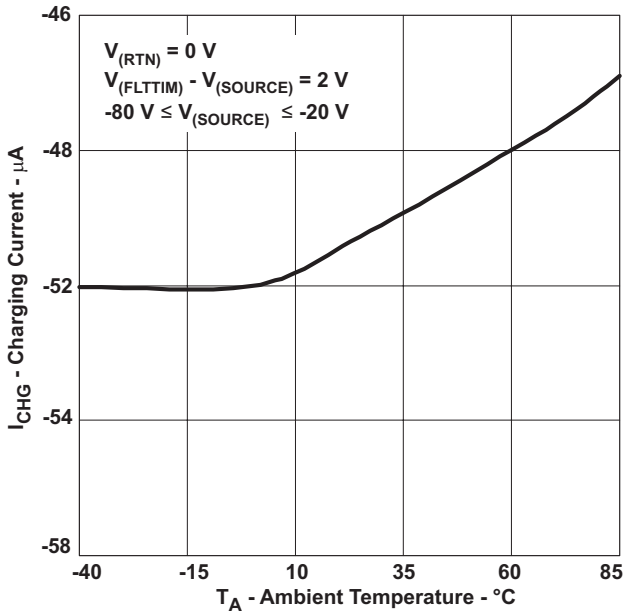


Figure 6.

TIMER DISCHARGE CURRENT vs AMBIENT TEMPERATURE

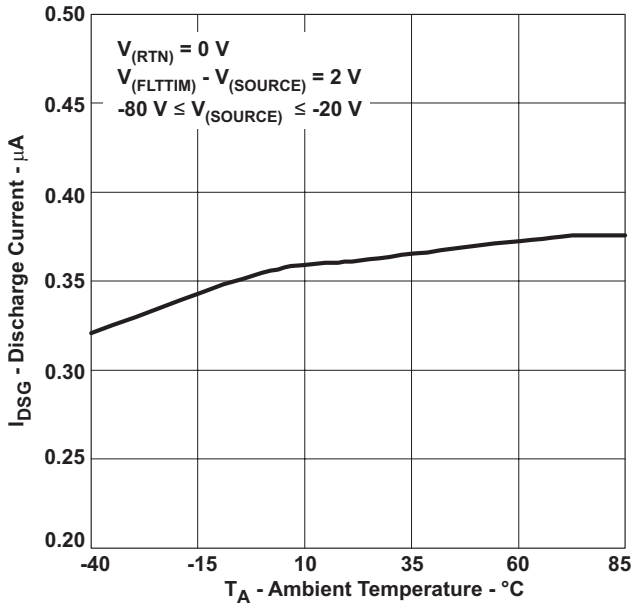


Figure 7.

FAULT LATCH THRESHOLD VOLTAGE vs AMBIENT TEMPERATURE

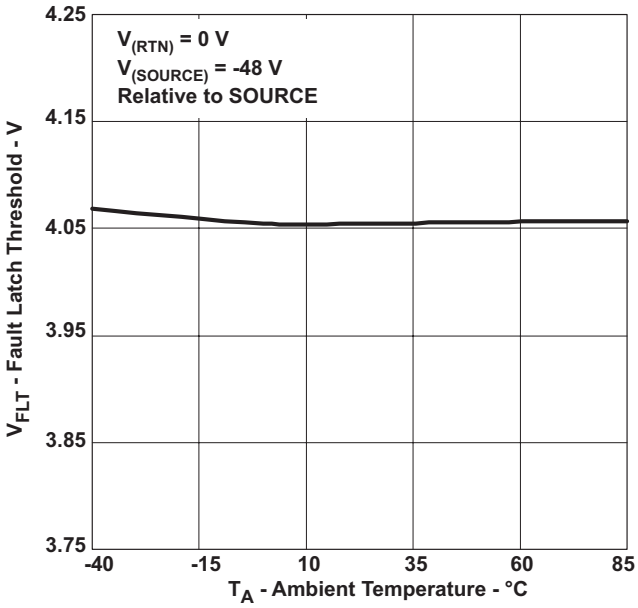
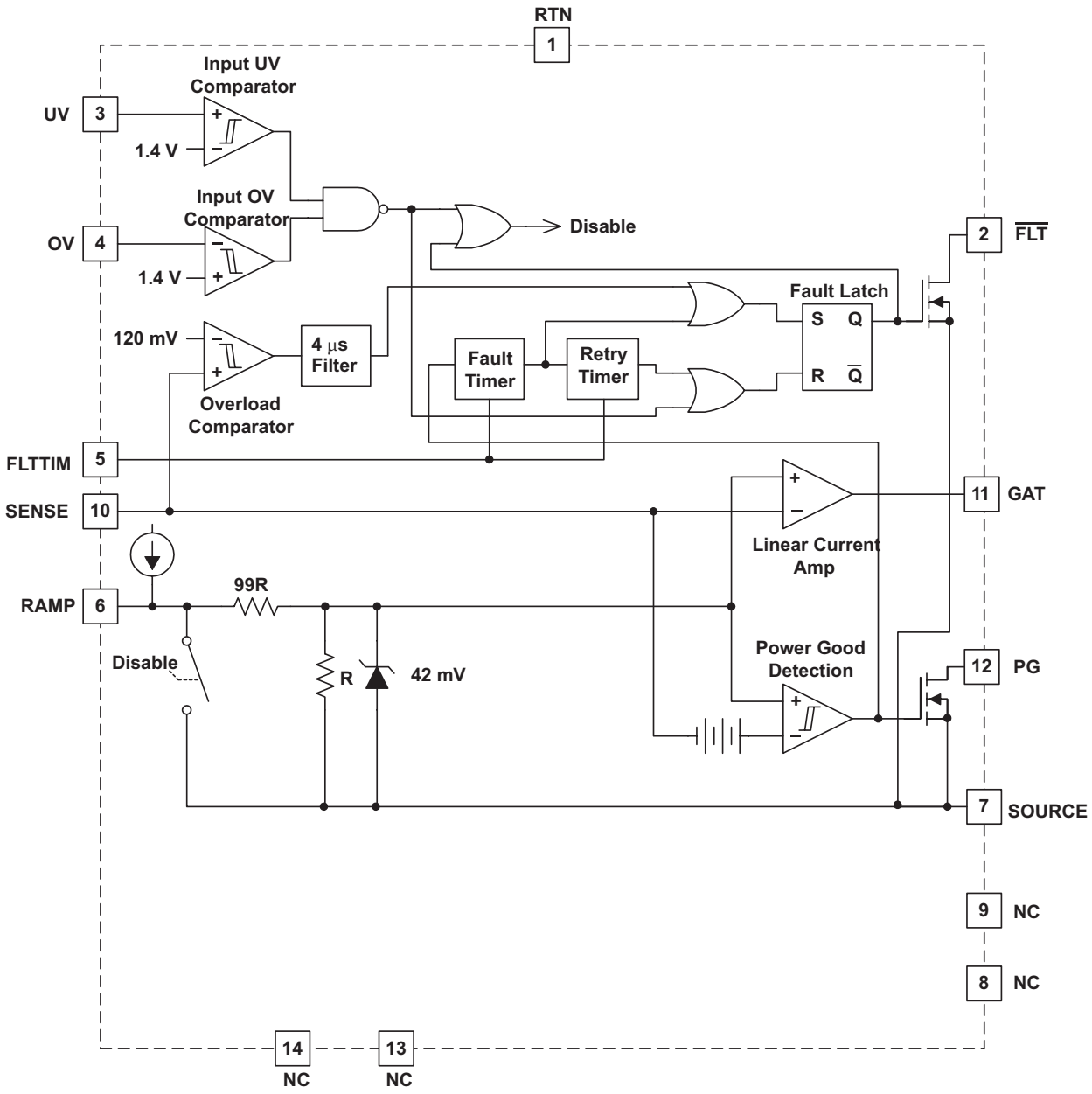


Figure 8.

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

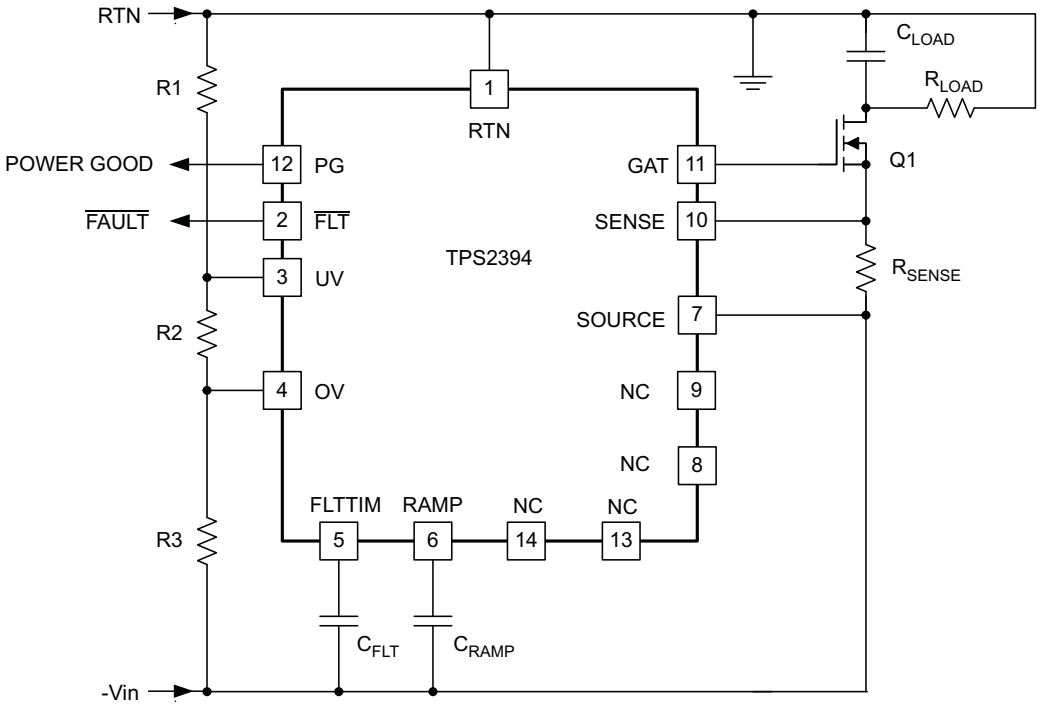


Figure 9. Typical Application

APPLICATION INFORMATION

Setting the Sense Resistor Value

Due to the current-limiting action of the internal LCA, the maximum allowable load current for an implementation is easily programmed by selecting the appropriate sense resistor value. The LCA acts to limit the sense voltage V(SENSE-SOURCE) to its internal reference. Once the voltage at the RAMP pin exceeds approximately 4 V, this limit is the clamp voltage, V_{REF_K}. Therefore; a maximum sense resistor value can be determined from Equation 1.

$$R_{SENSE} \leq \frac{34\ mV}{I_{IMAX}} \quad (1)$$

Where:

R_{SENSE} is the sensing resistor value

I_{IMAX} is the minimum desired current limit

When setting the sense resistor value, it is important to consider two factors, the minimum current limit that may be imposed by the TPS2394, and the maximum load under normal operation of the module. For the first factor, the specification minimum clamp value is used, as seen in Equation 1. Second factor is to ensure the peak operating load current is less than I_{IMAX}. One example of this is a switching converter which draws higher input current, for a given power output, when the output is at the low end of its voltage range. To avoid current limit operation under normal loading, some margin should be designed in between this maximum anticipated load and the minimum current limit level, or $I_{IMAX} > I_{LOAD(max)}$, for Equation 1.

For example, using a 10-mΩ sense resistor for a nominal 2-A load application provides a minimum of 1.4 A of overhead for load variance/margin. Typical bulk capacitor charging current during turn-on is 4.2 A (42 mV/10 mΩ).

Setting the Inrush Slew Rate

The TPS2394 device enables user-programming of the maximum current slew rate during load start-up events. A capacitor tied to the RAMP pin (C_{RAMP} in the typical application diagram) controls the di/dt rate. Once the sense resistor value has been established, a value for C_{RAMP}, in microfarads, can be determined from Equation 2.

$$C_{RAMP} = \frac{11.3}{100 \times R_{SENSE} \times \left(\frac{di}{dt}\right)_{(max)}} \quad (2)$$

Where:

R_{SENSE} is the sense resistor value in Ω

$(di/dt)_{(max)}$ is the desired maximum slew rate in A/s

For example, if the desired slew rate for the typical application shown is 1500 mA/ms, the calculated value for C_{RAMP} is about 7500 pF. Selecting the next larger standard value of 8200 pF provides some margin for capacitor and sense resistor tolerances.

Setting the Fault Timing Capacitor

The fault timeout period is established by the value of the capacitor connected to the FLTTIM pin, C_{FLT}. The timeout period permits riding out spurious current glitches and surges that may occur during operation of the system, and prevents indefinite sourcing into faulted loads. However, to ensure smooth voltage ramping under all conditions of load capacitance and input supply potential, the minimum timeout should be set to accommodate these system variables. To do this, a rough estimate of the maximum voltage ramp time for a completely discharged plug-in card provides a good basis for setting the minimum timer delay. This section presents a quick procedure for calculating the timing capacitance requirement. However, for proper operation of the TPS2394, there is an absolute minimum value of 0.01-µF for C_{FLT}. This minimum requirement overrides any smaller results of Equation 7 and Equation 8.

Due to the three-phase nature of the load current at turn-on, the load voltage ramp has potentially three distinct phases. This profile depends on the relative values of load capacitance, input DC potential, maximum current limit and other factors. The first two phases are characterized by the two different slopes of the current ramp; the third phase, if required to complete load charging, is the constant-current charging at IMAX. Considering the two current ramp phases to be one period at an average di/dt simplifies calculation of the required timing capacitor.

For the TPS2394, the typical duration of the soft-start period, t_{SS}, is given by Equation 3.

$$t_{SS} = 1260 \times C_{RAMP} \quad (3)$$

Where:

t_{SS} is the soft-start period in ms

C_{RAMP} is given in µF

During this current ramp period, the load voltage magnitude which is attained is estimated by Equation 4.

$$V_{LSS} = \frac{i_{AVG}}{2 \times C_{LOAD} \times C_{RAMP} \times 100 \times R_{SENSE}} \times (t_{SS})^2 \quad (4)$$

Where:

V_{LSS} is the load voltage reached during soft-start

i_{AVG} is 3.18 µA for the TPS2394

C_{LOAD} is the load capacitance in Farads

t_{SS} is the soft-start period in s

The quantity i_{AVG} in Equation 4 is a weighted average of the two charge currents applied to C_{RAMP} during turn-on, considering the typical output values.

If the result of Equation 4 is larger than the maximum input supply value, then the load can be expected to charge completely during the inrush slewing portion of the insertion event. However, if this voltage is less than the maximum supply input, $V_{IN(MAX)}$, the HSPM transitions to the constant-current charging of the load. The remaining amount of time required at I_{MAX} is determined from Equation 5.

$$t_{CC} = \frac{C_{LOAD} \times \left(V_{IN(MAX)} - V_{LSS}\right)}{\frac{V_{REF\_K(MIN)}}{R_{SENSE}}} \quad (5)$$

Where:

t_{CC} is the constant-current voltage ramp time, in seconds

$V_{REF\_K(MIN)}$ is the minimum clamp voltage, 34 mV

With this information, the minimum recommended value timing capacitor C_{FLT} can be determined. The delay time needed will be either a time t_{SS2} or the sum of t_{SS2} and t_{CC}, according to the estimated time to charge the load. The quantity t_{SS2} is the duration of the normal rate current ramp period, and is given by Equation 6.

$$t_{SS2} = 0.35 \times C_{RAMP} \quad (6)$$

Where:

C_{RAMP} is given in µF

Since fault timing is generated by the constant-current charging of C_{FLT}, the capacitor value is determined from either Equation 7 or Equation 8, as appropriate.

$$C_{FLT(MIN)} = \frac{54 \times t_{SS2}}{3.75} \quad (7)$$

$$C_{FLT(MIN)} = \frac{54 \times \left(t_{SS2} + t_{CC}\right)}{3.75} \quad (8)$$

Where:

$C_{FLT(MIN)}$ is the recommended capacitor value, in µ-Farads

t_{SS2} is the result of Equation 6, in seconds

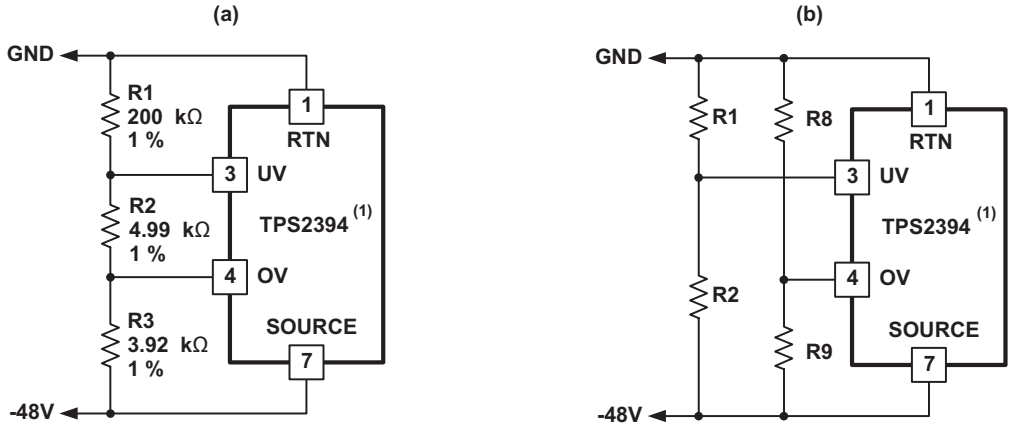
t_{CC} is the result of Equation 5, in seconds

Continuing this calculation example, using a 220-µF input capacitor (C_{LOAD}), Equation 3 and Equation 4 estimate the load voltage ramping to approximately –45 V during the soft-start period. If the module should operate down to –72-V input supply, approximately another 1.4 ms of constant-current charging may be required. Therefore, Equation 6 and Equation 8 are used to determine $C_{FLT(MIN)}$, and the result is approximately 0.039-µF.

Setting the Undervoltage and Overvoltage Thresholds

The UV and OV pins can be used to set the undervoltage (V_{UV}) and overvoltage (V_{OV}) thresholds of the hot swap circuit. When the input supply is below V_{UV} or above V_{OV}, the GAT pin is held low, disconnecting power from the load, and the PG output is deasserted. When input voltage is within the UV/OV window, the GAT pin drive is enabled, assuming all other input conditions are valid for turn-on.

Threshold hysteresis is provided via two internal sources which are switched to either pin whenever the corresponding input level exceeds the internal 1.4-V reference. The additional bias shifts the pin voltage in proportion to the external resistance connected to it. This small voltage shift at the device pin is gained up by the external divider to input supply levels.



$$V_{UV\_L} = \frac{R1 + R2 + R3}{R2 \quad R3} \times V_{THUV}$$

$$V_{OV\_L} = \frac{R1 + R2 + R3}{R3} \times V_{THOV} \quad -I_{HYSUV} \times R1$$

$$V_{UV\_L} = \frac{R1 + R2}{R2} \times V_{THUV}$$

$$V_{OV\_L} = \frac{R8 + R9}{R9} \times V_{THOV}$$

Note (1): Additional details omitted for clarity.

Figure 10. Programming the Undervoltage and Overvoltage Thresholds

The UV and OV thresholds can be individually programmed with a three-resistor divider connected to the TPS2394 as shown in the typical application diagram, and again in Figure 10a. When the desired trip voltages and undervoltage hysteresis have been established for the protected board, the resistor values needed can be determined from the following equations. First, select the top leg of the divider (R1 in the diagram) to obtain the threshold hysteresis. This value is calculated using Equation 9.

$$R1 = \frac{V_{HYS\_UV}}{10\ \mu A} \tag{9}$$

Where:

V_{HYS_UV} is the undervoltage hysteresis value

For example, assume the typical application design targets have been set to undervoltage turn-on at 33 V (input supply rising), turn-off at 31 V (input voltage falling), and overvoltage shutdown at 72 V. Then Equation 9 yields R1 = 200 kΩ for the 2-V hysteresis. Once the value of R1 is selected, it is used to calculate resistors R2 and R3.

$$R2 = \frac{1.4 \times R1}{\left(V_{UV\_L} - 1.4\right)} \times \left[1 - \frac{V_{UV\_L}}{\left(V_{OV\_L} + 10^{-5} \times R1\right)}\right] \tag{10}$$

$$R3 = \frac{1.4 \times R1 \times V_{UV\_L}}{\left(V_{UV\_L} - 1.4\right) \times \left(V_{OV\_L} + 10^{-5} \times R1\right)} \quad (11)$$

Where:

V_{UV_L} is the UVLO threshold when the input supply is low; i.e., less than V_{UV}, and

V_{OV_L} is the OVLO threshold when the input supply is low; i.e., less than V_{OV}

Referring to Figure 10a, Equation 10 and Equation 11 produce R2 = 4.909 kW (4.99 kΩ selected) and R3 = 3.951 kΩ (3.92 kΩ selected), as shown. For the selected values, the expected nominal supply thresholds are V_{UV_L} = 32.8 V, V_{UV_H} = 30.8 V, and V_{OV_L} = 72.6 V. The hysteresis of the overvoltage threshold, as seen at the supply inputs, is given by the quantity (10 µA) × (R1 + R2). For the majority of applications, this value is almost the same as the UV hysteresis, since typically R1 >> R2.

If more independent control is needed for the OVLO hysteresis, there are several options. One option is to use separate dividers for both the UV and OV pins, as shown in Figure 10b. In this case, once R1 and R8 have been selected for the required hysteresis per Equation 9, and values for the bottom resistors in the divider (R2 and R9 in Figure 10b) can be calculated using Equation 12.

$$R_{XVLO} = \frac{V_{REF}}{\left(V_{XV\_L} - V_{REF}\right)} \times R_{(TOP)} \quad (12)$$

Where:

R_{XVLO} is R2 or R9

$R_{(TOP)}$ is R1 or R8 as appropriate for the threshold being set

V_{XV_L} is the under (V_{UV_L}) or overvoltage (V_{OV_L}) threshold at the supply input, and

V_{REF} is either V_{THUV} or V_{THOV} from the specification table, as required for the resistor being calculated.

Reverse Voltage Protection

In some applications, it may be necessary to protect the TPS2394 against reverse polarity supply connections or input transients. If the potential at SOURCE pin rises above that of the RTN pin, device damage may result. If the application environment is such that these conditions are anticipated, a small-signal diode should be inserted between the supply return bus and the TPS2394 RTN pin, as shown in the Typical Application diagram. A 75-V to 100-V rated device (VRRM), such as MMBD4148 or BAV19, is recommended.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2394PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2394	Samples
TPS2394PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2394	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

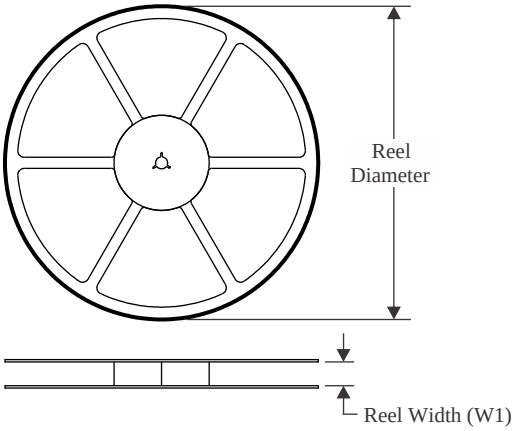
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

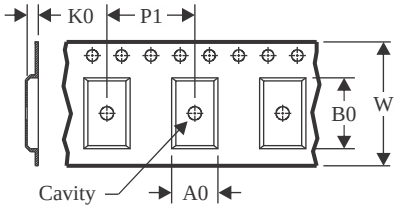
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

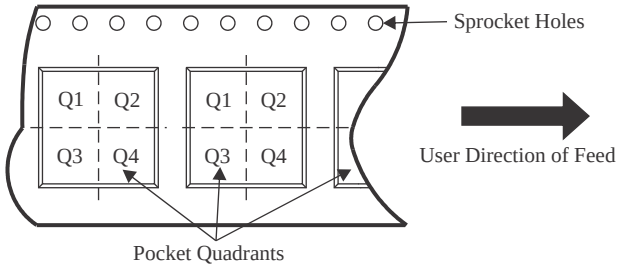


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

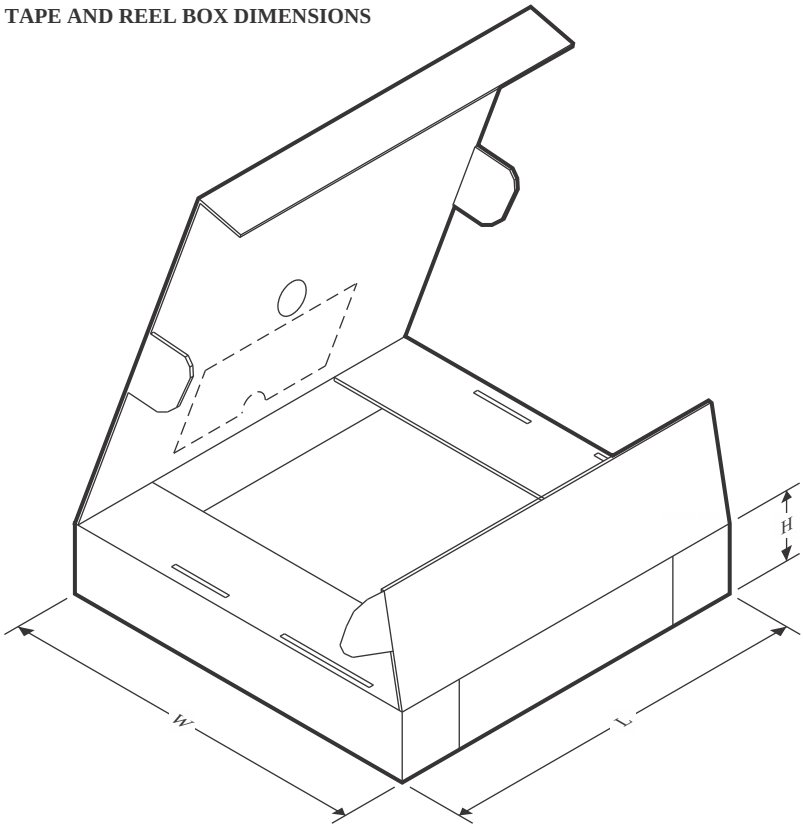
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2394PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

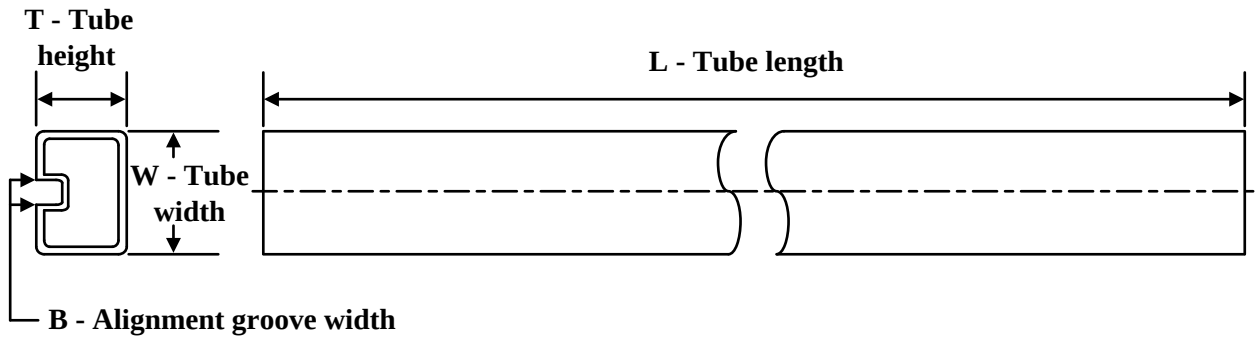
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2394PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

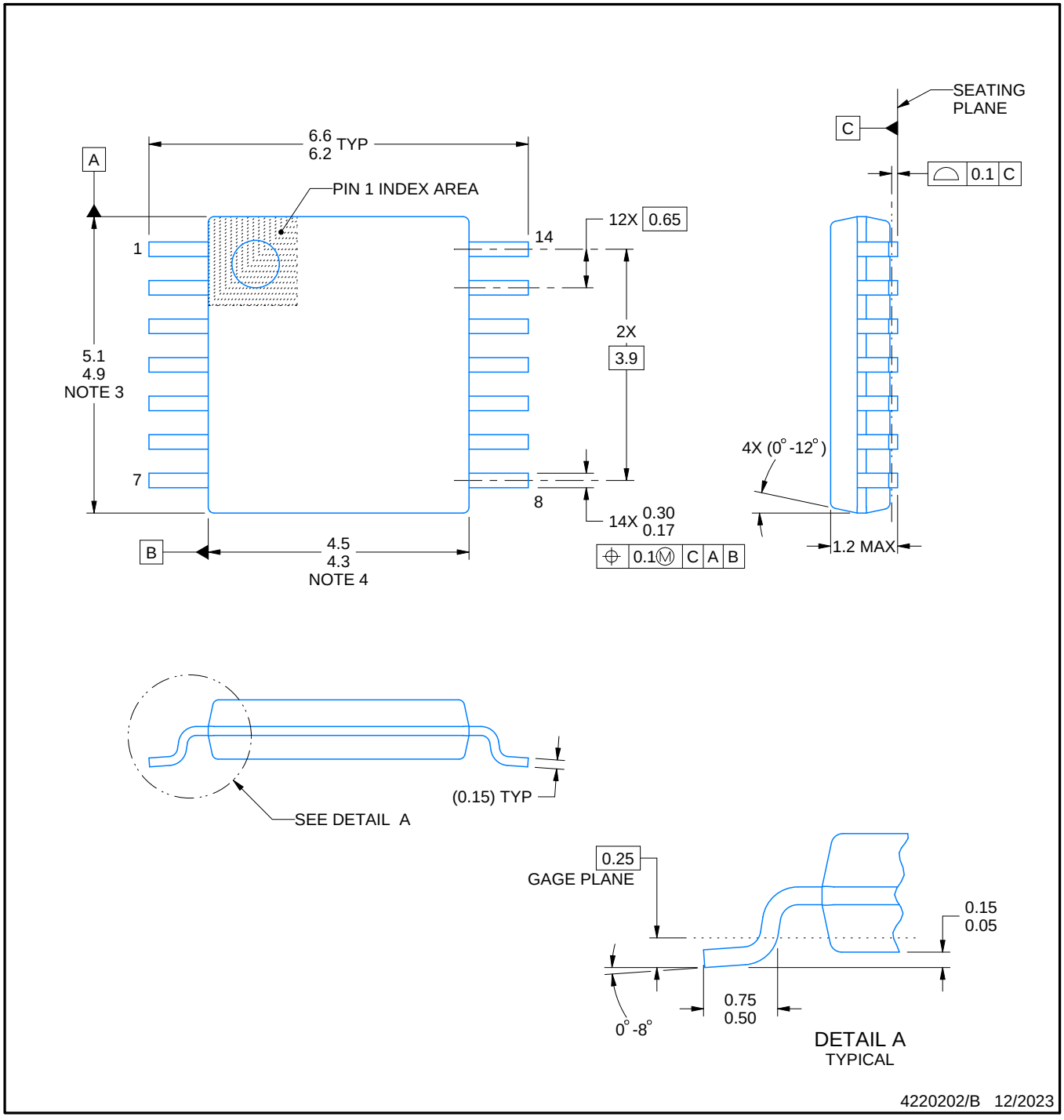
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2394PW	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

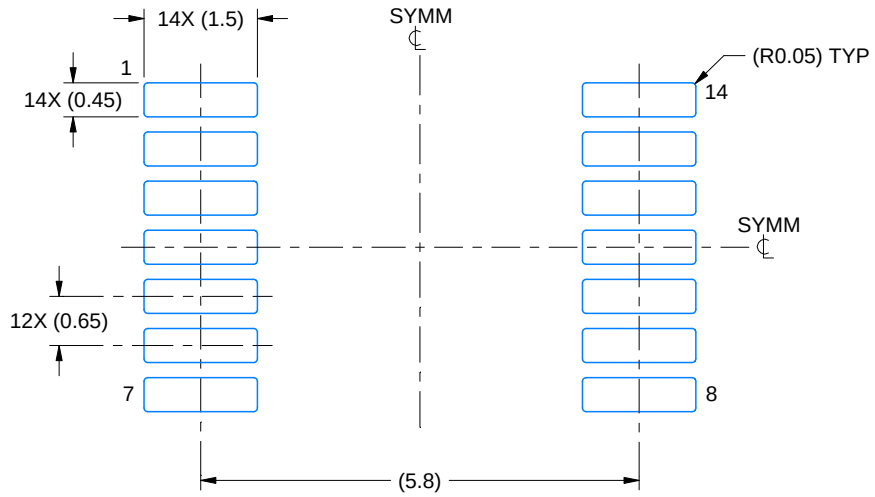
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

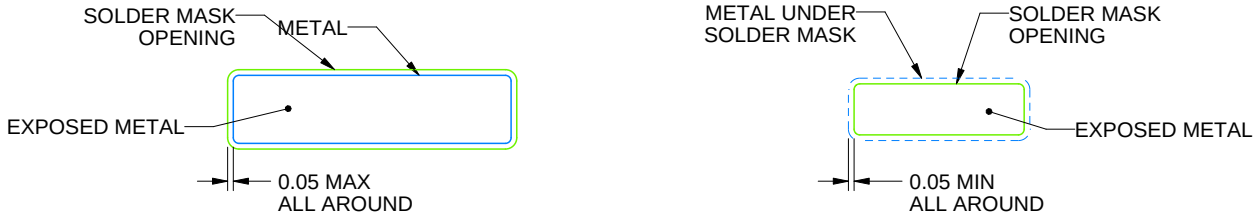


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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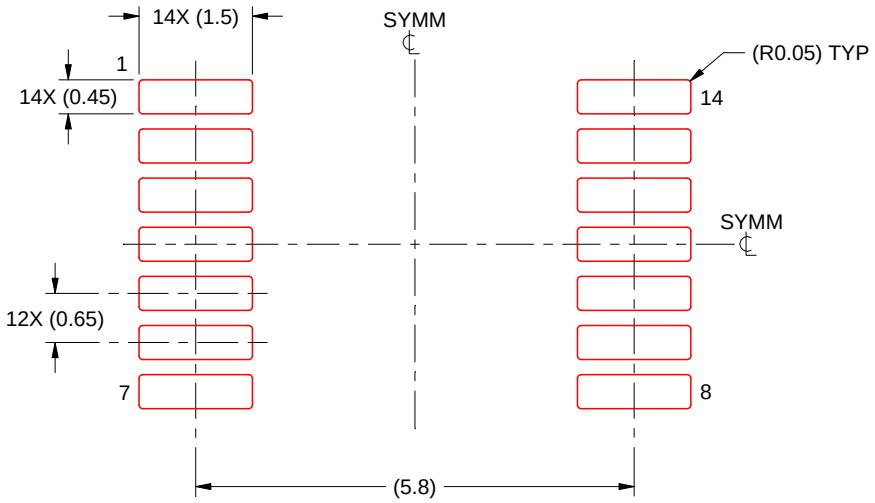
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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