

TPS27082L 1.2-V to 8-V, 3-A PFET Load Switch With Configurable Slew Rate, Fast Transient Isolation and Hysteretic Control

1 Features

- Low ON-Resistance, High Current PFET
 - $R_{ON} = 32\text{ m}\Omega$ (Typical) at $V_{GS} = -4.5\text{ V}$
 - $R_{ON} = 44\text{ m}\Omega$ (Typical) at $V_{GS} = -3.0\text{ V}$
 - $R_{ON} = 85\text{ m}\Omega$ (Typical) at $V_{GS} = -1.8\text{ V}$
 - $R_{ON} = 97\text{ m}\Omega$ (Typical) at $V_{GS} = -1.5\text{ V}$
 - $R_{ON} = 155\text{ m}\Omega$ (Typical) at $V_{GS} = -1.2\text{ V}$
- Configurable Turn-ON and Turn-OFF Slew Rate
 - 10- μs Default Minimum Output Rise Time at $V_{IN}=5\text{ V}$
- Configurable Turnon and Turnoff Slew Rate
- Supports a Wide Range of V_{IN} 1.2 V Up to 8 V
- Excellent OFF Isolation Even Under Fast Input Transients
- 1.0V up to 8V NMOS Control Logic Interface With Configurable Hysteresis
- Fully Protected Against ESD (All Pins)
 - HBM 2000 V, CDM 500 V
- Very Low ON-state Quiescent Current (Down to 1.2 μA)
- Very Low OFF-state Leakage Current (Typical 100 nA)
- Available in 2.9 mm x 1.6 mm x 0.75mm SOT-23 (DDC) Package

2 Applications

- High-Side Load Switches
- Inrush-current Controls
- Power Sequencing and Controls
- Stand-by Power Isolation
- Portable Power Switches

3 Description

The TPS27082L IC is a high-side load switch that integrates a Power PFET and a control circuit in a tiny TSOT-23 package. TPS27082L requires very low ON-state quiescent current and offers very low OFF-state leakage thus optimizing system power efficiency.

TPS27082L ON/OFF logic interface features hysteresis, thus providing a robust logic interface even under very noisy operating conditions. TPS27082L ON/OFF interface supports direct interfacing to low voltage GPIOs down to 1 V. The TPS27082L level shifts ON/OFF logic signal to V_{IN} levels without requiring an external level shifter.

TPS27082L features a novel OFF isolation circuit that prevents PMOS from turning ON in applications that may have fast transients, at the V_{IN} pin when the load switch is in the OFF-state.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS27082DDC	SOT (6)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

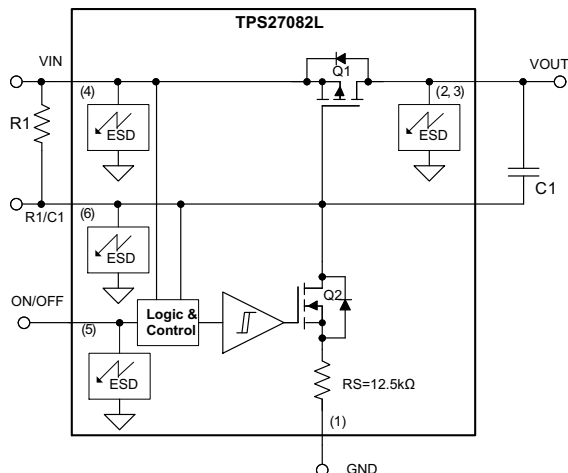


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4 Revision History

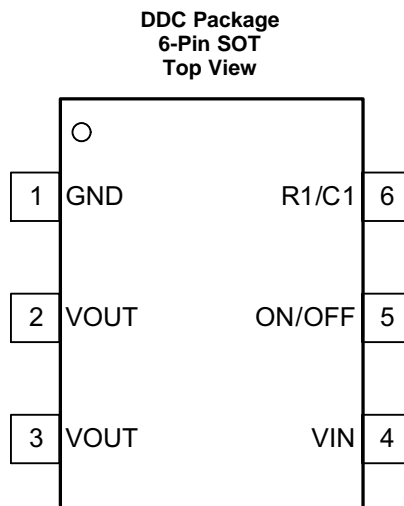
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2013) to Revision C	Page
<ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>Storage Conditions</i> table, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

Changes from Revision A (April 2013) to Revision B	Page
<ul style="list-style-type: none"> Removed <i>Ordering Information</i> table. Fixed UNIT typo for ON/OFF input logic hysteresis PARAMETER..... 	5

Changes from Original (December 2012) to Revision A	Page
<ul style="list-style-type: none"> Updated wording in the document..... 	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	I	Connect to the system GND
VOUT	2	O	Drain Terminal of Power PFET (Q1) – If required, connect a slew control capacitor between pins VOUT and R1/C
	3		
VIN	4	I	Source Terminal of Power PFET (Q1) – connect a pull-up resistor between the pins VIN and R1/C1
ON/OFF	5	I	Active high enable – when driven with a high impedance driver, connect an external pull down resistor to GND
R1/C1	6	I	Gate Terminal of Power PFET (Q1)

6 Specifications

6.1 Absolute Maximum Ratings

 Specified at $T_J = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

		MIN	MAX	UNIT
$V_{IN_{max}}$, $V_{OUT_{max}}$	VIN, VOUT pin maximum voltage with respect to GND pin	-0.1	8	V
$V_{ON/OFF}$	ON/OFF control voltage	-0.3	8	V
I_{Q1-ON}	Max continuous drain current of Q1		3	A
	Max pulsed drain current of Q1 ⁽⁴⁾		9.5	
P_D	Max power dissipation at $T_A = 25^{\circ}\text{C}$, $T_J = 150^{\circ}\text{C}$ ⁽⁴⁾		1190	mW
T_A	Operating free-air ambient temperature	-40	125 ⁽⁵⁾	$^{\circ}\text{C}$
T_{J-max}	Operating virtual junction temperature		150	$^{\circ}\text{C}$
T_{stg}	Storage temperature	-65	150	$^{\circ}\text{C}$

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Operating at the absolute T_{J-max} of 150°C can affect reliability – for higher reliability it is recommended to ensure $T_J < 125^{\circ}\text{C}$
- Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance.
- Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2\%$
- T_{J-max} limits and other related conditions apply. Refer to SOA charts, [Figure 8](#) through [Figure 13](#)

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000	V
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 500		

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input Voltage Range	1	8	V
T_A	Operating free-air ambient temperature range	-40	85	$^{\circ}\text{C}$
T_J	Junction Temperature	-40	105	$^{\circ}\text{C}$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS27082L	UNIT
		DDC (SOT)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43	$^{\circ}\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	17.8	$^{\circ}\text{C}/\text{W}$
Ψ_{JT}	Junction-to-top characterization parameter	6.5	$^{\circ}\text{C}/\text{W}$
Ψ_{JB}	Junction-to-board characterization parameter	16.2	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	$^{\circ}\text{C}/\text{W}$

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

 Full temperature range spans $T_J = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = T_J = 25^{\circ}\text{C}$			FULL TEMP RANGE ⁽¹⁾		UNIT	
		MIN	TYP	MAX	MIN	MAX		
OFF CHARACTERISTICS								
BV_{IN}	VIN breakdown voltage	$V_{ON/OFF} = 0\text{ V}, V_{GS}(Q1) = 0\text{ V}, I_{D}(Q1) = 250\text{ }\mu\text{A}$			-8		V	
I_{FIN}	VIN pin total forward leakage current ⁽²⁾	$V_{IN} = 8\text{ V}, V_{ON/OFF} = 0\text{ V}, R_L = 2.5\text{ }\Omega$			0.15		μA	
		$V_{IN} = 5\text{ V}, V_{ON/OFF} = 0\text{ V}, R_L = 2.5\text{ }\Omega$			0.04			
ON CHARACTERISTICS⁽³⁾								
V_{T+} (VIH)	Positive going ON/OFF threshold voltage ⁽⁴⁾	$V_{IN} = 5.0\text{ V}, R_1 = 125\text{ k}\Omega^{(1)}, R_L = 2.5\text{ }\Omega$			1.0		V	
		$V_{IN} = 5.0\text{ V}, R_1 = 1\text{ M}\Omega, R_L = 2.5\text{ }\Omega$			1.0			
V_{T-} (VIL)	Negative going ON/OFF threshold voltage ⁽⁴⁾	$V_{IN} = 5.0\text{ V}, I_{D}(Q1) < 175\text{ }\mu\text{A}, R_1 = 125\text{ k}\Omega^{(1)}$			400		mV	
		$V_{IN} = 5.0\text{ V}, I_{D}(Q1) < 175\text{ }\mu\text{A}, R_1 = 1\text{ M}\Omega$			270			
ΔV_T ($V_{T+} - V_{T-}$)	ON/OFF input logic hysteresis ⁽⁴⁾	$V_{IN} = 5.0\text{ V}, R_1 = 125\text{ k}\Omega^{(1)}$			600		mV	
		$V_{IN} = 5.0\text{ V}, R_1 = 1\text{ M}\Omega$			730			
$R_{Q1(ON)}$	Q1 Channel ON resistance ⁽⁵⁾	$V_{GSQ1} = -4.5\text{ V}, I_D = 3.0\text{ A}$			32	52	64	m Ω
		$V_{GS1Q1} = -3.0\text{ V}, I_D = 2.5\text{ A}$			44	66	84	
		$V_{GS1Q1} = -2.5\text{ V}, I_D = 2.5\text{ A}$			50	76	92	
		$V_{GSQ1} = -1.8\text{ V}, I_D = 2.0\text{ A}$			82	113	147	
		$V_{GSQ1} = -1.5\text{ V}, I_D = 1.0\text{ A}$			97	150	173	
		$V_{GSQ1} = -1.2\text{ V}, I_D = 0.50\text{ A}$			155	250	260	
$R_{GND_{ON}}$	R1/C1 pin to GND pin resistance when Q2 is ON	$V_{ON/OFF} = 1.8\text{ V}$			12.5	14.2	14.5	k Ω
Q1 DRAIN-SOURCE DIODE PARAMETERS⁽¹⁾⁽³⁾⁽⁶⁾								
I_{FSD}	Source-drain diode peak forward current	$V_{FSD(Q1)} = 0.8\text{ V}, V_{ON/OFF} = 0\text{ V}$			1			A
V_{FSD}	Source-drain diode forward voltage	$I_{FSD(Q1)} = -0.6\text{ A}, V_{ON/OFF} = 0\text{ V}$					1.0	V

- (1) Specified by design only
- (2) Refer to I_{FIN} plots for more information
- (3) Pulse width $< 300\mu\text{s}$, Duty cycle $< 2\%$
- (4) Refer to charts for more information on V_{T+}/V_{T-} thresholds
- (5) Refer to SOA charts for operating current information
- (6) Not rated for continuous current operation

6.6 Dissipation Ratings

 See ⁽¹⁾⁽²⁾⁽³⁾.

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$ ⁽⁴⁾	$T_A < 25^{\circ}\text{C}$	$T_A = 70^{\circ}\text{C}$	$T_A = 85^{\circ}\text{C}$	$T_A = 105^{\circ}\text{C}$	DERATING FACTOR ABOVE $T_A = 25^{\circ}\text{C}$
High-K (JEDEC 51-7)	6-Pin TSOT (DDC)	43°C/W	105°C/W	1190 mW	760 mW	619 mW	428 mW	9.55 mW/°C

- (1) Maximum dissipation values for retaining a maximum allowable device junction temperature of 150°C
- (2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance
- (3) Package thermal data based on a 76x114x1.6mm, 4-layer board with 2-oz Copper on outer layers
- (4) Operating at the absolute $T_{J,max}$ of 150°C can affect reliability; $T_J \leq 125^{\circ}\text{C}$ is recommended

6.7 Typical Characteristics

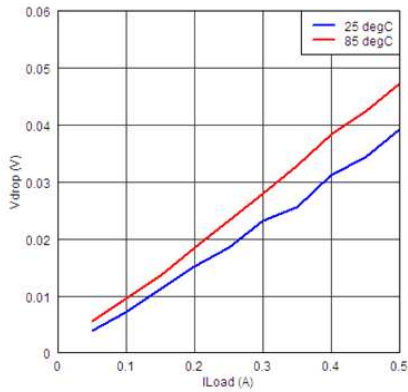


Figure 1. Vdrop vs IL; VGS_Q1 = -1.2 V

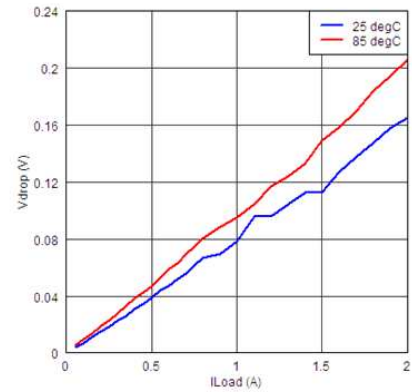


Figure 2. Vdrop vs IL; VGS_Q1 = -1.8 V

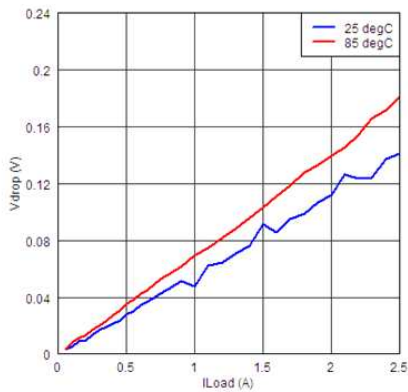


Figure 3. Vdrop vs IL; VGS_Q1 = -2.5 V

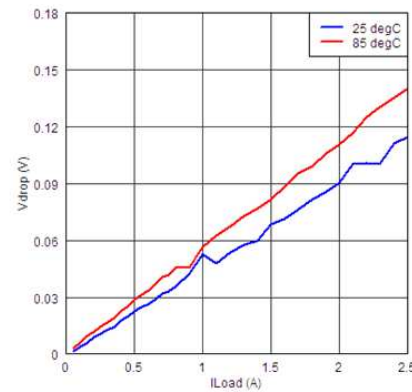


Figure 4. Vdrop vs IL; VGS_Q1 = -3.3 V

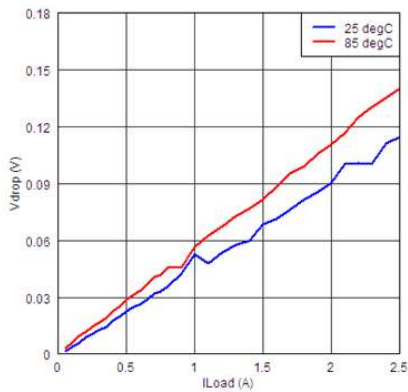


Figure 5. Vdrop vs IL; VGS_Q1 = -4.5 V

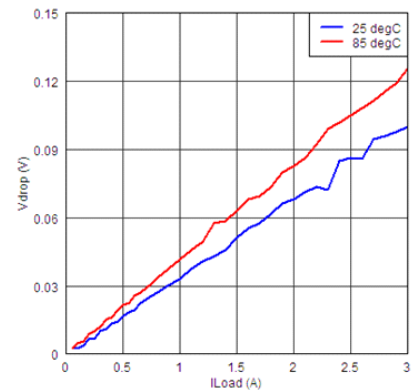
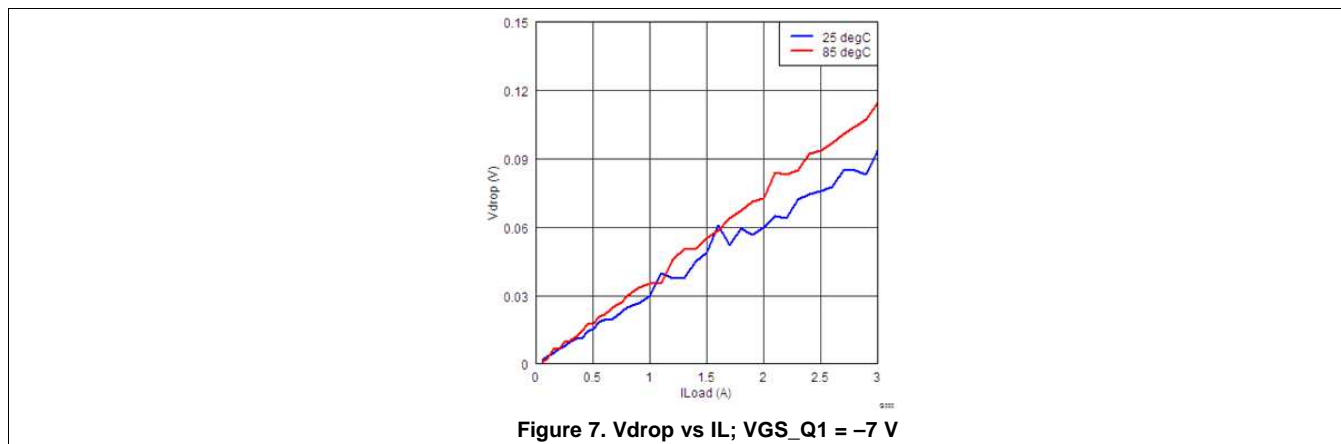


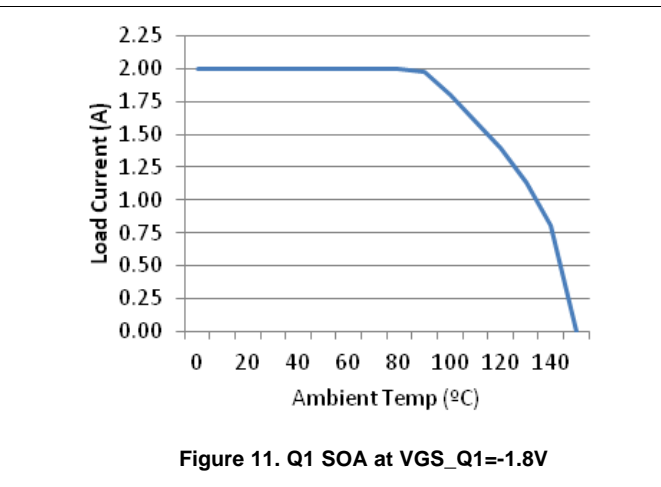
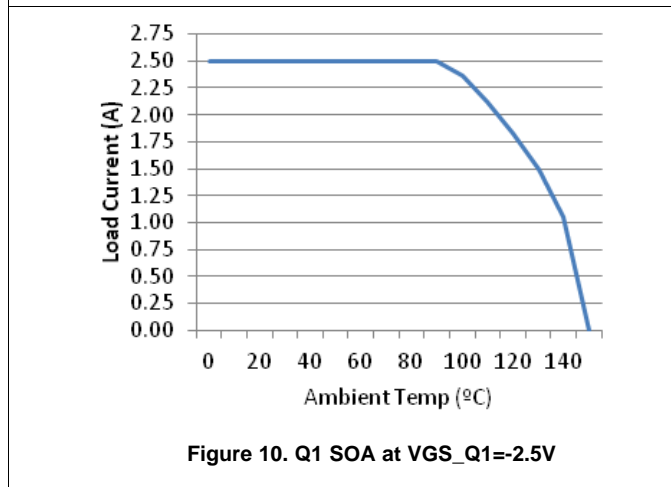
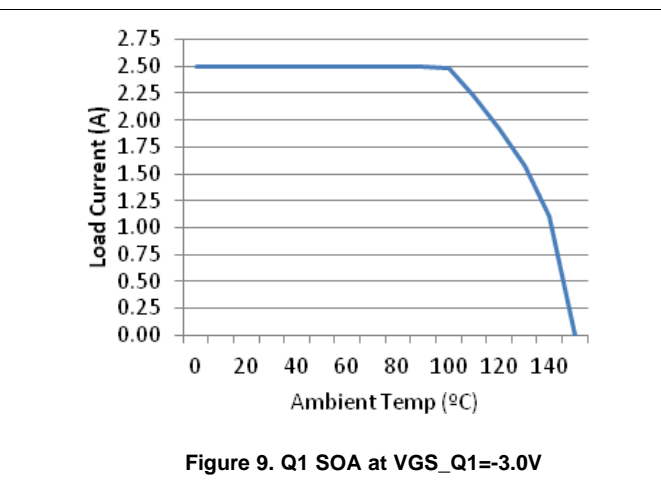
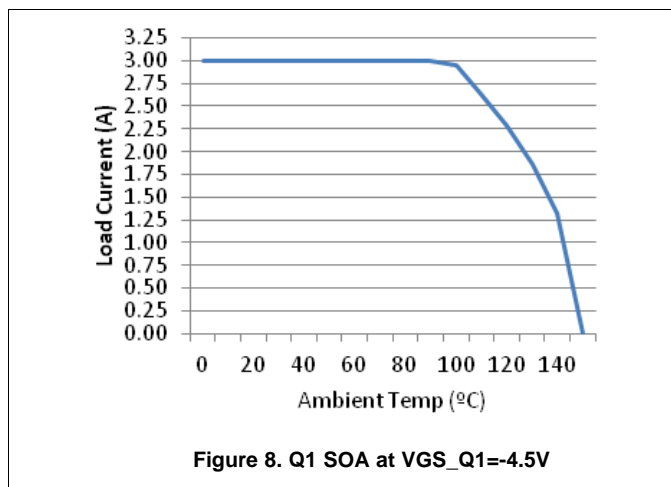
Figure 6. Vdrop vs IL; VGS_Q1 = -5.5 V

Typical Characteristics (continued)



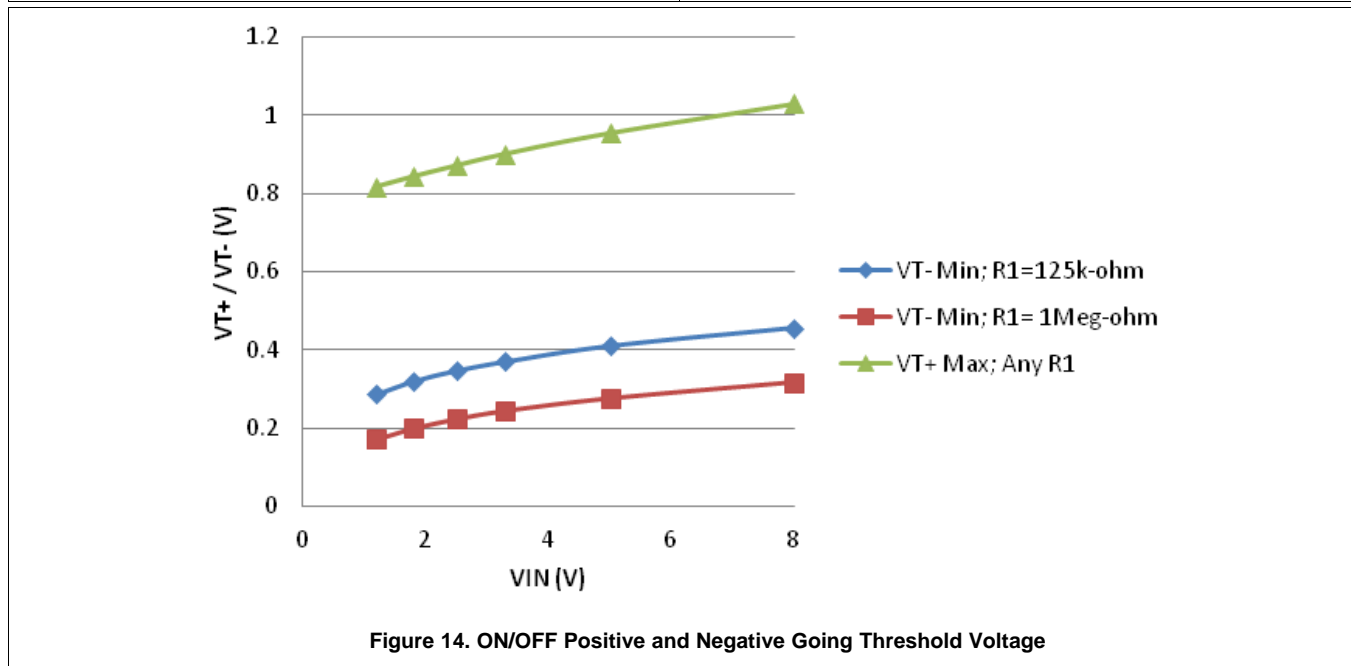
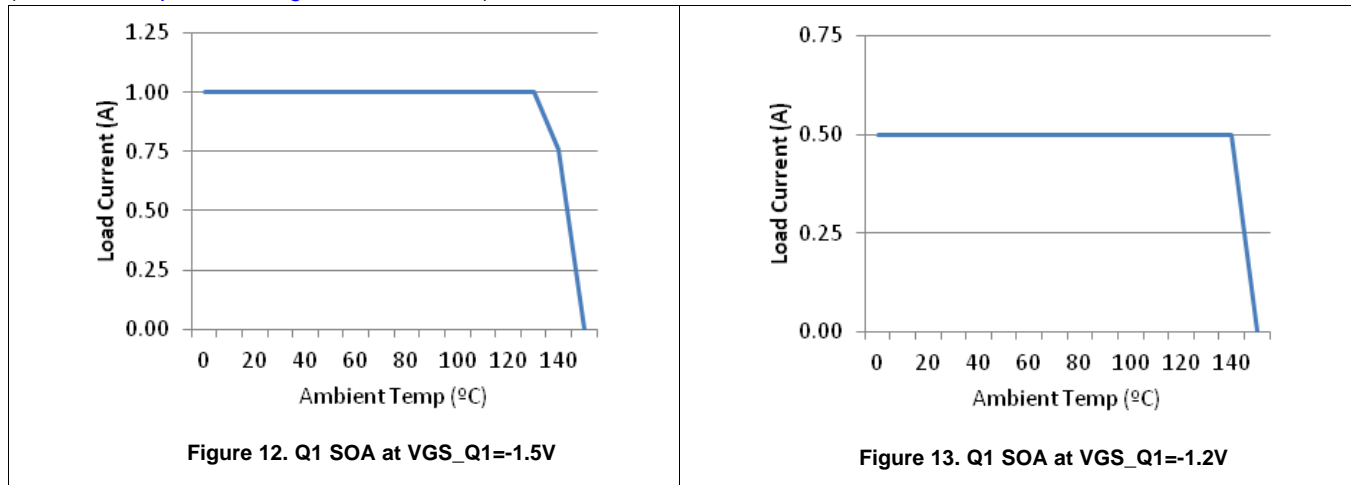
6.7.1 PFET Q1 Minimum Safe Operating Area (SOA)

(Refer to *Dissipation Ratings* for PCB details)



PFET Q1 Minimum Safe Operating Area (SOA) (continued)

(Refer to [Dissipation Ratings](#) for PCB details)

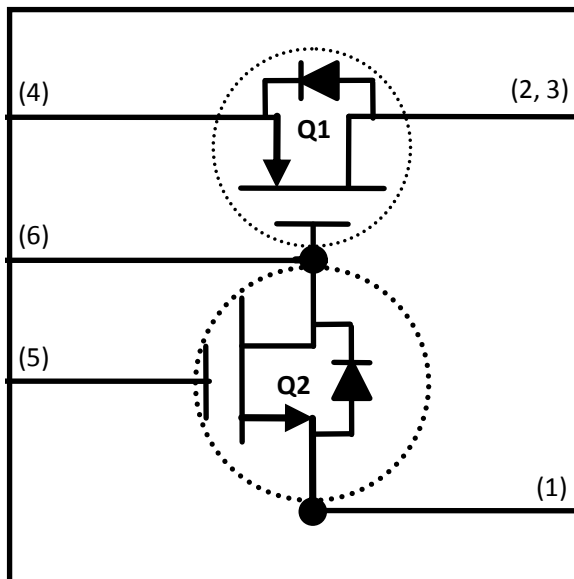


7 Detailed Description

7.1 Overview

The TPS27082L IC is a high side load switch that integrates a Power PFET and its control circuit in a tiny TSOT-23 package. TPS27082L supports up to 8V supply input and up to 3A of load current. The TPS27082L can be used in a variety of applications. The device has a programmable slew rate which helps reduce or eliminate power supply droop due to large inrush currents. During shutdown, the device has very low leakage currents.

7.2 Functional Block Diagram



7.3 Feature Description

TPS27082L uses a low-voltage power PMOS transistor used as the pass element or switch between the supply and load. It also integrates an NMOS transistor to turn the PMOS on and off by interfacing with a wide range of GPIO voltages. Asserting an input voltage higher than V_{ih} (1V) enables the PMOS switch by turning the NMOS and the NMOS driving the PMOS gate towards ground. Series resistance of 12.5 k connect at the source of NPN is integrated for TPS27082L. To control output rise time is programmed by connecting external capacitor at pin 6 of the device to design a delay time for PMOS to turn on.

7.4 Device Functional Modes

7.4.1 ON/OFF

When $V_{in} >$ about 1 V and $V(ON/OFF) >$ 1 V, the switch will turn on and $V_{out} \approx V_{in}$.

When $V_{in} >$ about 1 V and $V(ON/OFF) <$ 1 V, the switch will turn off and $V_{out} \neq V_{in}$.

7.4.2 Fastest Output Rise Time

Whenever it is desired to achieve the fastest output rise time, do not put a capacitor between V_{out} (Pins 2 and 3) and R1/C1 (pin 6).

7.4.3 Controlled Output Rise Time

Whenever it is desired to control the output rise time, tie pin 1 (R2) to a resistance (R2) and put a capacitor (C1) between V_{out} (Pins 2 and 3) and R1/C1 (pin 6).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS27082L IC is a high side load switch that integrates a Power PFET and a Control NMOS in a tiny package. The TPS27082L internal components are rated for up to 8V supply and support up to 3A of load current.

8.2 Typical Application

The TPS27082L can be used in a variety applications. Figure 15 shows a general application of TPS27082L to control the load inrush current. This section will highlight some of the design considerations when implementing this device in various applications.

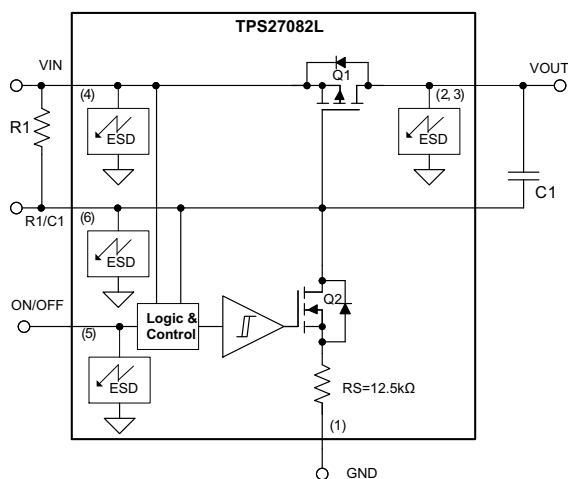


Figure 15. Typical Application Diagram

8.2.1 Design Requirements

Add an external pullup resistor R1 between VIN and R1/C1 to control the ON-resistance of the load switch. Guidelines for sizing R1 can be found in [Configuring Q1 ON-Resistance](#). In addition, TI recommends an output capacitor at VOUT to minimize the impact of inrush current from instantaneous switching. See [Configuring Turnon Slew Rate](#) for details regarding capacitor sizing.

8.2.2 Detailed Design Procedure

8.2.2.1 Configuring Q1 ON-Resistance

V_{GS-Q1} , Gate-Source voltage, of PMOS transistor Q1 sets its ON-resistance $R_{Q1(ON)}$. Connecting a high value pull up resistor R1 maximizes ON-state V_{GS-Q1} and thus minimizes the VIN to VOUT voltage drop. Use the following equation for calculating V_{GS-Q1} :

$$V_{GS_{Q1}} = -VIN \times \frac{R1}{R1 + 12.5 \text{ k}\Omega} \text{ V} \quad (1)$$

For example, R1= 125 kΩ, VIN = 5 V sets $V_{GS_{Q1}} = -4.5 \text{ V}$

Typical Application (continued)

NOTE

It is recommended to keep $R1 \geq 125 \text{ k}\Omega$. Higher value resistor R1 reduces ON-state quiescent current, increases turn-OFF delay, while reducing ON/OFF negative going threshold voltage V_{T-} .

8.2.2.2 Configuring Turnon Slew Rate

Switching a large capacitive load CL instantaneously results in a load inrush current given by the following equation:

$$I_{\text{inrush}} = C_{\text{load}} \times \frac{dv}{dt} = C_{\text{load}} \times \frac{V_{\text{OUT}_{\text{final}}} - V_{\text{OUT}_{\text{initial}}}}{\text{Vout Slew Rate}} \quad (2)$$

An uncontrolled fast rising ON/OFF logic input may result in a high slew rate (dv/dt) at the output thus leading to a higher load inrush current. To control the inrush current connect a capacitor C1 as shown in the [Figure 15](#). Use the following approximate empirical equation to configure the TPS27082L slew rate to a specific value.

$$t_{\text{rise}} = \frac{50 \times 10^3 \times C1}{VIN^{2/3}} \text{ sec}$$

where

- t_{rise} is the time delta starting from the ON/OFF signal's rising edge to charge up the load capacitor CL from 10% to 90% of VIN voltage (3)

Table 1. Capacitor C1 Selection for Standard Output Rise Time

t_{rise} (μSec) (Typical)	C1 (F) R1 = 125 k Ω				
	VIN=7V	VIN=5V	VIN=3.3V	VIN=1.8V	VIN=1.2V
5	0	0	0	0	0
50	3.46n	2.77n	2.10n	1.41n	1.08n
100	6.91n	5.54n	4.21n	2.82n	2.16n
250	17.3n	13.8n	10.5n	7.05n	5.40n
470	32.5n	26.0n	19.8n	13.3n	10.1n
1000	69.1n	55.4n	42.1n	28.2n	21.6n

NOTE

The t_{rise} equation and the capacitor C1 values recommended in the table above are under typical conditions and are accurate to within $\pm 20\%$. Ensure $R1 > 125 \text{ k}\Omega$; and select a closest standard valued capacitor C1.

8.2.2.3 Configuring Turnoff Delay

TPS27082L PMOS turnoff delay from the falling edge of ON/OFF logic signal depends upon the component values of resistor R1 and capacitor C1. Lower values of resistor R1 ensures quicker turnoff.

$$t_{\text{off}} > (R1 \times C1 \text{ sec}) \quad (4)$$

8.2.2.4 OFF Isolation Under VIN Transients

TPS27082L architecture helps isolate fast transients at the VIN when PFET is in the OFF state. Best transient isolation is achieved when an external capacitor C1 is not connected across VOUT and R1/C1 pins. When a capacitor C1 is present the VIN to VOUT coupling is capacitive and is set by the C1 to CL capacitance ratio. TPS27082L architecture prevents direct conduction through PFET.

8.2.2.5 Low Voltage ON/OFF Interface

To turn on the load switch apply a voltage > 1.0 V at the ON/OFF pin. The TPS27082L features hysteresis at its ON/OFF input. The turnon and turnoff thresholds are dependent upon the value of resistor R1. Refer to the [Electrical Characteristics](#) table and [Figure 14](#) for details on the positive and negative going ON/OFF thresholds.

In applications where ON/OFF signal is not available connect ON/OFF pin to the VIN pin. The TPS27082L will turn ON and OFF in sync with the input supply connected to VIN.

8.2.2.6 On-Chip Power Dissipation

Use below approximate equation to calculate TPS27082L's on-chip power dissipation P_D :

$$PD = I_{DQ1}^2 \times R_{Q1(ON)}$$

where

- I_{DQ1} is the DC current flowing through the transistor Q1 (5)

Refer to [Electrical Characteristics](#) table and the [Figure 1](#) through [Figure 7](#) to estimate $R_{Q1(ON)}$ for various values of V_{GSQ1} .

Note: MOS switches can get extremely hot when operated in saturation region. As a general guideline, to avoid transistors Q1 going into saturation region set $V_{GS} > V_{DS} + 1.0$ V. E.g. $V_{GS} > 1.5$ V and $V_{DS} < 200$ mV ensures switching region.

8.2.3 Application Curve

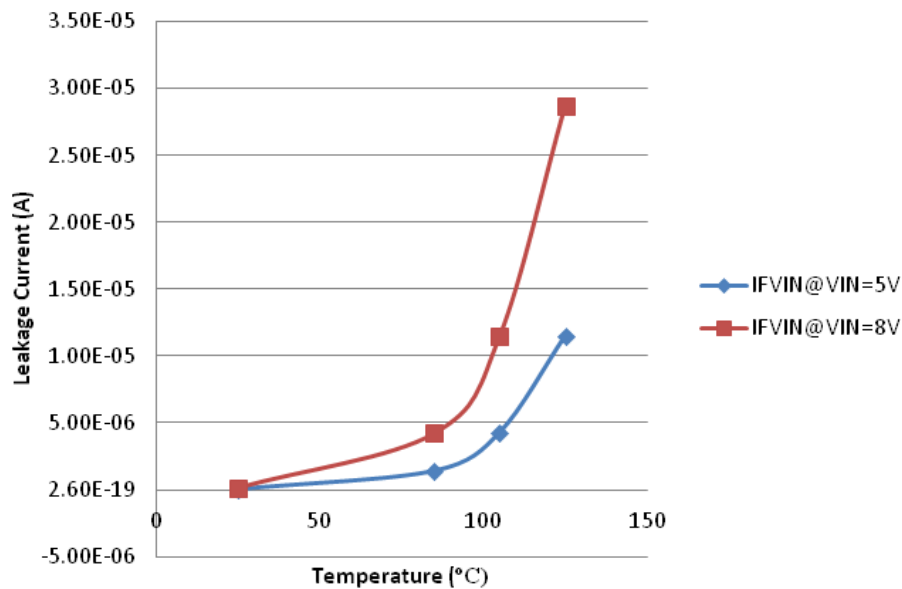


Figure 16. VIN Pin Leakage Current

8.3 System Examples

8.3.1 TFT LCD Module Inrush Current Control

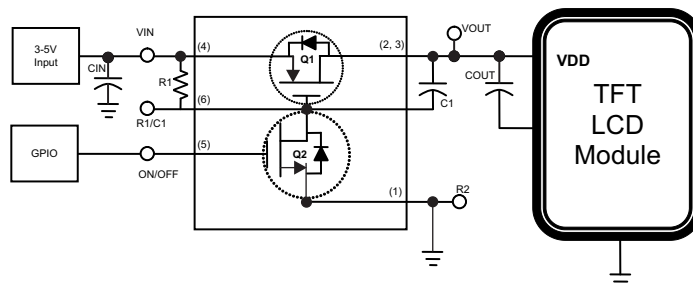


Figure 17. Inrush Current Control Using TPS27082L

LCD panels require inrush current control to prevent permanent system damages during turn-ON and turn-OFF events.

8.3.2 Standby Power Isolation

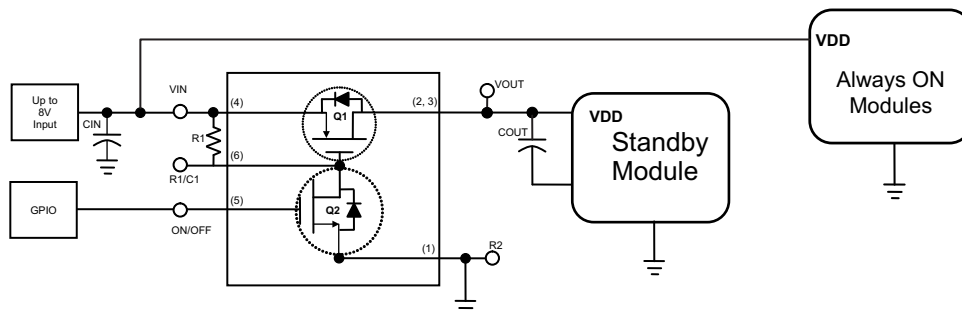


Figure 18. Boost

Many applications have some always ON modules to support various core functions. However, some modules are selectively powered ON or OFF to save power and multiplexing of various on board resources. Such modules that are selectively turned ON or OFF require standby power generation. In such applications TPS27082L requires only a single pull-up resistor. In this configuration the VOUT voltage rise time is approximately 250ns when VIN = 5V.

8.3.3 Boost Regulator With True Shutdown

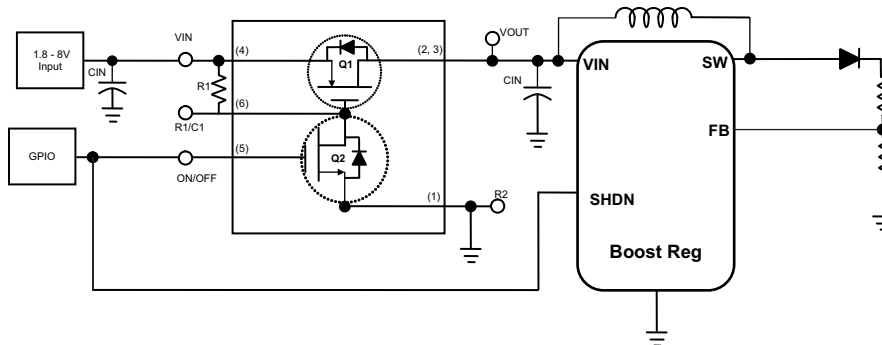


Figure 19. True Shutdown Using TPS27082L

System Examples (continued)

The most common boost regulator topology provides a current leakage path through inductor and diode into the feedback resistor even when the regulator is shut down. Adding a TPS27082L in the input side power path prevents this leakage current and thus providing a true shutdown.

8.3.4 Single Module Multiple Power Supply Sequencing

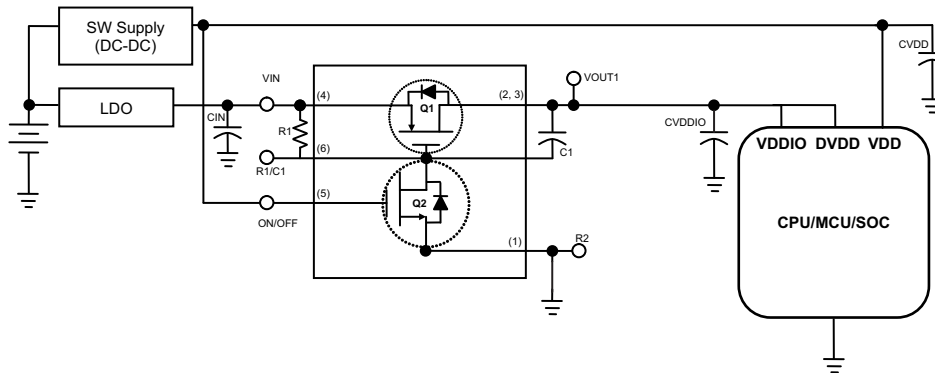


Figure 20. Power Sequencing Using TPS27082L, Example 1

Most modern SOCs and CPUs require multiple voltage inputs for its Analog, Digital cores and IO interfaces. These ICs require that these supplies be applied simultaneously or in a certain sequence. TPS27082L when configured, as shown in Figure 20, with the VOUT1 rise time adjusted appropriately through resistor R2 and capacitor C1, will delay the early arriving LDO output to match up with late arriving DC-DC output and thus achieving power sequencing.

8.3.5 Multiple Modules Interdependent Power Supply Sequencing

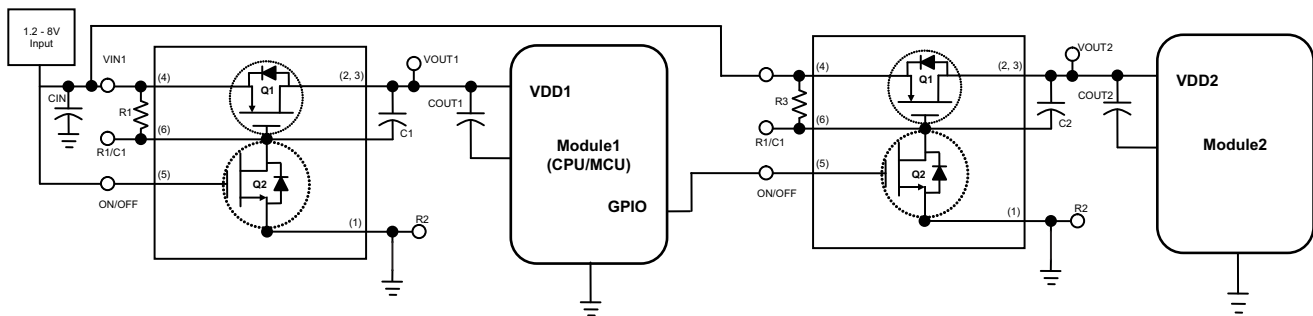


Figure 21. Power Sequencing Using TPS27082L, Example 2

For system integrity reasons a certain power sequencing may be required among various modules. As shown in Figure 21, Module 2 will power up only after Module 1 is powered up and the Module 1 GPIO output is enabled to turn ON Module 2. TPS27082L when used as shown in Figure 21 will not only sequence the Module 2 power, but also it will help prevent inrush current into the power path of Module 1 and 2.

System Examples (continued)

8.3.6 Multiple Modules Interdependent Supply Sequencing Without a GPIO Input

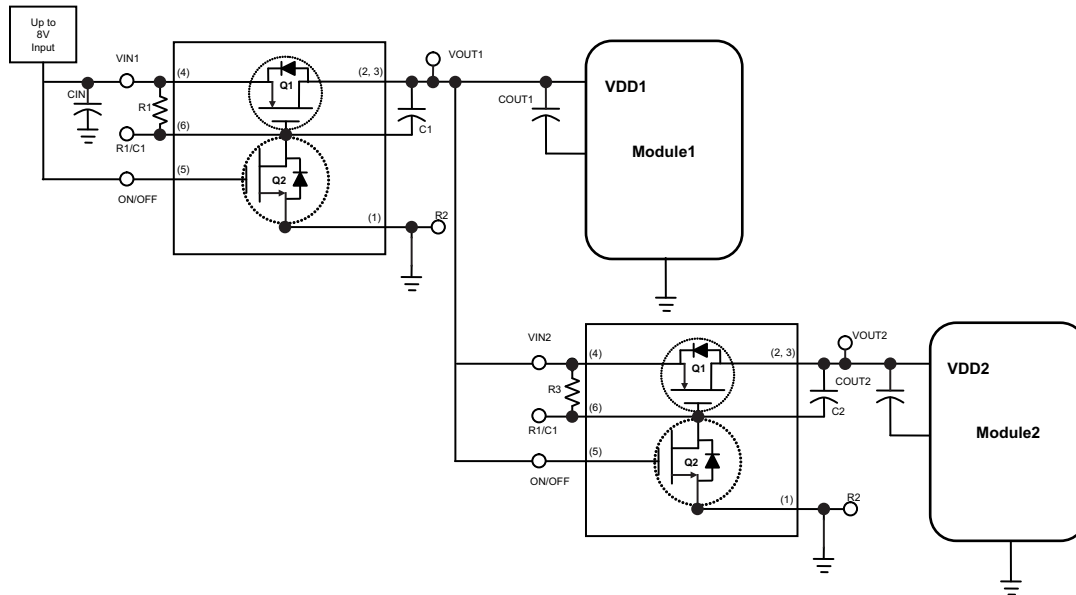


Figure 22. Power Sequencing using TPS27082L, Example 3

When a GPIO signal is not available connecting the ON/OFF pin of TPS27082 connected to Module 2 will power up Module 2 after Module 1, when resistor R4 and capacitor C1 are chosen appropriately. The two TPS27082L in this configuration will also control load inrush current.

9 Power Supply Recommendations

The device is designed to operate from a VIN range of 1.0 V to 8.0 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1- μ F bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 μ F may be sufficient.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- The VIN pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1- μ F ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The VOUT pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.

10.2 Layout Example

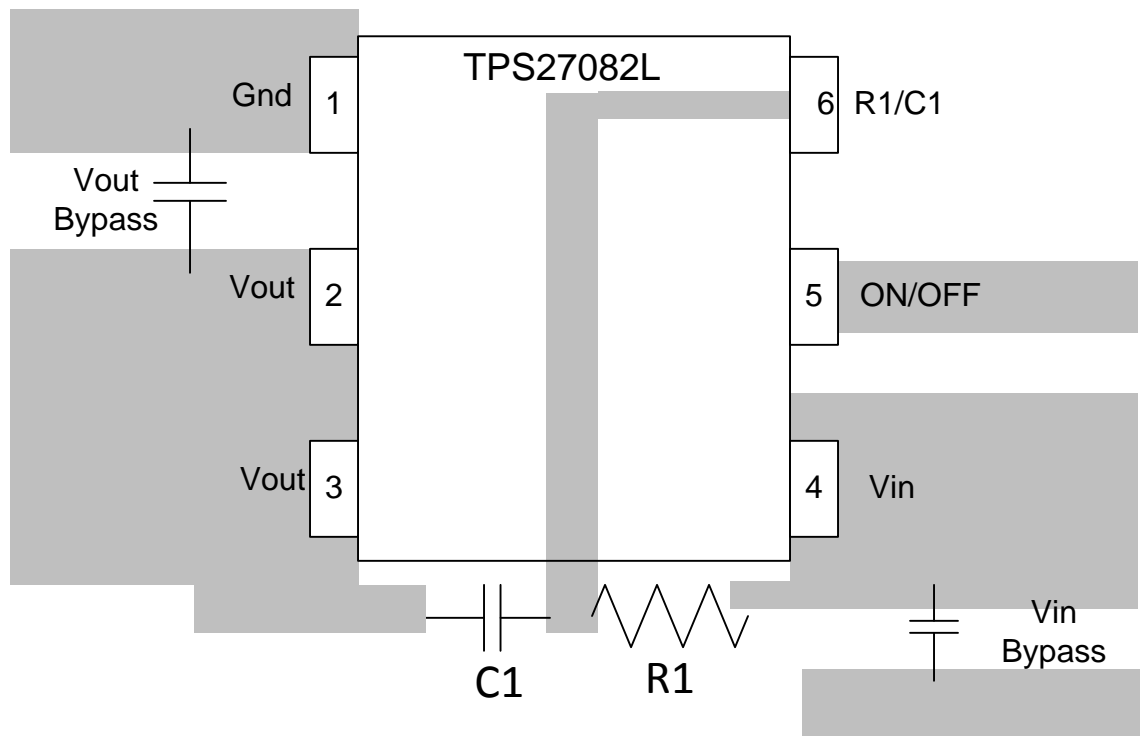


Figure 23. Layout Diagram

10.3 Thermal Considerations

For higher reliability it is recommended to limit TPS27082L IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate maximum on-chip power dissipation to restrict the die junction temperature target to safe limits:

$$PD_{(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature,
- T_A is the operating ambient temperature,
- and $R_{\theta JA}$ is the package junction to ambient thermal resistance. (6)

10.3.1 Improving Package Thermal Performance

The package $R_{\theta JA}$ value under standard conditions on a High-K board is available in [Dissipation Ratings](#). $R_{\theta JA}$ value depends upon the PCB layout. An external heat sink and/or a cooling mechanism like a cold air fan can help reduce $R_{\theta JA}$ and thus improving device thermal capability. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS27082LDDCR	NRND	Production	SOT-23- THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	BUA
TPS27082LDDCR.B	NRND	Production	SOT-23- THIN (DDC) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	BUA

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

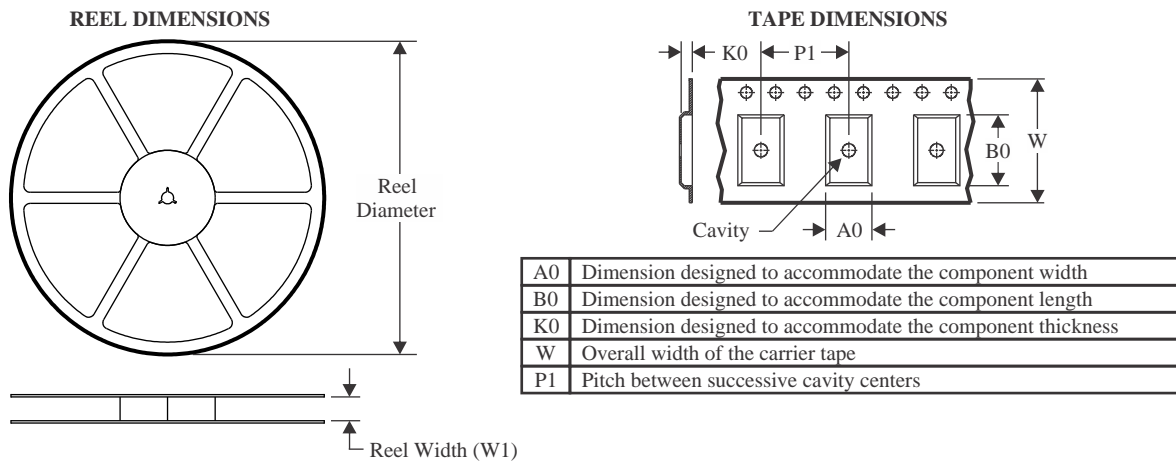
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

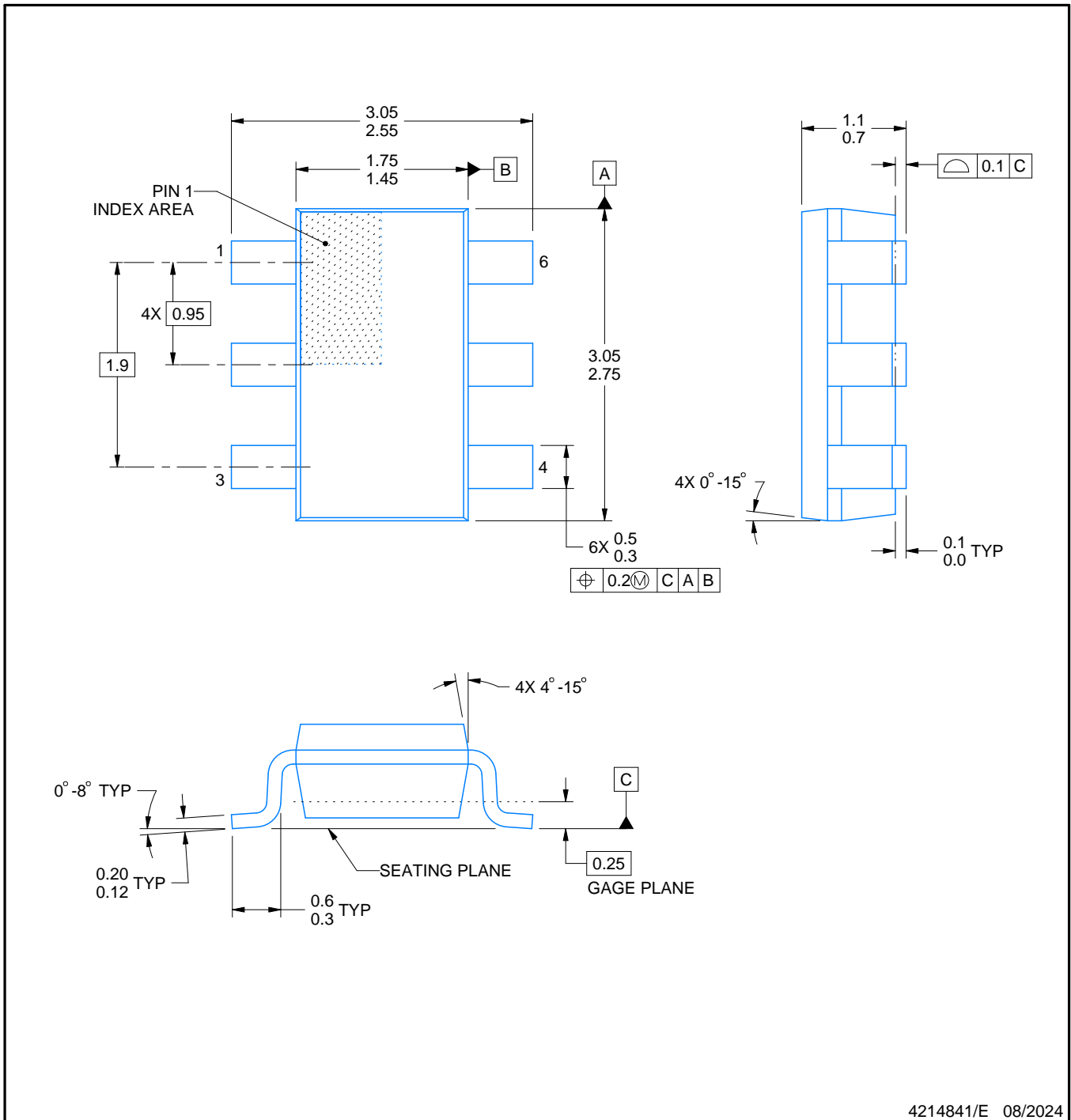

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS27082LDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

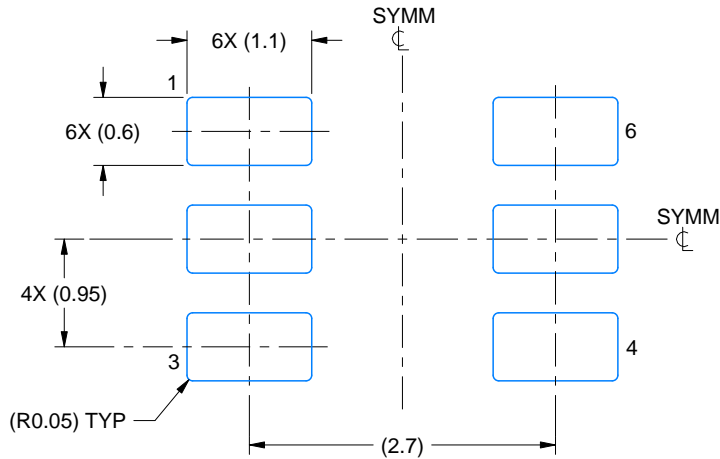

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS27082LDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X



SOLDEMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

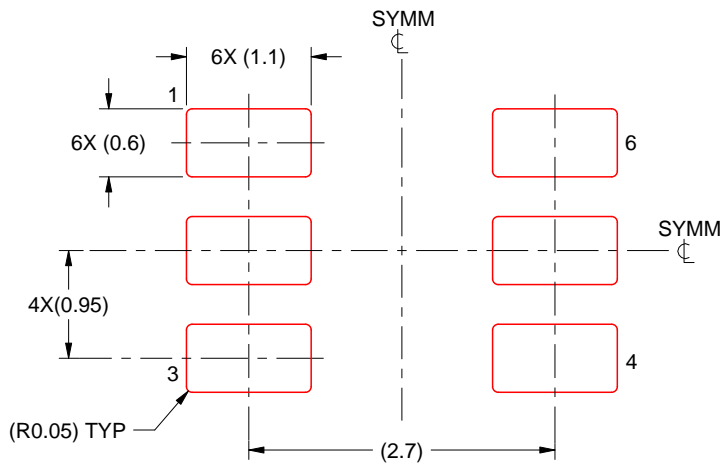
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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