TPS53840 Integrated Step-Down Converter for DDR5 MRDIMM Server Power Supply

1 Features

- Compliant to JEDEC PMIC5020 for DDR5 MRDIMM and RDIMM
- 4 Buck regulators
  - SWA (1.1V) 8.5A DC/10A Pk
  - SWB (1.1V) 8.5A DC/10A Pk
  - SWC (1.1V) 10A DC/11.5A Pk
  - SWD (1.8V) 3A DC/3.5A Pk
- Single or dual phase for SWA and SWB
- 2 LDO: 1.8V / 25mA and 1.0V / 20mA
- VIN_Bulk (4.25V to 15V) and VIN_Mgmt (3.0V to 3.6V) input supplies
- Automatic switchover from VIN_Mgmt to VIN_Bulk
- Overvoltage, under voltage, over current, temperature warning and temperature shutdown
- Error injection capability
- DIMM specific registers for customization (EEPROM)
- Persistent error log registers
- Programmable switching frequency: 500kHz to 1.375MHz
- Power good pin (CAMP) and General status interrupt pin (GSI_n)
- I^2C and I3C Bus interface for telemetry of voltage, current, power, temperature, and fault conditions
- Enable with I^2C/I3C, VR_EN pin or Auto power on
- 5mm × 5mm, 35-Pin, QFN PowerPad™ package

2 Applications

- DDR5 MRDIMM and RDIMM Power Supply for Server
- DDR5 CXL module power supply

3 Description

The TPS53840 is a D-CAP+™ mode integrated step-down converter for DDR5 on-DIMM power supply in servers fully compliant to Jedec PMIC5020. It provides VDD, VDDQ and VPP voltages to the DRAM chips on the DIMM module with configurable current capability. SWA and SWB can be configured to be either a dual phase output (20A) or 2 single outputs (10A each), while SWC is a single phase rail capable of 11.5A. The converter also employs internal compensation for ease of use and reduce external components.

The converter provides a full set of telemetry, including input voltage, output voltage, output current and output power. Protection features include input and output over voltage, input and output undervoltage, buck overcurrent limit, and die over temperature.

TPS53840 with its significantly higher current capability than JEDEC PMIC5000, and configurable Auto power on or VR_EN pin, is suitable for CXL memory module applications.

The TPS53840 is packaged in a thermally-enhanced 35-pin QFN and operates from -40°C to +105°C.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS53840	RWZ	5.00mm x 5.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

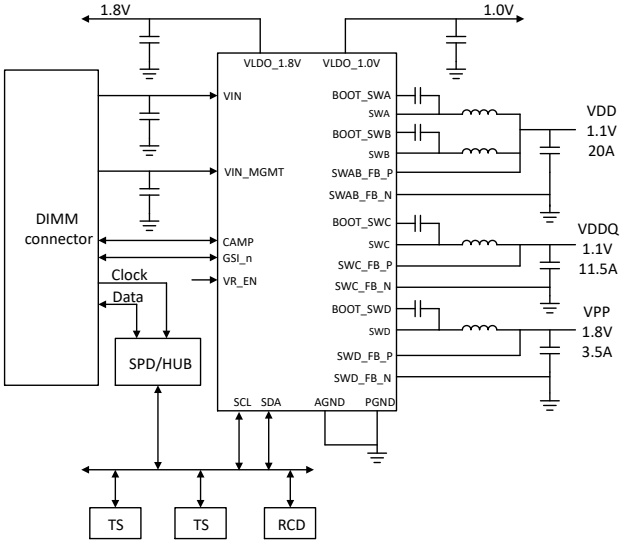

Figure 3-1. Simplified Application

4 Device and Documentation Support

4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

4.3 Trademarks

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4.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2024	*	Initial release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TPS53840RWZR	ACTIVE	VQFN-HR	RWZ	35	3000	RoHS & Green	NiPdAU	Level-2-260C-1 Year	–40 to 105	TPS53840
TPS53840M1RWZR	ACTIVE	VQFN-HR	RWZ	35	3000	RoHS & Green	NiPdAU	Level-2-260C-1 Year	–40 to 105	TPS53840
TPS53840H1RWZR	ACTIVE	VQFN-HR	RWZ	35	3000	RoHS & Green	NiPdAU	Level-2-260C-1 Year	–40 to 105	TPS53840
TPS53840S1RWZR	ACTIVE	VQFN-HR	RWZ	35	3000	RoHS & Green	NiPdAU	Level-2-260C-1 Year	–40 to 105	TPS53840

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

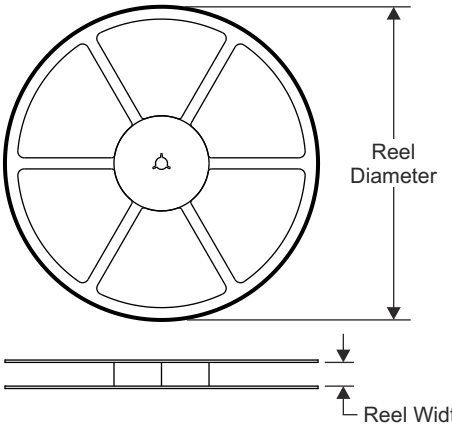
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

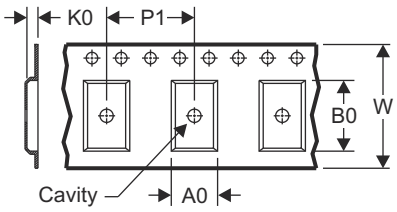
(6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

6.2 Tape and Reel Information

REEL DIMENSIONS

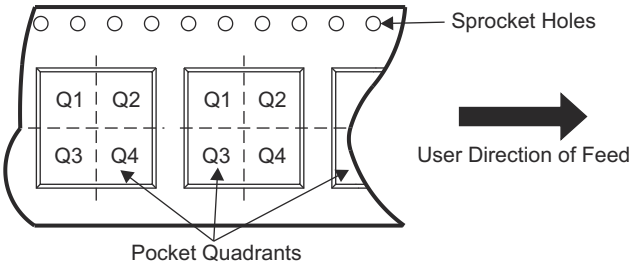


TAPE DIMENSIONS



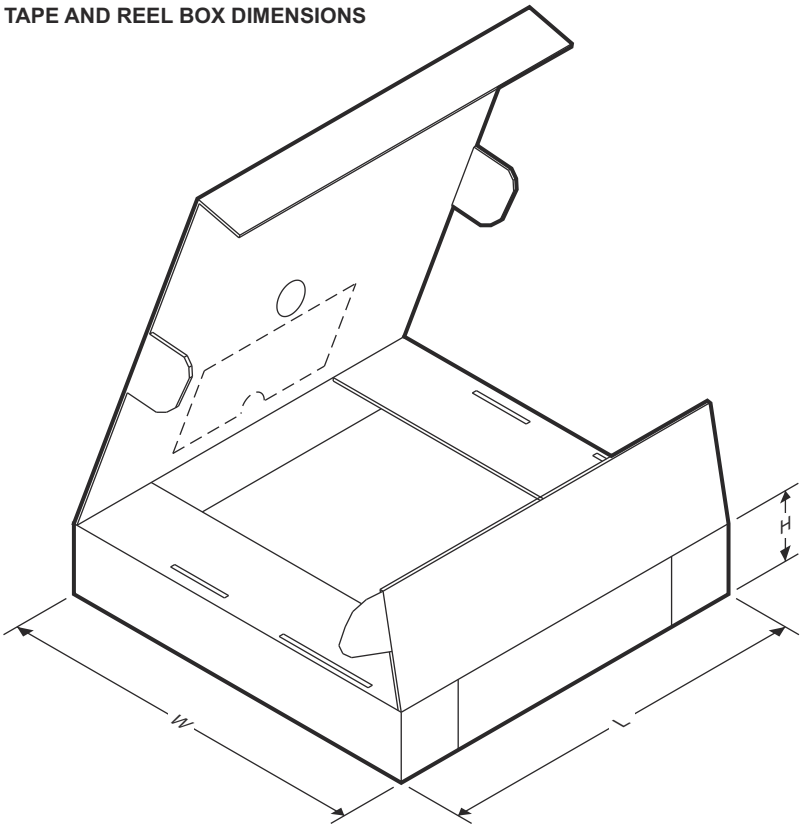
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53840RWZR	VQFN-HR	RWZ	35	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
TPS53840M1RWZR	VQFN-HR	RWZ	35	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
TPS53840H1RWZR	VQFN-HR	RWZ	35	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1
TPS53840S1RWZR	VQFN-HR	RWZ	35	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



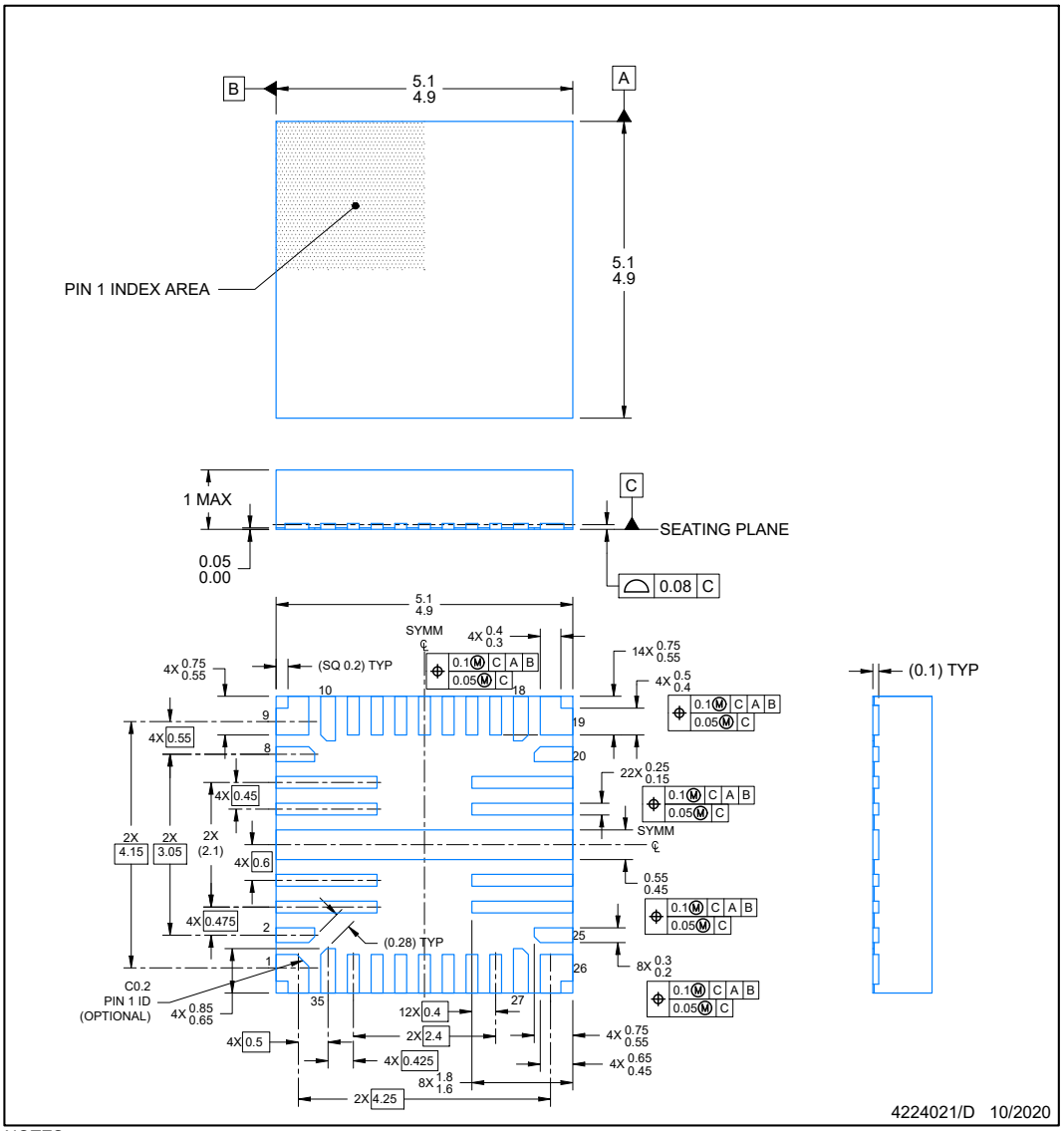
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53840RWZR	VQFN-HR	RWZ	35	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RWZ0035A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLAT-NO LEAD



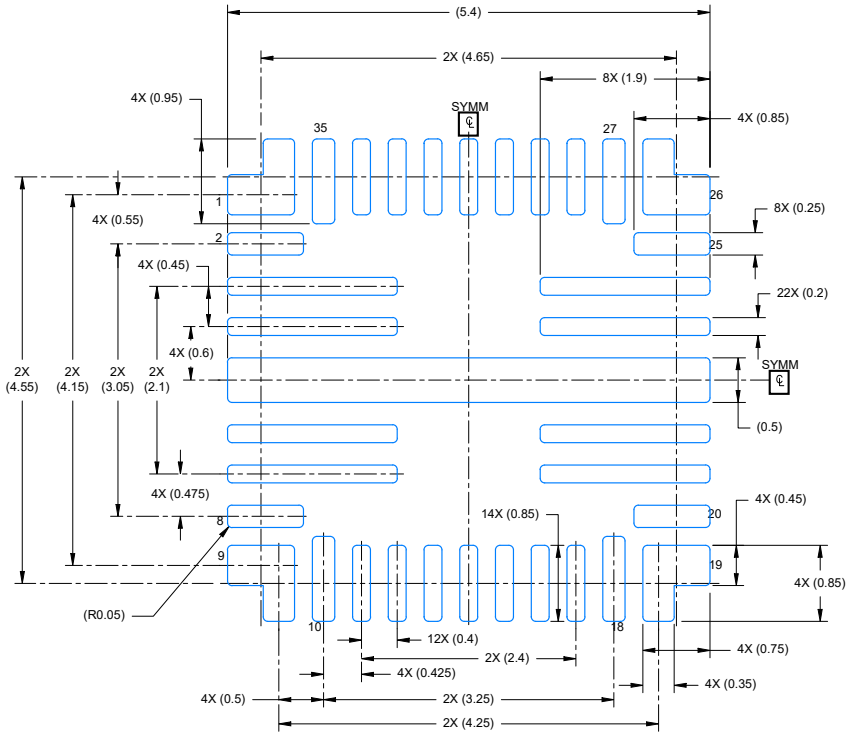
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

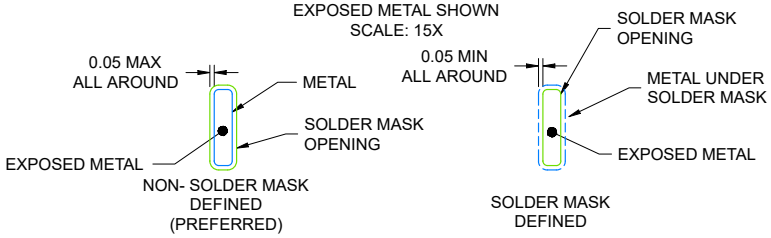
EXAMPLE BOARD LAYOUT

RWZ0035A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLAT-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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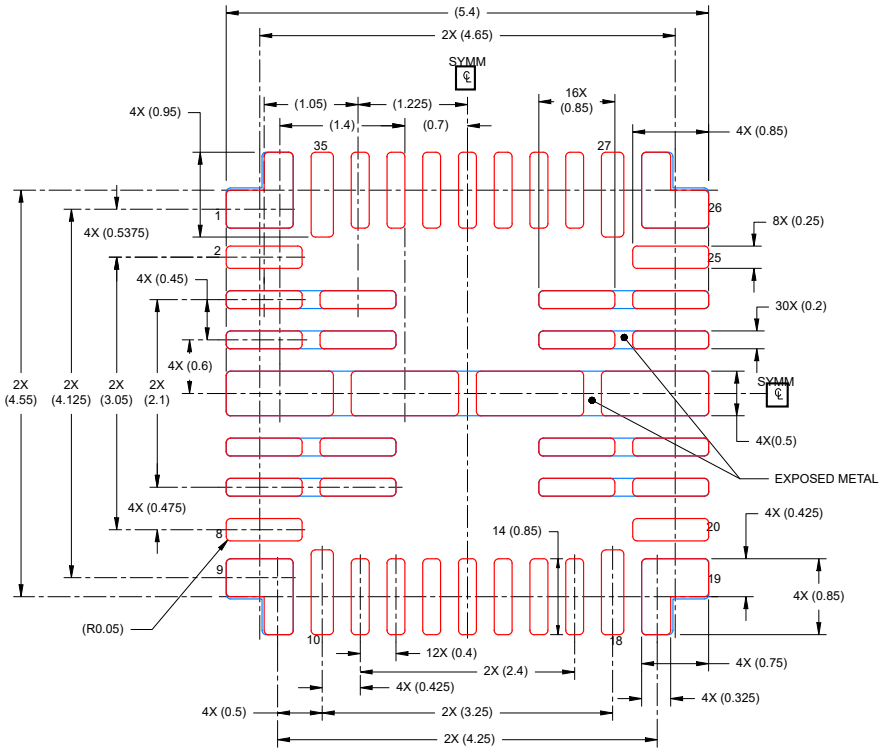
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RWZ0035A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLAT-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 9, 19 & 26: 96% & PADS 3-7, 21-22, 24-25:89%
SCALE: 15X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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