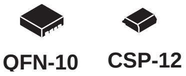


800-mA / 1000-mA, 3-MHz SYNCHRONOUS STEP-DOWN CONVERTER WITH I^2C™ COMPATIBLE INTERFACE IN CHIP SCALE PACKAGING

FEATURES

- **88% Efficiency at 3-MHz Operation**
- **800-mA Output Current at V_I = 2.7 V**
- **3-MHz Fixed Frequency Operation**
- ***Best in Class* Load and Line Transient**
- **Complete 1-mm Component Profile Solution**
- **±2% PWM DC Voltage Accuracy**
- **35-ns Minimum On-Time**
- **Efficiency Optimized Power-Save Mode (Light PFM)**
- **Transient Optimized Power-Save Mode (Fast PFM)**
- **28-µA Typical Quiescent Current**
- **I^2C Compatible Interface up to 3.4 Mbps**
- **Pin-Selectable Output Voltage**
- **Synchronizable *On the Fly* to External Clock Signal**
- **Available in a 10-Pin QFN (3 x 3 mm) and 12-Pin NanoFree™ (CSP) Packaging**

APPLICATIONS

- **SmartReflex™ Compliant Power Supply**
- **Split Supply DSPs and µP Solutions OMAP™, XSCALE™**
- **Cell Phones, Smart-Phones**
- **PDAs, Pocket PCs**
- **Digital Cameras**
- **Micro DC-DC Converter Modules**

DESCRIPTION

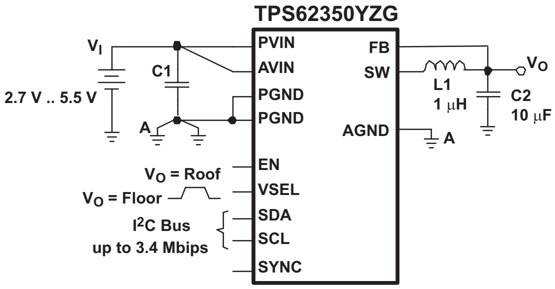
The TPS6235x device is a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. Intended for low-power applications, the TPS6235x supports up to 800-mA load current and allows the use of small, low cost inductors and capacitors.

The device is ideal for mobile phones and similar portable applications powered by a single-cell Li-Ion battery. With an output voltage range adjustable via I^2C interface down to 0.6 V, the device supports low-voltage DSPs and processors core power supplies in smart-phones, PDAs, and handheld computers.

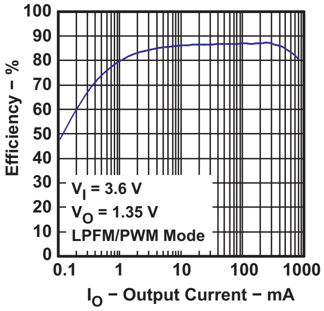
The TPS6235x operates at 3-MHz fixed switching frequency and enters the efficiency optimized power-save mode operation at light load currents to maintain high efficiency over the entire load current range. In the shutdown mode, the current consumption is reduced to less than 2 µA.

The serial interface is compatible with Fast/Standard and High-Speed mode I^2C specification allowing transfers at up to 3.4 Mbps. This communication interface is used for dynamic voltage scaling with voltage steps down to 12.5 mV, for reprogramming the mode of operation (Light PFM, Fast PFM or Forced PWM) or disable/enabling the output voltage.

TYPICAL APPLICATION



EFFICIENCY vs LOAD CURRENT



NanoFree, SmartReflex, OMAP, PowerPAD are trademarks of Texas Instruments.
XSCALE is a trademark of Intel Corporation.
I2C is a trademark of Philips Corporation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER(1)	OUTPUT VOLTAGE RANGE (2)	DEFAULT OUTPUT VOLTAGE(2)		DEFAULT VALUE EN_DCDC BIT(2)	SYNC	I^2C LSB ADDRESS BITS(2)		PACKAGE	ORDERING(3)	PACKAGE MARKING
		VSEL0	**VSEL1**			**A1**	**A0**			
TPS62350(4)	0.75 V to 1.5375 V	1.05 V	1.35 V	1	YES	0	0	CSP-12	TPS62350YZG	TPS62350
TPS62351	0.9 V to 1.6875 V	1.10 V	1.50 V	0	NO	1	0	QFN-10	TPS62351DRC	BNT
					YES	1	0	CSP-12	TPS62351YZG	TPS62351
TPS62352(4)	0.75 V to 1.4375 V	1.05 V	1.20 V	1	YES	1	0	CSP-12	TPS62352YZG	TPS62352
TPS62353	0.75 V to 1.5375 V	1.00 V	1.20 V	1	YES	0	0	CSP-12	TPS62353YZG	TPS62353
TPS62354(4)	0.75 V to 1.5375 V	1.05 V	1.30 V	1	YES	1	0	CSP-12	TPS62354YZG	TPS62354
TPS62355(4)	0.75 V to 1.5375 V	0.90 V	1.15 V	1	NO	1	1	QFN-10	TPS62355DRC	CCP
TPS62356	1.5 V to 1.975 V	1.80 V	1.80 V	1	YES	0	0	CSP-12	TPS62356YZG	TPS62356

(1) All devices are specified for operation in the commercial temperature range, –40°C to 85°C.
(2) For customized output voltage range, default output voltage and I^2C address, contact the factory.
(3) The YZG package is available in tape and reel. Add R suffix (TPS6235xYZGR, TPS6235xDRCR) to order quantities of 3000 parts. Add T suffix (TPS6235xYZGT, TPS6235xDRCT) to order quantities of 250 parts. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(4) The following registers bits are set by internal hardware logic and not user programmable through I^2C:
  a. VSEL0[7:6] = 11
  b. VSEL1[7:6] = 11
  c. CONTROL1[4:2] = 100
  d. CONTROL2[7:6] = 10, CONTROL2[4:3] = 00

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNITS
V_I	Voltage at AVIN, PVIN(2)	-0.3 V to 7 V
	Voltage at SW (2)	-0.3 V to 7 V
	Voltage at EN, VSEL, SCL, SDA, SYNC (2)	-0.3 V to 7 V
	Voltage at FB(2)	-0.3 V to 4.2 V
	Power dissipation	Internally limited
T_J	Maximum operating junction temperature	150°C
T_{stg}	Storage temperature range	–65°C to 150°C
ESD rating(3)	Human body model	2 kV
	Charge device model	1 kV
	Machine model	200 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	2.7		5.5	V
T_A	Operating temperature range (1)	-40		85	°C
T_J	Operating virtual junction temperature range	-40		125	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$ (2)	POWER RATING FOR $T_A \leq 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
DRC	49°C/W	2050 mW	21 mW/°C
YZG	89°C/W	1100 mW	12 mW/°C

(1) Maximum power dissipation is a function of T_J(max), θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(max) – T_A] / \theta_{JA}$.

(2) This thermal data is measured with high-K board (4 layers board according to JESD51-7 JEDEC standard).

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply with V_I = 3.6 V, EN = V_I, VSEL = V_I, SYNC = GND, VSEL0[6] bit = 1.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current	TPS62350/1/2/3/4/5	I_O = 0 mA, Fast PFM mode enabled Device not switching		110	150	µA
		TPS62356			117	160	
		TPS62350/1/2/3/4/5	I_O = 0 mA, Light PFM mode enabled Device not switching		28	45	µA
		TPS62356			35	52	
		TPS62350/1/2/3/4/5/6	I_O = 0 mA, 3-MHz PWM mode operation		4.8		mA
$I_{(SD)}$	Shutdown current		EN = GND, EN_DCDC bit = X		0.1	2	µA
			EN = V_I, EN_DCDC bit = 0		6.5		µA
$V_{(UVLO)}$	Undervoltage lockout threshold				2.20	2.3	V
ENABLE, VSEL, SDA, SCL, SYNC							
V_{IH}	High-level input voltage			1.2			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input tied to GND or V_I		0.01	1	µA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on resistance	TPS62350/1/2/3/4/5	$V_I = V_{(GS)}$ = 3.6 V, YZG package		250	500	mΩ
			$V_I = V_{(GS)}$ = 3.6 V, DRC package		275	500	
			$V_I = V_{(GS)}$ = 2.7 V, DRC package		350	750	
		TPS62356	$V_I = V_{(GS)}$ = 3.2 V, YZG package		320	500	
I_{lkg}	P-channel leakage current		$V_{(DS)}$ = 6 V			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance	TPS62350/1/2/3/4/5/6	$V_I = V_{(GS)}$ = 3.6 V, YZG package		150	350	mΩ
			$V_I = V_{(GS)}$ = 3.6 V, DRC package		165	350	
			$V_I = V_{(GS)}$ = 2.7 V, YZG / DRC package		210	500	
I_{lkg}	N-channel leakage current		$V_{(DS)}$ = 6 V			1	µA
$R_{(DIS)}$	Discharge resistor for power-down sequence				15	50	Ω
	P-MOS current limit	TPS62350/1/2/3/4/5	2.7 V ≤ V_I ≤ 5.5 V	1150	1350	1600	mA
		TPS62356		1300	1550	1800	mA

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply with V_I = 3.6 V, EN = V_I, VSEL = V_I, SYNC = GND, VSEL0[6] bit = 1.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	N-MOS current limit (sourcing)	TPS62350/1/2/3/4/5	2.7 V ≤ V_I ≤ 5.5 V	900	1100	1300	mA
		TPS62356		1200	1400	1700	mA
	N-MOS current limit (sinking)	TPS62350/1/2/3/4/5	2.7 V ≤ V_I ≤ 5.5 V	-500	-700	-900	mA
		TPS62356		-500	-700	-900	mA
	Input current limit under short-circuit conditions	TPS62350/1/2/3/4/5	V_O = 0 V		675		mA
		TPS62356			775		mA
	Thermal shutdown				150		°C
	Thermal shutdown hysteresis				20		°C
OSCILLATOR							
f_{SW}	Oscillator frequency		CONTROL2[4:3] = 00	2.65	3	3.35	MHz
$f_{(SYNC)}$	Synchronization range			2.65		3.35	MHz
	Duty cycle of external clock signal			20%		80%	
OUTPUT							
V_O	Output voltage range	TPS62350		0.75		1.5375	V
		TPS62351		0.90		1.6875	V
		TPS62352		0.75		1.4375	V
		TPS62353		0.75		1.5375	V
		TPS62354		0.75		1.5375	V
		TPS62355		0.75		1.5375	V
		TPS62356		1.50		1.975	V
$t_{on(MIN)}$	Minimum on-time (P-channel MOSFET)				35		ns
	Resistance into FB sense pin			700	1000		kΩ
V_O	Output voltage DC accuracy	TPS62350	V_I = 3.6 V, V_O = 1.35 V, $I_{O(DC)}$ = 0 mA PWM operation	–1.5%		1.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 0.75 V, 1.05 V, 1.35 V, 1.5375 V PWM operation	–2%		2%	
			2.7 V ≤ V_I ≤ 5.5 V, $I_{O(DC)}$ = 0 mA V_O = 1.05 V, L = 1 μH, Light PFM	–1%		4.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.35 V, L = 1 μH, Fast PFM/PWM	–2%		3%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.05 V, L = 1 μH, Light or Fast PFM/PWM	–2%		4.5%	
V_O	Output voltage DC accuracy	TPS62351	V_I = 3.6 V, V_O = 1.50 V, $I_{O(DC)}$ = 0 mA PWM operation	–1.5%		1.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 0.90 V, 1.10 V, 1.50 V, 1.6875 V PWM operation	–2%		2%	
			2.7 V ≤ V_I ≤ 5.5 V, $I_{O(DC)}$ = 0 mA V_O = 1.10 V, L = 1 μH, Light PFM	–1%		4.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.10 V, L = 1 μH, Light or Fast PFM/PWM	–2%		4.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.50 V, L = 1 μH, Light or Fast PFM/PWM	–2%		4.0%	
V_O	Output voltage DC accuracy	TPS62352	V_I = 3.6 V, V_O = 1.20 V, $I_{O(DC)}$ = 0 mA PWM operation	–1.5%		1.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 0.75 V, 1.05 V, 1.20 V, 1.4375 V PWM operation	–2%		2%	
			2.7 V ≤ V_I ≤ 5.5 V, $I_{O(DC)}$ = 0 mA V_O = 1.05 V, L = 1 μH, Light PFM	–1%		4.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.20 V, L = 1 μH, Fast PFM/PWM	–2%		3%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.05 V, L = 1 μH, Light or Fast PFM/PWM	–2%		4.5%	

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply with V_I = 3.6 V, EN = V_I, VSEL = V_I, SYNC = GND, VSEL0[6] bit = 1.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage DC accuracy	TPS62353	V_I = 3.6 V, V_O = 1.20 V, $I_{O(DC)}$ = 0 mA PWM operation	–1.5%		1.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 0.75 V, 1.00 V, 1.20 V, 1.5375 V PWM operation	–2%		2%	
			2.7 V ≤ V_I ≤ 5.5 V, $I_{O(DC)}$ = 0 mA, V_O = 1.00 V, L = 1 μH, Light PFM	–1%		4.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.20 V, L = 1 μH, Fast PFM/PWM	–2%		3%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.00 V, L = 1 μH, Light or Fast PFM/PWM	–2%		4.5%	
V_O	Output voltage DC accuracy	TPS62354	V_I = 3.6 V, V_O = 1.30 V, $I_{O(DC)}$ = 0 mA, PWM operation	–1.5%		1.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 0.75 V, 1.05 V, 1.30 V, 1.5375 V PWM operation	–2%		2%	
			2.7 V ≤ V_I ≤ 5.5 V, $I_{O(DC)}$ = 0 mA, V_O = 1.05 V, L = 1 μH, Light PFM	–1%		4.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.30 V, L = 1 μH, Fast PFM/PWM	–2%		3%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.05 V, L = 1 μH, Light or Fast PFM/PWM	–2%		4.5%	
V_O	Output voltage DC accuracy	TPS62355	V_I = 3.6 V, V_O = 1.15 V, $I_{O(DC)}$ = 0 mA, PWM operation	–1.5%		1.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 0.75 V, 0.9 V, 1.15 V, 1.5375 V PWM operation	–2%		2%	
			2.7 V ≤ V_I ≤ 5.5 V, $I_{O(DC)}$ = 0 mA V_O = 0.9 V, L = 1 μH, Light PFM	–1%		4.5%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 1.15 V, L = 1 μH, Fast PFM/PWM	–2%		3%	
			2.7 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 0.9 V, L = 1 μH, Light or Fast PFM/PWM	–2%		4.5%	
V_O	Output voltage DC accuracy	TPS62356	2.7 V ≤ V_I ≤ 3.2 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA 3.2 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 1000 mA(1) V_O = 1.80 V PWM operation	–2%		2%	
			2.7 V ≤ V_I ≤ 5.5 V, $I_{O(DC)}$ = 0 mA V_O = 1.80 V, L = 1 μH, Light PFM	–1%		4.5%	
			2.7 V ≤ V_I ≤ 3.2 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA 3.2 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 1000 mA(1) V_O = 1.80 V, L = 1 μH, Fast PFM/PWM	–2%		3%	
			2.7 V ≤ V_I ≤ 3.2 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA 3.2 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 1000 mA(1) V_O = 1.80 V, L = 1 μH, Light or Fast PFM/PWM	–2%		4.5%	
ΔV_O	DC output voltage load regulation		$I_{O(DC)}$ = 0 mA to 800 mA, PWM operation		–0.0003		%/mA
	DC output voltage line regulation		V_I = V_O + 0.5 V (min 2.7 V) to 5.5 V, $I_{O(DC)}$ = 300 mA		0		%/V
	Power-save mode ripple voltage		V_O = 0.9 V, $I_{O(DC)}$ = 0 mA, L = 1 μH, Light PFM operation		33		mV_{PP}
			V_O = 1.05 V, $I_{O(DC)}$ = 1 mA , L = 1 μH, Light PFM operation		30		mV_{PP}
			V_O = 1.10 V, $I_{O(DC)}$ = 1 mA, L = 1 μH, Light PFM operation, VSEL0[6] bit = 0		12		mV_{PP}
			V_O = 1.35 V, $I_{O(DC)}$ = 1 mA, L = 1 μH, Fast PFM operation		0.025 V_O		V_{PP}

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(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply with V_I = 3.6 V, EN = V_I, VSEL = V_I, SYNC = GND, VSEL0[6] bit = 1.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{lkg}	Leakage current into SW pin		$V_I > V_O$, 0 V ≤ $V_{(SW)}$ ≤ V_I, EN = GND		0.01	1	µA
	Reverse leakage current into SW pin		V_I = open, $V_{(SW)}$ = 6 V, EN = GND		0.01	1	
DAC							
	Resolution	TPS62350 TPS62351 TPS62352 TPS62353 TPS62354 TPS62355 TPS62356		6			Bits
	Differential nonlinearity		Specified monotonic by design			±0.8	LSB
TIMING							
	Setup Time Between Rising EN and Start of I²C Stream			250			µs
V_O	Output voltage settling time	TPS62350	From min to max output voltage, $I_{O(DC)}$ = 500 mA, PWM operation		3		µs
	Start-up time	TPS62350	Time from active EN to V_O V_O = 1.35 V, R_L = 5Ω, PWM operation		180		µs
			Time from active EN to V_O V_O = 1.05 V, $I_{O(DC)}$ = 0 mA, Light PFM operation		170		
		TPS62351	Time from active EN_DCDC bit to V_O V_O = 1.5 V, R_L = 5Ω, PWM operation		45		
		TPS62352	Time from active EN to V_O V_O = 1.2 V, R_L = 5Ω, PWM operation		175		
			Time from active EN to V_O V_O = 1.05 V, $I_{O(DC)}$ = 0 mA, Light PFM operation		170		

I²C INTERFACE TIMING CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL Clock Frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		High-speed mode (write operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (read operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (write operation), C_B – 400 pF max		1.7	MHz
		High-speed mode (read operation), C_B – 400 pF max		1.7	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard mode	4.7		µs
		Fast mode	1.3		µs
t_{HD}, t_{STA}	Hold Time (Repeated) START Condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{LOW}	LOW Period of the SCL Clock	Standard mode	4.7		µs
		Fast mode	1.3		µs
		High-speed mode, C_B – 100 pF max	160		ns
		High-speed mode, C_B – 400 pF max	320		ns
t_{HIGH}	HIGH Period of the SCL Clock	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode, C_B – 100 pF max	60		ns
		High-speed mode, C_B – 400 pF max	120		ns

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(1) Specified by design. Not tested in production.

I^{2}C INTERFACE TIMING CHARACTERISTICS (continued)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{SU}, t_{DAT}	Data Setup Time	Standard mode	250		ns
		Fast mode	100		ns
		High-speed mode	10		ns
t_{HD}, t_{DAT}	Data Hold Time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		High-speed mode, C_B – 100 pF max	0	70	ns
		High-speed mode, C_B – 400 pF max	0	150	ns
t_{RCL}	Rise Time of SCL Signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	40	ns
		High-speed mode, C_B – 400 pF max	20	80	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{FCL}	Fall Time of SCL Signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	40	ns
		High-speed mode, C_B – 400 pF max	20	80	ns
t_{RDA}	Rise Time of SDA Signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{FDA}	Fall Time of SDA Signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{SU}, t_{STO}	Setup Time for STOP Condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
C_B	Capacitive Load for SDA and SCL			400	pF

I^2C TIMING DIAGRAMS

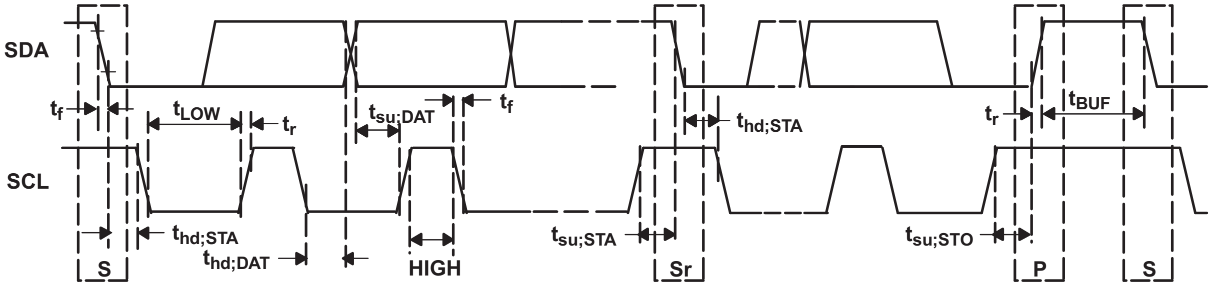
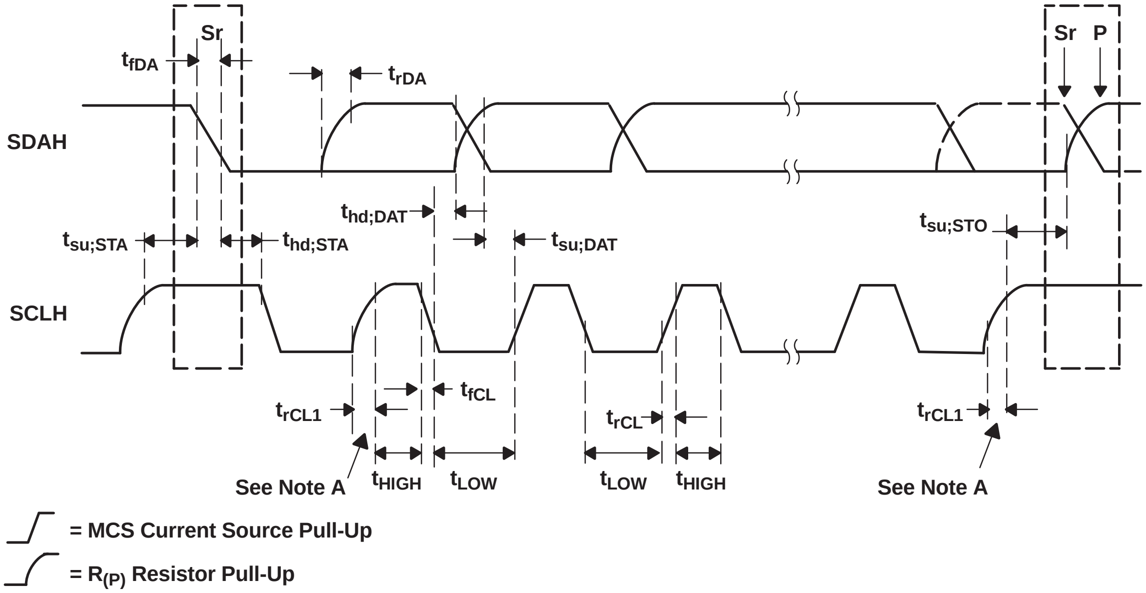


Figure 1. Serial Interface Timing Diagram for F/S-Mode

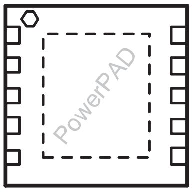


Note A: First rising edge of the SCLH signal after Sr and after each acknowledge bit.

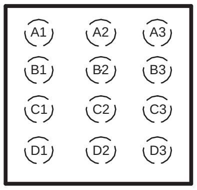
Figure 2. Serial Interface Timing Diagram for HS-Mode

PIN ASSIGNMENTS

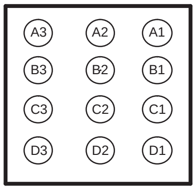
TPS6235x
QFN−10
(TOP VIEW)



TPS6235x
CSP−12
(TOP VIEW)



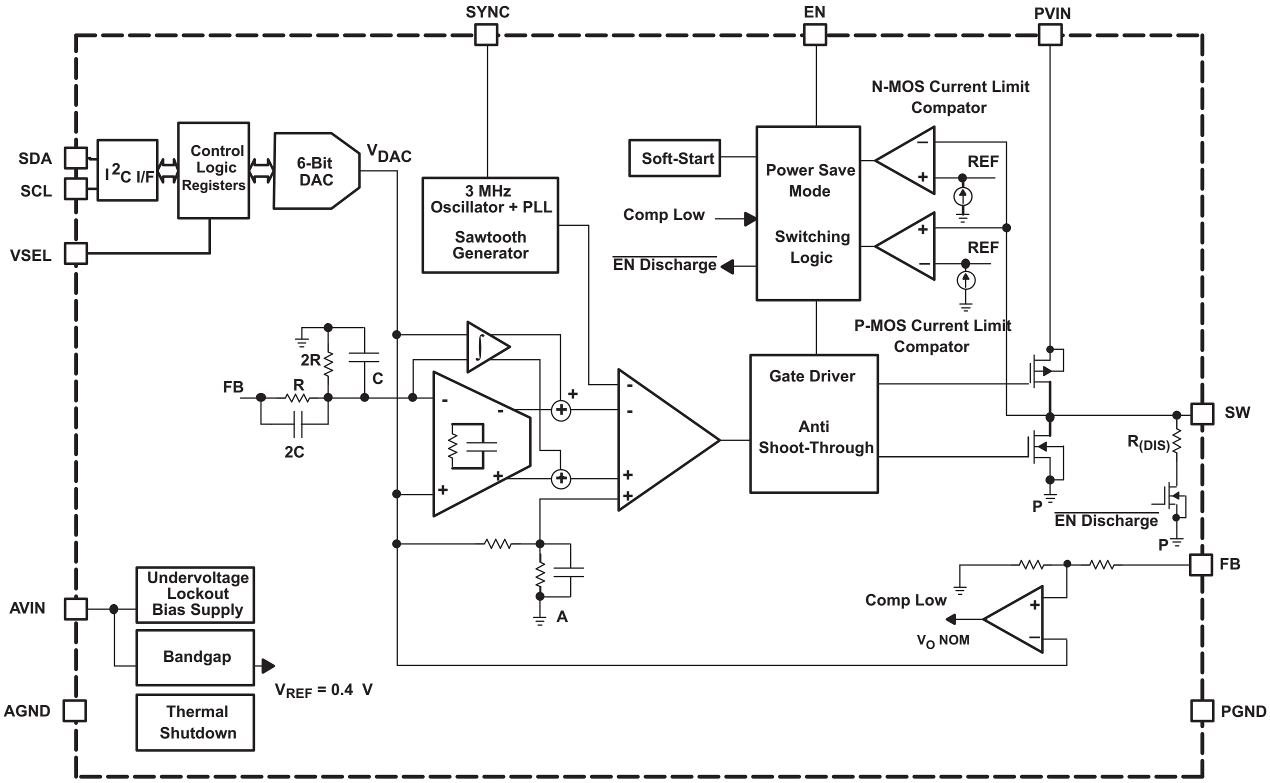
TPS6235x
CSP−12
(BOTTOM VIEW)



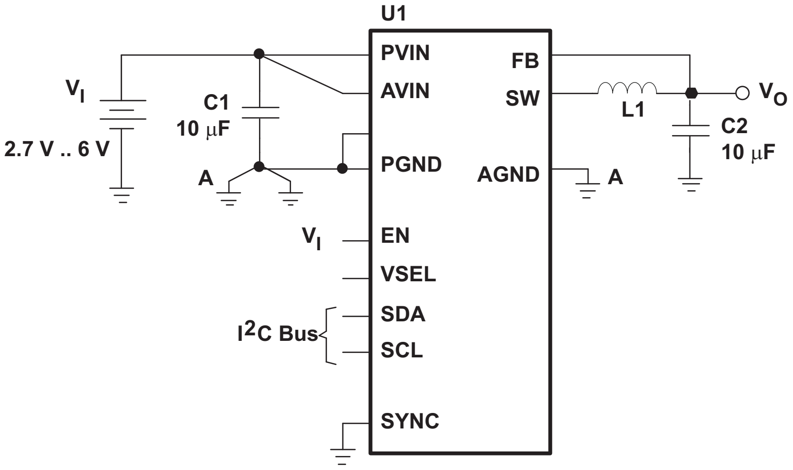
TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NO. QFN	NO. CSP		
PVIN	1	A3		Supply voltage for output power stage.
AVIN	2	B3		This is the input voltage pin of the device. Connect directly to the input bypass capacitor.
EN	7	C2	I	This is the enable pin of the device. Connect this pin to ground forces the device into shutdown mode. Pulling this pin to V_I enables the device. On the rising edge of the enable pin, all the registers are reset with their default values. This pin must not be left floating and must be terminated.
VSEL	5	D2	I	VSEL signal is primarily used to scale the output voltage and to set the TPS6235x operation between active mode (VSEL=HIGH) and sleep mode (VSEL=LOW). The mode of operation can also be adapted by I^2C settings. This pin must not be left floating and must be terminated.
SDA	3	C3	I/O	Serial interface address/data line
SCL	4	D3	I	Serial interface clock line
FB	6	D1	I	Output feedback sense input. Connect FB to the converter output.
AGND	8	C1		Analog ground
SYNC	N/A	B2	I	Input for synchronization to external clock signal. Synchronizes the converter switching frequency to an external clock signal. This pin must not be left floating and must be terminated. Connecting SYNC to static high or low state has no effect on the converter operation.
PGND	9	A1 B1		Power ground. Connect to AGND underneath IC.
SW	10	A2	I/O	This is the switch pin of the converter and connected to the drain of the internal power MOSFETs.
PowerPAD™			N/A	Internally connected to PGND.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



List of Components:
U1 = TPS6235x
L1 = FDK MIPSA2520 Series
C1, C2 = TDK C1608X5R0G106MT

Note: The internal registers are set to their default values.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Output current	3, 4, 5, 6
		vs Input voltage	7
V_O	DC output voltage	vs Output current	8, 9, 12
		vs Input voltage	10, 11
		vs Ambient temperature	13
	Measured output voltage	vs DAC target output voltage	14
I_Q	Quiescent current	vs Input voltage	15
I_{SD}	Shutdown current	vs Input voltage	16
$f_{(OSC)}$	Oscillator frequency	vs Input voltage	17
$r_{DS(on)}$	P-channel MOSFET $r_{DS(on)}$	vs Input voltage	18
	N-channel MOSFET $r_{DS(on)}$	vs Input voltage	19
I_P	Inductor peak current	vs Ambient temperature	20
	Load transient response		21, 22, 23, 24, 25, 26 27, 28, 29, 30, 31, 32
	Line transient response		33
	Combined line and load transient response		34
	PWM operation		35
	Duty cycle jitter		36
	Power-save mode operation		37, 38
	Dynamic voltage management		39, 40
	Output voltage ramp control		41
	Start-up		42, 43

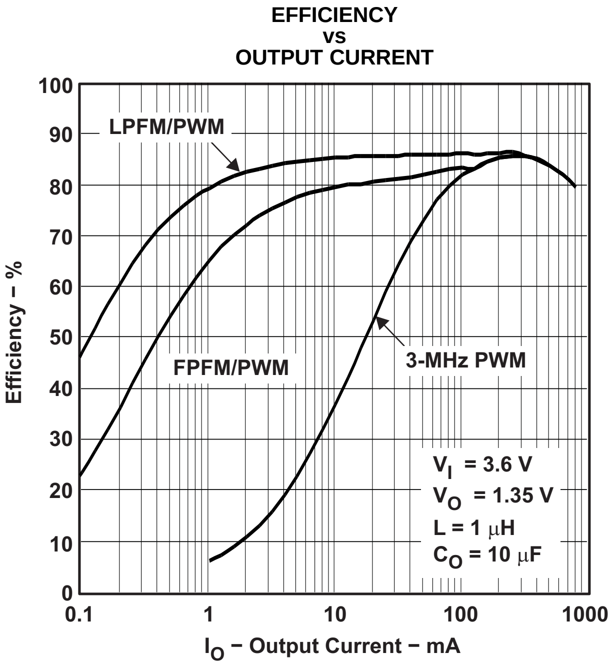


Figure 3.

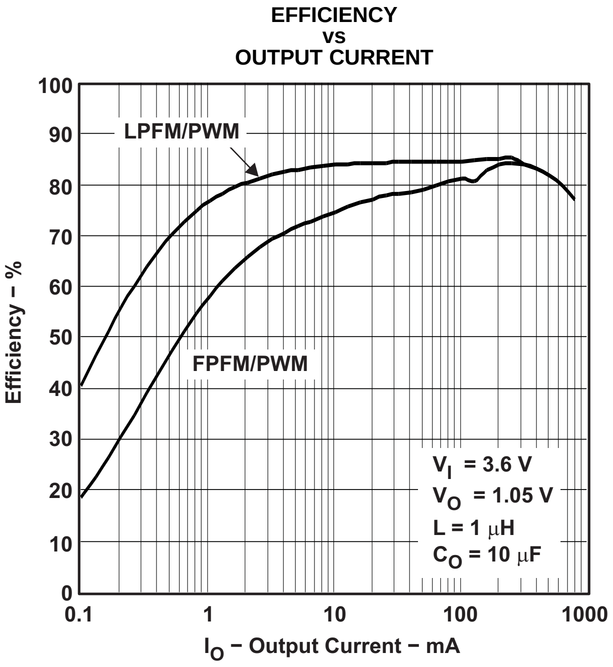


Figure 4.

EFFICIENCY
vs
OUTPUT CURRENT

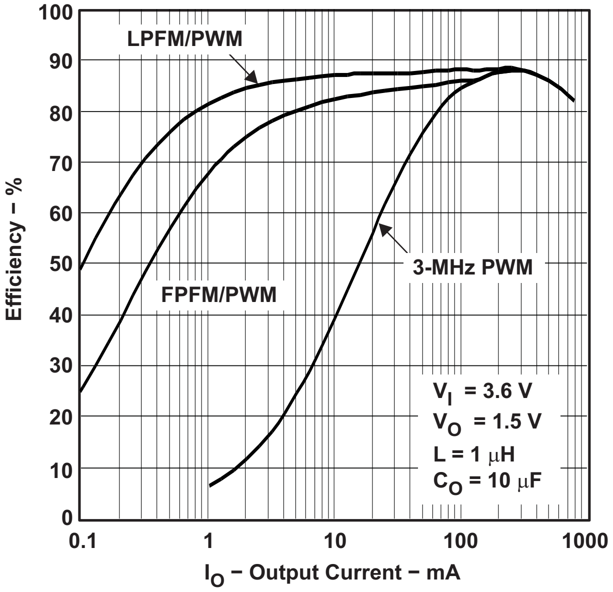


Figure 5.

EFFICIENCY
vs
OUTPUT CURRENT

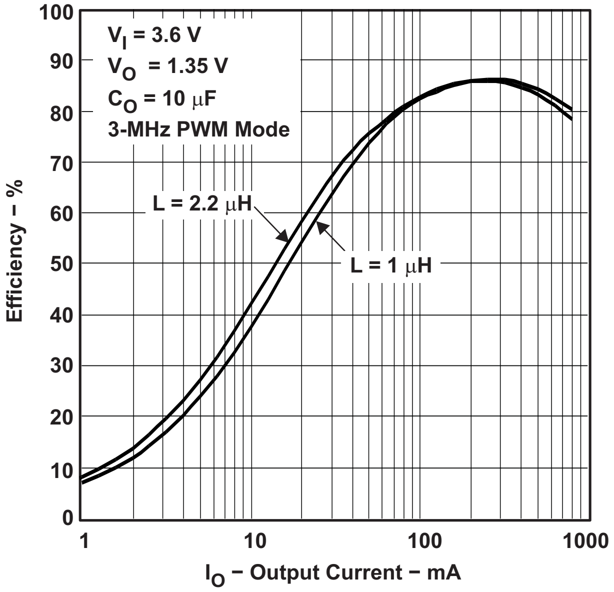


Figure 6.

EFFICIENCY
vs
INPUT VOLTAGE

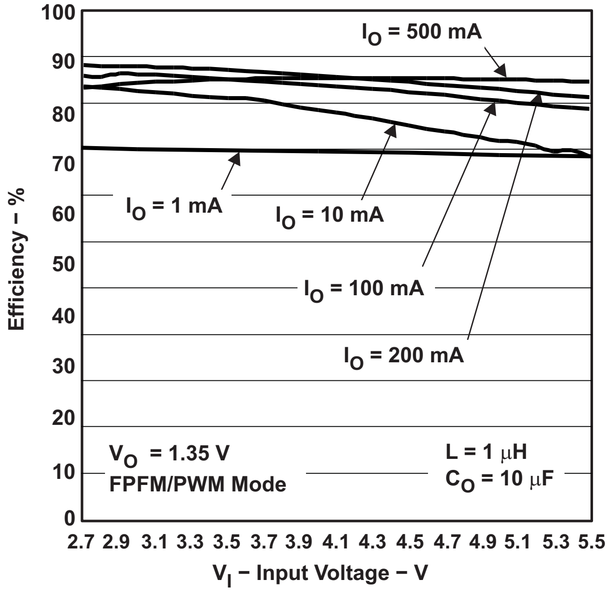


Figure 7.

DC OUTPUT VOLTAGE
vs
OUTPUT CURRENT

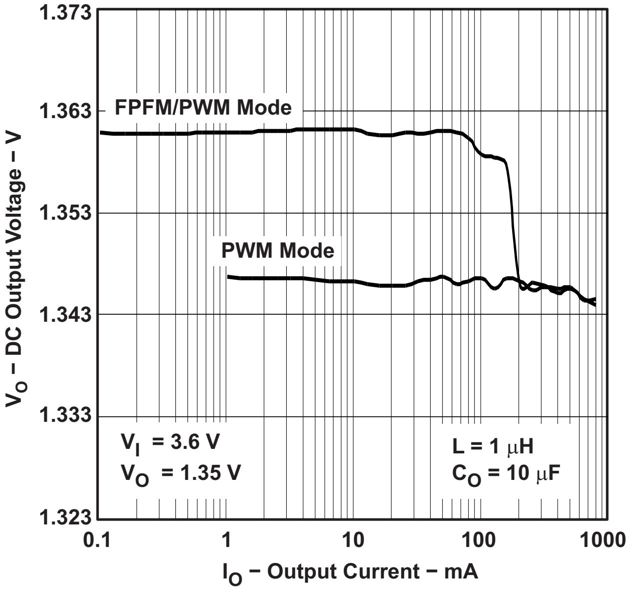


Figure 8.

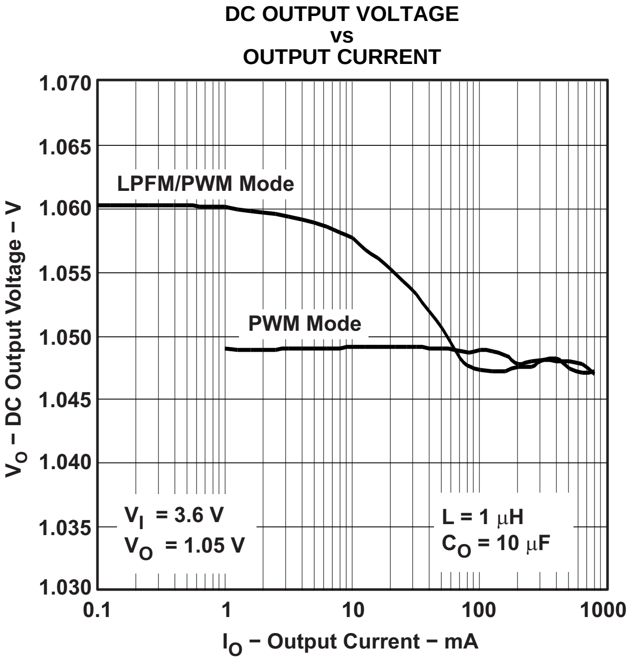


Figure 9.

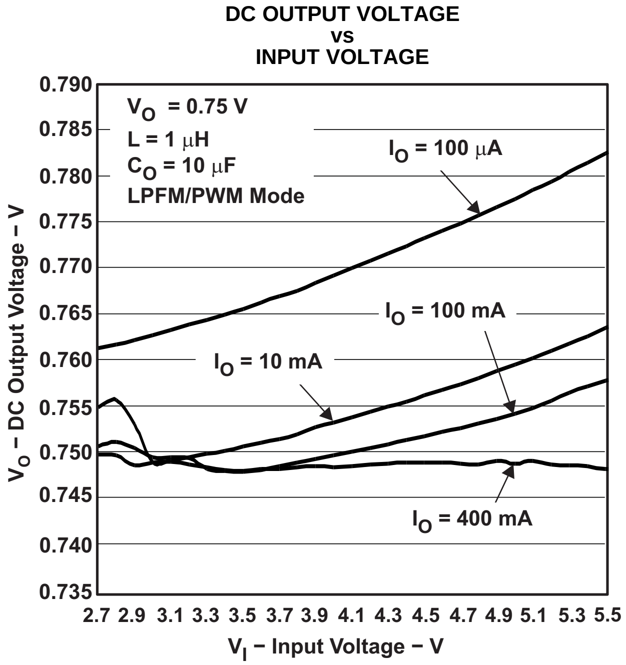


Figure 10.

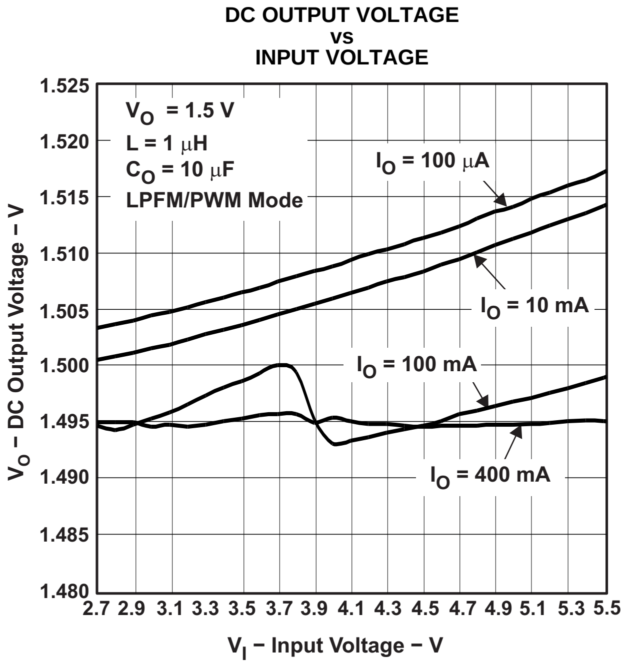


Figure 11.

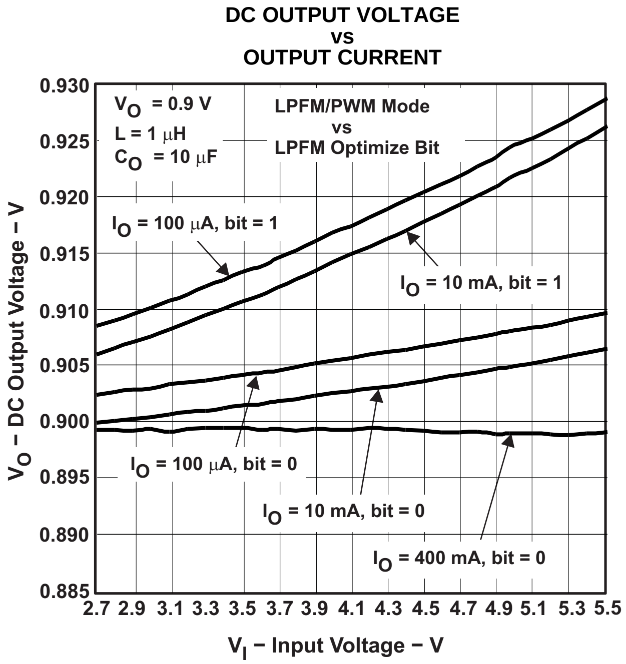


Figure 12.

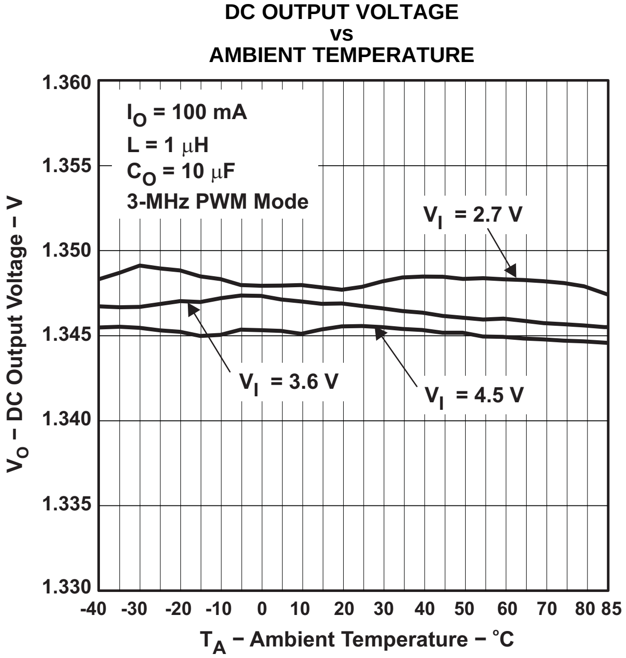


Figure 13.

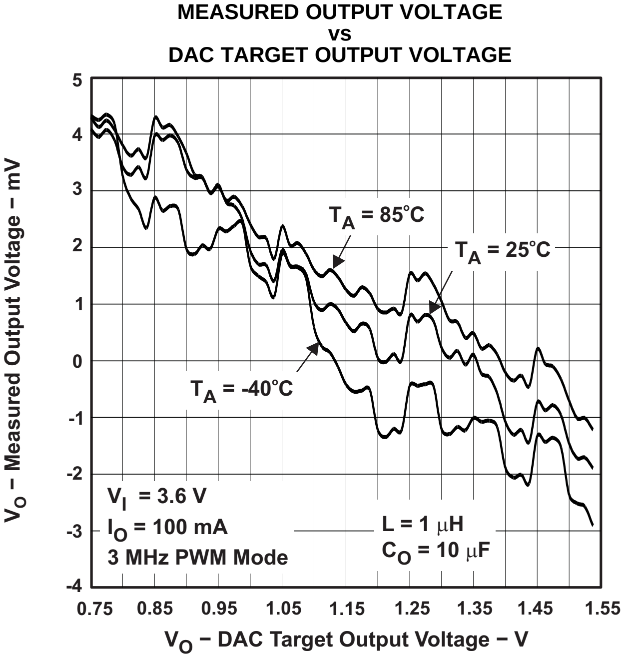


Figure 14.

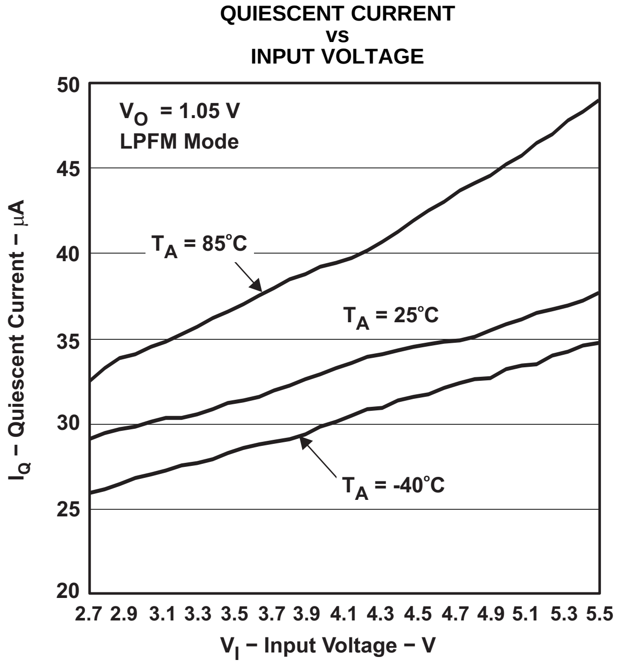


Figure 15.

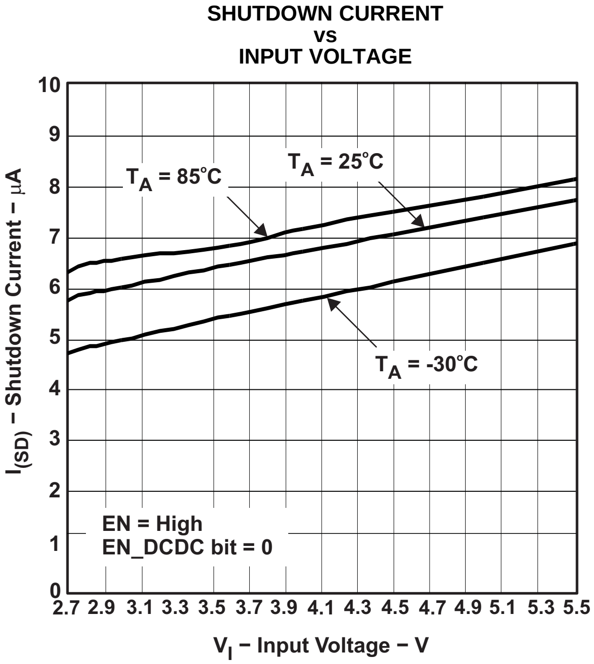


Figure 16.

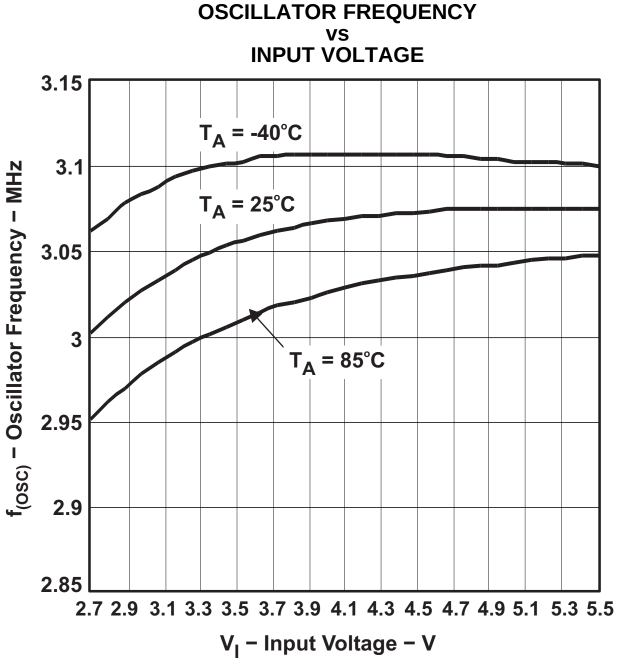


Figure 17.

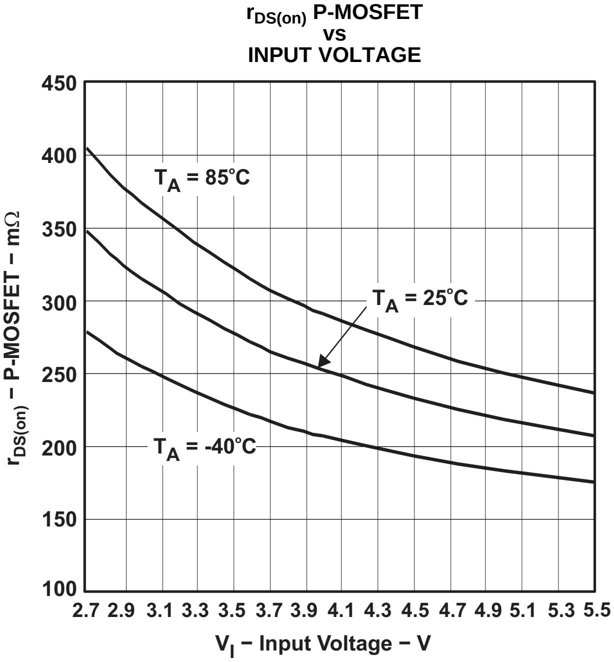


Figure 18.

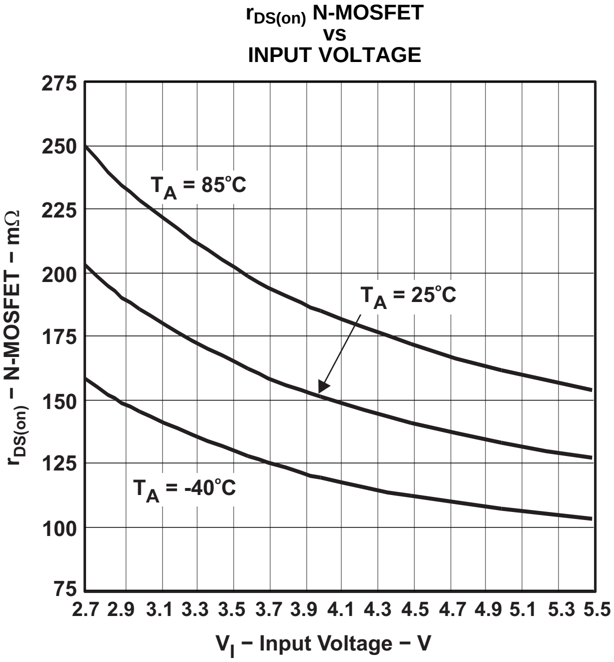


Figure 19.

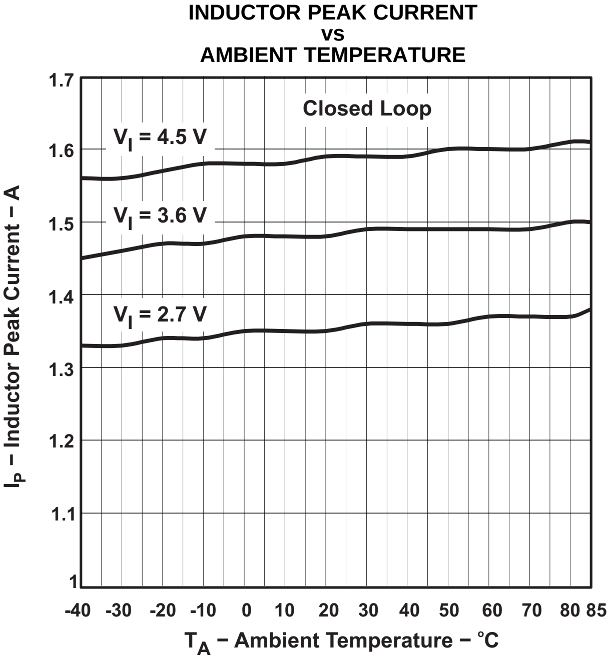


Figure 20.

LOAD TRANSIENT: 50 mA / 400 mA / 50 mA
PWM OPERATION

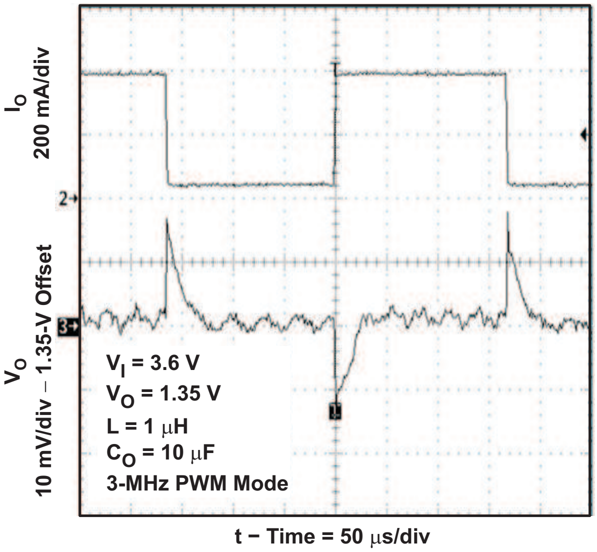


Figure 21.

LOAD TRANSIENT: 50 mA / 400 mA
PWM OPERATION

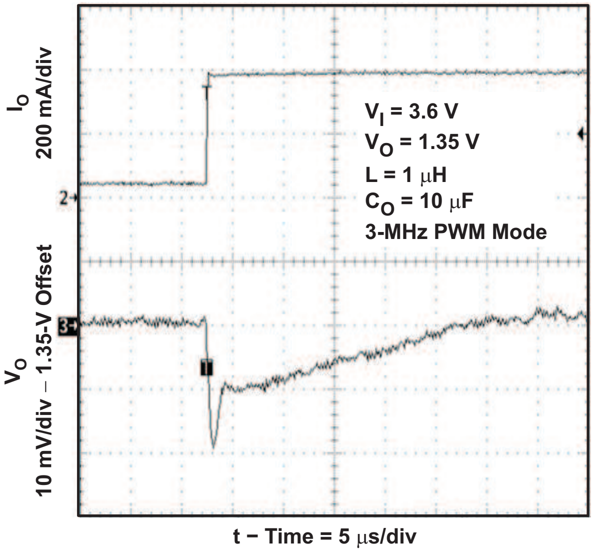


Figure 22.

LOAD TRANSIENT: 400 mA / 50 mA
PWM OPERATION

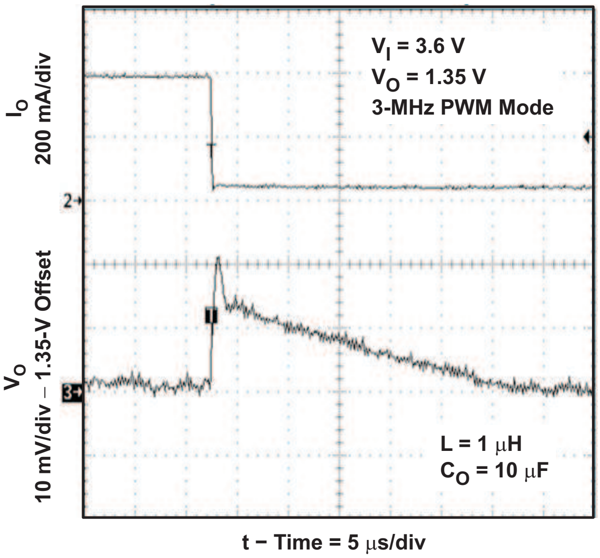


Figure 23.

LOAD TRANSIENT: 50 mA / 400 mA / 50 mA
FPFM/PWM OPERATION

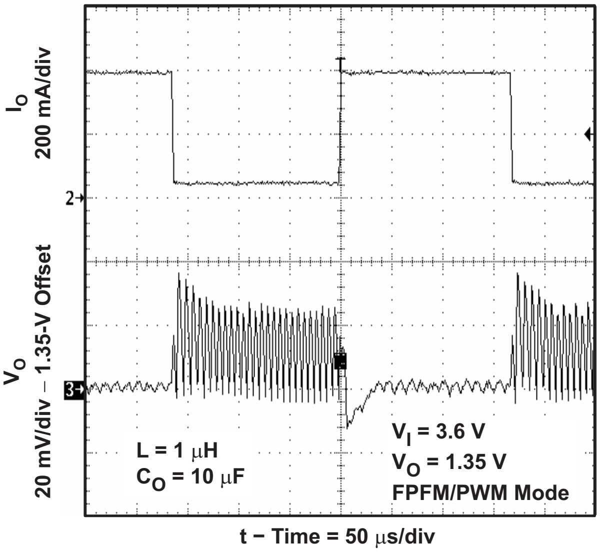


Figure 24.

LOAD TRANSIENT: 50 mA / 400 mA
FPFM/PWM OPERATION

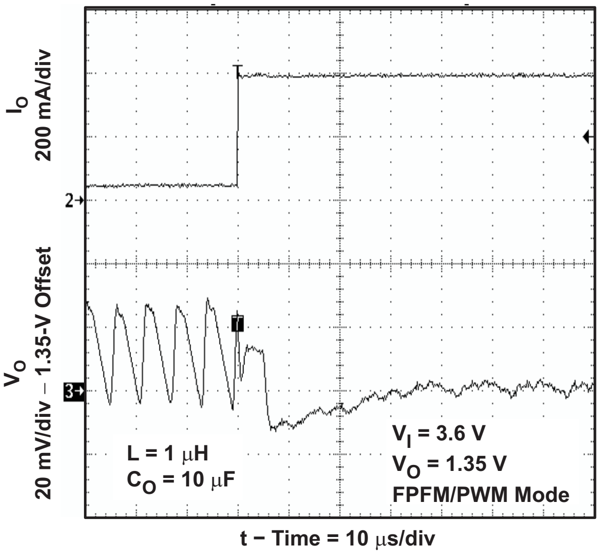


Figure 25.

LOAD TRANSIENT: 400 mA / 50 mA
FPFM/PWM OPERATION

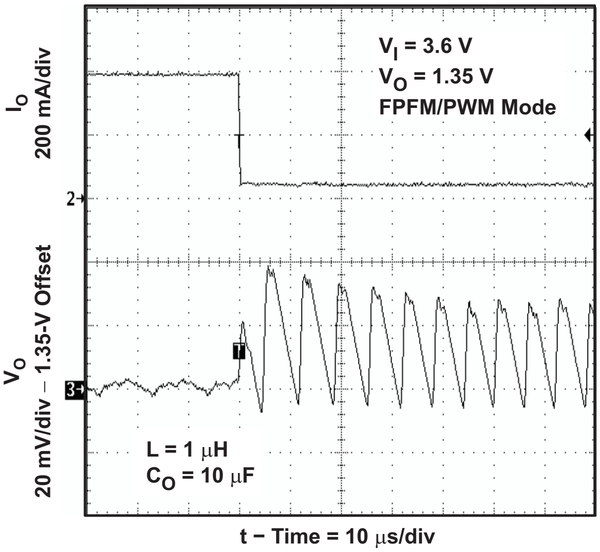


Figure 26.

LOAD TRANSIENT: 400 mA / 750 mA / 400 mA
PWM OPERATION

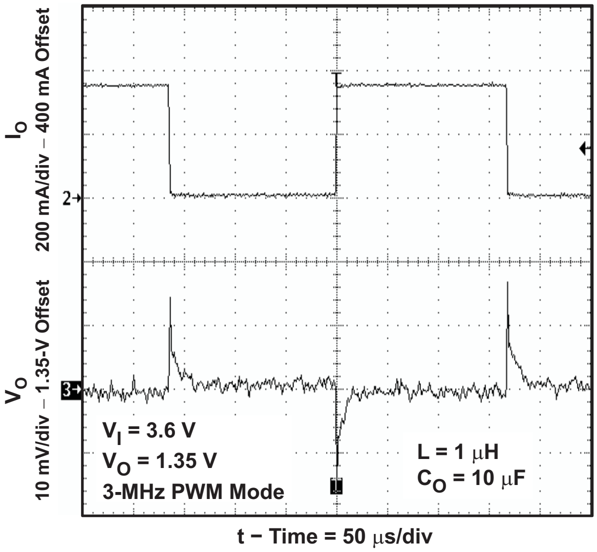


Figure 27.

LOAD TRANSIENT: 400 mA / 750 mA
PWM OPERATION

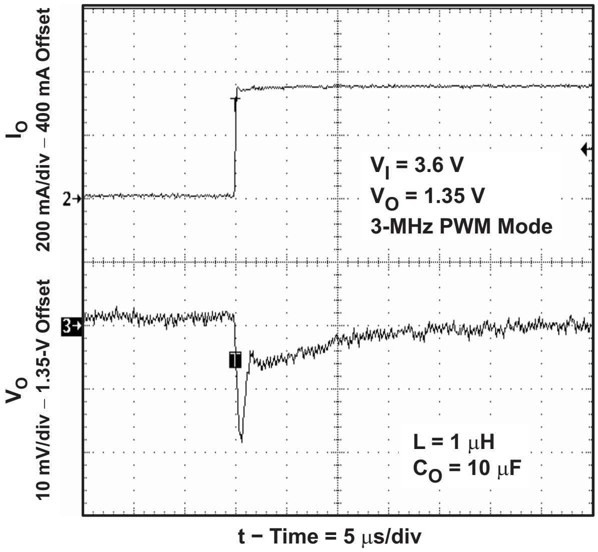


Figure 28.

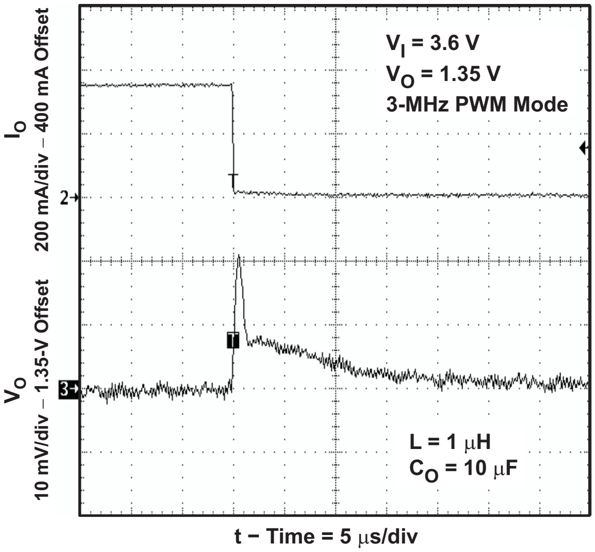

LOAD TRANSIENT: 750 mA / 400 mA
PWM OPERATION

Figure 29.

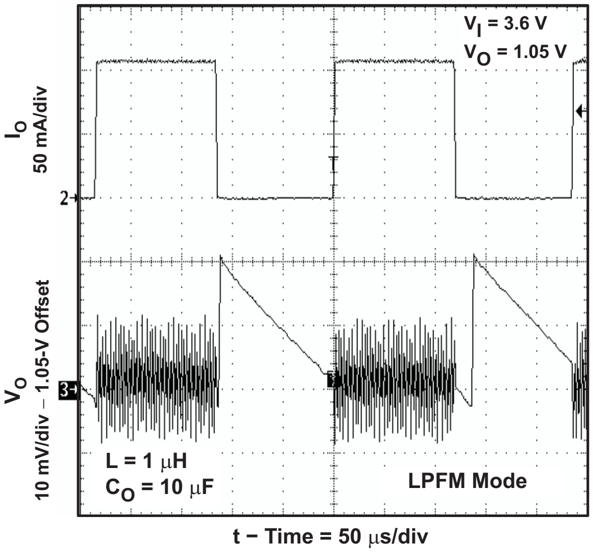

LOAD TRANSIENT: 1 mA / 100 mA / 1 mA
LFPM/PWM OPERATION

Figure 30.

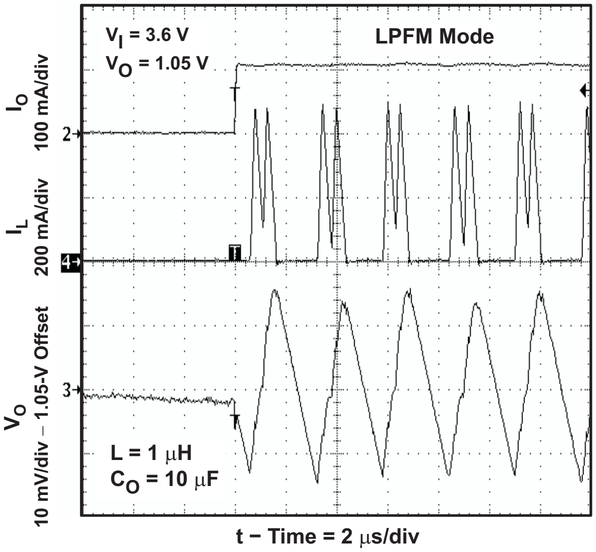

LOAD TRANSIENT: 1 mA / 100 mA
LPFM/PWM OPERATION

Figure 31.

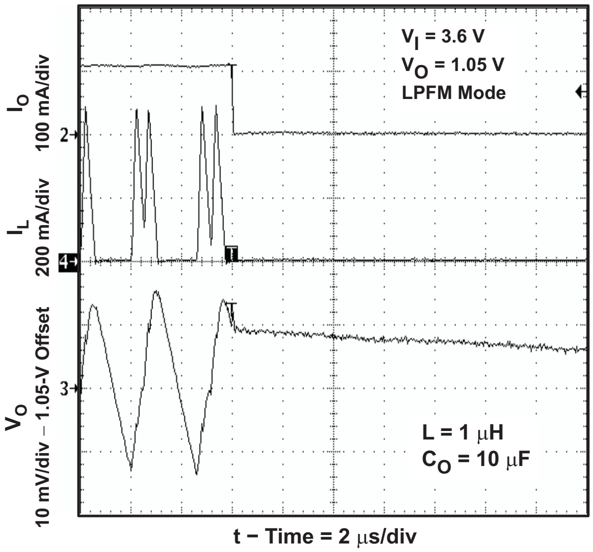

LOAD TRANSIENT: 100 mA / 1 mA
LPFM/PWM OPERATION

Figure 32.

LINE TRANSIENT
PWM OPERATION

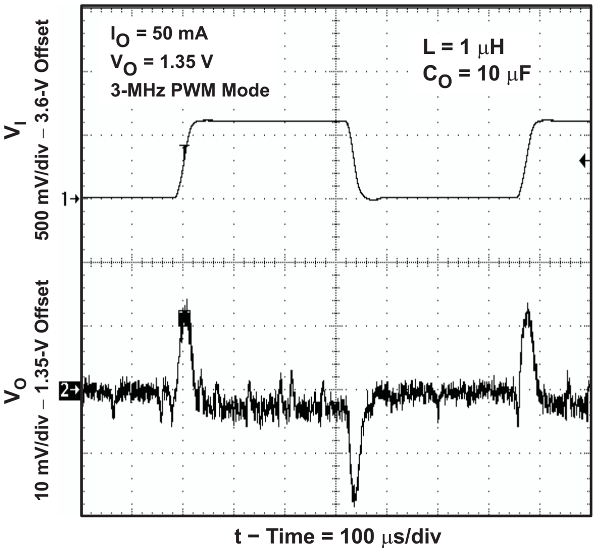


Figure 33.

COMBINED LINE/LOAD TRANSIENT
(3.6 V TO 4.2 V, 400 mA TO 800 mA)
PWM OPERATION

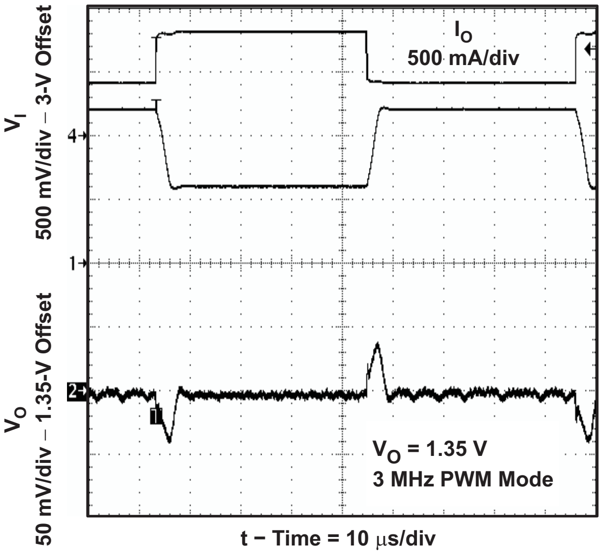


Figure 34.

PWM OPERATION

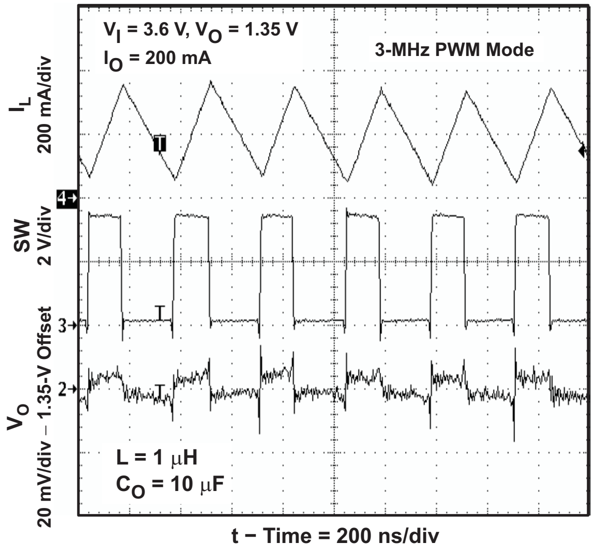


Figure 35.

DUTY CYCLE JITTER

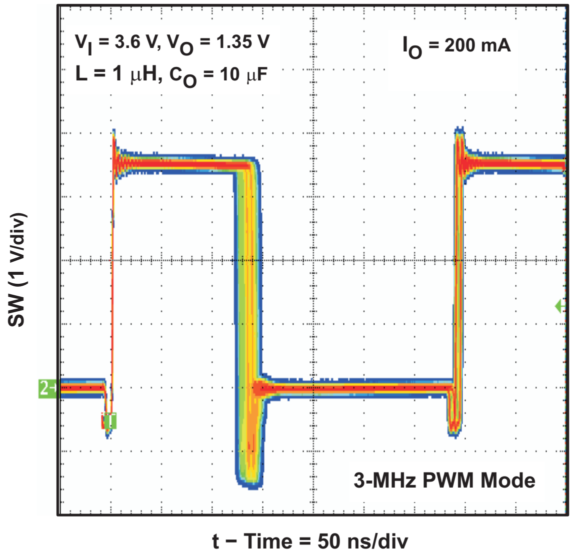


Figure 36.

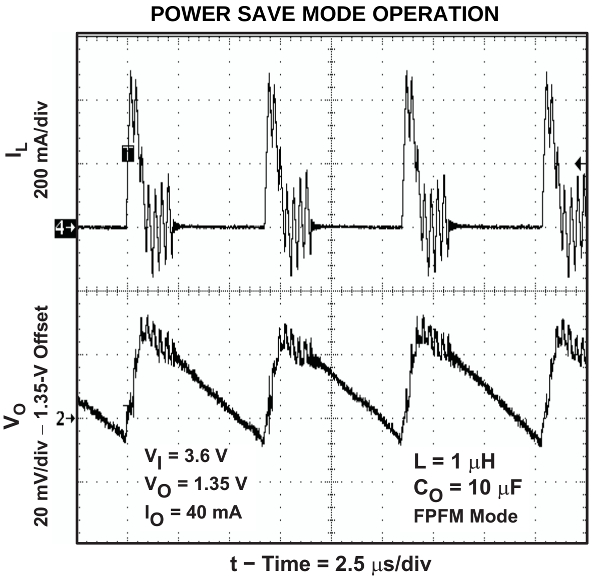

POWER SAVE MODE OPERATION

Figure 37.

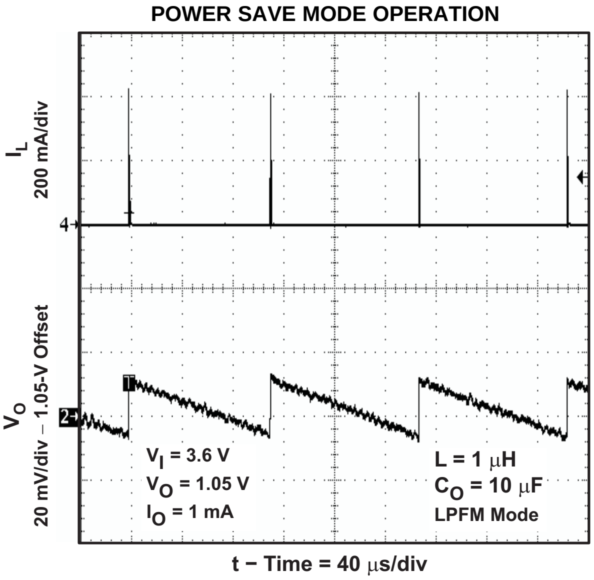

POWER SAVE MODE OPERATION

Figure 38.

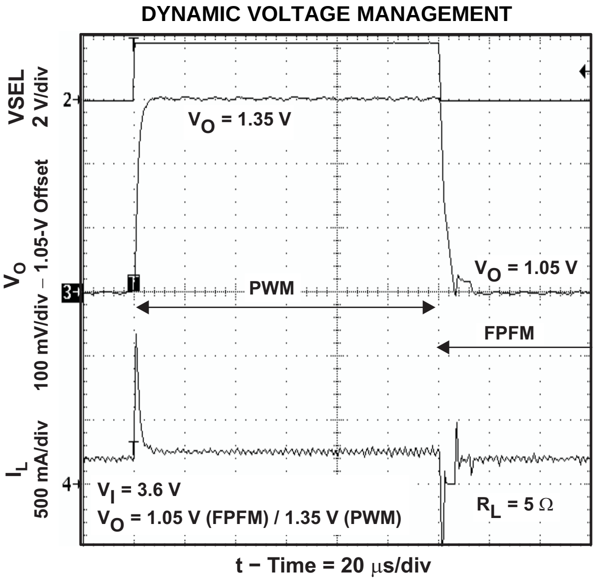

DYNAMIC VOLTAGE MANAGEMENT

Figure 39.

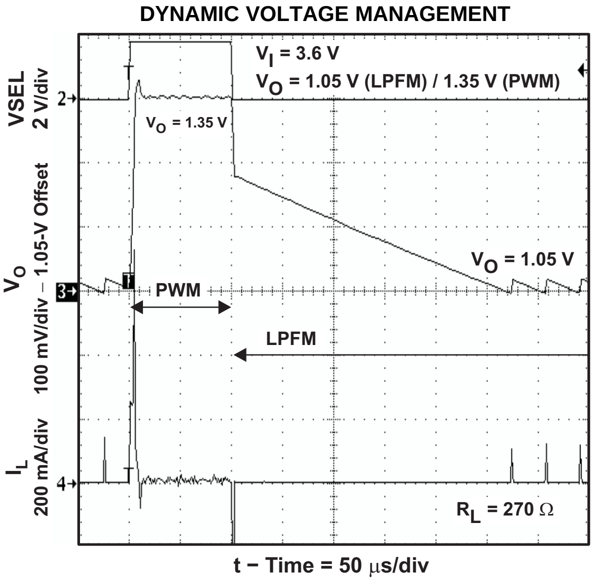

DYNAMIC VOLTAGE MANAGEMENT

Figure 40.

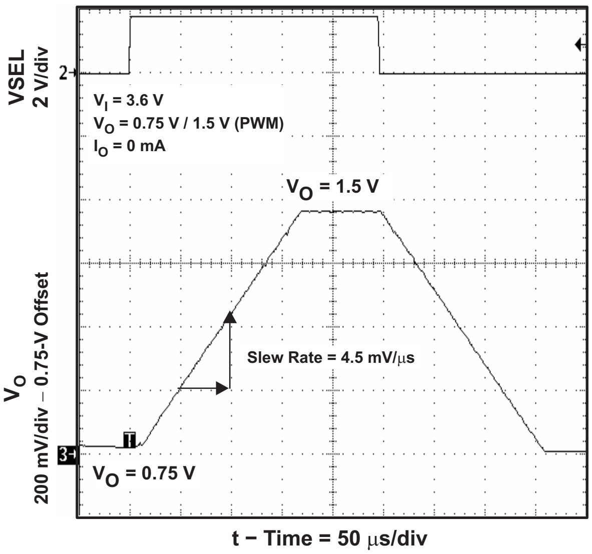

OUTPUT VOLTAGE RAMP CONTROL

Figure 41.

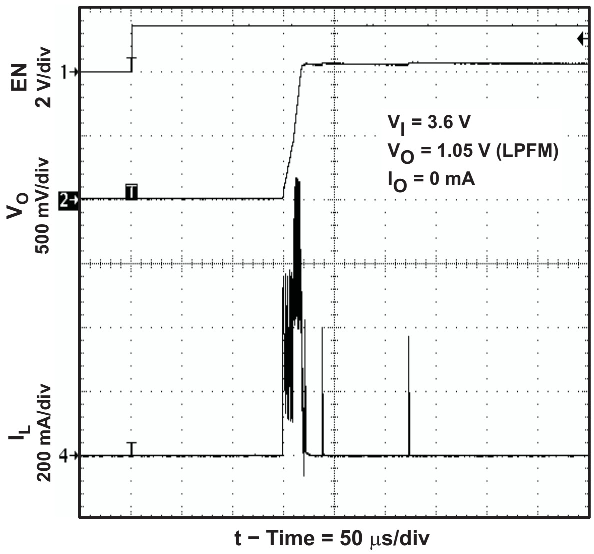

START UP

Figure 42.

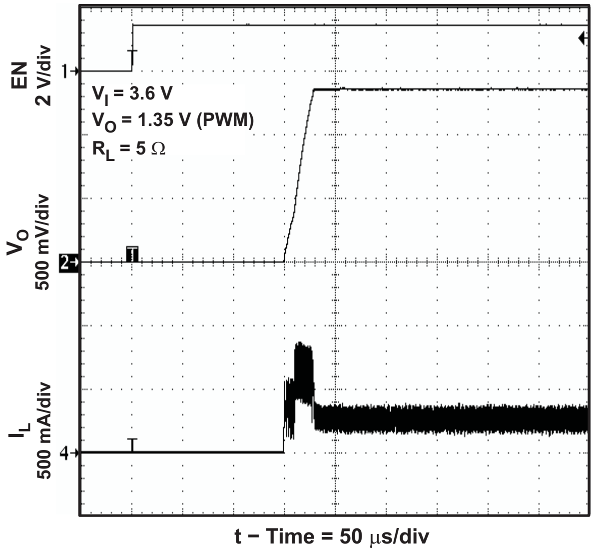

START UP

Figure 43.

DETAILED DESCRIPTION

Operation

The TPS6235x is a synchronous step-down converter typically operating with a 3-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter operates in power-save mode with pulse frequency modulation (PFM). The device integrates two power-save modes optimized either for ultra-high efficiency at light load (light PFM) or for transient response when turning in PWM operation (fast PFM). Both power-save modes automatically transition to PWM operation when the load current increases.

The TPS6235x integrates an I^{2}C compatible interface allowing transfers up to 3.4 Mbps. This communication interface can be used for dynamic voltage scaling with voltage steps down to 12.5 mV (or to 25 mV steps for TPS62356), for reprogramming the mode of operation (light PFM, fast PFM or forced PWM) or disable/enabling the output voltage for instance. For more details, see the I^{2}C interface and register description section.

During PWM operation, the converter uses a unique fast response, voltage mode, control scheme with input voltage feed-forward. This achieves *best-in-class* load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The operating frequency is set to 3 MHz and can be synchronized *on-the-fly* to an external oscillator or to a master dc/dc converter (refer to application examples).

The device integrates two current limits, one in the P-channel MOSFET and another one in the N-channel MOSFET. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. When the current in the N-channel MOSFET is above the N-MOS current limit threshold, the N-channel MOSFET remains on until the current drops below its current limit. The current limit in the N-channel MOSFET is important for small duty-cycle operation when the current in the inductor does not decrease because of the P-channel MOSFET current limit delay, or because of start-up conditions where the output voltage is low.

Power-Save Mode : Fast PFM

With decreasing load current, the device automatically switches into pulse skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically, the switching losses are minimized, and the device runs with a minimum quiescent current and maintains high efficiency.

In fast PFM mode, the converter only operates when the output voltage trips below a set threshold voltage (V_O nominal). It ramps up the output voltage with several pulses and goes into power-save mode when the inductor current reaches zero. As a consequence in power-save mode the average output voltage is slightly higher than its nominal value in PWM mode. The fast PFM mode is optimized for fast response when transitioning between pulse skipping and PWM operation.

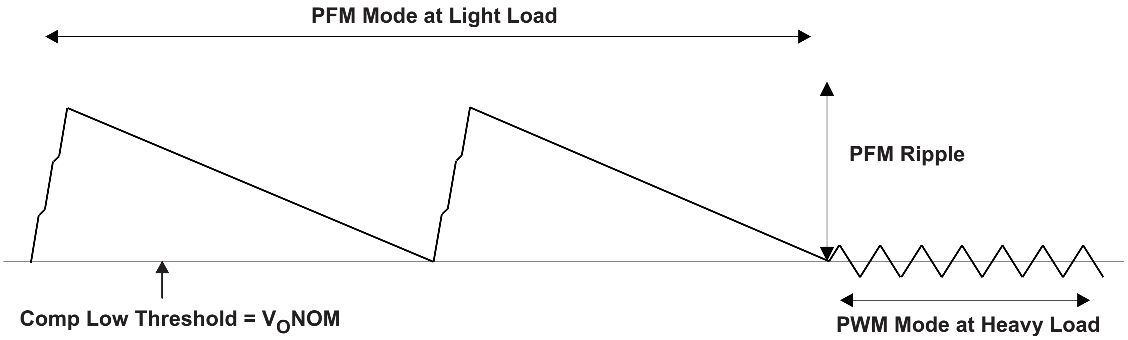


Figure 44. Operation in PFM Mode and Transfer to PWM Mode

Power-Save Mode : Light PFM

With decreasing load current, the device can also automatically switch into light PFM pulse skipping operation in which the power stage operates intermittently based on load demand. The advantage of the light PFM is much lower I_Q (28 µA) and drastically higher efficiency compared with fast PFM in low output loads.

In light PFM mode, the converter only operates when the output voltage trips below a set threshold voltage ($V_O$nominal). It ramps up the output voltage with one or several pulses and goes back into power-save mode. As a consequence in power-save mode the average output voltage is slightly higher than its nominal value in PWM mode.

In order to get a proper transition between light PFM and PWM operation, the output voltage ripple (in light PFM mode) has been made proportional to the input voltage. It is possible to reduce the output voltage ripple by setting the LIGHTPFM OPTIMIZE (VSEL0[6] or VSEL1[6]) bit low. However, this is only practical in applications operating with a 1-µH (typical) inductor, with a load current less than V_I / 25 Ω and which do not require the auto-mode transition function.

When operating with a 2.2-µH (typical) inductor, the LIGHTPFM OPTIMIZE (VSEL0[6] or VSEL1[6]) bit should always be set to low. In this case, the auto-mode transition is fully functional without any restriction on the load current.

Mode Selection and Frequency Synchronization

The TPS6235x can be synchronized to an external clock signal by the SYNC pin. Pulling the SYNC pin to a static state high or low state has no effect on the converter's operation.

Depending on the settings of CONTROL1 register the device can be operated in either the fixed frequency PWM mode or in the automatic PWM and power-save mode. In this mode, the converter operates in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range. For more details, see the *CONTROL1* register description.

The fixed frequency PWM mode has the tightest regulation and the best line/load transient performance. Furthermore, this mode of operation allows simple filtering of the switching frequency for noise-sensitive applications. In fixed frequency PWM mode, the efficiency is lower compared to the power-save mode during light loads. It is possible to switch from power-save mode (light or fast PWM) to forced PWM mode during operation either via the VSEL signal or by re-programming the CONTROL1 register. This allows adjustments to the converters operation to match the specific system requirements leading to more efficient and flexible power management.

When the synchronization is enabled (CONTROL2[5]=1), the mode is set to fixed-frequency operation and the P-channel MOSFET turn on is synchronized to the falling edge of the external clock. This creates the ability for multiple converters to be connected together in a master-slave configuration for frequency matching of the converters (see the application section for more details).

When CONTROL1[1:0]=00 and VSEL signal is low, the converter operates according to MODE0 bit and the synchronization is disabled regardless of EN_SYNC and HW_nSW bits.

Soft Start

The TPS6235x has an internal soft-start circuit that limits the inrush current during start-up. This prevents possible input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

In the TPS62350/1/2/3/4/5 devices, the soft start is implemented as a digital circuit increasing the switch current in steps of typically 350 mA, 675 mA, 1000 mA, and the typical switch current limit of 1350 mA. The current limit transitions to the next step every 256 clocks (≈ 88µs). To be able to switch from 675 mA to 1000 mA current limit step, the output voltage needs to be higher than 0.5 x $V_{O(NOM)}$ (otherwise the parts keeps operating at 675 mA current limit).

In the TPS62356 device, the soft start is implemented as a digital circuit increasing the switch current in steps of typically 400 mA, 775 mA, 1150 mA, and the typical switch current limit of 1550 mA. The current limit transitions to the next step every 256 clocks (≈ 88µs). To switch from 775 mA to 1150 mA current limit step, the output voltage needs to be higher than 0.5 x $V_{O(NOM)}$ (otherwise the parts keeps operating at 775 mA current limit).

This mechanism is used to limit the output current under short-circuit conditions. Therefore, the start-up time depends on the output capacitor and load current.

Enable

The device starts operation when EN pin is set high and starts up with the soft start. This signal is gated by the EN_DCDC bit defined in register VSEL0 and VSEL1. On rising edge of the EN pin, all the registers are reset with their default values. Enabling the converter's operation via the EN_DCDC bit does not affect internal register settings. This allows the output voltage to be programmed to other values than the default voltage before starting up the converter. For more details, see the *VSEL0/1* register description.

Pulling the EN pin, VSEL0[6] bit or VSEL1[6] bit low forces the device into shutdown, with a shutdown current as defined in the electrical characteristics table. In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off. When an output voltage is present during shutdown mode, which is caused by an external voltage source or super capacitor, the reverse leakage is specified under electrical characteristics. For proper operation, the EN pin must be terminated and must not be left floating.

In addition, depending on the setting of CONTROL2[6] bit, the device can actively discharge the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 15 Ω. The required time to discharge the output capacitor at V_O depends on load current and the output capacitance value.

Voltage and Mode Selection

The TPS6235x features a pin-selectable output voltage. VSEL is primarily used to scale the output voltage between active (VSEL=HIGH) and sleep mode (VSEL=LOW). For maximum flexibility, it is possible to reprogram the operating mode of the converter (e.g. fixed frequency PWM, fast PFM or light PFM) associated with VSEL signal via the I^2C interface

VSEL output voltage and mode selection is defined as following:

VSEL = LOW: DC/DC output voltage determined by VSEL0 register value. DC/DC mode of operation is determined by MODE0 bit in CONTROL1 register

VSEL = HIGH: DC/DC output voltage determined by VSEL1 register value. DC/DC mode of operation is determined by MODE1 bit in CONTROL1 register.

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

Short-Circuit Protection

As soon as the output voltage falls below 50% of the nominal output voltage, the converter current limit is reduced by 50% of the nominal value. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds 50% of the nominal output voltage. This needs to be considered when a load acting as a current sink is connected to the output of the converter.

Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C typical, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature falls below 130°C typical again.

THEORY OF OPERATION

Serial Interface Description

I^{2}C is a 2-wire serial interface developed by Philips Semiconductor (see I^{2}C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^{2}C compatible devices connect to the I^{2}C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS6235x device works as a slave and supports the following data transfer modes, as defined in the I^{2}C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (up to 3.4 Mbps in write mode). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.2 V (typical).

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as HS-mode. The TPS6235x device supports 7-bit addressing; 10-bit addressing and general call address are not supported.

The TPS6235x device has a 7-bit address with the 2 LSB bits factory programmable allowing up to four dc/dc converters to be connected to the same bus. The 5 MSBs are *10010*.

F/S-Mode Protocol

The *master* initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, see Figure 45. All I^{2}C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, see Figure 46. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge*, see Figure 47, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 45. This releases the bus and stops the communication link with the addressed slave. All I^{2}C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address

Attempting to read data from register addresses not listed in this section results in FFh being read out.

H/S-Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions are used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in FFh being read out.

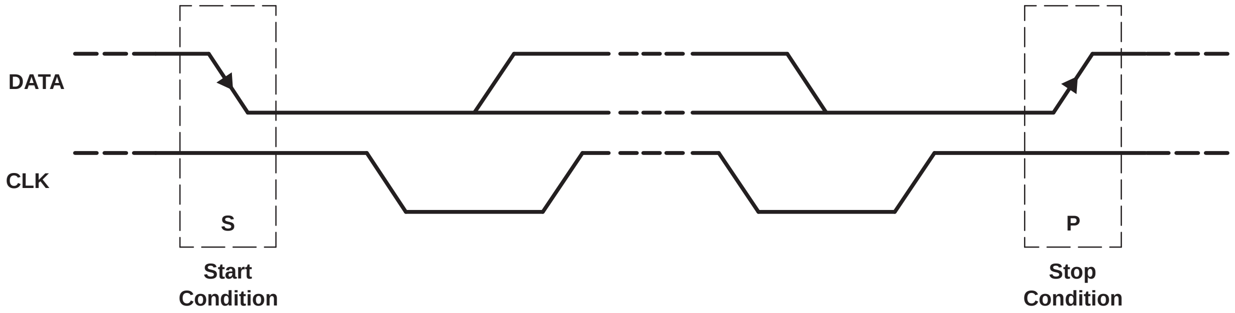


Figure 45. START and STOP Conditions

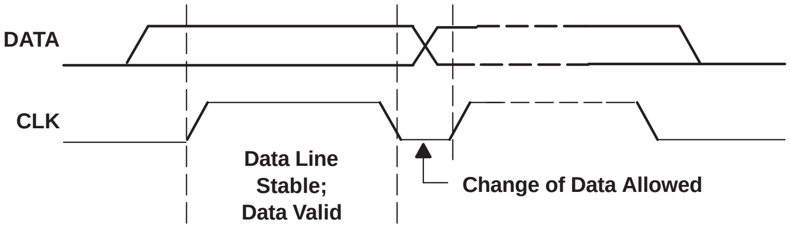


Figure 46. Bit Transfer on the Serial Interface

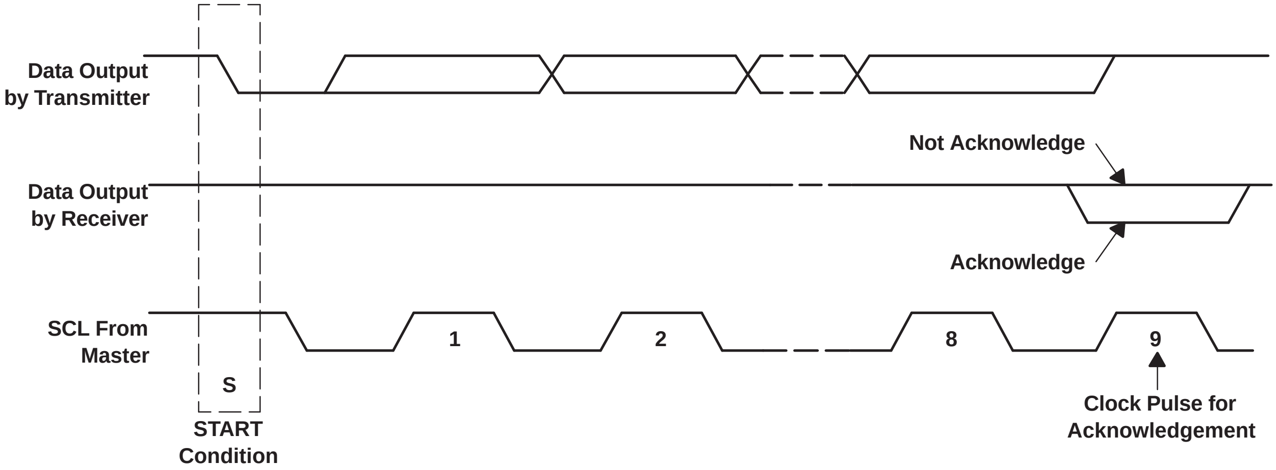


Figure 47. Acknowledge on the I^2C Bus

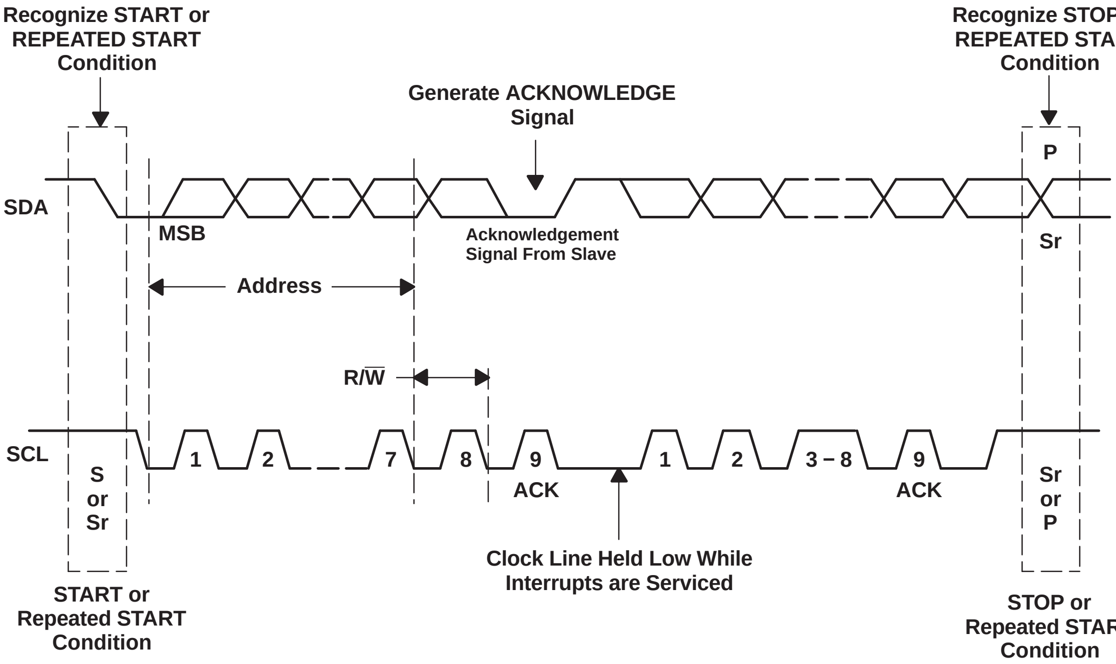


Figure 48. Bus Protocol

TPS6235x I^{2}C Update Sequence

The TPS6235x requires a start condition, a valid I^{2}C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS6235x device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^{2}C address selects the TPS6235x. TPS6235x performs an update on the falling edge of the LSB byte.

When the TPS6235x is in hardware shutdown (EN pin tied to ground) the device can not be updated via the I^{2}C interface. Conversely, the I^{2}C interface is fully functional during software shutdown (EN_DCDC bit=0).

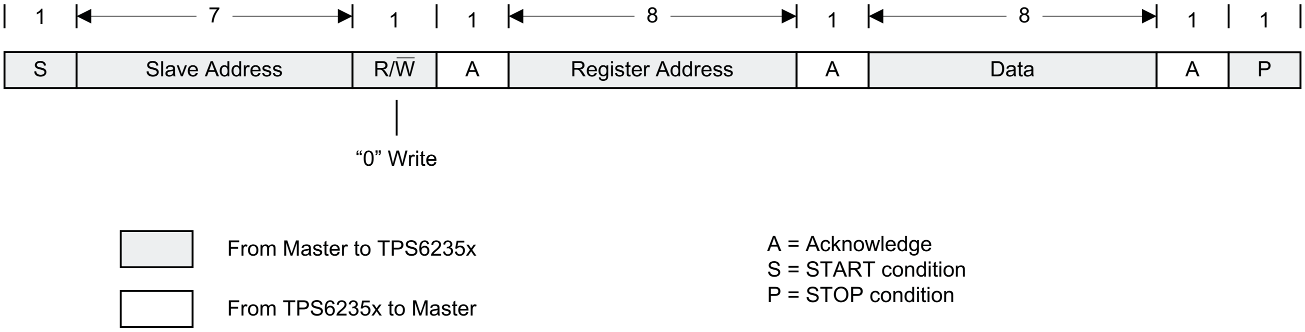


Figure 49. "Write" Data Transfer Format in F/S-Mode

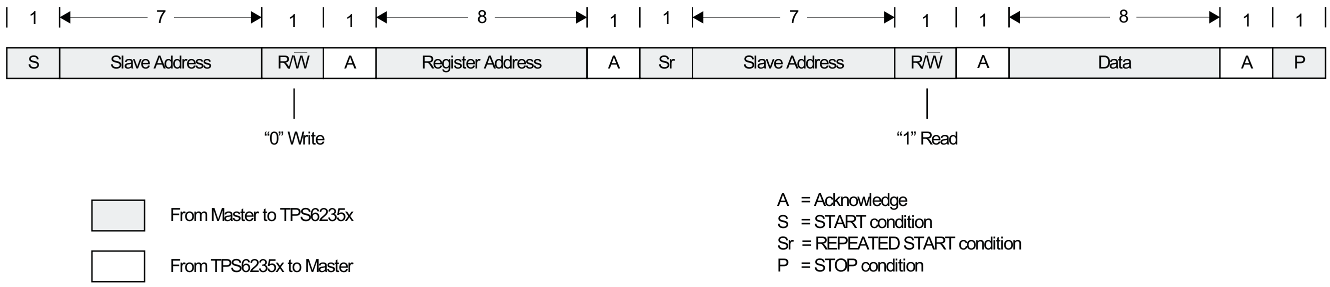


Figure 50. "Read" Data Transfer Format in F/S-Mode

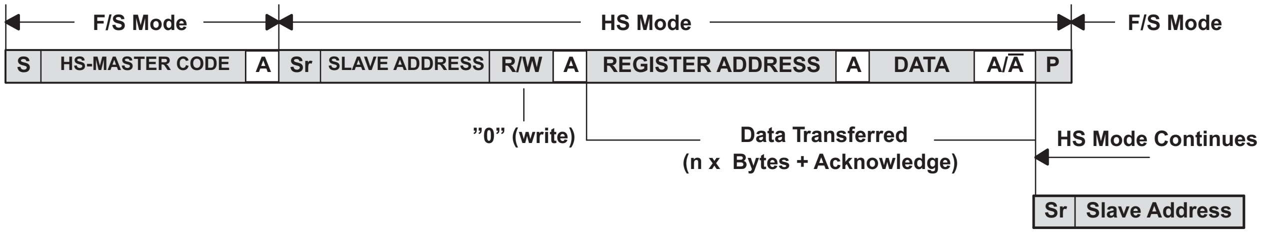


Figure 51. Data Transfer Format in H/S-Mode

Slave Address Byte

MSB							LSB
X	1	0	0	1	0	A1	A0

The slave address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the address are factory preset to 10010. The next two bits (A1, A0) of the address are device option dependent. For example, TPS62350 is factory preset to 00 and TPS62351 is preset to 10. Up to 4 TPS62350 type of devices can be connected to the same I^2C-Bus. See the ordering information table for more details.

Register Address Byte

MSB							LSB
0	0	0	0	0	0	D1	D0

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TPS6235x, which contains the address of the register to be accessed. The TPS6235x contains four 8-bit registers accessible via a bidirectional I^2C-bus interface. All internal registers have read and write access.

Table 1. Register Description

Name	Description
VSEL0 (read / write)	00
VSEL1 (read / write)	01
CONTROL1 (read / write)	10
CONTROL2 (read / write)	11

Voltage Scaling Management

In order to reduce the power consumption of the processor core, the TPS6235x can scale its output voltage. There are two different strategies: 1) by software or 2) by hardware. It can be selected by the HW_nSW bit (more information of the control and value bit mentioned below is shown in the *Register Description* section).

Synchronized Scaling Hardware Strategy (HW_nSW = 1)

The application processor programs via I^{2}C the output voltages associated with the two states of VSEL signal: floor (VSEL0) and roof (VSEL1) values. The application processor also writes the DEFSLEW value in the CONTROL2 register to control the output voltage ramp rate.

These two registers can be continuously updated via I^{2}C to provide the appropriate output voltage according to the VSEL input. The voltage changes with the selected ramp rate immediately after writing to the VSEL0 or VSEL1 register.

In PFM mode, when the output voltage is programmed to a lower value by toggling VSEL signal from high to low, PWROK is defined as low, while the output capacitor is discharged by the load until the converter starts pulsing to maintain the voltage within regulation.

In multiple-step mode, PWROK is defined as low while the output voltage is ramping up or down. Under all other operating conditions, PWROK is defined to be low when the output voltage is below -1.5% of the target value.

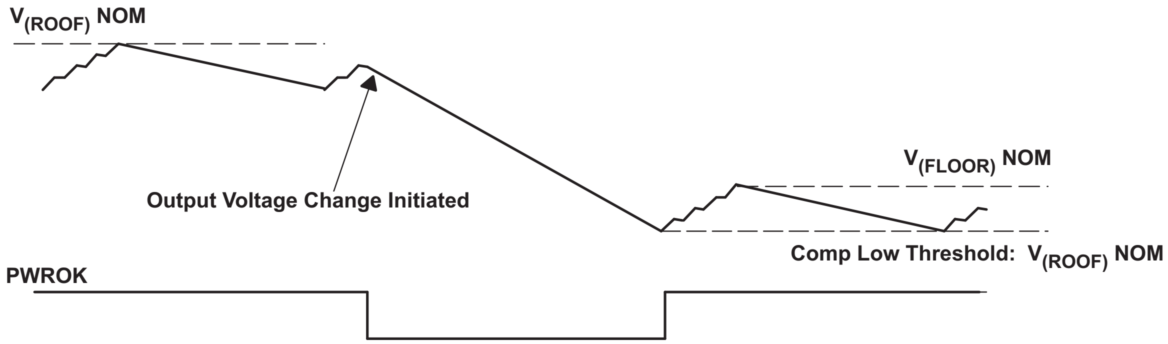


Figure 52. PWROK Operation (Transition to a Lower Voltage)

Table 2 shows the output voltage states depending on VSEL0, VSEL1 registers, and VSEL signal.

Table 2. Synchronized Scaling Hardware Strategy Overview (HW_nSW = 1)

VSEL PIN	VSEL0 REGISTER	VSEL1 REGISTER	OUTPUT VOLTAGE
Low	No action	No action	Floor
Low	Write new value	No action	Change to new value
Low	No action	Write	No change stays at floor voltage
High	No action	No action	Roof
High	Write new value	No action	No change stays at roof voltage
High	No action	Write new value	Change to new value

Direct Scaling Software Strategy (HW_nSW = 0)

The digital processor writes the output voltage needed directly to the register VSEL1 via I^{2}C interface. The application processor also writes the DEFSLEW value in the CONTROL2 register to control the output voltage ramp rate.

The voltage changes with the selected ramp rate after setting the GO bit in CONTROL2 register. This bit is reset when the output voltage has reached its target value. In this mode, the output voltage change is independent of VSEL signal and VSEL0 register is not used.

In PFM mode, when the output voltage is programmed to a lower value, PWROK is defined as low while the output capacitor is discharged by the load until the converter starts pulsing to maintain the voltage within regulation.

In multiple-step mode, PWROK is defined as low while the output voltage is ramping up or down. Under all other operating conditions, PWROK is defined to be low when the output voltage is below -1.5% of the target value.

Voltage Ramp Control

The TPS6235x offers a voltage ramp rate control that can operate in two different modes:

- Multiple-Step Mode
- Single-Step Mode

The mode is selected via DEFSLEW control bits in the CONTROL2 register.

Single-Step Voltage Scaling Mode (default), DEFSLEW[2:0] = [111]

In single-step mode, the TPS6235x ramps the output voltage with maximum slew-rate when transitioning between the floor and the roof voltages (switch to a higher voltage).

When switching between the roof and the floor voltages (transition to a lower voltage), the ramp rate control is dependent on the mode selection (see CONTROL1 register) associated with the target register (Forced PWM, Fast, or Light PFM).

Table 3 shows the ramp rate control when transitioning to a lower voltage with DEFSLEW set to immediate transition.

Table 3. Ramp Rate Control vs. Target Mode

Mode Associated with Target Voltage	HW_nSW	Output Voltage Ramp Rate
Forced PWM	X	Immediate
Fast PFM	X	Time to ramp down depends on output capacitance and load current
Light PFM	X	Time to ramp down depends on output capacitance and load current

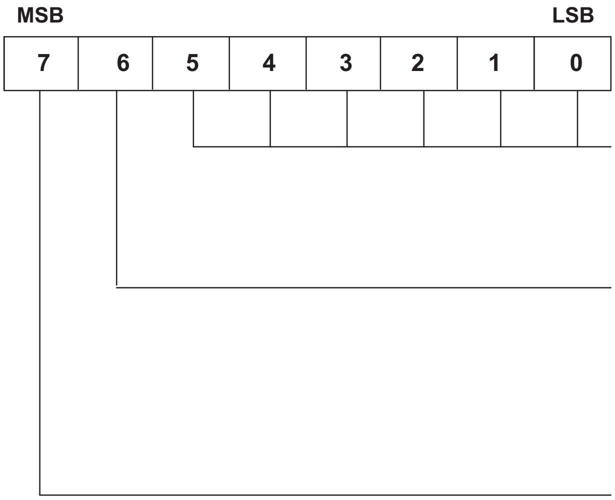
For instance, when the output is programmed to transition to a lower voltage with Light or Fast PFM operation enabled, the TPS6235x ramps down the output voltage without controlling the ramp rate or having intermediate micro-steps. The required time to ramp down the voltage depends on the capacitance present at the output of the TPS6235x and on the load current. From an overall system perspective, this is the most efficient way to perform dynamic voltage scaling.

Multiple-Step Voltage Scaling Mode, DEFSLEW[2:0] = [000] to [110]

In multiple-step mode the TPS6235x controls the output voltage ramp rate regardless of the HW_nSW bit and of the mode of operation (e.g. Forced PWM, Fast PFM, or Light PFM). The voltage ramp control is done by adjusting the time between the voltage micro-steps.

REGISTER DESCRIPTION

VSEL0 REGISTER (READ/WRITE)



Memory location: 00
Reset state: X1XX XXXX – See the Ordering Information Table

VOLTAGE STEP MULTIPLIER, VSM0

6-bit unsigned binary linear coding.
Code effective from 0 to 63 decimal

LIGHTPFM OPTIMIZE

0 : LightPFM optimized for 2.2-µH inductor
1 : LightPFM optimized for 1-µH inductor (default)

This bit is internally mapped by VSEL1[6]. Writing a value in VSEL0[6] automatically updates VSEL1[6].

EN_DCDC

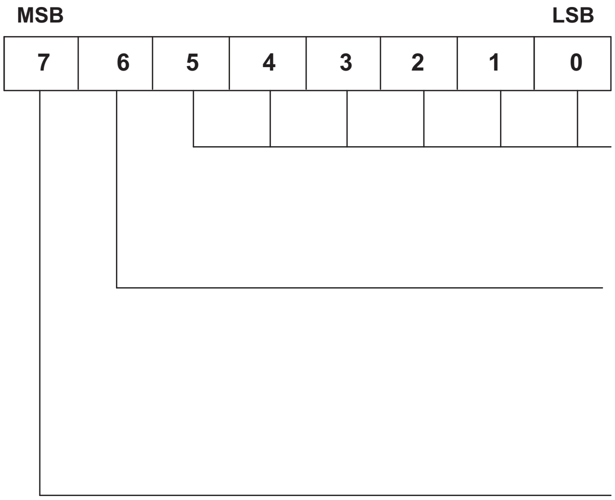
This bit gates the external EN pin signal

0 : Device in shutdown regardless of EN signal
1 : Device enabled when EN pin tied high (default)

This bit is internally mapped by VSEL1[7]. Writing a value in VSEL0[7] automatically updates VSEL1[7].

A. TPS62350, 51, 52, 53, 54, 55: Output Voltage = Minimum Output Voltage + (Voltage Step Multiplier 0 x 12.5 mV)
B. TPS62356: Output Voltage = Minimum Output Voltage + (Voltage Step Multiplier 0 x 25 mV)

VSEL1 REGISTER (READ/WRITE)



Memory location: 01
Reset state: X1XX XXXX – See the Ordering Information Table

VOLTAGE STEP MULTIPLIER, VSM1

6-bit unsigned binary linear coding.
Code effective from 0 to 63 decimal

LIGHTPFM OPTIMIZE

0 : LightPFM optimized for 2.2-µH inductor
1 : LightPFM optimized for 1-µH inductor (default)

This bit is internally mapped by VSEL0[6]. Writing a value in VSEL1[6] automatically updates VSEL0[6].

EN_DCDC

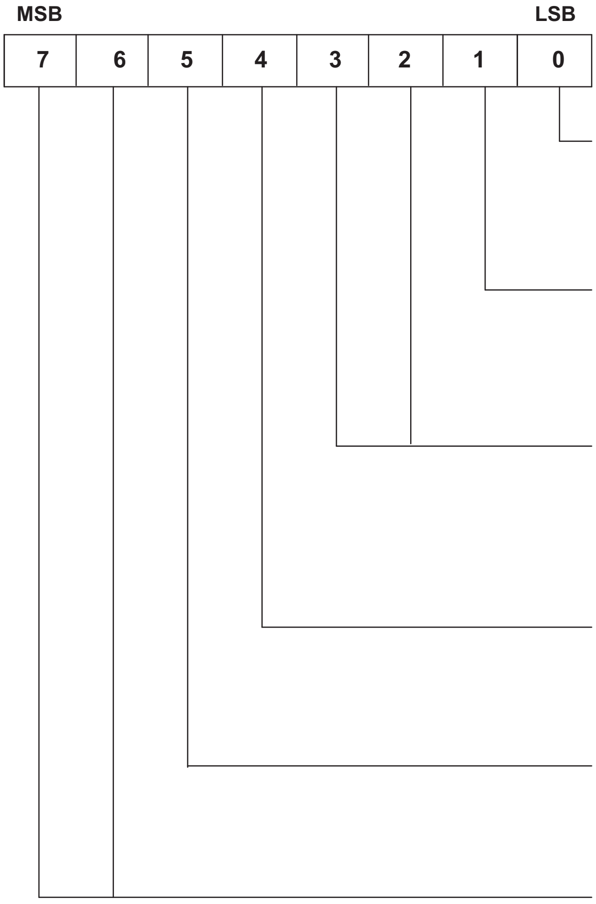
This bit gates the external EN pin signal

0 : Device in shutdown regardless of EN signal
1 : Device enabled when EN pin tied high (default)

This bit is internally mapped by VSEL0[7]. Writing a value in VSEL1[7] automatically updates VSEL0[7].

A. TPS62350, 51, 52, 53, 54, 55: Output Voltage = Minimum Output Voltage + (Voltage Step Multiplier 1 x 12.5 mV)
B. TPS62356: Output Voltage = Minimum Output Voltage + (Voltage Step Multiplier 1 x 25 mV)

CONTROL1 REGISTER (READ/WRITE)



Memory location: 02
Reset state: 0001 0000

MODE0
This bit defines the mode of operation for VSEL low
0 : Light PFM with auto. transition to PWM (default)
1 : Fast PFM with auto. transition to PWM

MODE1
This bit defines the mode of operation for VSEL high
0 : Forced PWM (default)
1 : Fast PFM with auto. transition to PWM

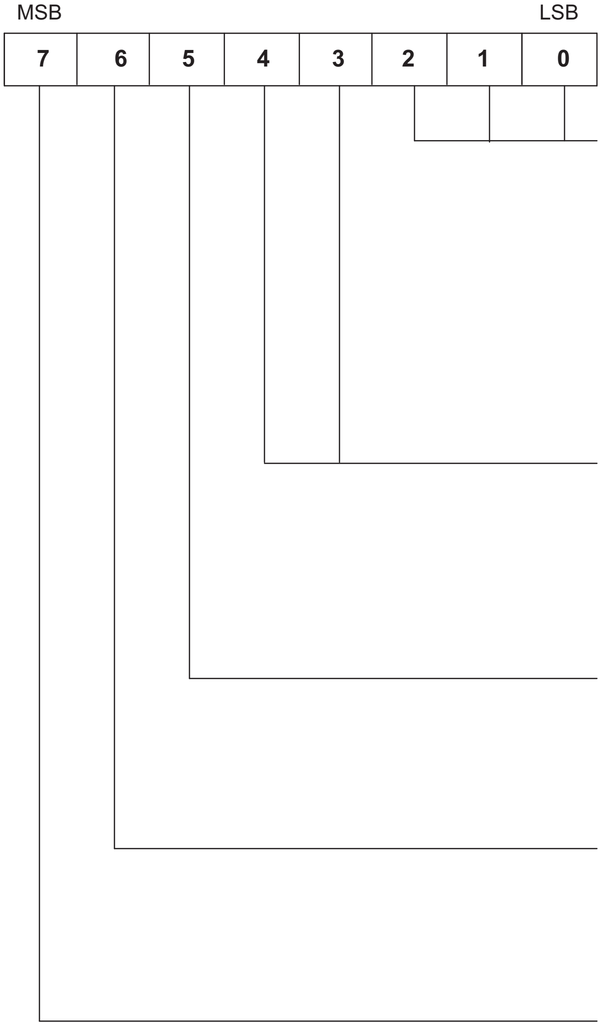
MODE_CTRL
00 : Operation follows MODE0, MODE1 (default)
01 : Light PFM with auto. transition to PWM (VSEL independent)
10 : Forced PWM (VSEL independent)
11 : Fast PFM with auto. transition to PWM (VSEL independent)

HW_nSW
0 : Output voltage controlled by software to the value defined in VSEL1.
1 : Output voltage controlled by VSEL pin (default)

EN_SYNC
0 : Disable synchronization to external clock signal (default)
1 : Enable synchronization to external clock signal

RESERVED (00)

CONTROL2 REGISTER (READ/WRITE)



Memory location: 03
Reset state: 0000 0111

DEFSLEW

DEFSLEW defines the output voltage ramp rate
000 : 0.15 mV/µs
001 : 0.3 mV/µs
010 : 0.6 mV/µs
011 : 1.2 mV/µs
100 : 2.4 mV/µs
101 : 4.8 mV/µs
110 : 9.6 mV/µs
111 : Immediate (default)

PLL_MULT

PLL_MULT defines the synchronization clock multiplier ratio
00 : x1 - $f_{(SYNC)}$ = 3 MHz ± 12% (default)
01 : x2 - $f_{(SYNC)}$ = 1.5 MHz ± 12%
10 : x3 - $f_{(SYNC)}$ = 1 MHz ± 12%
11 : x4 - $f_{(SYNC)}$ = 750 kHz ± 12%

PWROK (READ ONLY)

0 : Indicates that the output voltage is below its target regulation voltage. This bit is zero if the converter is disabled.
1 : Indicates that the output voltage is within its nominal range

OUTPUT_DISCHARGE

0 : The dc/dc output capacitor is not actively discharged when the converter is disabled (default).
1 : The dc/dc output capacitor is actively discharged when the converter is disabled.

GO

This bit is only valid when HW_nSW = 0
0 : No change in the output voltage (default).
1 : The output voltage is changed with the ramp rate defined in DEFSLEW.

APPLICATION INFORMATION

Output Filter Design (Inductor and Output Capacitor)

The TPS6235x step-down converter has an internal loop compensation. Therefore, the external L-C filter must be selected to work with the internal compensation.

The device has been designed to operate with inductance values between a minimum of 0.7 µH and maximum of 6.2 µH. The internal compensation is optimized to operate with an output filter of L = 1 µH and C_O = 10 µF. Such an output filter has its corner frequency at:

$$f_C = \frac{1}{2\pi\sqrt{L \times C_O}} = \frac{1}{2\pi\sqrt{1\,\mu H \times 10\,\mu F}} = 50.3\text{ kHz} \qquad (1)$$

Selecting a larger output capacitor value (e.g., 22 µF) is less critical because the corner frequency moves to lower frequencies with fewer stability problems. The possible output filter combinations are listed in Table 4.

Regardless of the inductance value, operation is recommended with 10-µF output capacitor in applications with high-load transients $\left(\frac{di}{dt}\right)$ (e.g., ≥ 1600 mA/µs).

Table 4. Output Filter Combinations

INDUCTANCE (L)	OUTPUT CAPACITANCE (C_O) FOR STABLE LOOP OPERATION	OUTPUT CAPACITANCE (C_O) FOR OPTIMIZED TRANSIENT PERFORMANCE
1.0 µH	≥ 10 µF (ceramic capacitor)	≥ 10 µF (ceramic capacitor)
2.2 µH	≥ 4.7 µF (ceramic capacitor)	≥ 22 µF (ceramic capacitor)

The inductor value also has an impact on the pulse skipping operation. The transition into power-save mode begins when the valley inductor current drops below a level set internally. Lower inductor values result in higher ripple current which occurs at lower load currents. This results in a dip in efficiency at light load operations.

Inductor Selection

Even though the inductor does not influence the operating frequency, the inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

$$\Delta I_L = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{SW}} \qquad \Delta I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2} \qquad (2)$$

where:

f_{SW} = switching frequency (3 MHz typical)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

$I_{L(MAX)}$ = maximum inductor current

Normally, it is advisable to operate with a ripple of less than 30% of the average output current. Accepting larger values of ripple current allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS62350 converters.

Table 5. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS
FDK	MIPSA2520	$2.5 \times 2.0 \times 1.2 = 6$ mm^3
TDK	VLF3010AT	$2.8 \times 2.6 \times 1 = 7.28$ mm^3
Coilcraft	LPS3010	$3 \times 3 \times 1 = 9$ mm^3
	LPS3015	$3 \times 3 \times 1.5 = 13.5$ mm^3

Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6235x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance overtemperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{sw}} \times \left(\frac{1}{8 \times C_O \times f_{sw}} + ESR \right), \text{maximum for high } V_I \tag{3}$$

At light loads, the device operates in power-save mode and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds and propagation delays. The typical output voltage ripple is 2% of the nominal output voltage V_O.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 10-µF capacitor is sufficient.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part.

Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The output capacitor must supply all of the load current during the time between the application of the load transient and the turn on of the P-channel MOSFET. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)} \times ESR$, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value.

During this recovery time, V_O is monitored for settling time, overshoot, or ringing that helps judge the converter stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis must be performed over the input voltage range, load current range, and temperature range.

Layout Considerations

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6235x device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths as indicated in bold on Figure 53.

The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common ground node for power ground and a different one for control ground (AGND) to minimize the effects of ground noise. Connect these ground nodes together (star point) underneath the IC and make sure that small signal components returning to the AGND pin do not share the high current path of C1 and C2.

The output voltage sense line (FB) should be connected right to the output capacitor and routed away from noisy components and traces (e.g., SW line). Its trace should be minimized and shielded by a guard-ring connected to the reference ground.

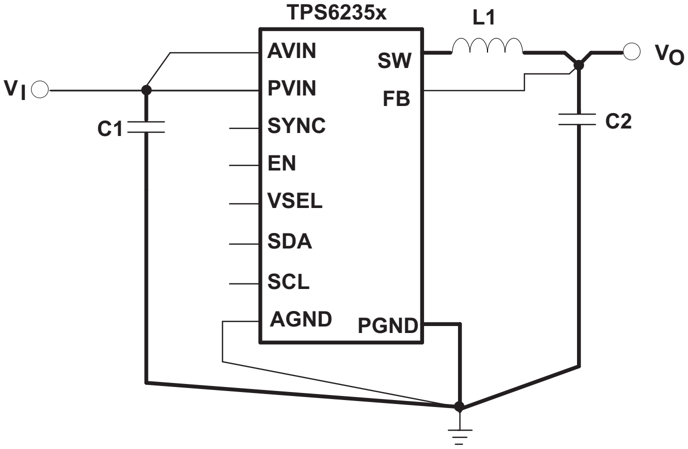


Figure 53. Layout Diagram

Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

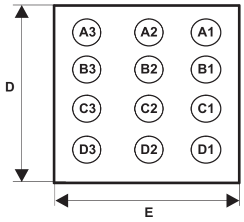
- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6235x device is 125°C. The thermal resistance of the 12-pin CSP package (YZG) is $R_{\theta JA}$ = 89°C/W. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 450 mW. More power can be dissipated if the maximum ambient temperature of the application is lower or if the PowerPAD™ package (DRC) is used.

$$P_DMAX = \frac{T_JMAX - T_A}{R_{\theta JA}} = \frac{125^\circ C - 85^\circ C}{89^\circ C/W} = 450\ mW \tag{4}$$

PACKAGE SUMMARY

CHIP SCALE PACKAGE (BOTTOM VIEW)



CHIP SCALE PACKAGE (TOP VIEW)

Code:

- Y — 2 digit date code
- LLLL - lot trace code
- S - assembly site code

PACKAGE DIMENSIONS

The dimensions for the YZG package are provided in the mechanical data package drawing at the end of this data sheet.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62350YZGR	ACTIVE	DSBGA	YZG	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS62350	Samples
TPS62350YZGT	ACTIVE	DSBGA	YZG	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS62350	Samples
TPS62352YZGR	ACTIVE	DSBGA	YZG	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS62352	Samples
TPS62353YZGR	ACTIVE	DSBGA	YZG	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS62353	Samples
TPS62353YZGT	ACTIVE	DSBGA	YZG	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS62353	Samples
TPS62354YZGR	ACTIVE	DSBGA	YZG	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS62354	Samples
TPS62355DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CCP	Samples
TPS62356YZGR	ACTIVE	DSBGA	YZG	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS62356	Samples
TPS62356YZGT	ACTIVE	DSBGA	YZG	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS62356	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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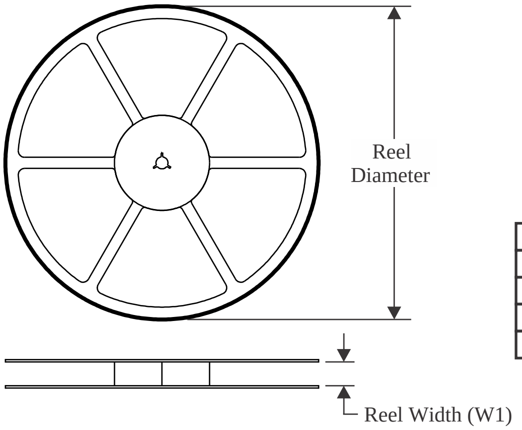
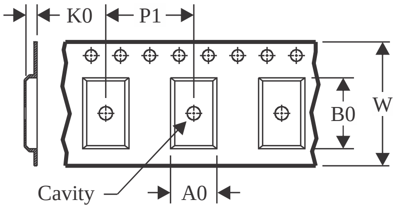
TAPE AND REEL INFORMATION

REEL DIMENSIONS

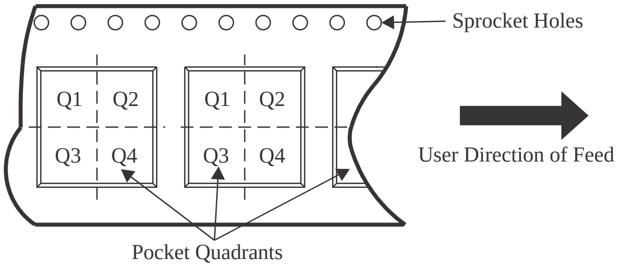


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

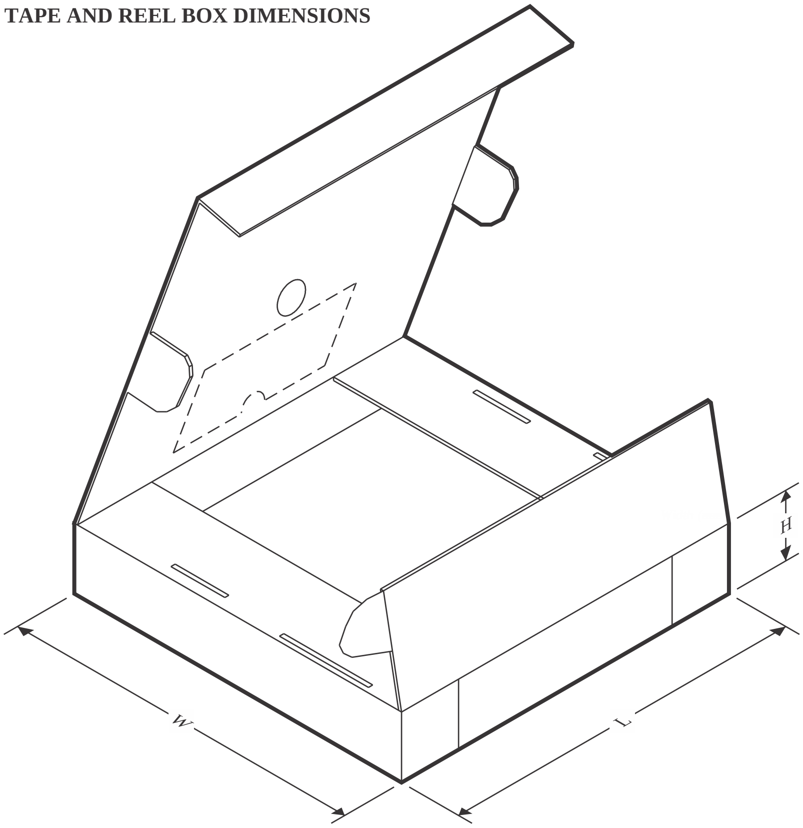
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62350YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.6	2.37	0.81	4.0	8.0	Q1
TPS62350YZGT	DSBGA	YZG	12	250	180.0	8.4	1.6	2.37	0.81	4.0	8.0	Q1
TPS62352YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.6	2.37	0.81	4.0	8.0	Q1
TPS62353YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.6	2.37	0.81	4.0	8.0	Q1
TPS62353YZGT	DSBGA	YZG	12	250	180.0	8.4	1.6	2.37	0.81	4.0	8.0	Q1
TPS62354YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.6	2.37	0.81	4.0	8.0	Q1
TPS62355DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62356YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.6	2.37	0.81	4.0	8.0	Q1
TPS62356YZGT	DSBGA	YZG	12	250	180.0	8.4	1.6	2.37	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62350YZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TPS62350YZGT	DSBGA	YZG	12	250	182.0	182.0	20.0
TPS62352YZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TPS62353YZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TPS62353YZGT	DSBGA	YZG	12	250	182.0	182.0	20.0
TPS62354YZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TPS62355DRCR	VSON	DRC	10	3000	356.0	356.0	35.0
TPS62356YZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TPS62356YZGT	DSBGA	YZG	12	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

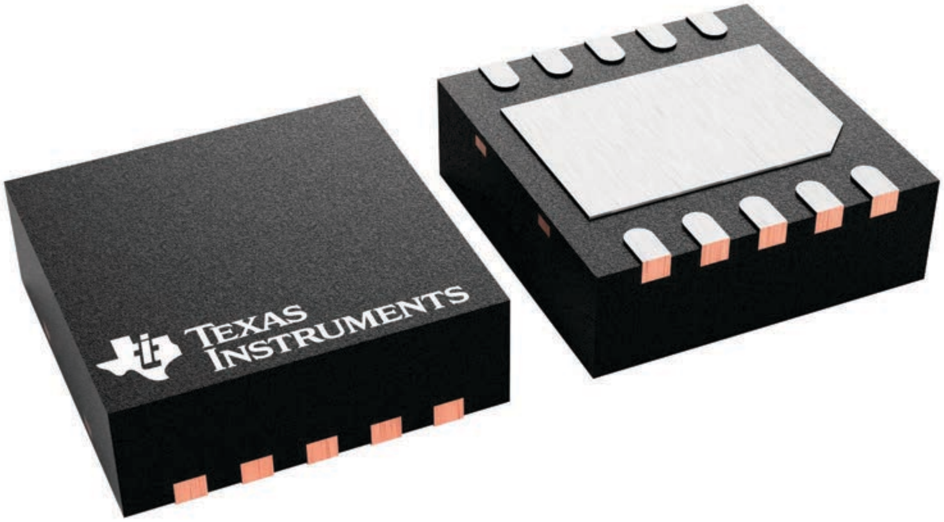
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

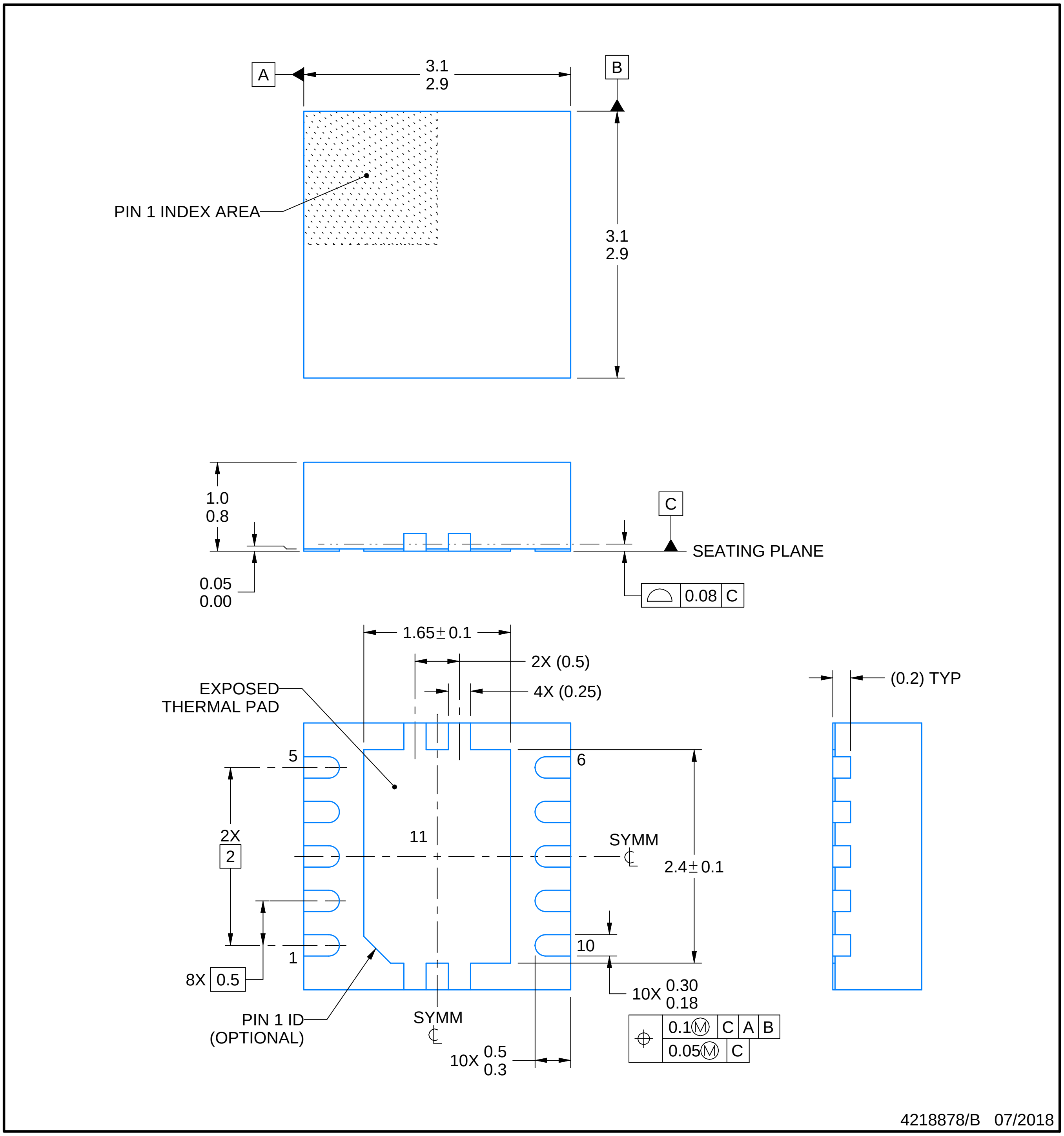
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

VSON - 1 mm max height

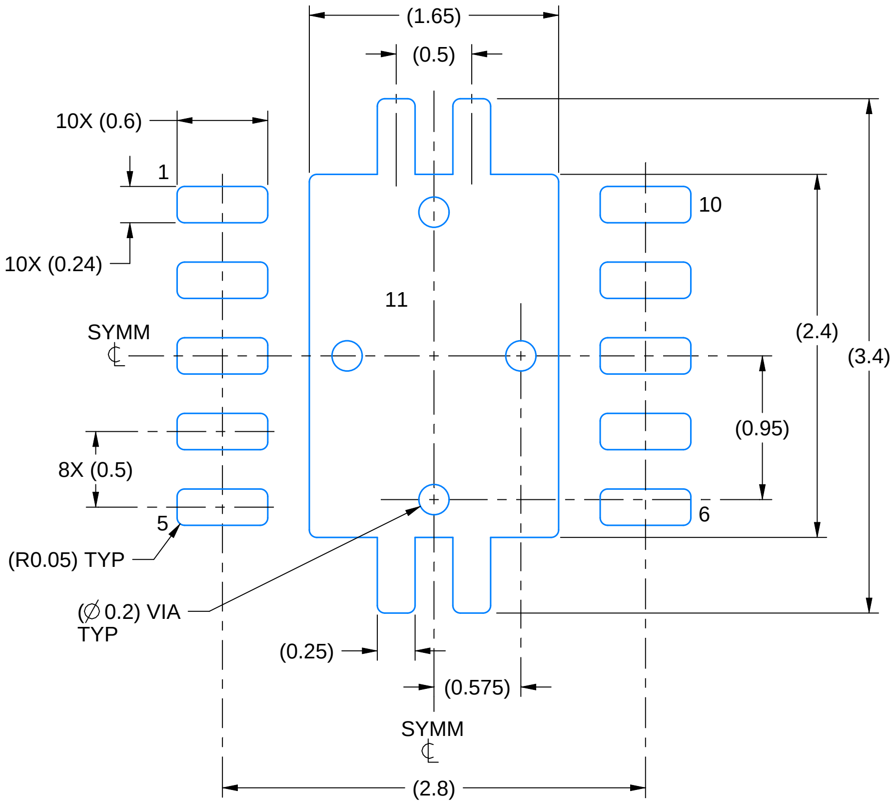
PLASTIC SMALL OUTLINE - NO LEAD



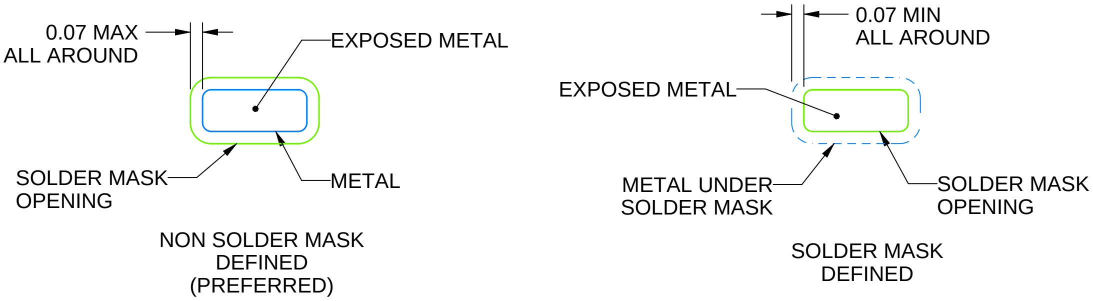
4218878/B 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

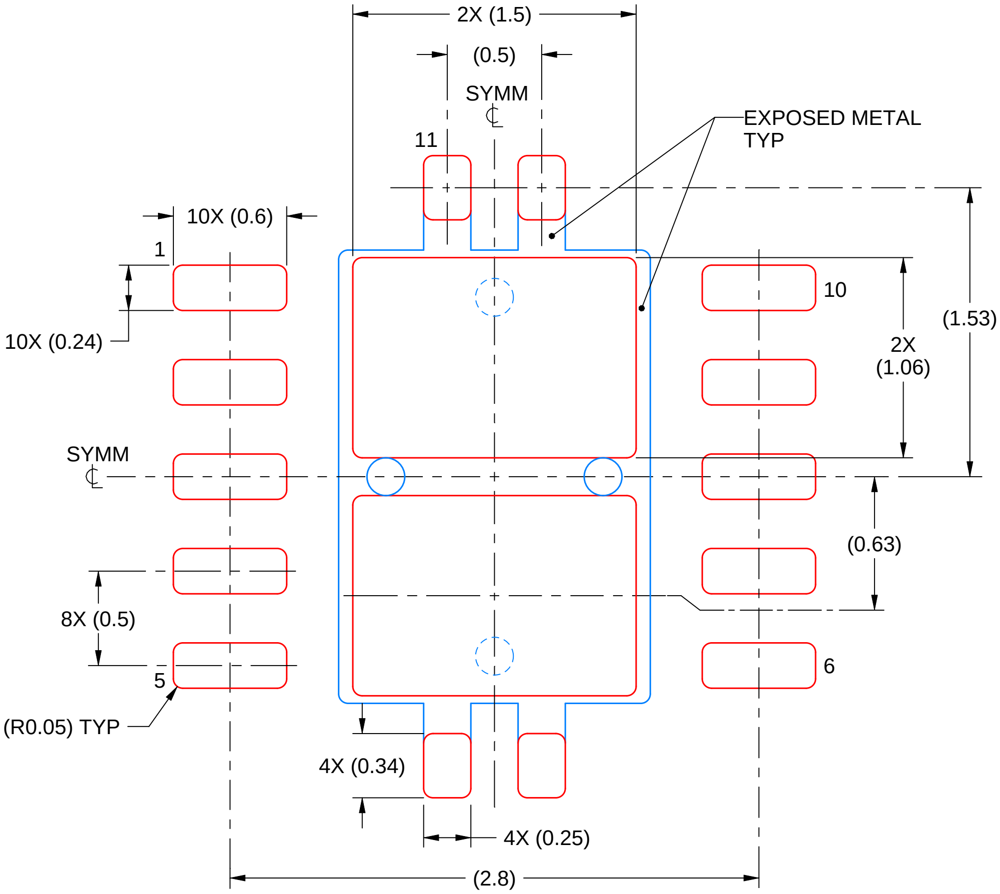


SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



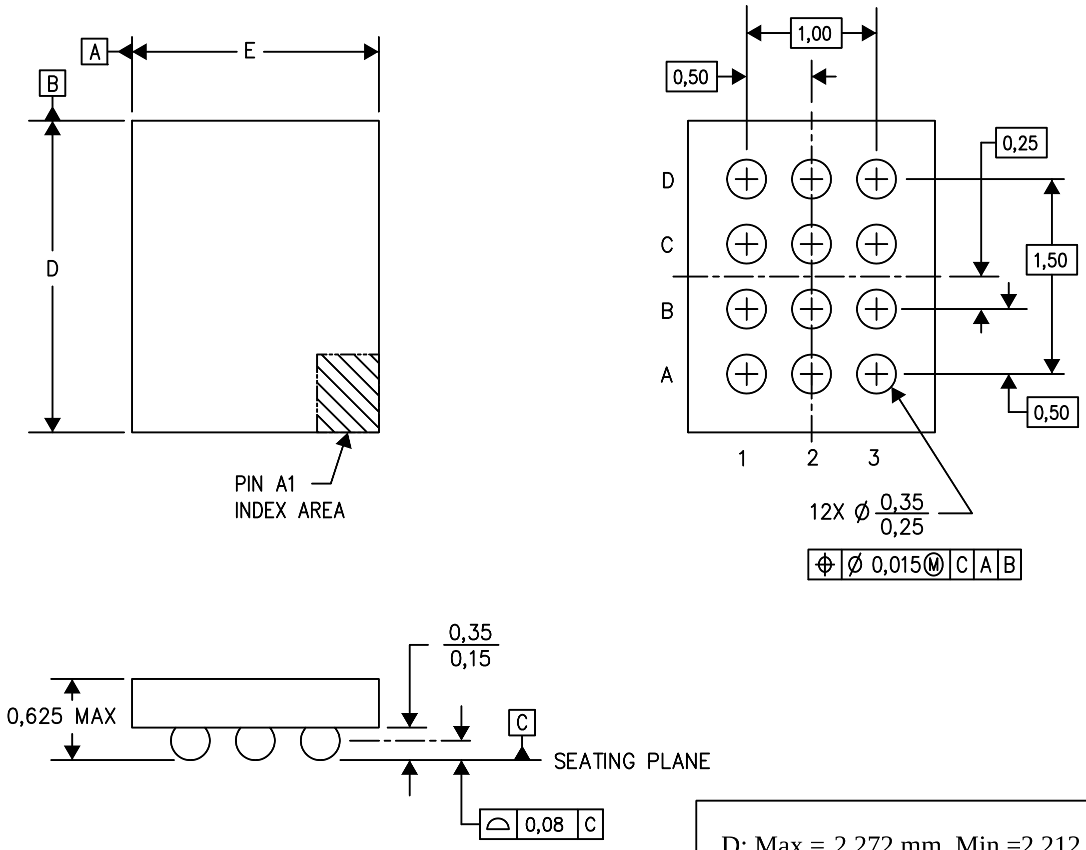
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YZG (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



D: Max = 2.272 mm, Min =2.212 mm

E: Max = 1.504 mm, Min =1.444 mm

4205059/E 07/13

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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