TPS631012 and TPS631013 1.6V to 5.5V Input Voltage 1.5A Buck-boost Converter with I²C in Wafer Chip Scale Package

1 Features

- 1.6V to 5.5V input voltage range
  - Device input voltage > 1.65V for start-up
- 1.0V to 5.5V output voltage range(adjustable)
- High output current capability, 3A peak switch current
  - 2A I_{OUT} for V_{IN} ≥ 3V, V_{OUT} = 3.3V
  - 1.5A I_{OUT} for V_{IN} ≥ 2.7V, V_{OUT} = 3.3V
- High efficiency over the entire load range
  - 8μA typical quiescent current
  - Automatic power save mode and forced PWM mode configurable
- Peak current buck-boost mode architecture
  - Seamless mode transition
  - Forward and reverse current operation
  - Start-up into pre-biased outputs
  - Fixed-frequency operation with 2MHz switching
- Safety and robust operation features
  - Overcurrent protection and short-circuit protection
  - Integrated soft start with active ramp adoption
  - Overtemperature protection and overvoltage protection
  - True shutdown function with load disconnection
  - Forward and backward current limit
- Default setting of internal EN
  - TPS631012 and TPS631012X(X=1,2,3): CONVERTER_EN = 0
  - TPS631013: CONVERTER_EN = 1
- Small solution size
  - Small 1μH inductor
  - 1.803mm × 0.905mm in WCSP

2 Applications

- TWS
- System pre-regulator (smartphone, tablet, terminal, telematics)
- Point-of-load regulation (wired sensor, port/cable adapter, and dongle)
- Fingerprint, camera sensors (electronic smart lock, IP network camera)
- Voltage stabilizer (datacom, optical modules, cooling/heating)

3 Description

The TPS631012 and TPS631013 are constant frequency peak current mode control buck-boost converters in tiny wafer chip scale package. They have a 3A peak current limit (typical) and 1.6V to 5.5V input voltage range, and provide a power supply solution for system pre-regulators and voltage stabilizers.

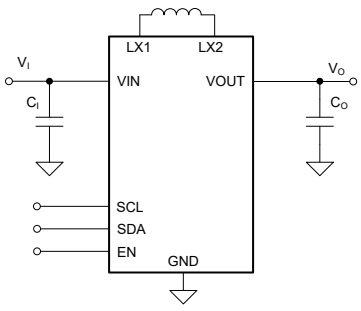
Depending on the input voltage, the TPS631012 and TPS631013 automatically operate in boost, buck, or in 3-cycle buck-boost mode when the input voltage is approximately equal to the output voltage. The transitions between modes happen at a defined duty cycle and avoid unwanted toggling within the modes to reduce output voltage ripple. 8μA quiescent current and power save mode enable the highest efficiency for light to no-load conditions.

The devices offer a very small solution size in WCSP.

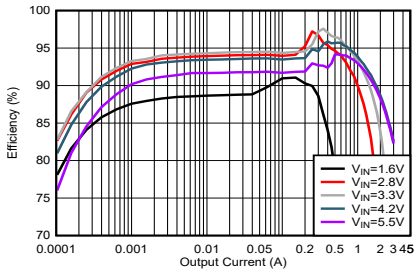
Package Information

Part Number	Package (1)	Body Size (NOM)
TPS631012	WCSP	1.803mm × 0.905mm
TPS631013 (2)		

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview information (not Production Data).



Typical Application



Efficiency vs Output Current (V_{OUT} = 3.3V)

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4 Device Comparison Table

PART NUMBER	Default Setting of Internal EN(3)	I²C Target Address
TPS631012	CONVERTER_EN = 0	0x2A
TPS6310121(1) (2)	CONVERTER_EN = 0	0x28
TPS6310122(1) (2)	CONVERTER_EN = 0	0x29
TPS6310123(1) (2)	CONVERTER_EN = 0	0x2B
TPS631013(1) (2)	CONVERTER_EN = 1	0x2A

(1) Product Preview. Contact TI factory for more information.
(2) TPS631012 and TPS631012X(X = 1, 2, 3) differ only in the I2C target address.
(3) Refer to the Register CONTROL1.

5 Pin Configuration and Functions

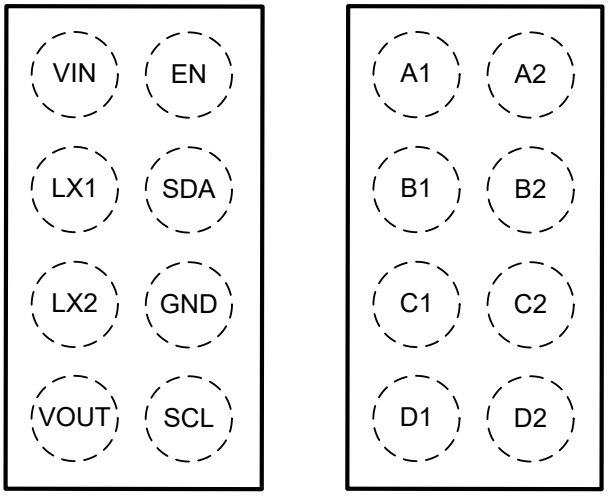


Figure 5-1. 8-Pin YBG WCSP Package (Top View)

Table 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
VIN	A1	PWR	Supply input voltage
EN	A2	I	Device enable. Set high to enable and low to disable. It must not be left floating.
LX1	B1	PWR	Inductor switching node of the buck stage
SDA	B2	I	I^2C serial interface data. Pull this pin up to the I^2C bus voltage with a resistor.
LX2	C1	PWR	Inductor switching node of the boost stage
GND	C2	PWR	Power ground
VOUT	D1	PWR	Power stage output
SCL	D2	I	I^2C serial interface clock. Pull this pin up to the I^2C bus voltage with a resistor.

(1) PWR = power, I = input

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage (VIN, LX1, LX2, VOUT, EN, SCL, SDA)(2)	–0.3	6.0	V
	Input voltage for less than 10 ns (LX1, LX2)(2)	–2.0	7.0	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Rating

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JS-002(2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		1.6		5.5	V
V_O	Output voltage		1.0		5.5	V
C_I	Effective Input capacitance	V_I = 1.6 V to 5.5 V	4.2			µF
C_O	Effective Output capacitance	1.2 V ≤ V_O ≤ 3.6 V, nominal value at V_O = 3.3 V	10.4	16.9	330	µF
		3.6 V < V_O ≤ 5.5 V, nominal value at V_O = 5 V	7.95	10.6	330	µF
L	Effective Inductance		0.7	1	1.3	µH
T_J	Operating junction temperature range		–40		125	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC		TPS631012 TPS631013 YBG(WCSP) 8 pins	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	84	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	43.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.7	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

6.5 Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.8 V , V_O = 3.3 V and T_J = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY								
I_{SD}	Shutdown current into VIN		V_I = 3.8 V, $V_{(EN)}$ = 0 V	T_J = 25°C		0.5	0.9	µA
I_Q	Quiescent current into VIN		V_I = 2.2 V, V_O = 3.3 V, $V_{(EN)}$ = 2.2 V, no switching			0.15	6.1	µA
I_Q	Quiescent current into VOUT		V_I = 2.2 V, V_O = 3.3 V, $V_{(EN)}$ = 2.2 V, no switching			8		µA
V_{IT+}	Positive-going UVLO threshold voltage		V_I rising		1.5	1.55	1.599	V
V_{IT-}	Negative-going UVLO threshold voltage		V_I falling		1.4	1.45	1.499	V
V_{hys}	UVLO threshold voltage hysteresis				99			mV
$V_{I(POR)T+}$	Positive-going POR threshold voltage(1)		maximum of V_I or V_O		1.25	1.45	1.65	V
$V_{I(POR)T-}$	Negative-going POR threshold voltage(1)				1.22	1.43	1.6	V
I/O SIGNALS								
V_{T+}	Positive-going threshold voltage	EN, SDA, SCL			0.77	0.98	1.2	V
V_{T-}	Negative-going threshold voltage	EN, SDA, SCL			0.5	0.66	0.76	V
V_{hys}	Hysteresis voltage	EN, SDA, SCL				300		mV
I_{IH}	High-level input current	EN, SDA, SCL	$V_{(EN)}$ = $V_{(SDA)}$ = $V_{(SCL)}$= 1.5 V, no pullup resistor			±0.01	±0.25	µA
I_{IL}	Low-level input current	EN, SDA, SCL	$V_{(EN)}$ = $V_{(SDA)}$ = $V_{(SCL)}$ = 0 V,			±0.01	±0.1	µA
I_{IB}	Input bias current	EN, SDA, SCL	$V_{(EN)}$ = 5.5 V			±0.01	±0.3	µA
POWER SWITCH								
$r_{DS(on)}$	On-state resistance	Q1	V_I = 3.8 V, V_O = 3.3 V, test current = 0.2 A			45		mΩ
		Q2				50		mΩ
		Q3				50		mΩ
		Q4				85		mΩ
CURRENT LIMIT								
$I_{L(PEAK)}$	Switch peak current limit (2)	Q1	V_O = 3.3 V	Output sourcing current	2.6	3	3.35	A
				Output sinking current, V_I = 3.3 V	–0.7	–0.55	–0.45	A
I_{PFM_entry}	PFM mode entry threshold (peak) current (2)		I_O falling			145		mA
PROTECTION FEATURES								
$V_{T+(OVP)}$	Positive-going OVP threshold voltage				5.55	5.75	5.95	V
$V_{T+(IVP)}$	Positive-going IVP threshold voltage				5.55	5.75	5.95	V
T_{SD_R}	Thermal shutdown threshold temperature		T_J rising			160		°C
T_{SD_HYS}	Thermal shutdown hysteresis					25		°C
TIMING PARAMETERS								
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of the output voltage ramp					0.87	1.5	ms
$t_{d(ramp)}$	Soft-start ramp time				6.42	7.55	8.68	ms
f_{SW}	Switching frequency				1.8	2	2.2	MHz

(1) The POR (Power On Reset) threshold is the minimum supply of the internal VMAX block that allows the device to operate
(2) Current limit production test are performed under DC conditions. The current limit in operation is somewhat higher and depending on propagation delay and the applied external components

6.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I²C INTERFACE						
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus (1)	0		1000	
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus (1)	0.5			
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus (1)	0.5			
$t_{SU:STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{HD:STA}$	Hold time (repeated) START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{HD:DAT}$	Data hold time	Standard mode	0			µs
		Fast mode	0			
		Fast mode plus (1)	0			
t_r	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus (1)			20	
t_f	Fall time of both SDA and SCL signals	Standard mode			300	ns
		Fast mode	$20\times V_{DD}/5.5$		300	
		Fast mode plus (1)	$20\times V_{DD}/5.5$		120	
$t_{su:STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{VD;DAT}$	Data valid time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus (1)			0.45	
$t_{VD;ACK}$	Data valid acknowledge time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus (1)			0.45	
C_b	Capacitive load for each bus line	Standard mode			400	pF
		Fast mode			400	

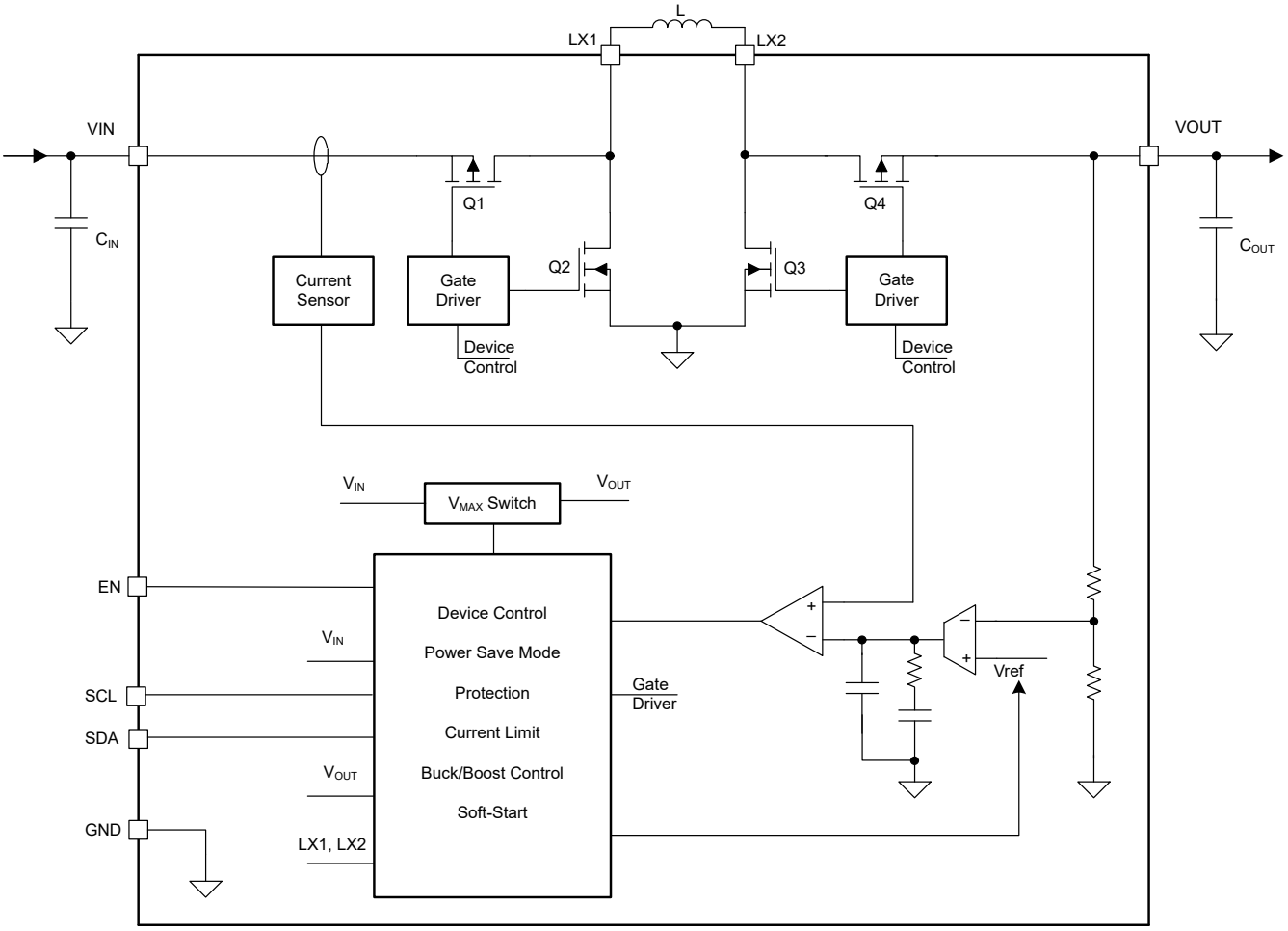
(1) Fast mode plus is compatible but not compliant with I²C standard

7 Detailed Description

7.1 Overview

The TPS631012 and TPS631013 are constant frequency peak current mode control buck-boost converters. The converters use a fixed-frequency with approximately 2-MHz switching frequency. The modulation scheme has three clearly defined operation modes where the converters enter with defined thresholds over the full operation range of V_{IN} and V_{OUT}. The maximum output current is determined by the Q1 peak current limit, which is typically 3 A.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The input voltage of the VIN pin is continuously monitored if the device is not in shutdown mode. UVLO only stops or starts the converter operation. The UVLO does not impact the core logic of the device. UVLO avoids a brownout of the device during device operation. In case the supply voltage on the VIN pin is lower than the negative-going threshold of UVLO, the converter stops its operation. To avoid a false disturbance of the power conversion, the UVLO falling threshold logic signal is digitally de-glitched.

If the supply voltage on the VIN pin recovers to be higher than the UVLO rising threshold, the converter returns to operation. In this case, the soft-start procedure restarts faster than under start-up without a pre-biased output.

7.3.2 Enable and Soft Start

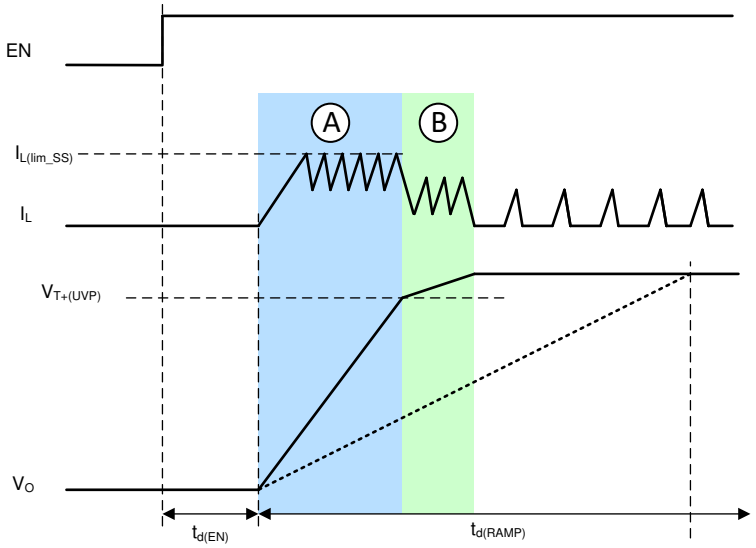


Figure 7-1. Typical Soft-Start Behavior

When the input voltage is above the UVLO rising threshold and the EN pin is pulled to a voltage above 1.2 V, the TPS631012 and TPS631013 are enabled and start up after a short delay time, $t_{d(EN)}$.

The TPS631012 and TPS631013 have two start-up mechanisms that are controlled by the FAST_RAMP_EN bit in Register CONTROL2. Figure 7-1 shows a typical start-up case (low output load, typical output capacitance).

- When FAST_RAMP_EN = 1, the fast ramp mode is enabled. The output ramp behavior is shown as the solid line Vo in Figure 7-1
- When FAST_RAMP_EN = 0, the fast ramp mode is disabled. The output ramp behavior is shown as the dash line Vo in Figure 7-1

When fast ramp mode is enabled, the devices control the inductor peak current to limit the inrush current and ensure the fastest possible soft start if the capacitance is chosen lower than that for which the ramp time $t_{d(RAMP)}$ was selected. The output voltage then rises faster than the reference voltage ramp (see phase A in Figure 7-1). To avoid an output overshoot, the current clamp is deactivated when the output is close to the target voltage and follows the reference voltage ramp slew value given by the voltage ramp, which is finishing the start up (see phase B in Figure 7-1). Transition from the current clamp operation is detected using the $V_{T+(UVP)}$ threshold, which is typically 90% of the target output voltage. After phase B, the output voltage is well regulated to the nominal target voltage. The current waveform depends on the output load and operation mode. The current limit during start-up has two options and is controlled by the CL_RAMP_MIN bit in Register CONTROL2.

- When CL_RAMP_MIN = 0, the typical current limit during start-up (phase A in Figure 7-1) is 500mA
- When CL_RAMP_MIN = 1, the typical current limit during start-up (phase A in Figure 7-1) is 1000mA

When fast ramp mode is disabled, the output voltage is totally controlled by the internal reference voltage ramp slew rate. There are three bits of TD_RAMP in Register CONTROL2 to define the output voltage ramp time.

Note that if, during start-up, the current limit ($I_{L(lim\_SS)}$) is lower than the current required to follow the voltage ramp controlled by TD_RAMP, the current automatically increases to follow the voltage ramp.

7.3.3 Device Enable (EN)

The EN pin enables and disables the device.

- When the EN pin is high, the device is enabled.
- When the EN pin is low, the device is disabled.

The CONVERTER_EN bit in the Register CONTROL1 can also be used to enable and disable the output of the converter.

- For TPS631012, the default bit of CONVERTER_EN = 0.
- For TPS631013, the default bit of CONVERTER_EN = 1.

Table 7-1. Device Enable Truth Table

EXTERNAL EN PIN	INTERNAL EN (CONVERTER_EN)	DEVICE STATE	OUTPUT STATE
0	X	Device in Shutdown	No Output
1	0	Programming Interface Active	No Output
1	1	Device Active	Output Enabled

Note that when the EN pin is connected to logic low, all the I^2C registers are cleaned and reset to the default values. While setting CONVERTER_EN to 0 has no influences on the I^2C registers

7.3.4 Output Voltage Control

The TPS631012 and TPS631013 can generate output voltages from 1.0 V to 5.5 V with a 25 mV step. The Register VOUT is used to set the output voltage:

- VOUT = 1.000 + (VOUT[7 :0] × 0.025) V, when 0x00<=VOUT[7 :0]<=0xB4;
- VOUT = 5.5 V, when 0xB5<=VOUT[7 :0]<=0xFF

VOUT[7 :0] is the 8-bit value in the Register VOUT.

The dynamic voltage scaling control bit of EN_FAST_DVS in Register CONTROL1 controls the VOUT settling time when VOUT is set between different voltages.

- When EN_FAST_DVS = 1, the typical VOUT slew rate is 7.2 V/ms;
- When EN_FAST_DVS = 0, the typical VOUT slew rate is 0.4 V/ms

7.3.5 Mode Selection (PFM/FPWM)

The TPS631012 and TPS631013 have two modes of PFM and FPWM. During PFM mode operation, the devices feature a power save mode to maintain the highest efficiency over the full operating output current range. In PFM mode the devices automatically change the converter operation from CCM to pulse frequency modulation. During FPWM mode, the devices use PWM for all operating conditions regardless of the output current to achieve minimum output ripple.

The PFM/FPWM mode selection is controlled by the FPWM bit in Register CONTROL2:

- When FPWM = 0b0, the devices work in PFM mode
- When FPWM = 0b1, the devices work in FPWM mode

7.3.6 Output Discharge

The TPS631012 and TPS631013 provide an active pull down current to quickly discharge output when the EN pin is logic low or the CONVERTER_EN bit is set to 0. With this function, the VOUT is connected to ground through internal circuitry, preventing the output from “floating” or entering into an undetermined state. The output discharge function makes the power on and off sequencing smooth. Pay attention to the output discharge function if use this device in applications such as power multiplexing, because the output discharge circuitry creates a constant current path between the multiplexer output and the ground.

The output discharge is controlled by the two bits named with EN_DISCH_VOUT. The output discharge can be disabled or set to three different options. Please refer to the EN_DISCH_VOUT bits in Register CONTROL2 for detailed I^2C settings.

7.3.7 Reverse Current Operation

The device can support reverse current operation (the current flows from VOUT pin to VIN pin) in FPWM mode. If the internal output feedback voltage is higher than the reference voltage, the converter regulation forces a

current into the input capacitor. The reverse current operation is independent of the V_{IN} voltage or V_{OUT} voltage ratio, hence it is possible on all device operation modes boost, buck, or buck-boost.

7.3.8 Protection Features

The following sections describe the protection features of the device.

7.3.8.1 Input Overvoltage Protection

The TPS631012 and TPS631013 have input overvoltage protection which avoids any damage to the device in case the current flows from the output to the input and the input source cannot sink current (for example, a diode in the supply path).

If forced PWM mode is active, the current can go negative until it reaches the sink current limit. Once the input voltage threshold, $V_{T+(IVP)}$, is reached on the VIN pin, the protection disables forced PWM mode and only allows current to flow from VIN to VOUT. After the input voltage drops under the input voltage protection threshold, forced PWM mode can be activated again.

7.3.8.2 Output Overvoltage Protection

The devices have the output overvoltage protection which avoids any damage to the device. When the output voltage threshold $V_{T+(OVP)}$ is reached on the VOUT pin, the protection disables the converter power stage and makes the switching nodes high impedance.

7.3.8.3 Short Circuit Protection/Hiccup

The device features peak current limit performance at short circuit protection. Figure 7-2 shows a typical device behavior of an short/overload event of the short circuit protection.

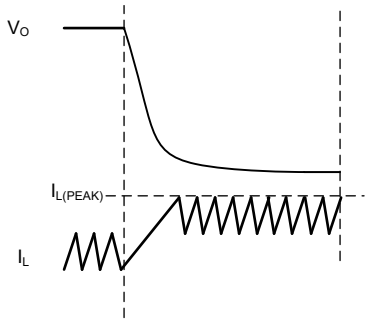


Figure 7-2. Typical Device Behavior During Short Circuit Protection

When the EN_SCP bit in Register CONTROL1 is set to 1 to enable the short circuit hiccup protection, the hiccup timer works, limiting the switching on time to a typical 9 ms followed by a typical off time of 22 ms, then the device restarts. If the short condition disappears, the device automatically enters the normal working mode.

7.3.8.4 Thermal Shutdown

To avoid thermal damage of the device, the temperature of the die is monitored. The device stops operation once the sensed temperature rises over the typical thermal threshold 160 ˚C. After the temperature drops below the typical thermal shutdown hysteresis 25 ˚C, the converter returns to normal operation.

7.4 Device Functional Modes

The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

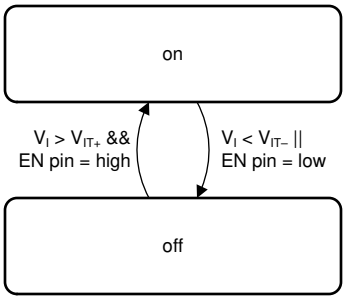


Figure 7-3. Device Functional Modes

7.5 Programming

7.5.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see *NXP Semiconductors, UM10204 – I^2C-Bus Specification and User Manual*). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through open-drain I/O pins, SDA, and SCL. A controller device, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A target device receives and transmits data on the bus under control of the controller device.

The device works as a target and supports the following data transfer modes, as defined in the I^2C-Bus Specification:

- Standard-mode (100 kbps)
- Fast-mode (400 kbps)
- Fast-mode Plus (1 Mbps)

The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values, depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above $V_{IT+(POR)}$.

The data transfer protocol for standard and fast modes is exactly the same, therefore, it is referred to as F/S-mode in this document. The device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is 2Ah (00101010b).

To make sure that the I^2C function in the device is correctly reset, it is recommended that the I^2C controller initiates a STOP condition on the I^2C bus after the initial power up of SDA and SCL pullup voltages.

7.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The controller initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 7-4. All I^2C-compatible devices recognize a start condition.

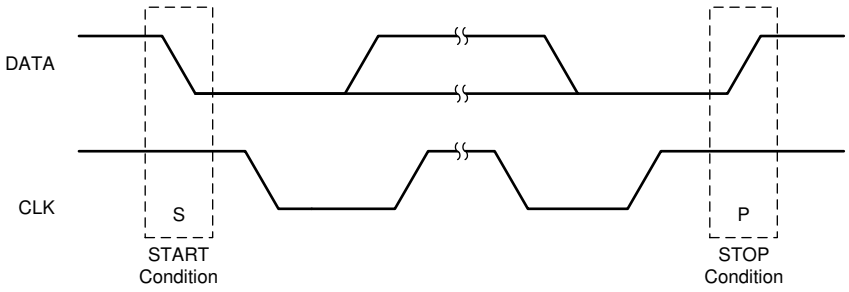


Figure 7-4. START and STOP Conditions

The controller then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit, R/W, on the SDA line. During all transmissions, the controller ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 7-5). All devices recognize the address sent by the controller and compare it to their internal fixed addresses. Only the target device with a matching address generates an acknowledge (see Figure 7-6) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that communication link with a target has been established.

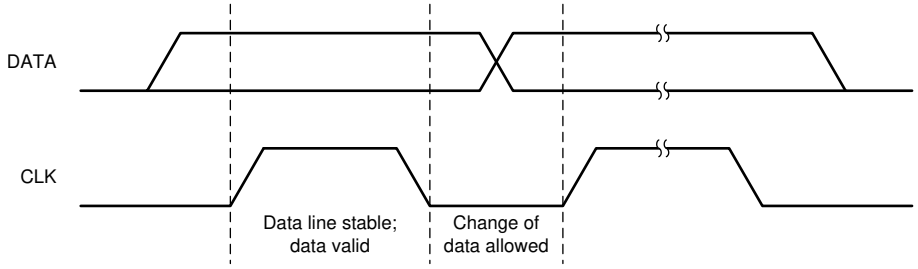


Figure 7-5. Bit Transfer on the Serial Interface

The controller generates further SCL cycles to either transmit data to the target (R/W bit 1) or receive data from the target (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 7-4). This low level to high level transition on the SDA line when the SCL is at high releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

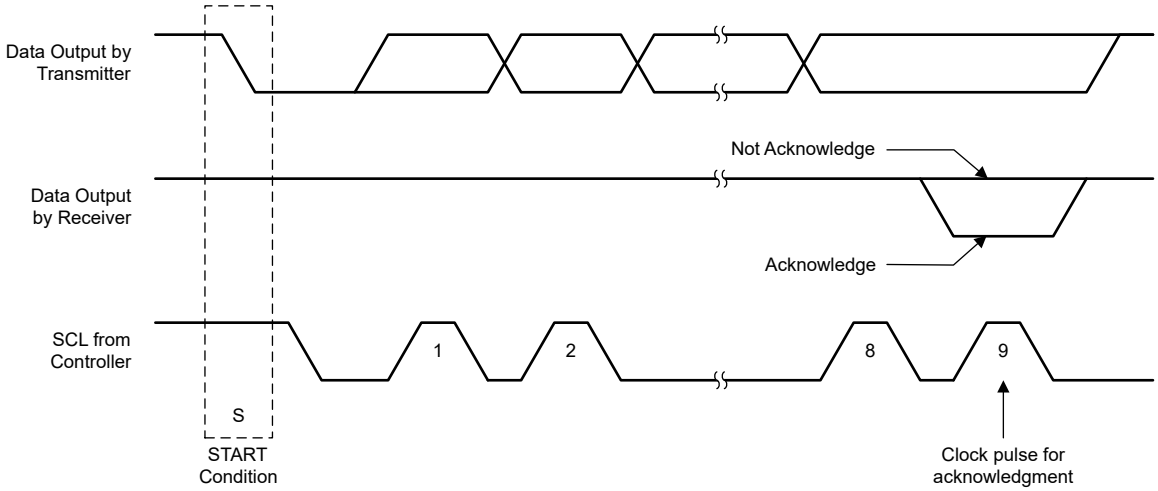


Figure 7-6. Acknowledge on the I^2C Bus

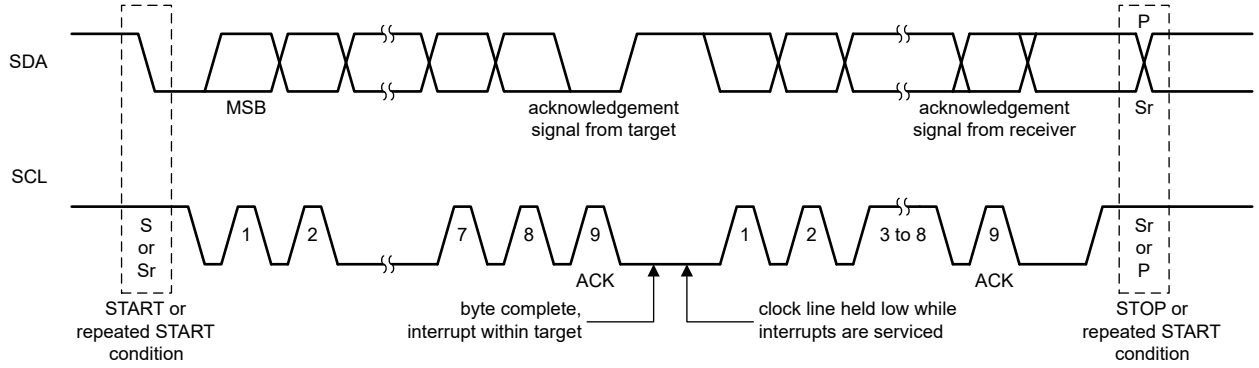


Figure 7-7. Bus Protocol

7.5.3 I²C Update Sequence

A single update requires the following:

- A start condition
- A valid I²C target address
- A register address
- A data byte

To acknowledge the receipt of each byte, the device pulls the SDA line low during the high period of a single clock pulse. The device performs an update on the falling edge of the acknowledge signal that follows the last byte.

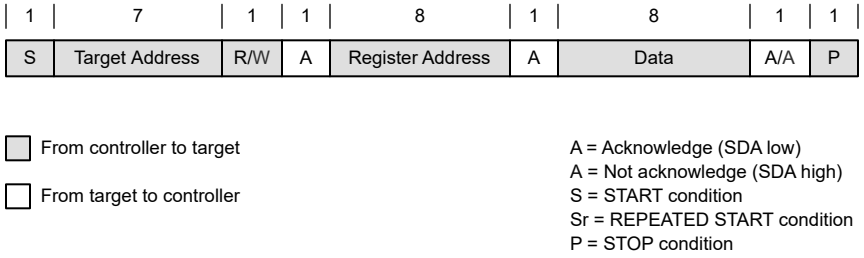


Figure 7-8. "Write" Data Transfer Format in Standard, Fast, and Fast-Plus Modes

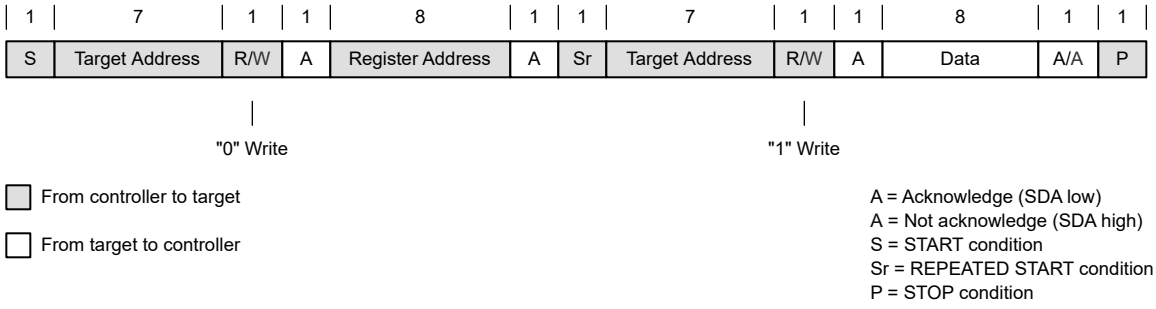


Figure 7-9. "Read" Data Transfer Format in Standard, Fast, and Fast-Plus Modes

7.6 Register Map

7.6.1 Register Description

7.6.1.1 Register Map

Table 7-2. Register Map

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0x02	CONTROL1	Control 1 Register	Go
0x03	VOUT	VOUT Register	Go
0x05	CONTROL2	Control 2 Register	Go

7.6.1.2 Register CONTROL1 (Register address: 0x02; Default: 0x08)

Return to Register Map

Table 7-3. Register CONTROL1 Format

7	6	5	4	3	2	1	0
NIL[3:0]				EN_FAST_DVS	EN_SCP	NIL	CONVERTER_EN
R				R/W	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only

SCP: Short Circuit Protection

Table 7-4. Register CONTROL1 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	NIL[3:0]	R	0b0000	Not used. During write operations data for these bits are ignored. During read operations 0 is returned
3	EN_FAST_DVS	R/W	0b1	Sets DVS to fast mode 0 : DISABLE, 1 : ENABLE
2	EN_SCP	R/W	0b0	Enable short circuit hiccup protection 0 : DISABLE, 1 : ENABLE
1	NIL	R	0b0	Not used.
0	CONVERTER_EN	R/W	0b0	Enable Converter ('AND'ed with EN-pin) 0 : DISABLE, 1 : ENABLE

7.6.1.3 Register VOUT (Register address: 0x03; Default: 0x5C)

Return to Register Map

Table 7-5. Register VOUT Format

7	6	5	4	3	2	1	0
VOUT[7 :0]							
R/W							

LEGEND: R/W = Read/Write

Table 7-6. Register VOUT Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT[7:0]	R/W	0x5C	These bits set the output voltage Output voltage = 1.000 + (VOUT[7 :0] × 0.025) V when 0x00<=VOUT[7 :0]<=0xB4; Output voltage = 5.5 V when 0xB5<=VOUT[7 :0]<=0xFF

7.6.1.4 Register CONTROL2 (Register address: 0x05; Default: 0x45)

Return to Register Map

Table 7-7. Register CONTROL2 Format

7	6	5	4	3	2	1	0
FPWM	FAST_RAMP_EN	EN_DISCH_VOUT[1:0]		CL_RAMP_MIN	TD_RAMP[2:0]		
R/W	R/W	R/W		R/W	R/W		

LEGEND: R/W = Read/Write

Table 7-8. Register CONTROL2 Field Descriptions

Bit	Field	Type	Reset	Description
7	FPWM	R/W	0b0	Force PWM operation 0 : DISABLE, 1 : ENABLE
6	FAST_RAMP_EN	R/W	0b1	Device can start-up faster than VOUT ramp 0 : DISABLE, 1 : ENABLE
5:4	EN_DISCH_VOUT[1:0]	R/W	0b00	Enable of BUBO Vout Discharge 00 : DISABLE 01 : SLOW (34mA) 10 : MEDIUM (67mA) 11 : FAST (100mA)
3	CL_RAMP_MIN	R/W	0b0	Define the minimum current limit during the soft start ramp 0 : Low (500mA) 1 : High (2x Low)
2:0	TD_RAMP[2:0]	R/W	0b101	Defines the ramp time for the Vo soft start ramp 000: 0.256ms 001: 0.512ms 010: 1.024ms 011: 1.920ms 100: 3.584ms 101: 7.552ms 110: 9.600ms 111: 24.320ms

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS631012 and TPS631013 are high-efficiency, low-quiescent current, buck-boost converters. The devices are suitable for applications needing a regulated output voltage from an input supply that can be higher or lower than the output voltage.

8.2 Typical Application

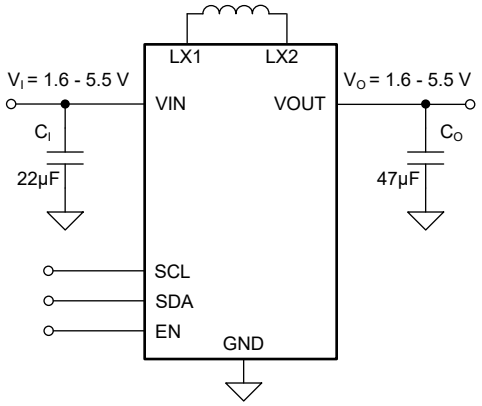


Figure 8-1. 3.3-V_{OUT} Typical Application

8.2.1 Design Requirements

The design parameters are listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETERS	VALUES
Input voltage	2.7 V to 4.3 V
Output voltage	3.3 V
Output current	1.5 A

8.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, Section 6.3 outlines minimum and maximum values for inductance and capacitance. Pay attention to the tolerance and derating when selecting nominal inductance and capacitance.

8.2.2.1 Inductor Selection

The inductor selection is affected by several parameters such as the following:

- Inductor ripple current
- Output voltage ripple
- Transition point into power save mode
- Efficiency

See Table 8-2 for typical inductors.

For high efficiencies, the inductor with a low DC resistance is needed to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. Core losses need to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 2. Only the equation that defines the switch current in boost mode is shown because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{2}$$

where:

- D = duty cycle in boost mode
- *f* = converter switching frequency (typical 2 MHz)
- L = inductor value
- η = estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption)

Note

The calculation must be done for the minimum input voltage in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated using Equation 2. Possible inductors are listed in Table 8-2.

Table 8-2. List of Recommended Inductors

INDUCTOR VALUE [µH]	SATURATION CURRENT [A]	DCR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (L × W × H mm)
1	4.3	42	DFE252012P-1R0M=P2	MuRata	2.5 × 2.0 × 1.2
1	4.2	43	HTEK20161T-1R0MSR	Cyntec	2.0 × 1.6 × 1.0
1	2.2	75	MAKK2016T1R0M (2)	Taiyo Yuden	2.0 × 1.6 × 1.0
1	2.0	144	DFE18SAN1R0ME0 (2)	Murata	1.6 × 0.8 × 0.8

(1) See the Section 9.1.1.
(2) This inductor does not support full output current range.

8.2.2.2 Output Capacitor Selection

For the output capacitor, use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. The recommended total nominal output capacitor value is 47 µF. If, for any reason, the application requires the use of large capacitors that cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor, and place the small capacitor as close as possible to the VOUT and PGND pins of the IC.

It is important that the effective capacitance is given according to the recommended value in Section 6.3. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a tradeoff between size and transient behavior as higher capacitance reduces transient response over/undershoot and increases transient response time. Possible output capacitors are listed in Table 8-3.

Table 8-3. List of Recommended Capacitors

CAPACITOR VALUE [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (METRIC)
47	6.3	10	GRM219R60J476ME44	Murata	0805 (2012)
47	10	40	CL10A476MQ8QRN	Semco	0603 (1608)

(1) See the Section 9.1.1.

8.2.2.3 Input Capacitor Selection

A 22-µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

Table 8-4. List of Recommended Capacitors

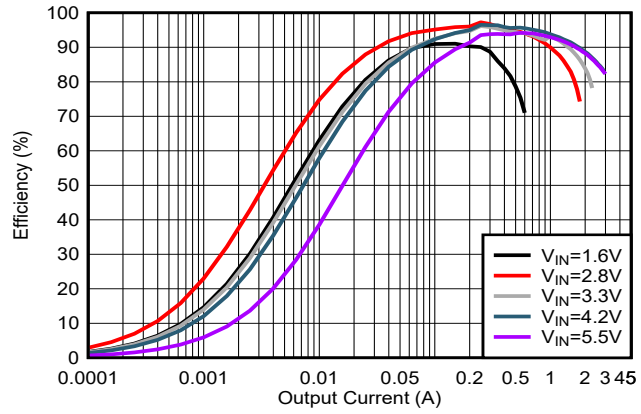
CAPACITOR VALUE [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (METRIC)
22	6.3	43	GRM187R61A226ME15	Murata	0603 (1608)
10	10	40	GRM188R61A106ME69	Murata	0603 (1608)

(1) See the Section 9.1.1.

8.2.2.4 Setting the Output Voltage

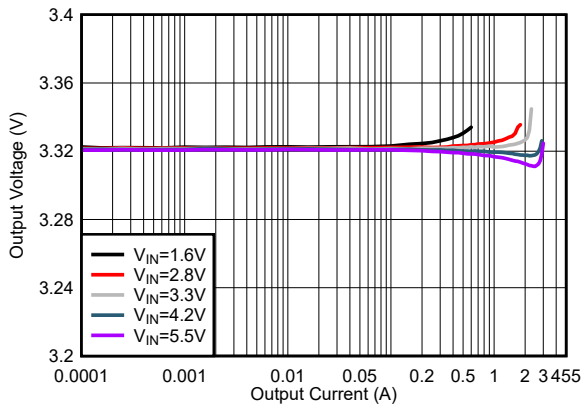
The output voltage is set by I^2C. Please refer to the part of Output Voltage Control for the detailed output voltage settings.

8.2.3 Application Curves



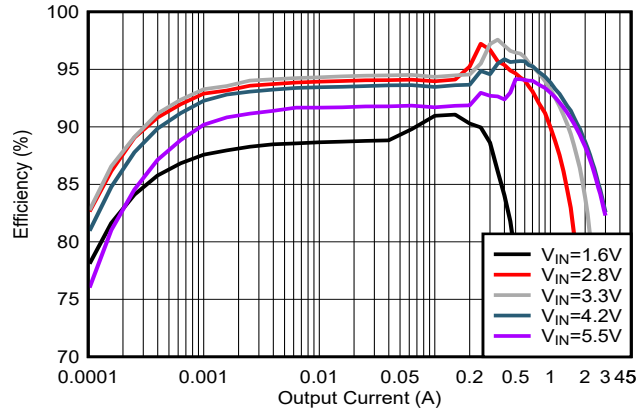
V_{OUT} = 3.3V FPWM

Figure 8-2. Efficiency vs Output Current (FPWM)



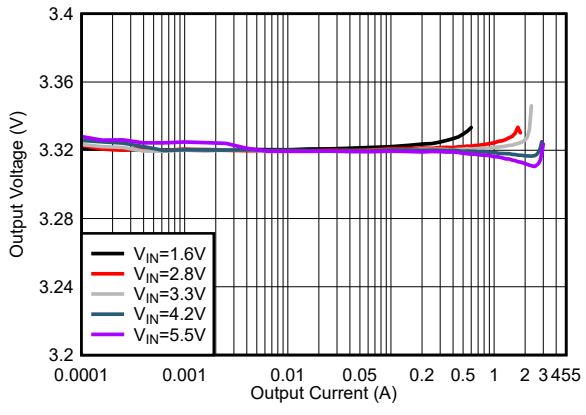
V_{OUT} = 3.3V FPWM

Figure 8-3. Load Regulation (FPWM)



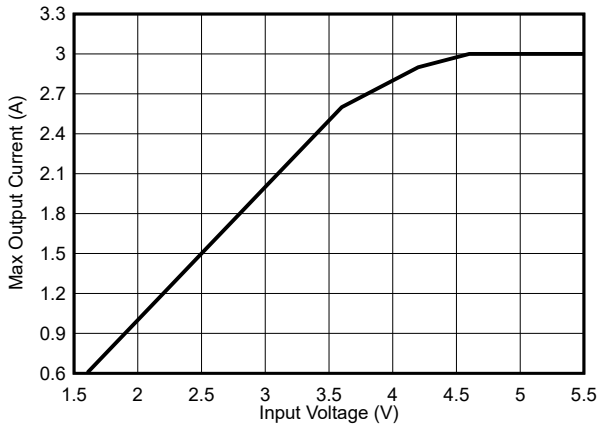
V_{OUT} = 3.3V PFM

Figure 8-4. Efficiency vs Input Voltage (PFM)



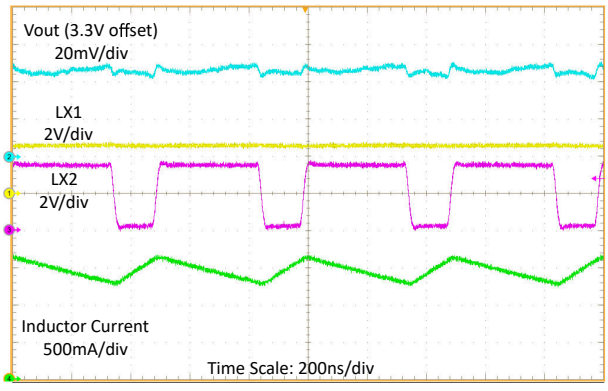
V_O = 3.3V PFM

Figure 8-5. Load Regulation (PFM)



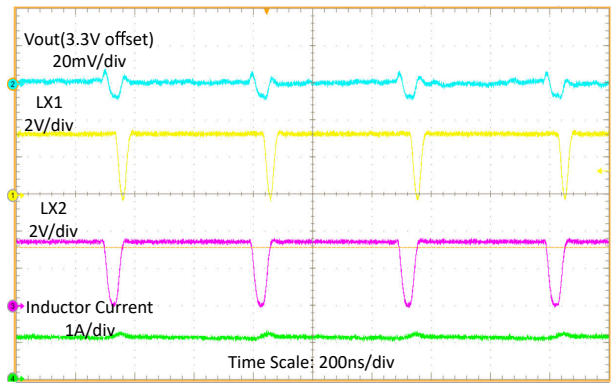
V_{OUT} = 3.3V

Figure 8-6. Typical Output Current Capability vs Input Voltage



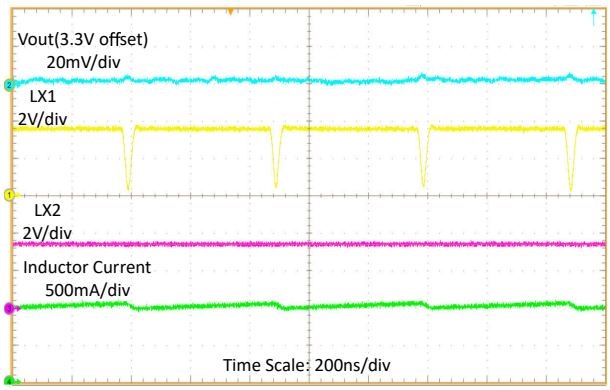
V_{IN} = 2.7V, V_{OUT} = 3.3V I_{OUT} = 1A, PFM

Figure 8-7. Switching Waveforms, Boost Operation with 1A Load



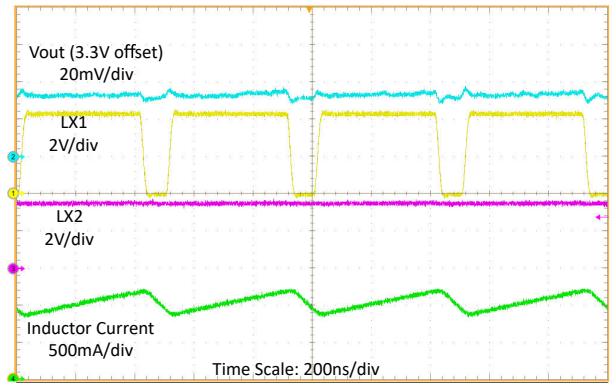
V_{IN} = 3.4V, V_{OUT} = 3.3V I_{OUT} = 1A, FPWM

Figure 8-8. Switching Waveforms, Buck-Boost Operation with 1A Load



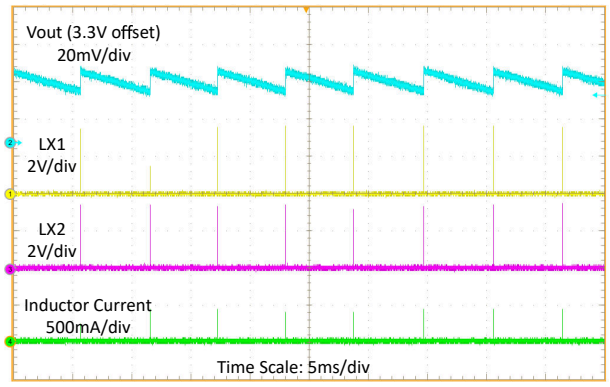
V_{IN} = 3.6V, V_{OUT} = 3.3gV I_{OUT} = 1A, PFM

Figure 8-9. Switching Waveforms, Buck Operation with 1-A Load



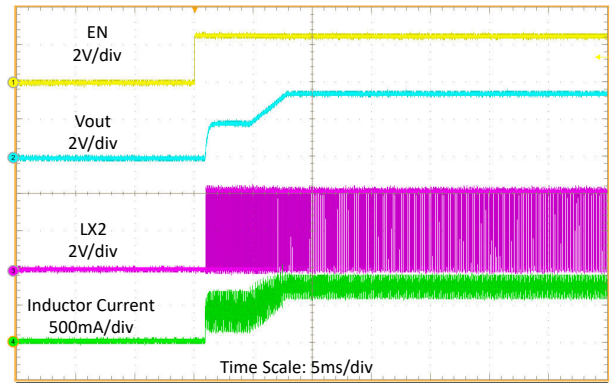
V_{IN} = 4.3V, V_{OUT} = 3.3V I_{OUT} = 1A, PFM

Figure 8-10. Switching Waveforms, Buck Operation with 1A Load



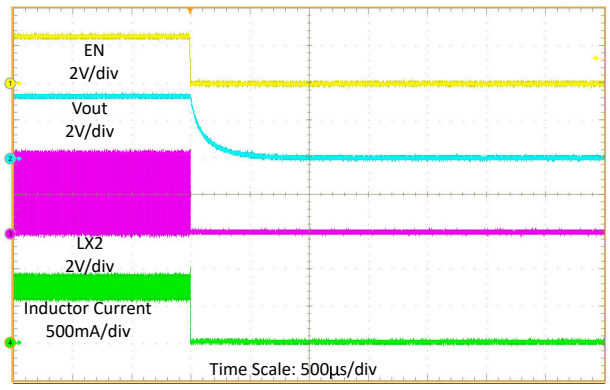
V_{IN} = 3.6V, V_{OUT} = 3.3V I_{OUT} = 1mA, PFM

Figure 8-11. Switching Waveforms at 1mA Load



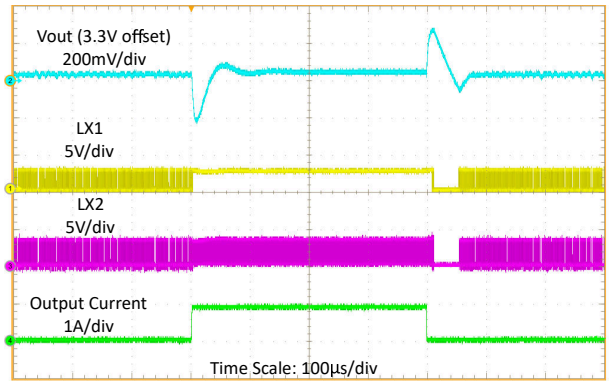
V_{IN} = 3.3V, V_{OUT} = 3.3V R_{load} = 4Ω, PFM

Figure 8-12. Start-Up by EN (Measured on TPS631013)



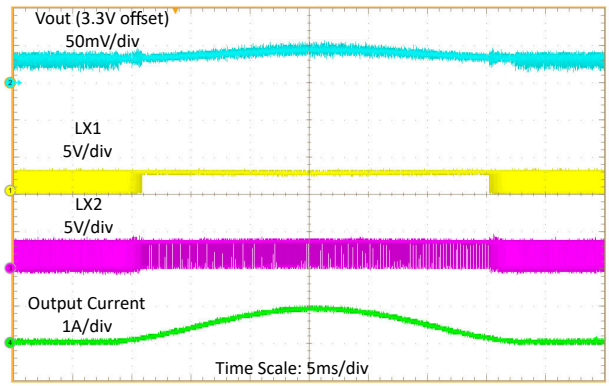
V_{IN} = 3.3V, V_{OUT} = 3.3V R_{load} = 4Ω, PFM

Figure 8-13. Shutdown by EN



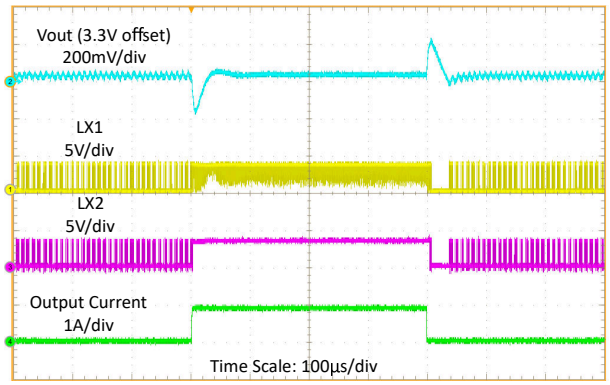
V_{IN} = 2.7V, V_{OUT} = 3.3V I_{OUT} = 100mA to 1A with 20µs slew rate

Figure 8-14. Load Transient at 2.7V Input Voltage



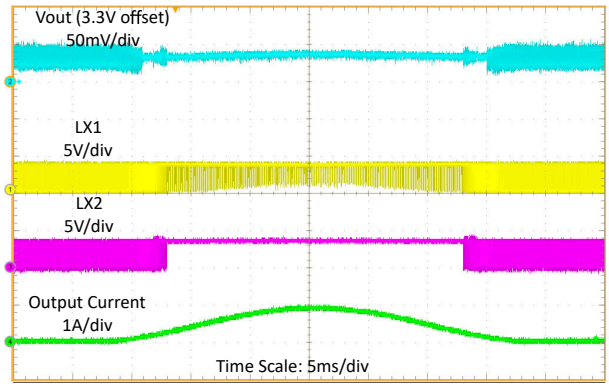
V_{IN} = 2.7V, V_{OUT} = 3.3V I_{OUT} = 100mA to 1A sweep

Figure 8-15. Load Sweep at 2.7V Input Voltage



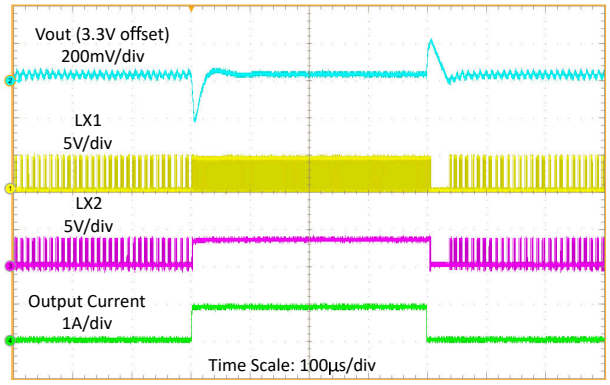
V_{IN} = 3.6V, V_{OUT} = 3.3V I_{OUT} = 100mA to 1A with 20µs slew rate

Figure 8-16. Load Transient at 3.6V Input Voltage



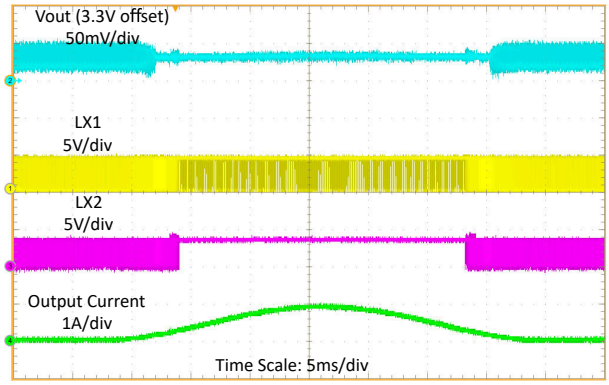
V_{IN} = 3.6V, V_{OUT} = 3.3V I_{OUT} = 100mA to 1A sweep

Figure 8-17. Load Sweep at 3.6V Input Voltage



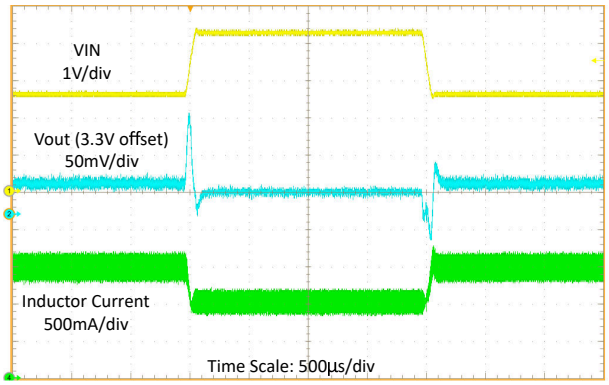
V_{IN} = 4.3V, V_{OUT} = 3.3V I_{OUT} = 100mA to 1A with 20µs slew rate

Figure 8-18. Load Transient at 4.3V Input Voltage



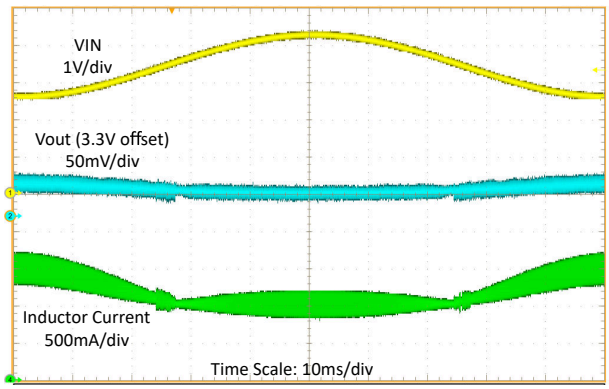
V_{IN} = 4.3V, V_{OUT} = 3.3V I_{OUT} = 100mA to 1A sweep

Figure 8-19. Load Sweep at 4.3V Input Voltage



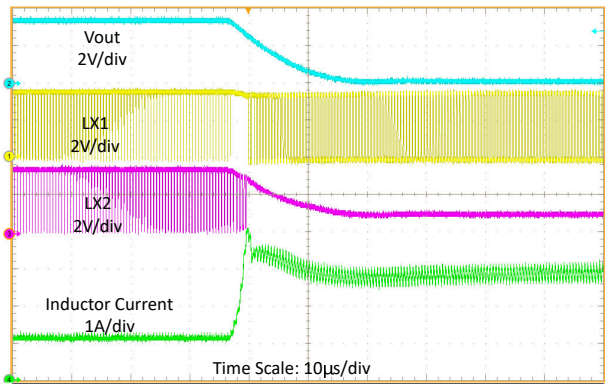
V_{IN} = 2.7V to 4.3V with 20µs slew rate, V_{OUT} = 3.3V I_{OUT} = 1A

Figure 8-20. Line Transient at 1A Load Current



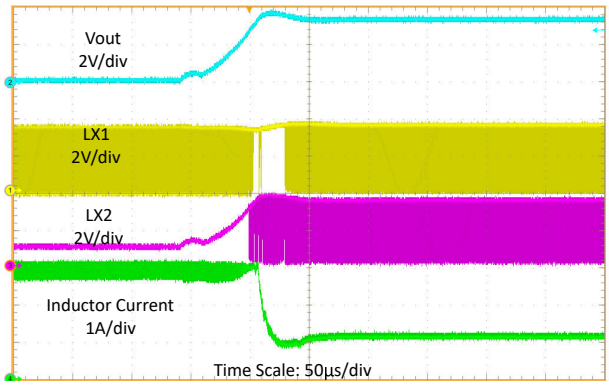
V_{IN} = 2.7V to 4.3V sweep, V_{OUT} = 3.3V I_{OUT} = 1A

Figure 8-21. Line Sweep at 1A Load Current



V_{IN} = 3.6V, V_{OUT} = 3.3V I_{OUT} = 1A, FPWM

Figure 8-22. Output Short Protection (Entry)



V_{IN} = 3.6V, V_{OUT} = 3.3V I_{OUT} = 1A, FPWM

Figure 8-23. Output Short Protection (Recover)

Table 8-5. Components for Application Characteristic Curves for V_{OUT} = 3.3V

REFERENCE	DESCRIPTION (2)	PART NUMBER	MANUFACTURER(1)
U1	High Power Density 1.5A Buck-Boost Converter	TPS631012 or TPS631013	Texas Instruments
L1	1.0µH, 2.5mm x 2.0mm, 4.3A, 42mΩ	DFE252012P-1R0M=P2	MuRata
C1	22 µF, 0603, Ceramic Capacitor, ±20%, 6.3V	GRM187R61A226ME15	Murata
C2	47µF, 0805, Ceramic Capacitor, ±20%, 6.3V	GRM219R60J476ME44	Murata

(1) See the Section 9.1.1.
(2) For other output voltages, refer to for resistor values.

8.3 Power Supply Recommendations

The TPS631012 and TPS631013 have no special requirements for its input power supply. The input power supply output current needs to be rated according to the supply voltage, output voltage, and output current.

8.4 Layout

8.4.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the device.

- Place input and output capacitors as close as possible to the IC. Traces need to be kept short. Route wide and direct traces to the input and output capacitors results in low trace resistance and low parasitic inductance.
- The sense trace connected to FB is signal trace. Keep these traces away from LX1 and LX2 nodes.

8.4.2 Layout Example

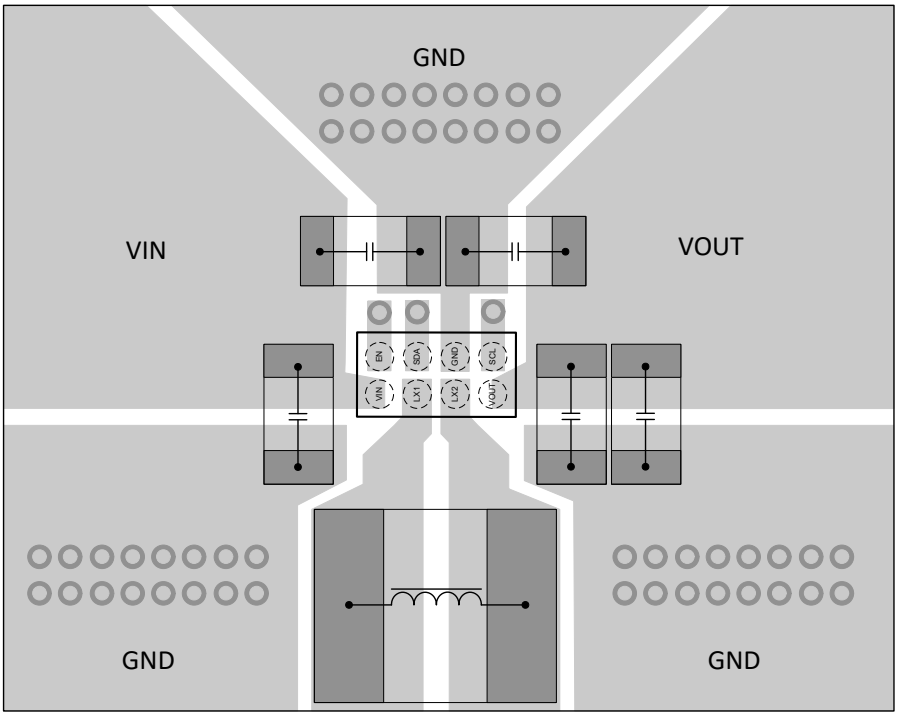


Figure 8-24. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

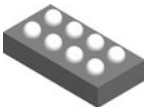
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2023) to Revision A (January 2025)	Page
• Updated mechanical data	27

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Mechanical Data

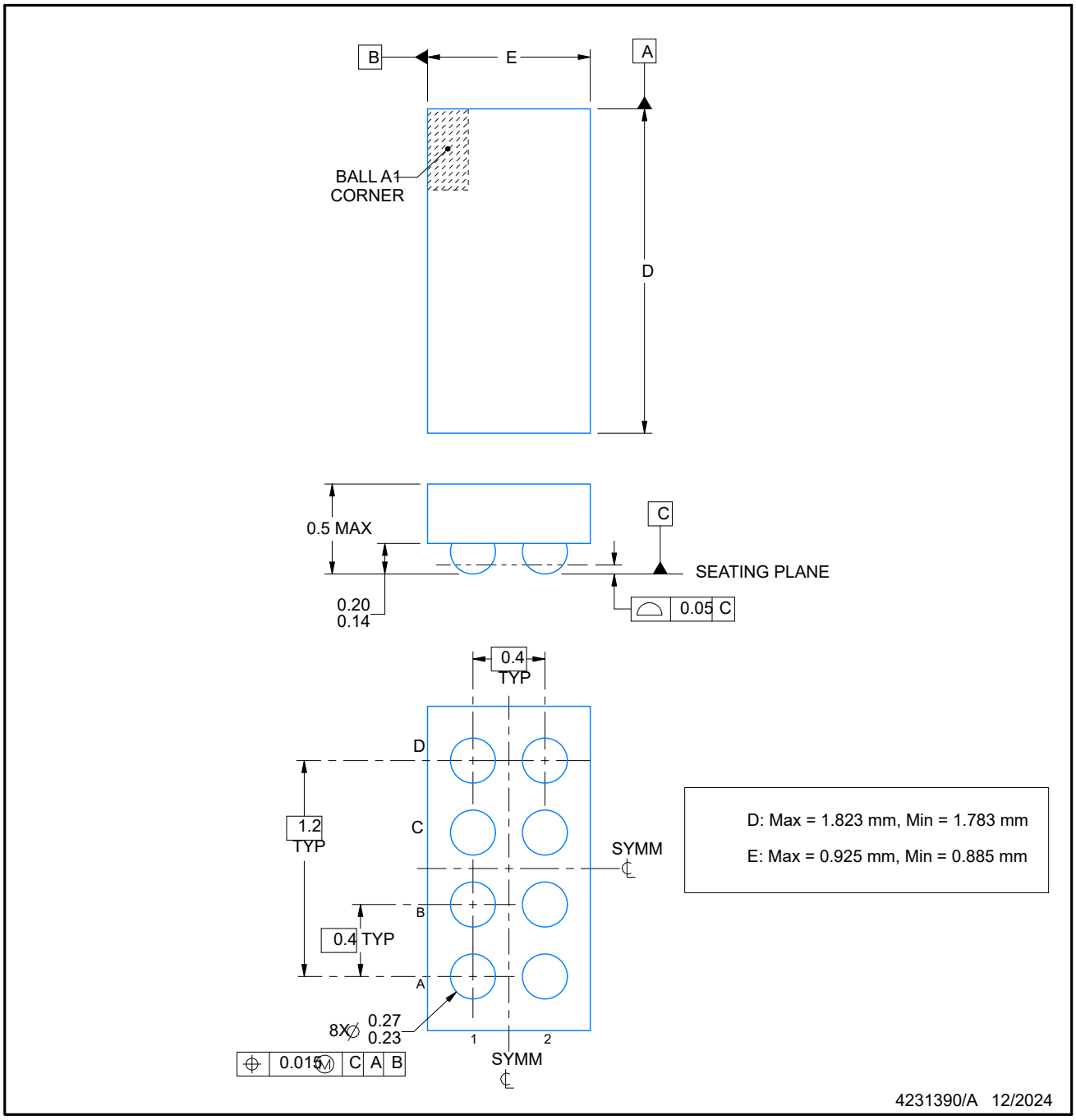


PACKAGE OUTLINE

YBG0008-C02

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

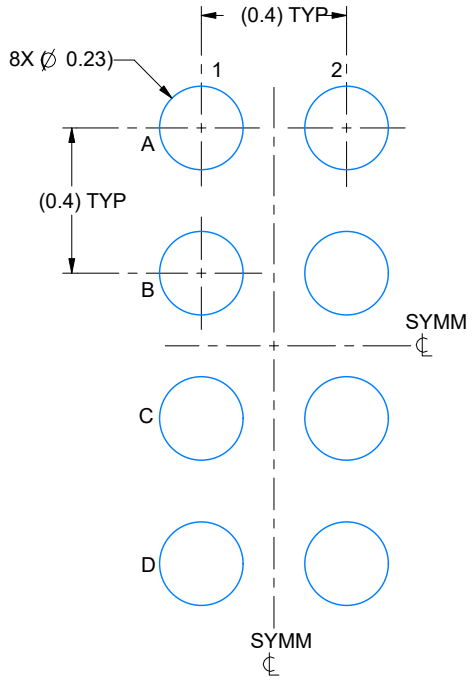
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

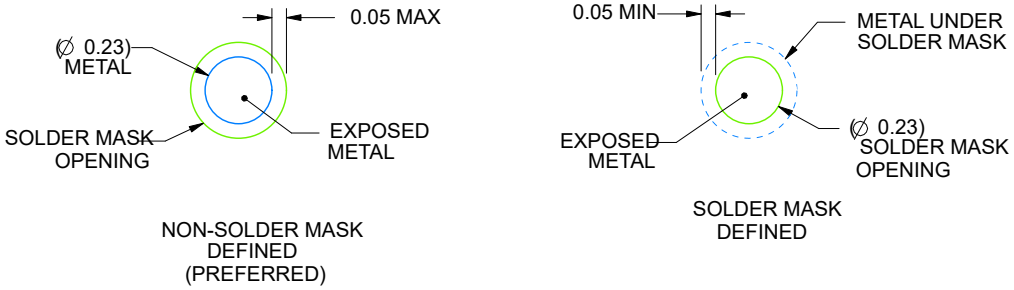
YBG0008-C02

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4231390/A 12/2024

NOTES: (continued)

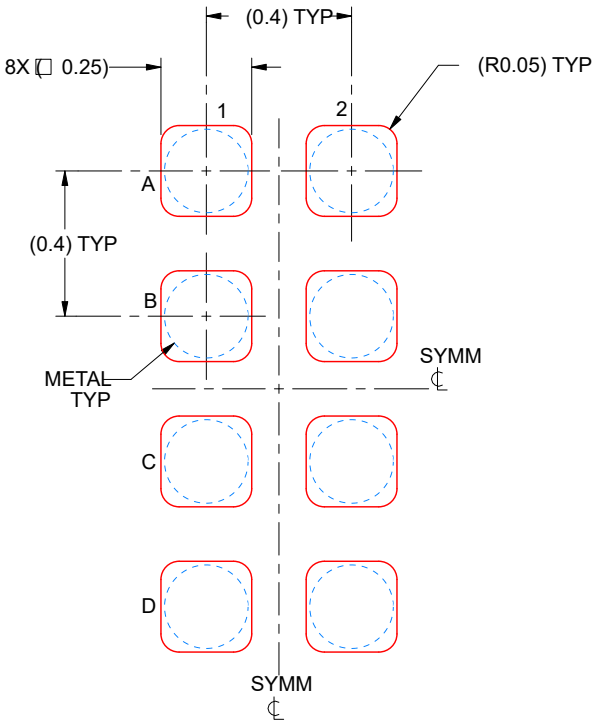
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBG0008-C02

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4231390/A 12/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS631012YBGR	ACTIVE	DSBGA	YBG	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1OL	Samples
TPS631013YBGR	ACTIVE	DSBGA	YBG	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1P7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

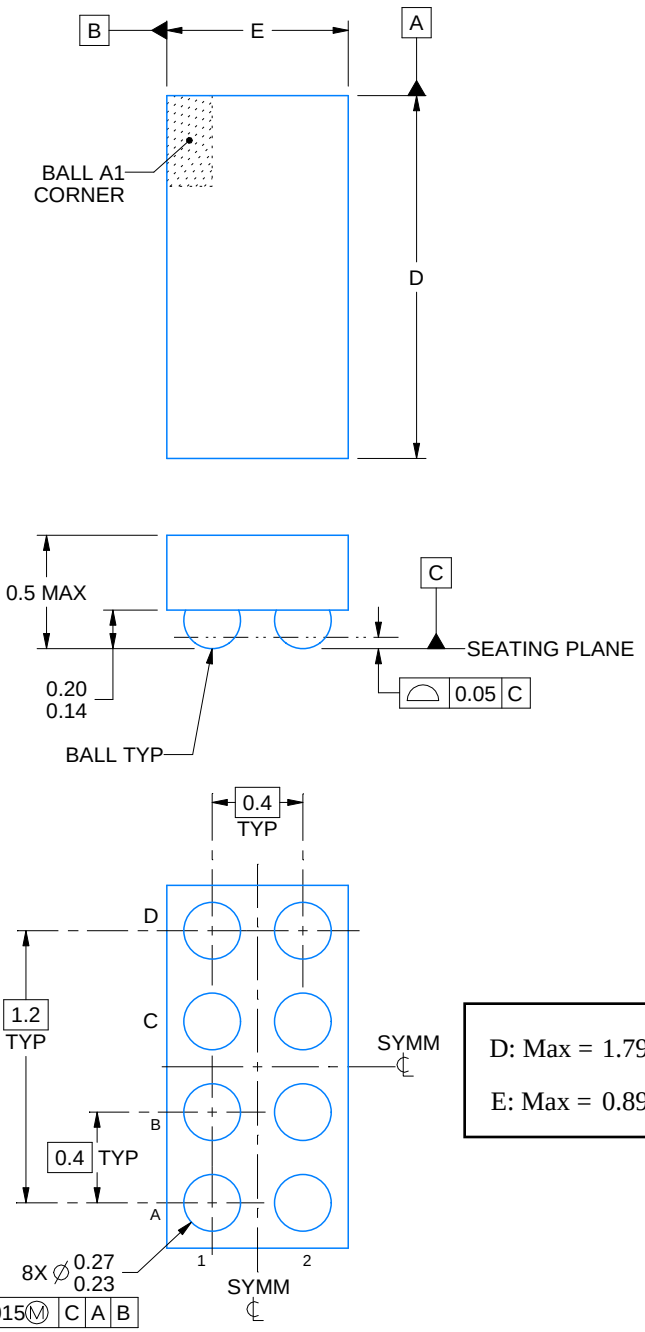
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

YBG0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.793 mm, Min =1.733 mm

E: Max = 0.895 mm, Min =0.835 mm

4224718/A 12/2018

NOTES:

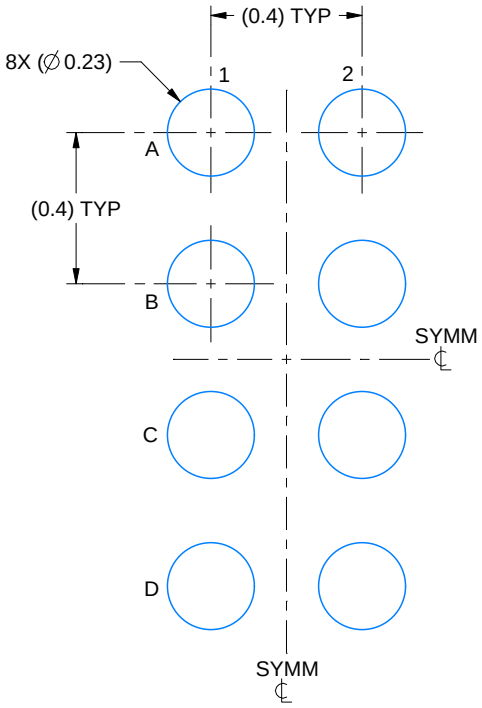
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

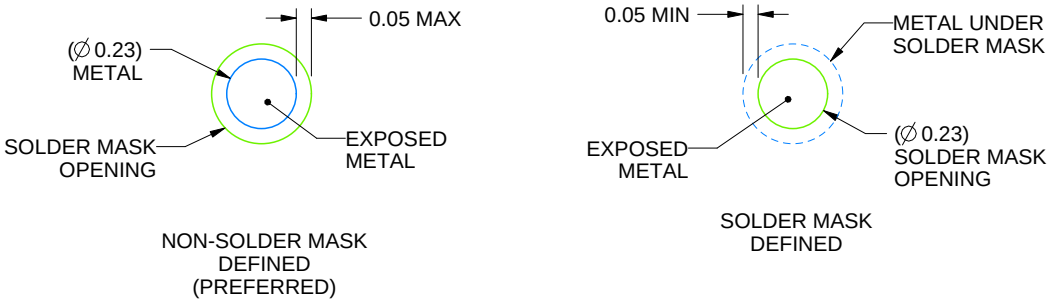
YBG0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

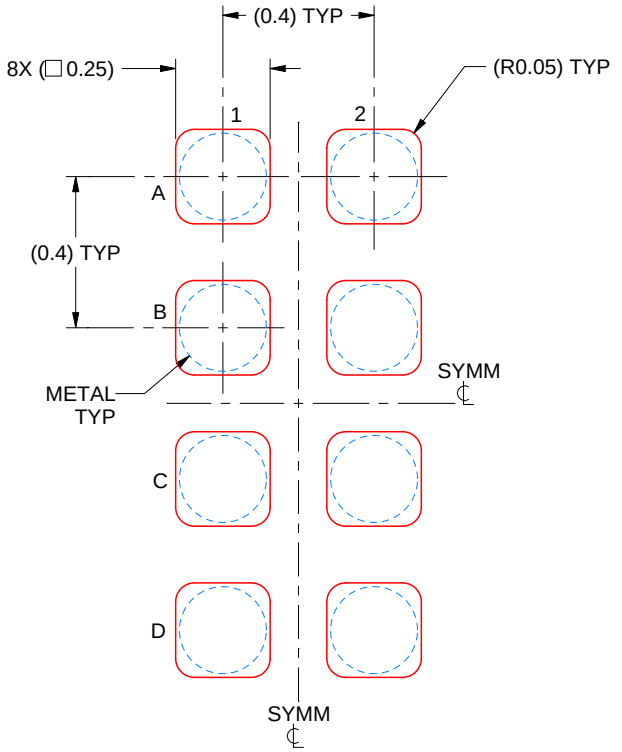


SOLDER MASK DETAILS
NOT TO SCALE

4224718/A 12/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4224718/A 12/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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