TPS7C84-Q1 Automotive, 150mA, 40V, Adjustable, Low-Dropout Regulator With Power-Good

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: −40°C to +125°C, T_A
  - Junction temperature: −40°C to +150°C, T_J
- Wide input voltage range:
  - V_{IN} range: 2.1V to 40V
- Wide output voltage range (V_{OUT}):
  - Fixed option: 3.3V, 5.0V
  - Adjustable option: 1.2V to 39V
- Output current: Up to 150mA
- V_{OUT} accuracy:
  - ±1% over line, load, and temperature
- Quiescent current (I_Q) : 50μA (typical)
- Low dropout: 480mV (typical)
- Open-drain, power-good output
- Output current limiting and thermal shutdown
- Stable over a wide range of ceramic output capacitor values:
  - C_{OUT} range: 1μF to 100μF
  - ESR range: 0Ω to 2Ω
- Package options:
  - D (8-pin SOIC)
  - DRB (8-pin VSON)

2 Applications

- Traction inverters
- Body control modules (BCM)
- Onboard chargers
- Telematics controls

3 Description

The TPS7C84-Q1 is a wide input, low-dropout regulator (LDO) supporting a 2.1V to 40V input voltage range and up to 150mA of load current. The TPS7C84-Q1 outputs either a fixed or adjustable output. Fixed output options include 3.3V and 5V, or set the output between 1.2V to 39V with the adjustable device.

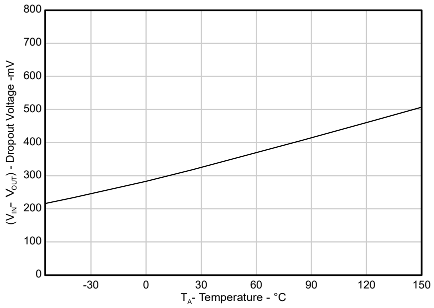
This device has a power-good (PG) output that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output are used for sequencing multiple power supplies in the system.

The TPS7C84-Q1 is designed for up to 40V V_{IN} battery-connected applications. With a very wide output voltage range, the device is designed for for powering microcontrollers and controller area networks and local interconnect network (CAN/LIN) transceivers. The device is also designed for providing bias supplies for gate drivers.

Package Information

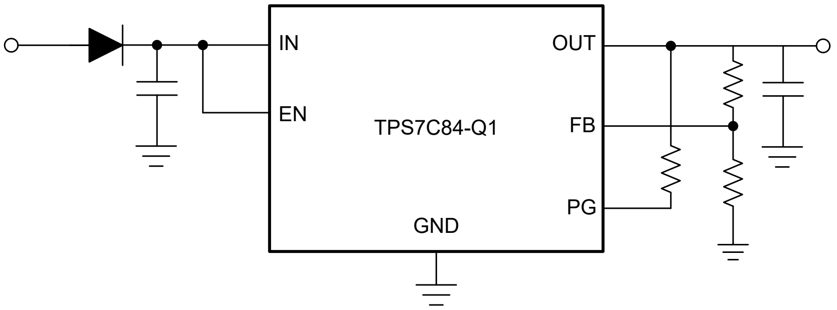
PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TPS7C84-Q1	D (SOIC, 8)	4.9mm × 6mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



V_{IN} = 4.9V, I_{OUT} = 150mA

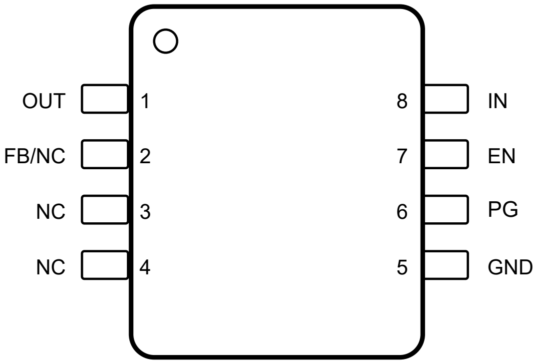
Dropout Voltage vs Temperature



Typical Application Circuit

Table of Contents

4 Pin Configuration and Functions



Not to scale

Figure 4-1. D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN	7	I	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). To make sure the device is enabled, drive the EN pin above the logic high level (V_{IH}). Do not leave this pin floating because this pin is high impedance. If this pin is left floating, the pin state becomes undefined and the device potentially enables or disables.
FB/NC	2	I	This pin is a feedback pin when using an external resistor divider or an NC pin when using the device with a fixed output voltage. When using the adjustable device, connect this pin through a resistor divider to the output for the device to function. See the *Feedback Resistor Selection* section for more information. If using a fixed output, leave this pin floating or connected to GND.
GND	5	—	Ground
IN	8	I	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section. Place the input capacitor as close to the input of the device as possible.
NC	3, 4	—	No internal connection. Leave this pin floating or tied to GND for best thermal performance.
OUT	1	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to GND[2]. Place the output capacitor as close to the device output as possible. See the *Input and Output Capacitor Requirements* section for more details.
PG	6	O	Active-high, open-drain power-good output. This pin goes low when V_{OUT} drops by 6% of the nominal value. The power-good feature is functional when the device is enabled ($V_{EN} > V_{IH}$).

(1) I = input; O = output.
(2) Make sure the nominal output capacitance is greater than 1μF. Throughout this document, the nominal derating on these capacitors is 50%. Verify that the effective capacitance at the pin is greater than 1μF.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN	Continuous input voltage	–0.3	42	V
OUT	Output voltage	–0.3	39	
EN	EN input voltage	–0.3	42	
PG	PG comparator output voltage(2)	–0.3	42	
FB	FEEDBACK input voltage	–0.3	5	
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

(2) Can exceed input supply voltage.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±3000	V
		Charged-device model (CDM), per AEC V Q100-011	All pins	±1000	
			Corner pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.1		40	V
V_{EN}	Enable voltage	0		40	V
V_{OUT}	Output voltage	1.2		39	V
I_{OUT}	Output current	0		150	mA
C_{OUT}	Output capacitor(1)	1	2.2	100	µF
C_{OUT} ESR	Output capacitor ESR	0		2	Ω
C_{IN}	Input capacitor		1		µF
C_{FF}	Feed-forward capacitor (optional(2), for adjustable device only)		10		pF
$I_{FB\_DIVIDER}$	Feedback divider current(2) (adjustable device only)	12			µA
T_J	Junction temperature	–40		150	°C

(1) Effective output capacitance of 0.5µF minimum required for stability.
(2) C_{FF} required for stability if the feedback divider current < 12µA. Feedback divider current = V_{OUT} / (R_1 + R_2). See the *Feed-Forward Capacitor (C_{FF})* section for details.

5.4 Thermal Information

THERMAL METRIC(1) (2)		D	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.8	°C/W

(1) The thermal data is based on the JEDEC standard high K profile,JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

at V_{IN} = V_{OUT} (nominal) + 1V, I_{OUT} = 100 µA, C_{OUT} = 2.2µF, V_{EN} ≥ 2V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage accuracy	V_{IN} = [$V_{OUT(NOM)}$ + 1V] to 40V, I_{OUT} = 100µA to 150mA	25°C	–0.5		0.5	%
			–40°C to 150°C	–1		1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	V_{IN} = [$V_{OUT(NOM)}$ + 1V] to 40V	–40°C to 150°C			0.2	%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	I_{OUT} = 100 µA to 150mA				0.2	%
V_{DO}	Dropout voltage	V_{IN} = 2.1V, I_{OUT} = 150mA			480	900	mV
		V_{IN} = 3.5V, I_{OUT} = 150mA			450	600	
		V_{IN}=V_{OUT}= 3.3V, I_{OUT} = 150mA				620	
		V_{IN}=V_{OUT}= 5V, I_{OUT} = 150mA				550	
I_Q	Quiescent current	I_{OUT} = 100µA			50	68	µA
		I_{OUT} = 150mA				3.2	mA
$I_{SHUTDOWN}$	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.7V, V_{IN} ≤ 40V, V_{OUT} = 0V	25°C		4	6	µA
			–40°C to 150°C			7.5	

5.5 Electrical Characteristics (continued)

at V_{IN} = V_{OUT} (nominal) + 1V, I_{OUT} = 100 µA, C_{OUT} = 2.2µF, V_{EN} ≥ 2V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
UVLO	UVLO V_{IN} rising	I_{OUT} = 100µA	–40°C to 150°C	1.8	1.9	2.0	V
	UVLO V_{IN} falling	I_{OUT} = 100µA		1.7	1.8	1.9	
	Hysteresis	I_{OUT} = 100µA			100		mV
I_{CL}	Current limit	V_{OUT} = 0V		165	225	280	mA
V_n	Output noise (RMS), 10Hz to 100KHz	C_{OUT} = 1µF (5V only)	25°C		265		µV
PSRR	Power supply ripple rejection	V_{IN} - V_{OUT} = 1V, frequency = 100Hz, I_{OUT} = 5mA	25°C		80		dB
I_{FB}	FEEDBACK bias current		25°C		5	10	nA
			–40°C to 150°C			15	
$V_{PG(OL)}$	PG pin low level output voltage	V_{IN} ≥ 2V, I_{OL} = 400µA	25°C		180	250	mV
			–40°C to 150°C			350	
$V_{PG(TH,RISING)}$	V_{OUT} rising		–40°C to 150°C			97	%V_{OUT}
$V_{PG(TH,FALLING)}$	V_{OUT} falling			92			
$V_{PG(HYST)}$	Hysteresis		25°C		2		
V_{IL}	Enable logic input low level	Low (regulator OFF)	–40°C to 150°C			0.7	V
V_{IH}	Enable logic input high level	High (regulator ON)		1.9			
I_{EN}	EN pin current	V_{EN} = 40V	–40°C to 150°C			1	µA

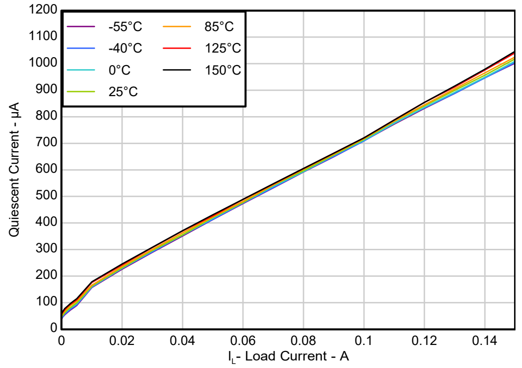
5.6 Timing Requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PGDH}	PG delay time rising, time from 92% V_{OUT} to 20% of PG (1)		40		µs
t_{PGDL}	PG delay time falling, time from 90% V_{OUT} to 80% of PG(1)		10		µs

(1) Output Overdrive = 10%

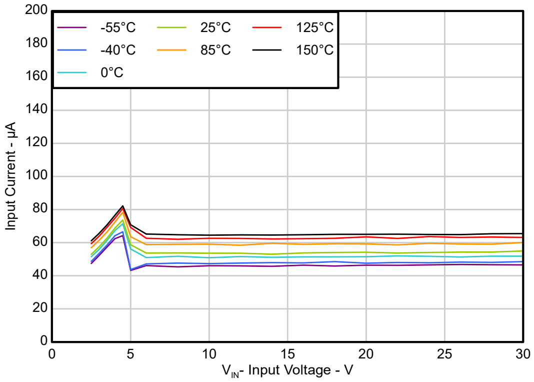
5.7 Typical Characteristics

at V_{IN} = V_{OUT} (nominal) + 1V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, and V_{EN} ≥ 2V (unless otherwise noted)



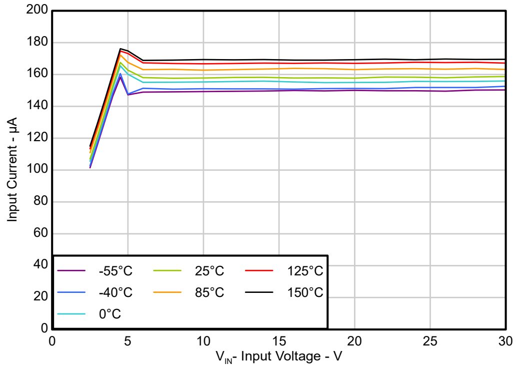
V_{IN} = 6V, V_{OUT} = 5V

Figure 5-1. Quiescent Current vs Load Current



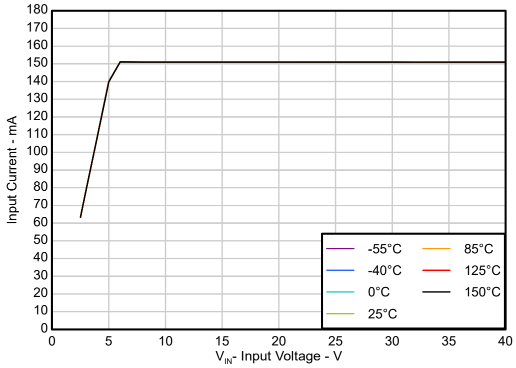
V_{OUT} = 5V, I_{OUT} = 0mA

Figure 5-2. Input Current vs Input Voltage



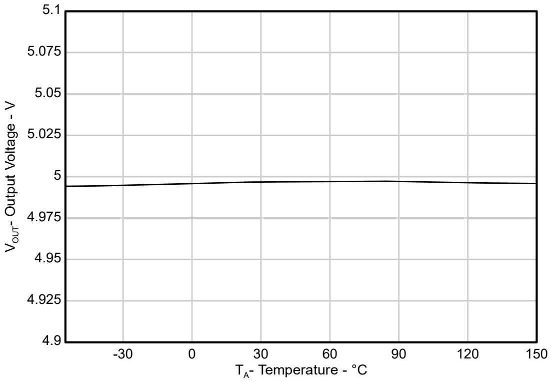
V_{OUT} = 5V, I_{OUT} = 100µA

Figure 5-3. Input Current vs Input Voltage



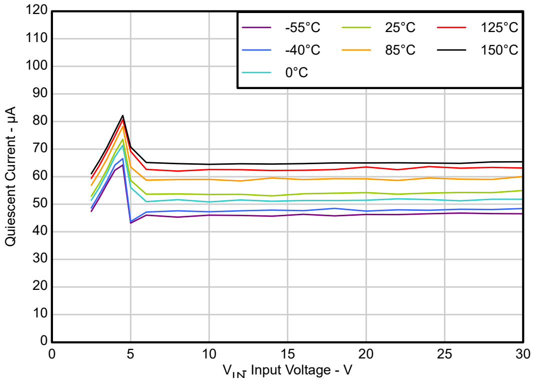
V_{OUT} = 5V, I_{OUT} = 150mA

Figure 5-4. Input Current vs Input Voltage



V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 150mA

Figure 5-5. Output Voltage vs Temperature

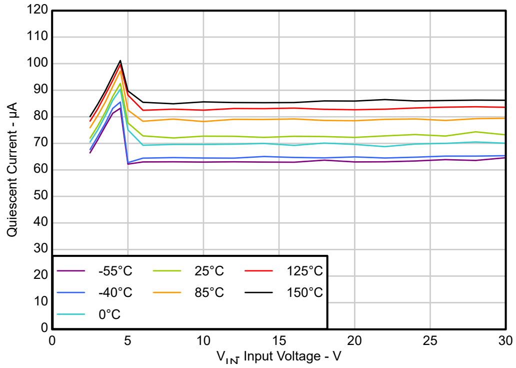


V_{OUT} = 5V

Figure 5-6. Quiescent Current vs Input Voltage (I_{OUT} = 0mA)

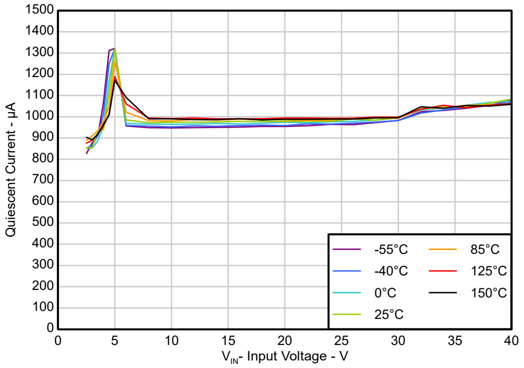
5.7 Typical Characteristics (continued)

at V_{IN} = V_{OUT} (nominal) + 1V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, and V_{EN} ≥ 2V (unless otherwise noted)



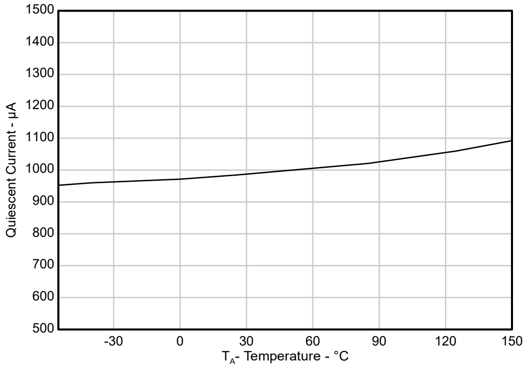
V_{OUT} = 5V

Figure 5-7. Quiescent Current vs Input Voltage (I_{OUT} = 1mA)



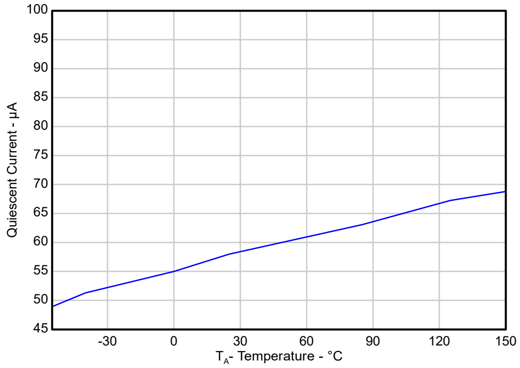
V_{OUT} = 5V

Figure 5-8. Quiescent Current vs Input Voltage (I_{OUT} = 150mA)



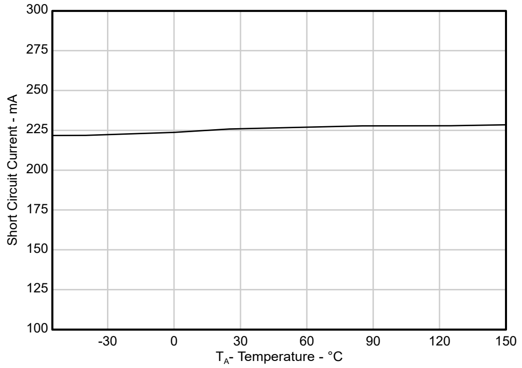
V_{IN} = 6V, V_{OUT} = 5V

Figure 5-9. Quiescent Current vs Temperature (I_{OUT} = 150mA)



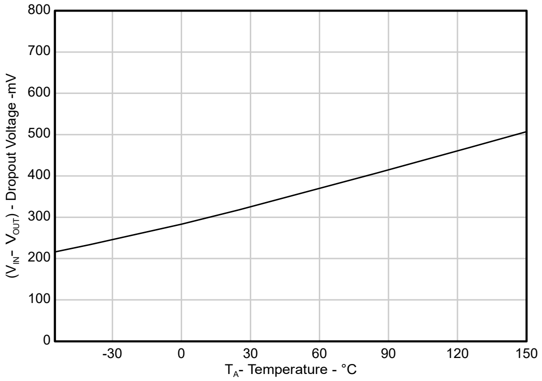
V_{IN} = 6V, V_{OUT} = 5V

Figure 5-10. Quiescent Current vs Temperature (I_{OUT} = 100µA)



V_{IN} = 6V, V_{OUT} = 0V

Figure 5-11. Short-Circuit Current vs Temperature

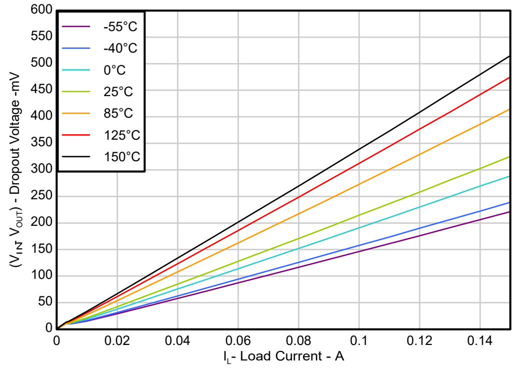


V_{IN} = 4.9V, I_{OUT} = 150mA

Figure 5-12. Dropout Voltage vs Temperature

5.7 Typical Characteristics (continued)

at V_{IN} = V_{OUT} (nominal) + 1V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, and V_{EN} ≥ 2V (unless otherwise noted)



V_{IN} = 4.9V

Figure 5-13. Dropout Voltage vs Output Current

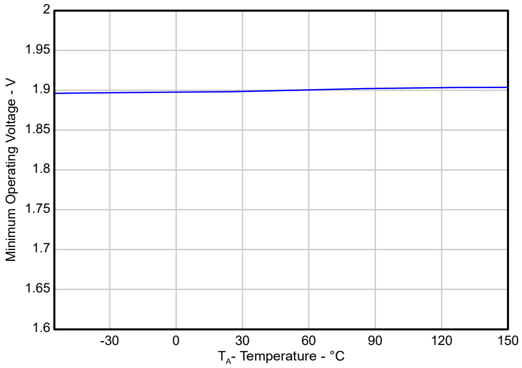


Figure 5-14. Minimum Operating Voltage vs Temperature

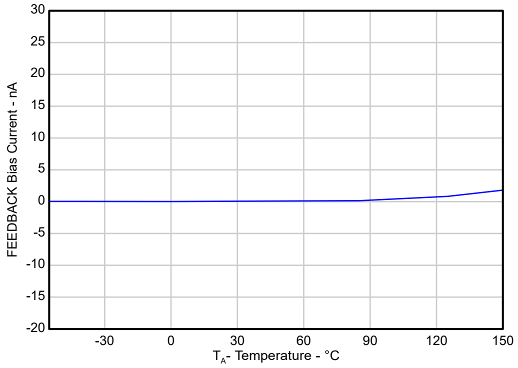


Figure 5-15. FB Bias Current vs Temperature

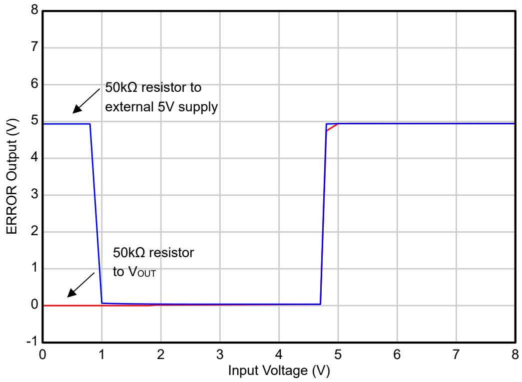


Figure 5-16. PG Comparator Output vs Input Voltage

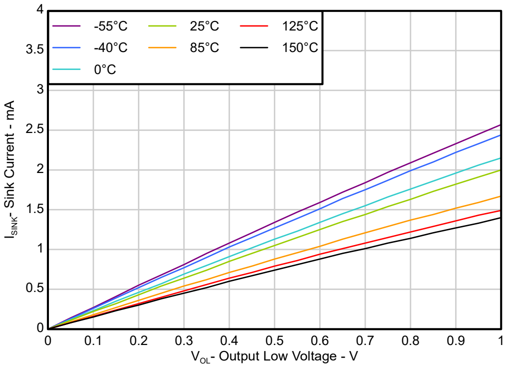


Figure 5-17. PG Comparator Sink Current vs Output Low Voltage

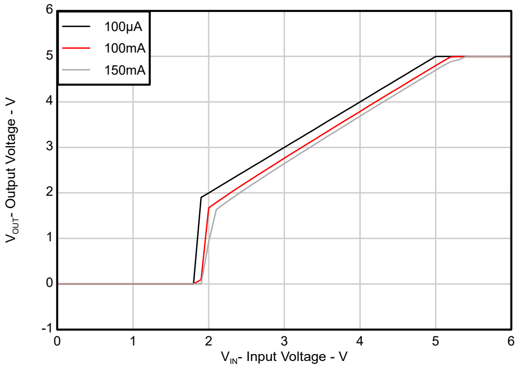
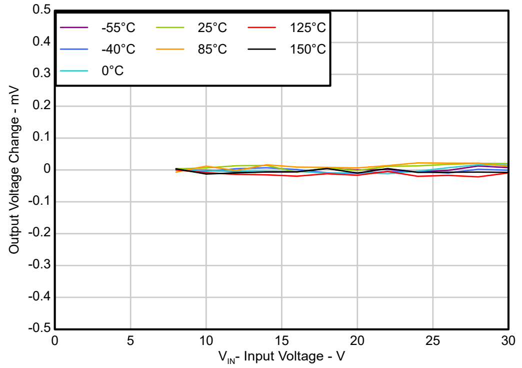


Figure 5-18. Output Voltage vs Input Voltage

ADVANCE INFORMATION

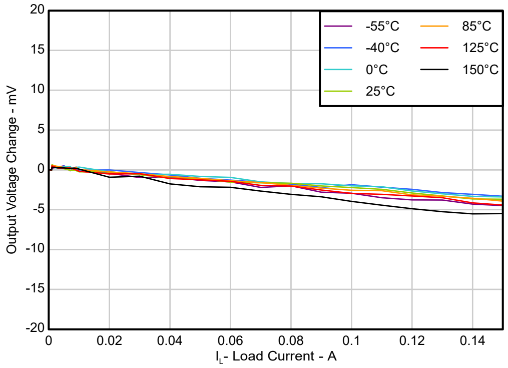
5.7 Typical Characteristics (continued)

at V_{IN} = V_{OUT} (nominal) + 1V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, and V_{EN} ≥ 2V (unless otherwise noted)



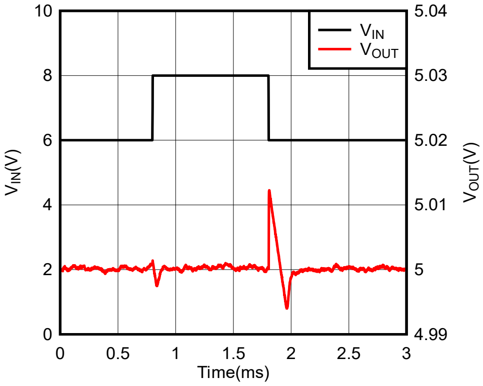
V_{OUT} = 5V, I_{OUT} = 100µA

Figure 5-19. Line Regulation vs Input Voltage



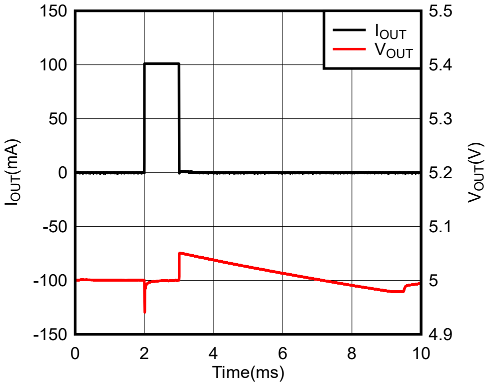
V_{IN} = 6V, V_{OUT} = 5V

Figure 5-20. Load Regulation vs Load Current



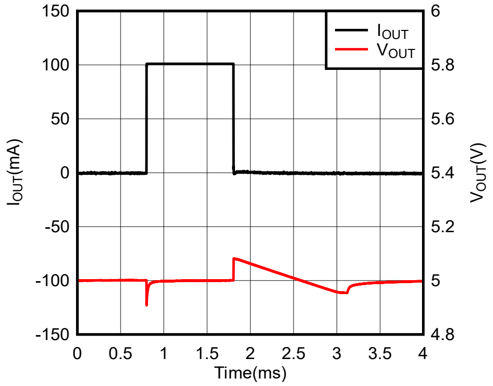
V_{IN} = 6V to 8V, V_{OUT} = 5V, C_{OUT} = 1µF, I_{OUT} = 100µA

Figure 5-21. Line Transient Response vs Time



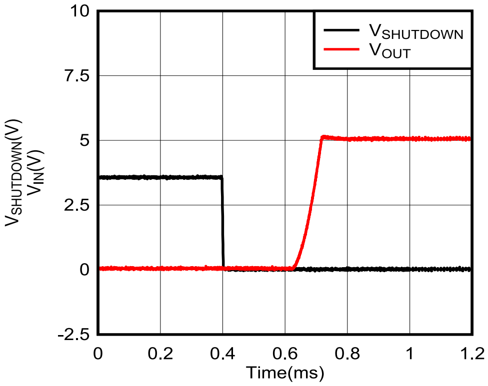
V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 0mA to 100mA, C_{OUT} = 10µF

Figure 5-22. Load Transient Response vs Time



V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 0mA to 100mA, C_{OUT} = 1µF

Figure 5-23. Load Transient Response vs Time

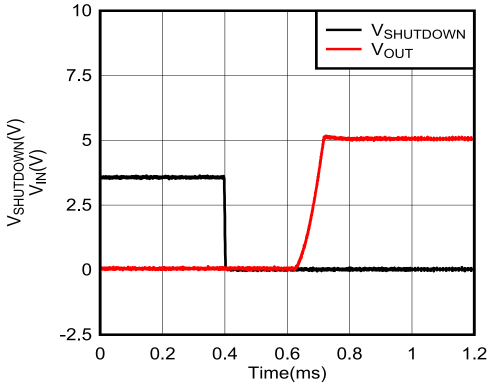


V_{IN} = 6V, V_{OUT} = 5V, C_{OUT} = 1µF, I_{OUT} = 1mA

Figure 5-24. Enable Transient Response vs Time

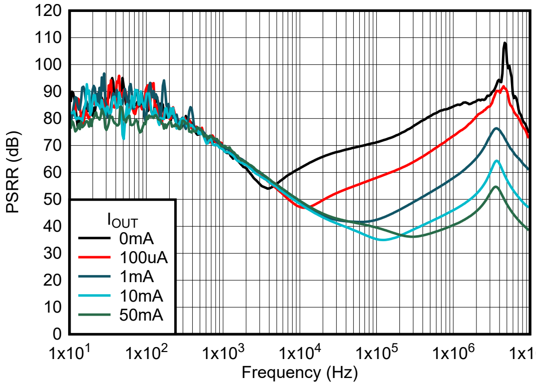
5.7 Typical Characteristics (continued)

at $V_{IN} = V_{OUT}$ (nominal) + 1V, I_{OUT} = 100μA, C_{OUT} = 2.2μF, and $V_{EN} \geq 2V$ (unless otherwise noted)



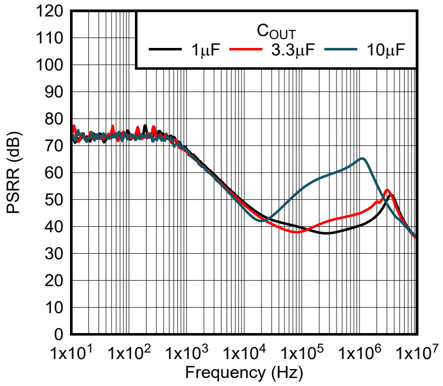
V_{IN} = 6V, V_{OUT} = 5V, C_{OUT} = 10μF, I_{OUT} = 1mA

Figure 5-25. Enable Transient Response vs Time



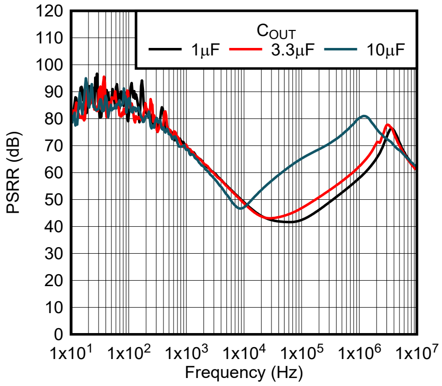
V_{IN} = 6V, V_{OUT} = 5V, C_{OUT} = 1μF

Figure 5-26. Ripple Rejection vs Frequency



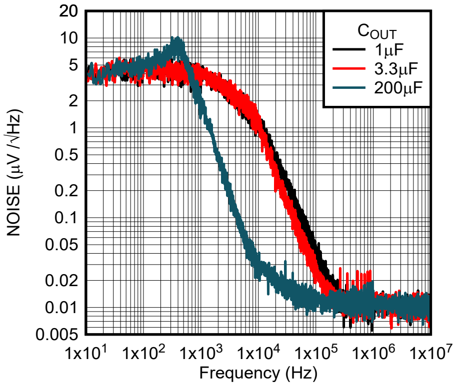
V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 100mA

Figure 5-27. Ripple Rejection vs Frequency



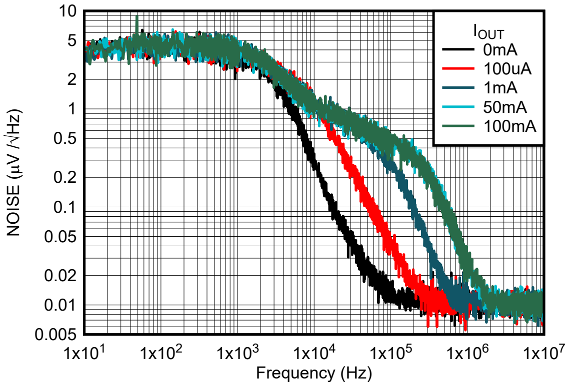
V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 1mA

Figure 5-28. Ripple Rejection vs Frequency



V_{IN} = 6V, V_{OUT} = 5V, I_{OUT} = 100μA

Figure 5-29. Output Noise vs Frequency



V_{IN} = 6V, V_{OUT} = 5V, C_{OUT} = 1μF

Figure 5-30. Output Noise vs Frequency

6 Detailed Description

6.1 Overview

The TPS7C84-Q1 is a low-dropout linear regulator (LDO) designed to connect to the battery in automotive applications. The device accommodates a wide input supply voltage range up to 40V. The TPS7C84-Q1 is available in 3.3V and 5V fixed output voltages. Alternatively, by connecting the FB pin to an external resistor divider, the output is able to be set to any value between 1.2V to 39V.

The TPS7C84-Q1 has a power-good output (PG) that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output are used for sequencing multiple power supplies in the system. The TPS7C84-Q1 is stable with small ceramic output capacitors, allowing for a small overall solution size. This device has an output tolerance of 1% across line, load, and temperature variation and is capable of delivering 150mA of continuous load current. This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. This device delivers excellent line and load transient performance. The operating junction temperature range of the device is from –40°C to +150°C.

6.2 Functional Block Diagrams

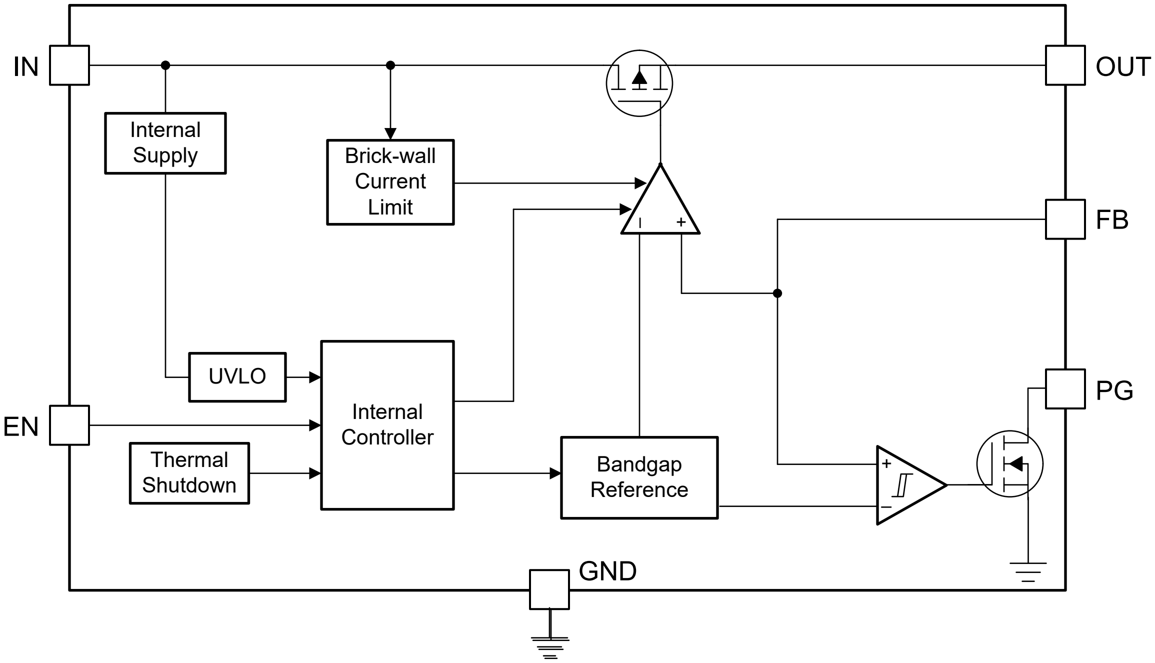


Figure 6-1. Adjustable Output Block Diagram

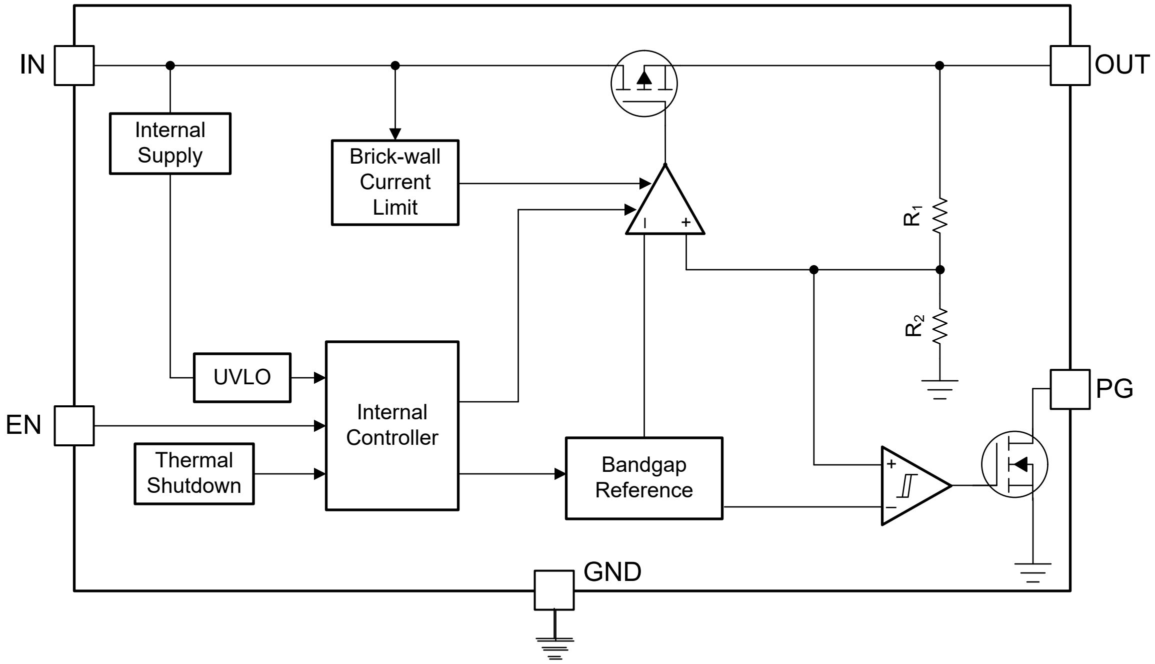


Figure 6-2. Fixed Output Block Diagram

6.3 Feature Description

6.3.1 Output Enable

The EN pin for the device is an active-high pin. The output voltage is enabled when the EN pin voltage is greater than the high-level input voltage of the EN pin. Conversely, the output voltage is disabled when the EN pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the EN pin to the device input voltage.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

6.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-3 shows a diagram of the current limit.

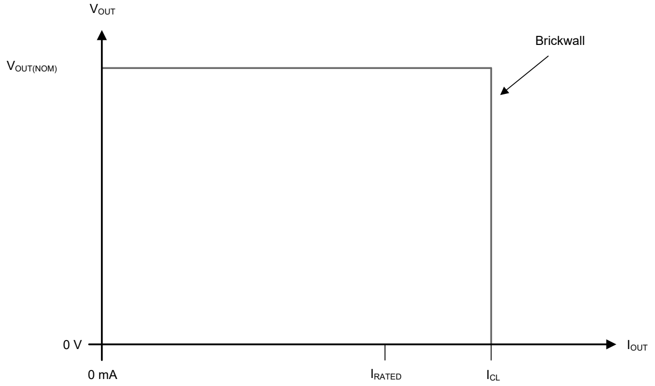


Figure 6-3. Current Limit

6.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage. This circuit allows for a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

6.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Shutdown Mode

Place this device in shutdown mode with a logic low at the EN pin. Return the logic level high to restore operation or tie EN to V_{IN} if this mode is not used.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Reverse Current

Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which potentially exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 7-1 shows one approach for protecting the device.

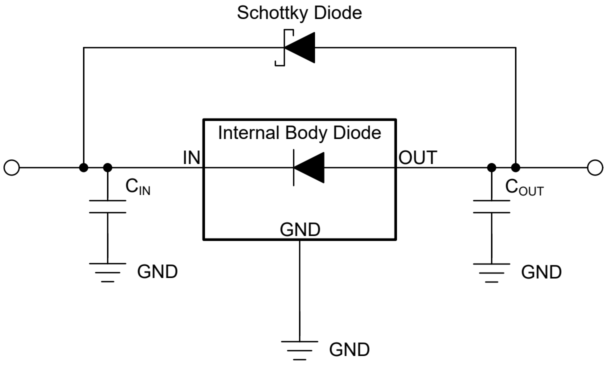


Figure 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher value capacitor if large, fast rise-time load or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.1.3 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the linear regulator junction temperatures when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the printed circuit board (PCB) surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \qquad (2)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \qquad (3)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use the metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the PCB, and correct sizing of the thermal plane. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \qquad (4)$$

Note

Power dissipation is minimized, and therefore greater efficiency achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. Make sure this pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the temperature of the ambient air. The following equation describes this relationship.

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. This resistance therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance.

7.2 Typical Application

Figure 7-2 shows a typical application circuit for the TPS7C84-Q1. Use different values of external components, depending on the end application. If needed, use a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low-ESR ceramic capacitor with an X5R or X7R dielectric.

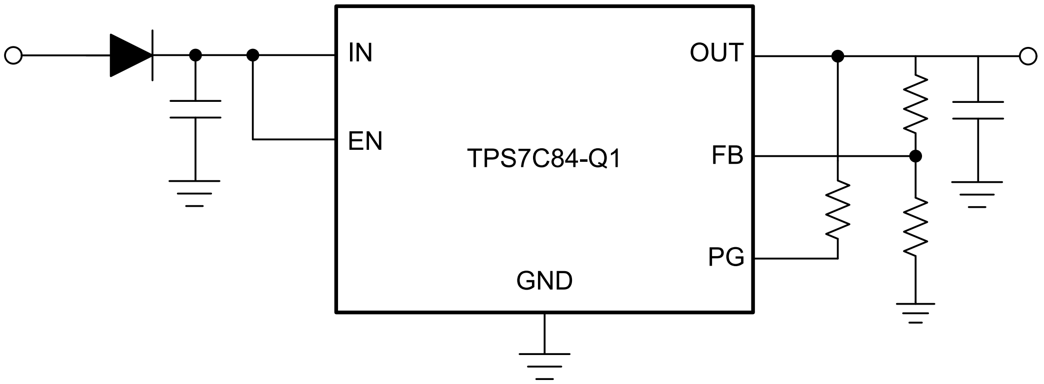


Figure 7-2. Typical Application Schematic for the TPS7C84-Q1

7.2.1 Design Requirements

Table 7-1 summarizes the design requirements for Figure 7-2.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range	6V to 40V
Output voltage	5V
Output current	150mA
Output capacitor	1µF

7.2.1.1 Recommended Capacitor Types

7.2.1.1.1 Recommended Capacitors

The TPS7C84-Q1 requires an output capacitor of at least 1µF for stability and an equivalent series resistance (ESR) between 0Ω and 2Ω. Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitor is 100µF. An input capacitor is not required for stability. However, good analog practice is to connect a capacitor (500nF or higher) between the GND and IN pins. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.2.2 Detailed Design Procedure

7.2.2.1 Feedback Resistor Selection

V_{OUT} is set by the external feedback resistors R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \tag{6}$$

In this equation, V_{FB} is the FB pin current error term. To ignore V_{FB} in this equation, set the feedback divider current to 100 times the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \le \frac{V_{OUT}}{(I_{FB} \times 100)} \quad (7)$$

7.2.2.2 Feedforward Capacitor

Connect a feedforward capacitor (C_{FF}) between the OUT pin and the FB pin. C_{FF} improves transient, noise, and PSRR performance. If a higher capacitance C_{FF} is used, the start-up time increases. For a detailed description of the C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

As shown in Figure 7-3, poor layout practices and using long traces at the FB pin results in the formation of a parasitic capacitor (C_{FB}).

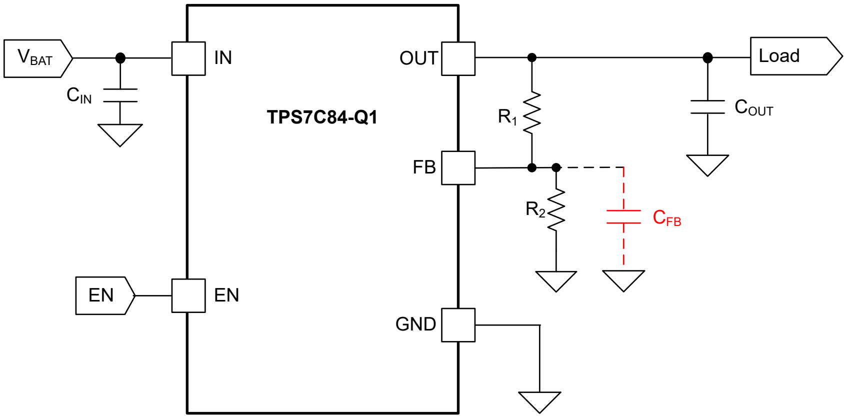


Figure 7-3. Formation of a Parasitic Capacitor at the FB Pin

C_{FB}, along with the feedback resistors R_1 and R_2 potentially results in the formation of an uncompensated pole in the transfer function of the loop gain. A C_{FB} value as small as 6pF potentially causes the parasitic pole frequency, given by Equation 8, to fall within the LDO bandwidth and result in instability.

$$f_P = \frac{1}{(2 \times \pi \times C_{FB} \times (R_1 \parallel R_2))} \quad (8)$$

Adding a feedforward capacitor (C_{FF}) creates a zero in the loop gain transfer function that compensates for the parasitic pole created by C_{FB}. Figure 7-4 shows this compensation. Equation 9 and Equation 10 calculate the pole and zero frequencies.

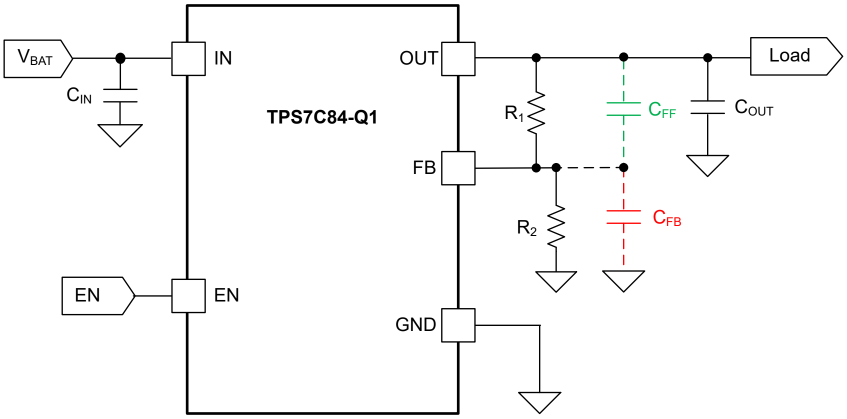


Figure 7-4. A Feedforward Capacitor Compensates the Effects of the Parasitic Capacitor

$$f_P = \frac{1}{(2 \times \pi \times (R_1 \parallel R_2) \times (C_{FF} + C_{FB}))} \tag{9}$$

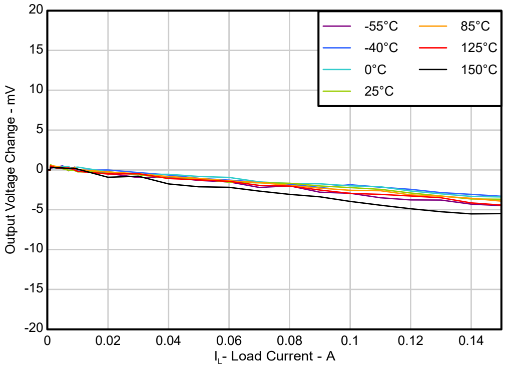
$$f_Z = \frac{1}{(2 \times \pi \times C_{FF} \times R_1)} \tag{10}$$

The C_{FF} value that makes f_P equal to f_Z depends on the values of C_{FB} and the feedback resistors used in the application. This C_{FF} value also results in a pole-zero cancellation. Alternatively, if the feedforward capacitor is selected so that $C_{FF} \gg C_{FB}$, then the pole and zero frequencies from Equation 9 and Equation 10 are related as:

$$\frac{f_P}{f_Z} \cong \left(1 + \frac{R_1}{R_2}\right) = \frac{V_{OUT}}{V_{FB}} \tag{11}$$

In most applications, particularly where a 3.3V or 5V V_{OUT} is generated, this ratio is not very large. Thus implying that the frequencies are located close to each other and therefore the parasitic pole is compensated. A C_{FF} value of approximately 100pF ≤ C_{FF} ≤ 10nF typically helps prevent instability caused by the parasitic capacitance on the feedback node. This C_{FF} range helps even for large V_{OUT} values, where this ratio is potentially as large as 20.

7.2.3 Application Curve



V_{OUT} = 5V, C_L = 1µF

Figure 7-5. Load Transient Response vs Time

7.3 Power Supply Recommendations

Limit maximum input voltage to 30V for proper operation. Place input and output capacitors as close to the device as possible to take advantage of the high-frequency, noise-filtering properties.

7.4 Layout

7.4.1 Layout Guidelines

- Verify that the traces on the input and outputs of the device are wide enough to handle the desired currents. For this device, use a larger output trace to accommodate the larger available current.
- Place input and output capacitors as close to the device as possible to take advantage of the high-frequency, noise-filtering properties.

7.4.2 Layout Example

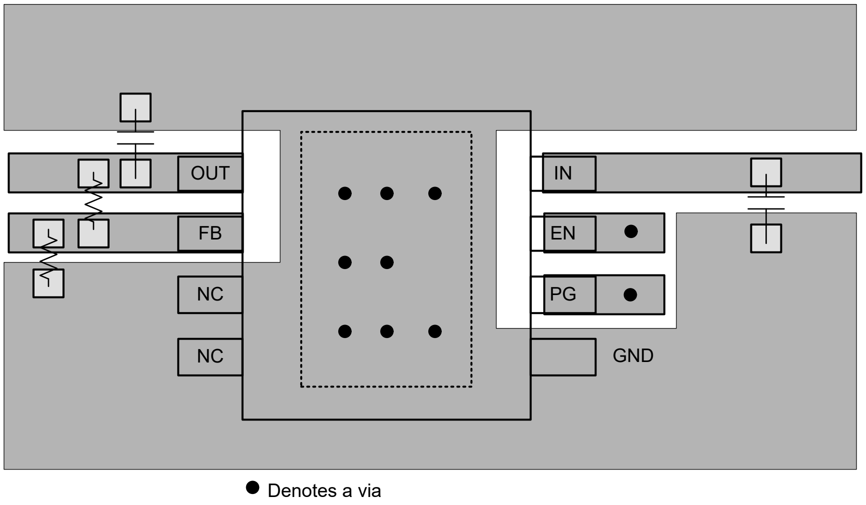


Figure 7-6. SOIC (D) Package Adjusable Output

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT(1)	V_{OUT}
TPS7C84**xx**Q ***yyyz***Q1	**xx** is the nominal output voltage (for example, 50 = 5.0V, 33 = 3.3V). **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **z** is the reel quantity. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.
TPS7C84**01**Q ***yyyz***Q1	**01** indicates that this device is the adjustable option. **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard **yyy** is the package designator. **z** is the reel quantity. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7C8401QDRQ1	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

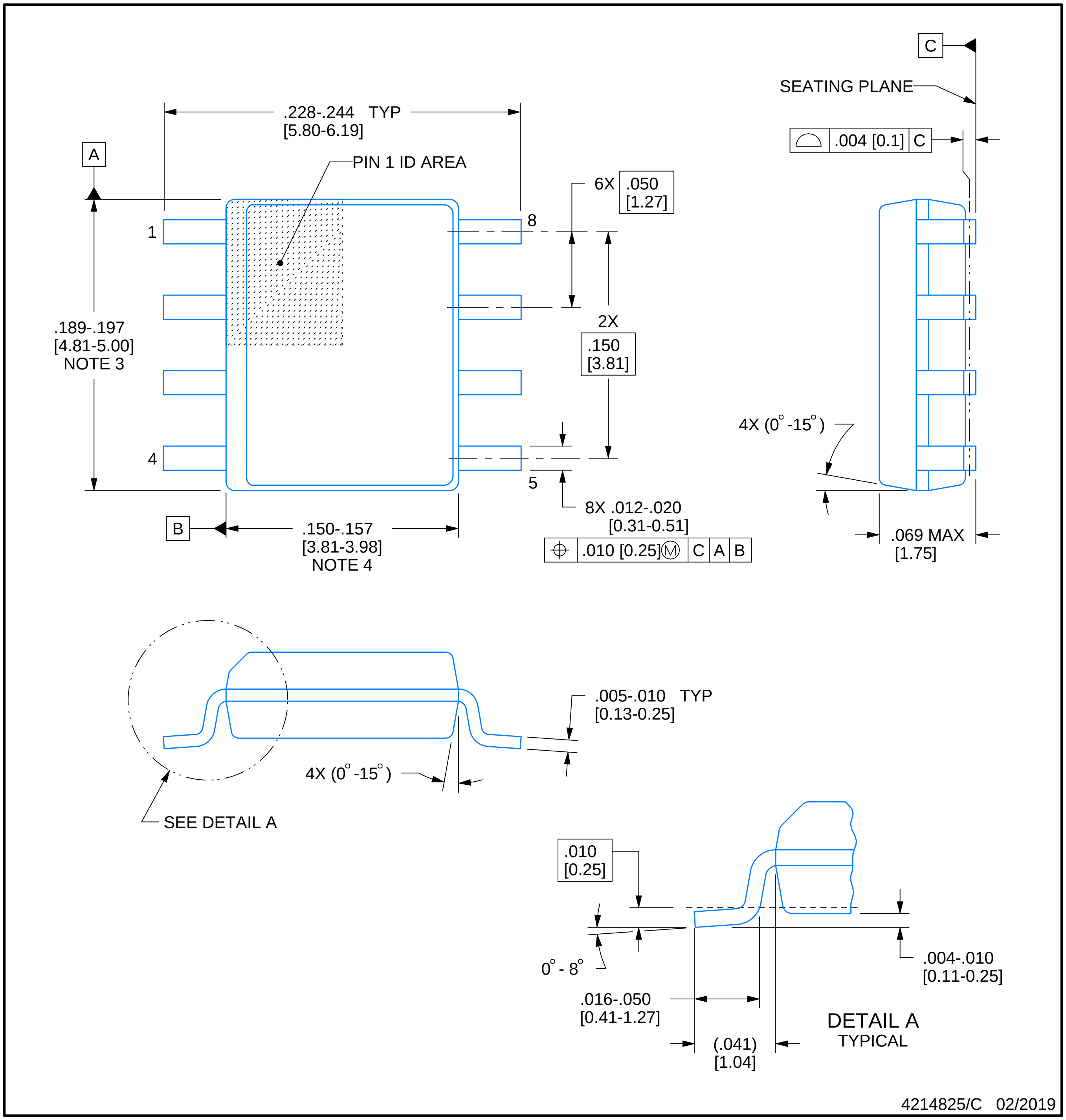
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

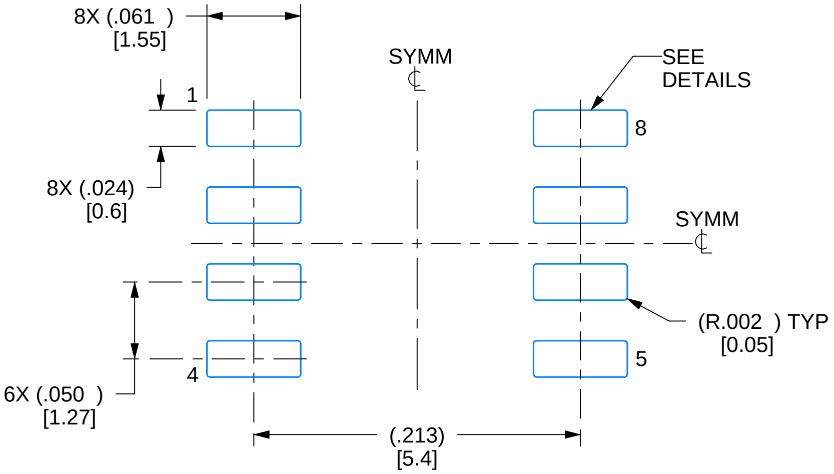
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



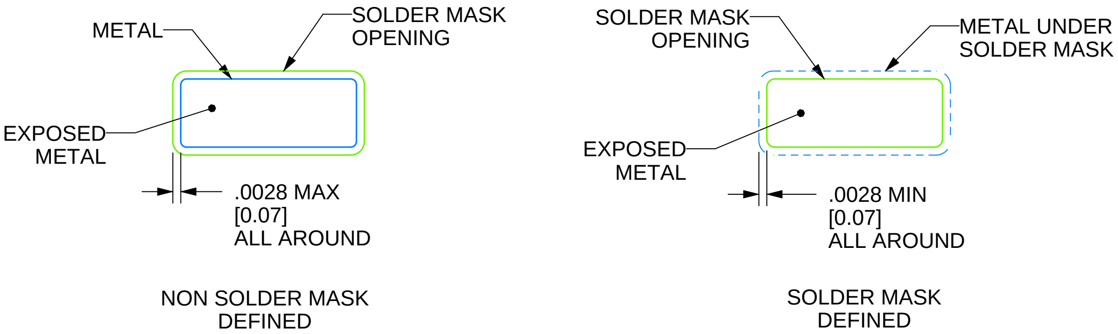
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



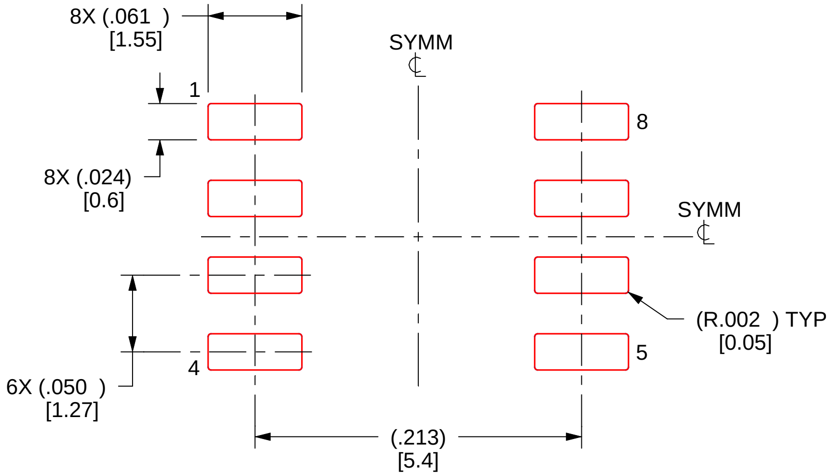
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated