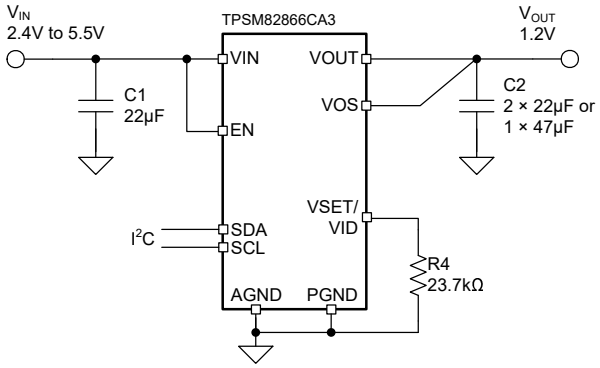
TPSM8286xx 2.4V to 5.5V Input, 4A/6A, Step-Down MagPack™ Power Module With Integrated Inductor and I²C interface

1 Features

- Up to 96% efficiency
- Excellent thermal performance
- I²C-compatible interface up to 3.4Mbps
- 1% output voltage accuracy
- DCS-Control topology for fast transient response
- I²C Programmable:
  - Output voltage
    - 0.4 – 1.675V in 5mV steps
    - 0.8 – 3.35V in 10mV steps
  - Forced PWM or power save mode
  - Output voltage discharge
- I²C device status readback of:
  - Thermal warning
  - Hiccup current limit
  - Vin below UVLO
- Resistor selectable:
  - I²C address
  - 16 start-up output voltage options
- Optimized for low EMI requirements
  - No bond wire package
  - MagPack technology shields inductor and IC
  - Simplified layout through optimized pinout
- 4µA operating quiescent current
- –40°C to 125°C operating temperature range
- 2.3mm × 3.0mm × 1.95mm QFN package
- 28mm² design size
- Also available without I²C interface: TPSM82866A

2 Applications

- Core supply for FPGAs, CPUs, ASICs
- Optical modules
- Medical imaging
- Factory automation and control
- Aerospace and defense



Typical Application Schematic

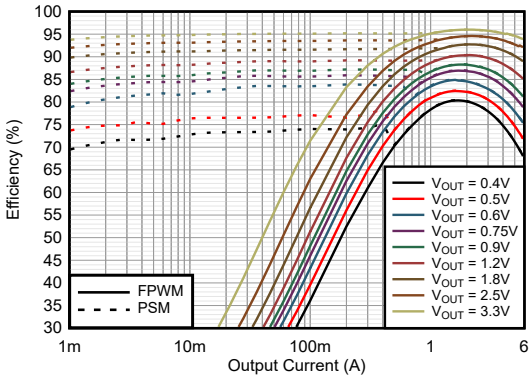
3 Description

The TPSM8286xx device family consists of 4A and 6A step-down converter power modules designed for small solution size and high efficiency. The power modules uses TI's MagPack technology to integrate a synchronous step-down converter and an inductor to simplify design, reduce external components, and save PCB area. The compact design is excellent for automated assembly by standard surface mount equipment. Tight output voltage accuracy, even with small output capacitors, is achieved though the DCS-Control architecture and the excellent load transient performance. At medium-to-heavy loads, the converter operates in PWM mode and automatically enters power save mode operation at light load to maintain high efficiency over the entire load current range. The devices can also be forced in PWM mode operation for the smallest output voltage ripple. The I²C interface provides an effective way of adjusting the output voltage, setting the V_{OUT} ramp rate when transitioning to a new setpoint or reading status information like thermal warning or current limit flags. An integrated soft start reduces the inrush current required from the input supply. Overtemperature protection and hiccup short-circuit protection deliver a robust and reliable design.

Device Information

PART NUMBER(3)	OUTPUT CURRENT	PACKAGE(1)	BODY SIZE (NOM)
TPSM82864xx(2)	4A	RCF (QFN-FCMOD, 15)	2.30mm × 3.00mm
TPSM82866xx	6A		

(1) For more information see Section 12.
(2) Preview information (not Advance Information).
(3) See the *Device Options* table.



TPSM82866C – Efficiency; V_{IN} = 5.0V

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4 Device Options

ORDERABLE PART NUMBER(1)	OUTPUT CURRENT	OPERATING FREQUENCY	OUTPUT VOLTAGE RANGE	DEVICE HEIGHT
TPSM82864CA2PRCFR(2)	4A	2.4MHz	0.4V – 1.675V	1.95mm
TPSM82864CA3PRCFR(2)			0.8V – 3.35V	
TPSM82866CA2PRCFR(2)	6A		0.4V – 1.675V	
TPSM82866CA3PRCFR			0.8V – 3.35V	

(1) For more information see Section 12.
(2) Preview information (not Advance Information).

5 Pin Configuration and Functions

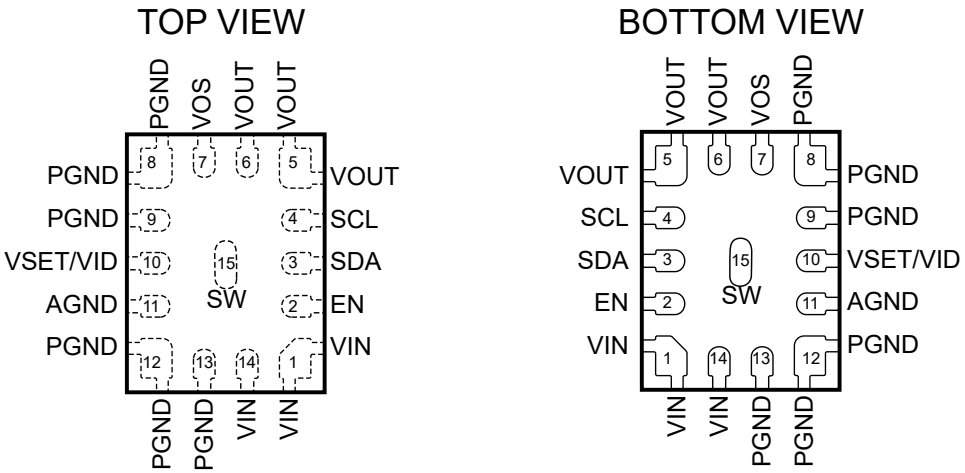

Figure 5-1. TPSM82864x, TPSM82866x - RCF (15 Pin) QFN-FCMOD

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	RCF		
AGND	11	P	Analog ground pin. Must be connected to a common GND plane.
EN	2	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave floating.
SDA	3	I/O	I^2C serial data pin. Do not leave floating. Connect a pullup resistor to a logic high level. If the I^2C interface is not used, connect the pin to GND.
SCL	4	I	I^2C serial clock pin. Do not leave this pin floating. Connect a pullup resistor to a logic high level. If the I^2C interface is not used, connect the pin to GND.
VSET/VID	10	I	Connecting a resistor to GND selects one of the Start-up output voltages and I^2C device address. After start-up, the pin can be used to switch between the V_{OUT} registers for the output voltage selection. (Low = V_{OUT} Register 1; High = V_{OUT} Register 2). See Section 7.4.3 for details.
PGND	8, 9, 12, 13	P	Power ground pin. Must be connected to common GND plane.
SW	15	O	Switch pin of the power stage. This pin can be left floating.
VIN	1, 14	P	Power supply input voltage pin
VOS	7	I	Output voltage sense pin. This pin must be directly connected to the output capacitor.
VOUT	5, 6	P	Output voltage pin

(1) I = Input, O = Output, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, VOS, FB, PG, VSET/VID	–0.3	6	V
	SW (DC), VOUT	–0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns)(3)	–2.5	10	
$I_{SINK\_SDA\_SCL}$	Sink current at SDA, SCL		2	mA
T_J	Junction temperature	–40	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage range	2.4		5.5	V
V_{OUT}	Output voltage range	0.6		V_{IN} or 3.35V	V
t_{F_VIN}	Falling transition time at VIN (1)			10	mV/µs
I_{OUT}	Output current, TPSM82864xx			4	A
	Output current, TPSM82866xx			6	
R_{VSET}	Nominal resistance range for external voltage selection resistor (E96 resistor series)	10		249	kΩ
	External voltage selection resistor tolerance			1%	
	External voltage selection resistor temperature coefficient			±200	ppm/°C
T_J	Junction temperature	–40		125	°C

(1) The falling slew rate of V_{IN} must be limited if V_{IN} goes below V_{UVLO} (see Power Supply Recommendations).

6.4 Thermal Information

THERMAL METRIC[1]		TPSM8286x 15 PINS RCF JEDEC 51-7	TPSM8286x 15 PINS RCF EVM	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.8	29.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.5	n/a[2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.6	n/a[2]	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.8	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19	15.1	°C/W

(1) For more information about thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Not applicable to an EVM.

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6.5 Electrical Characteristics

T_J = –40°C to 125°C, and V_{IN} = 2.4V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{Q_VIN}	Quiescent current into VIN pin	EN = High, no load, device not switching		4	10	µA
I_{Q_VOS}	Quiescent current into VOS pin	EN = High, no load, device not switching, V_{VOS} = 1.8V		18		µA
I_{SD}	Shutdown current	EN = Low, T_J = -40℃ to 85℃		0.24	1	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.2	2.3	2.4	V
		V_{IN} falling	2.1	2.2	2.3	V
T_{JW}	Thermal warning threshold	T_J rising		130		°C
	Thermal warning hysteresis	T_J falling		20		°C
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE						
V_{IH}	High-level input threshold voltage at EN, SCL, SDA and VSET/VID		0.84			V
V_{IL}	Low-level input threshold voltage at EN, SCL, SDA and VSET/VID				0.4	V
$I_{SCL,LKG}$	Input leakage current into SCL pin			0.01	0.8	µA
$I_{SDA,LKG}$	Input leakage current into SDA pin			0.01	0.1	µA
$I_{EN,LKG}$	Input leakage current into EN pin			0.01	0.1	µA
C_{SCL}	Parasitic capacitance at SCL			1		pF
C_{SDA}	Parasitic capacitance at SDA			2.4		pF
START-UP, POWER GOOD						
t_{Delay}	Enable delay time	Time from EN high to device starts switching with a 249kΩ resistor connected between VSET/VID and GND	420	650	1100	µs
OUTPUT						
V_{OUT}	Output voltage accuracy	FPWM, no Load, T_J = 0℃ to 85℃	–1		1	%
		FPWM, no Load	–2		2	%
$I_{VOS,LKG}$	Input leakage current into VOS pin	EN = Low, Output discharge disabled, V_{VOS} = 1.8V		0.2	2.5	µA
R_{DIS}	Output discharge resistor at VOS pin			3.5		Ω
	Load regulation	V_{OUT} = 0.9V, FPWM		0.04		%/A
POWER SWITCH						
R_{DP}	Dropout resistance	100% mode. V_{IN} = 3.3V, T_J = 25°C		22		mΩ
I_{LIM}	High-side FET forward current limit	TPSM82864xx	5	5.5	6	A
		TPSM82866xx	7	7.9	9	A
	Low-side FET forward current limit	TPSM82864xx		4.5		A
		TPSM82866xx		6.5		A
	Low-side FET negative current limit			–3		A
f_{SW}	PWM switching frequency	I_{OUT} = 1A, V_{OUT} = 0.9V		2.4		MHz

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6.6 I²C Interface Timing Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		Fast mode plus		1	MHz
		High-speed mode (write operation), C_B – 100pF max		3.4	MHz
		High-speed mode (read operation), C_B – 100pF max		3.4	MHz
		High-speed mode (write operation), C_B – 400pF max		1.7	MHz
		High-speed mode (read operation), C_B – 400pF max		1.7	MHz
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
t_{HD}, t_{STA}	Hold time (repeated) START condition	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode	160		ns
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
		High-speed mode, C_B – 100pF max	160		ns
		High-speed mode, C_B – 400pF max	320		ns
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode, C_B – 100pF max	60		ns
		High-speed mode, C_B – 400pF max	120		ns
t_{SU}, t_{STA}	Setup time for a repeated START condition	Standard mode	4.7		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode	160		ns
t_{SU}, t_{DAT}	Data setup time	Standard mode	250		ns
		Fast mode	100		ns
		Fast mode plus	50		ns
		High-speed mode	10		ns
t_{HD}, t_{DAT}	Data hold time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		Fast mode plus	0		µs
		High-speed mode, C_B – 100pF max	0	70	ns
		High-speed mode, C_B – 400pF max	0	150	ns

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6.6 I²C Interface Timing Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{RCL}	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	40	ns
		High-speed mode, C_B – 400pF max	20	80	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	80	ns
		High-speed mode, C_B – 400pF max	20	160	ns
t_{FCL}	Fall time of SCL signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode		300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	40	ns
		High-speed mode, C_B – 400pF max	20	80	ns
t_{RDA}	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	80	ns
		High-speed mode, C_B – 400pF max	20	160	ns
t_{FDA}	Fall time of SDA signal	Standard mode		300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100pF max	10	80	ns
		High-speed mode, C_B – 400pF max	20	160	ns
t_{SU}, t_{STO}	Setup time of STOP condition	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-Speed mode	160		ns
C_B	Capacitive load for SDA and SCL	Standard mode		400	pF
		Fast mode		400	pF
		Fast mode plus		550	pF
		High-Speed mode		400	pF

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6.7 Typical Characteristics

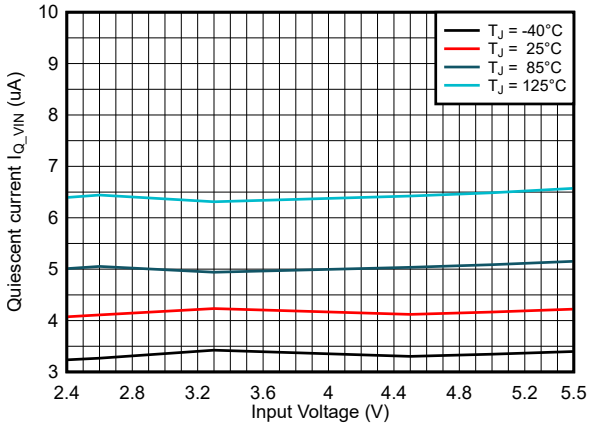

Figure 6-1. Quiescent Current into V_{IN} I_{Q_VIN}

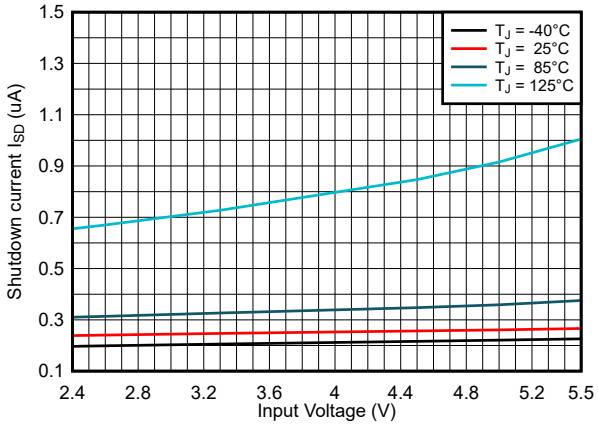

Figure 6-2. Shutdown Current I_{SD}

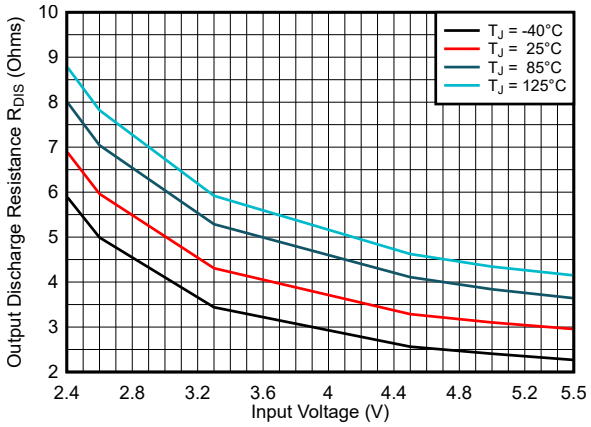

Figure 6-3. Output Discharge Resistance R_{DIS}

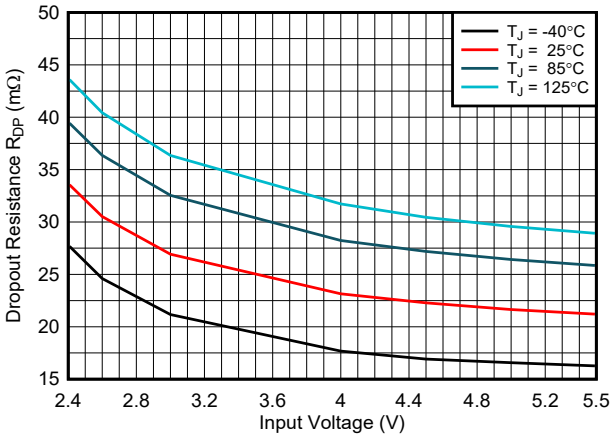

Figure 6-4. Dropout Resistance R_{DP}

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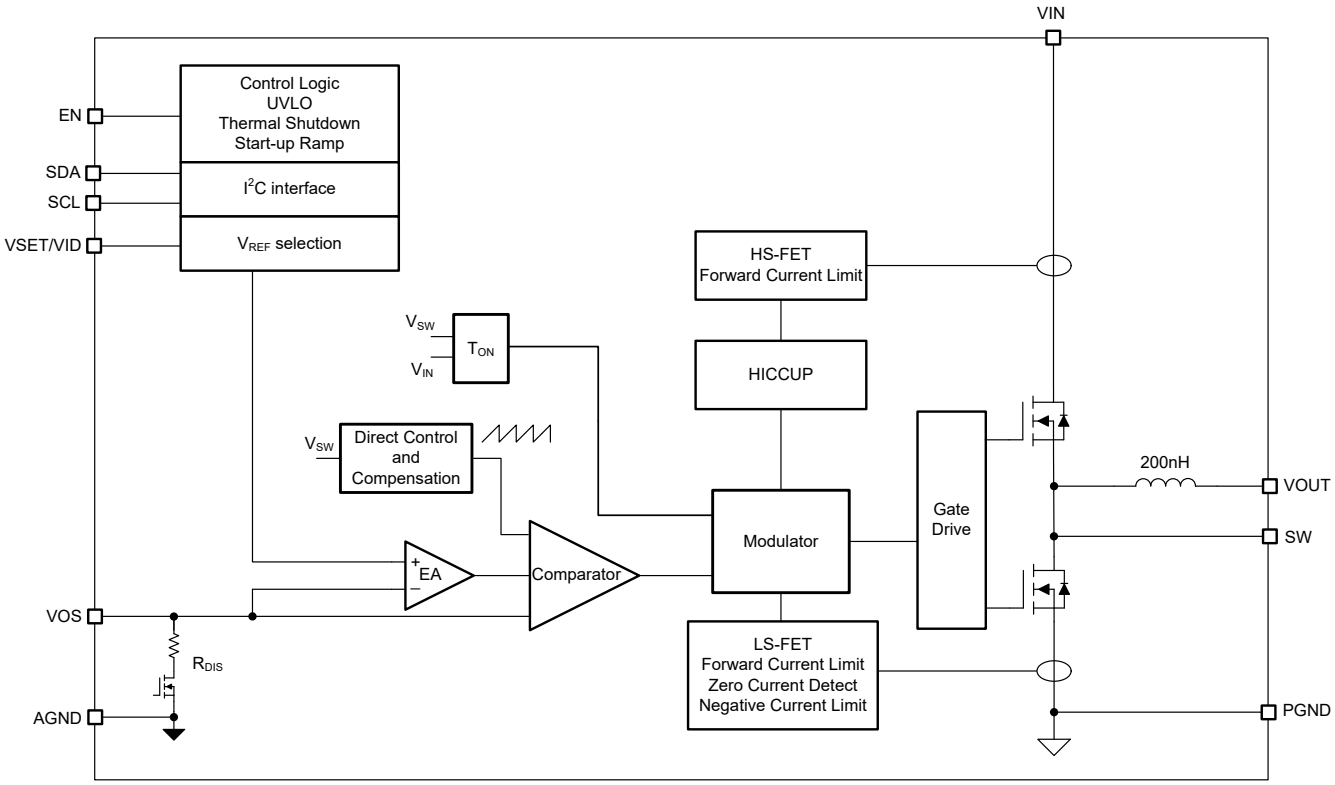
7 Detailed Description

7.1 Overview

The TPSM8286xx synchronous, step-down converter power module uses the DCS-Control (Direct Control with seamless transition into power save mode) topology. This topology is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control. The DCS-Control topology operates in PWM (pulse width modulation) mode for medium-to-heavy load conditions and in PSM (power save mode) at light load currents. In PWM, the converter operates with the nominal switching frequency of 2.4MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the quiescent current of the IC to achieve high efficiency over the entire load current range. DCS-Control supports both operation modes using a single building block and, therefore, has a seamless transition from PWM to PSM without effects on the output voltage. The TPSM8286xx offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

The TPSM8286xxxxP versions in the RCF package use MagPack technology to deliver the highest-performance power module design. Leveraging our proprietary integrated-magnetics packaging technology, MagPack (magnetics in package) power modules deliver industry-leading power density, high efficiency, good thermal performance, ease of use, and reduced EMI emissions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

As the load current decreases, the device seamlessly enters power save mode (PSM) operation. In PSM, the converter operates with a reduced switching frequency and a minimum quiescent current to maintain high efficiency. Power save mode is based on a fixed on-time architecture, as shown in Equation 1. The inductance used in the TPSM8286xx is 200nH typical.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (1)$$

For very small output voltages, an absolute minimum on time of approximately 50ns is kept to limit switching losses. The operating frequency is thereby reduced from the nominal value, which keeps efficiency high. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (2)$$

The load current at which PSM is entered is at one half of the ripple current of the inductor and can be estimated as:

$$I_{Load(PSM-entry)} = \frac{V_{IN} \times t_{ON}}{2} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L} \quad (3)$$

In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitance.

7.3.2 Forced PWM Mode

When setting the Enable FPWM Mode bit = 1 in the Control register, the device enters forced PWM (FPWM) mode and operates with a constant switching frequency over the entire load range, even at very light loads. This action reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications but lowers efficiency at light loads.

7.3.3 Optimized Transient Performance from PWM to PSM Operation

For most converters, the load transient response in PWM mode is improved compared to PSM, because the converter reacts faster on the load step and actively sinks energy on the load release. As an additional feature, the TPSM8286xx automatically stays in PWM mode for 128 cycles after a heavy load release to bring the output voltage back to the regulation level faster. After these 128 cycles of PWM mode, the device automatically returns to PSM (if the Enable FPWM Mode bit = 0). See Figure 7-1. Without this optimization, the output voltage overshoot is higher.

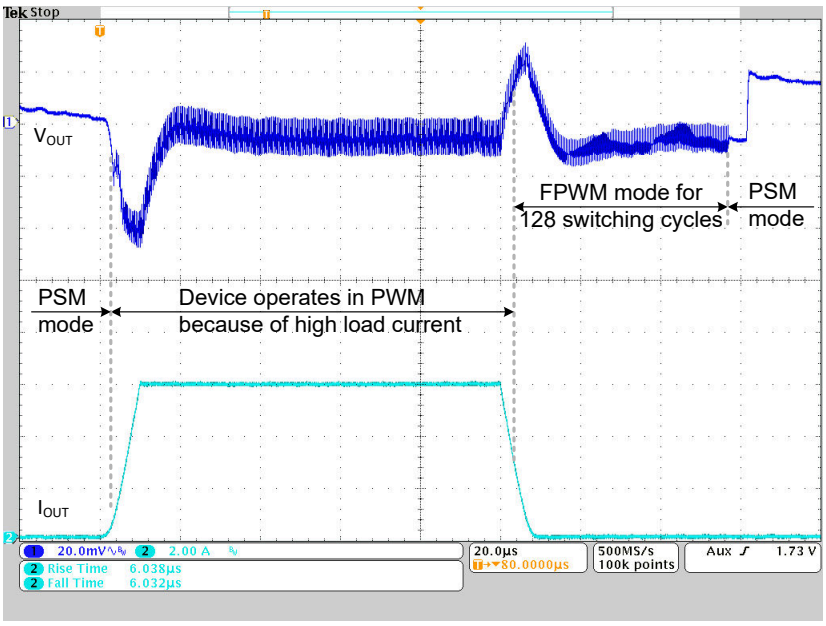


Figure 7-1. Optimized Transient Performance from PWM to PSM

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7.3.4 Low Dropout Operation (100% Duty Cycle)

The device offers a low dropout operation by entering 100% duty cycle mode if the input voltage comes close to the target output voltage. In this mode, the high-side MOSFET switch is constantly turned on. This constant is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN\ (min)} = V_{OUT\ (min)} + I_{OUT\ (max)} \times R_{DP} \quad (4)$$

where

- $V_{OUT\ (min)}$ = Minimum output voltage the load can accept
- $I_{OUT\ (max)}$ = Maximum output current
- R_{DP} = Resistance from VIN to VOUT (high-side $R_{DS(on)}$ + R_{DC} of the inductor)

7.3.5 Enable and Soft-Start Ramp

After enabling the device, there is a 650µs enable delay (t_{Delay}) before the I^2C interface is active. The t_{Delay} time varies with the VSET/MODE resistor used and is longest with a resistance of 249kΩ. After the enable delay, all registers can be read and written by the I^2C interface. The Voltage Ramp Speed bits in the Control register set the slope of the Output Voltage soft start ramp (default = 1mV / µs). This action avoids excessive inrush current and creates a smooth output voltage ramp up. This action also prevents excessive voltage drop of batteries or prior voltage regulators which have a high internal impedance.

Figure 7-2 shows the start-up sequence.

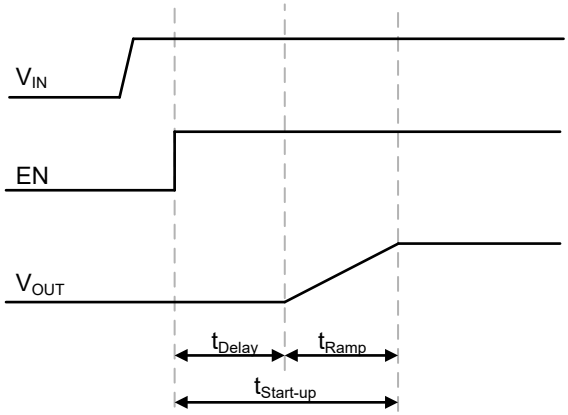

Figure 7-2. Start-Up Sequence

The device is able to start into a prebiased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.3.6 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, cycle by cycle, the high-side MOSFET is turned off and the low-side MOSFET is turned on until the inductor current ramps down to the low-side MOSFET current limit.

When the high-side MOSFET current limit is triggered 32 times, the device stops switching. The device then automatically re-starts with soft start after a typical delay time of 128µs has passed. The device repeats this mode until the high load condition disappears. This HICCUP short-circuit protection reduces the current consumed from the input supply during an overload condition. Figure 9-23 shows the hiccup short-circuit protection.

The HICCUP can be disabled by the CONTROL register bit Enable HICCUP. Disabling HICCUP changes the overcurrent protection to latching protection. The device stops switching after the high-side MOSFET current

limit is triggered 32 times. Toggling the EN pin, removing and reapplying the input voltage, or writing to the CONTROL register bit Software Enable Device unlatches the device.

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle. The negative current limit is only active in forced PWM mode.

7.3.7 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, undervoltage lockout (UVLO) disables the device when the input voltage is lower than V_{UVLO}. When the input voltage recovers, the device automatically returns to operation with soft start. The UVLO bit in the STATUS Register is set when the input voltage is below the UVLO falling threshold.

In case the input voltage falls below 1.8V (typical), all registers are reset.

7.3.8 Thermal Warning and Shutdown

The module features a thermal warning indicator bit in the Status register. This bit is set to 1 if the junction temperature exceeds the rising T_{JW} temperature and is reset when the junction temperature falls below the threshold by the hysteresis. The device continues operating.

In case the junction temperature exceeds T_{JSD}, the device goes into thermal shutdown, stops switching, and activates the output voltage discharge (in case this is enabled). When the device temperature falls below the threshold by the hysteresis, the device returns to normal operation automatically with soft start.

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7.4 Device Functional Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off and all the registers are reset to the default values, except for the Enable Output Discharge bit. An internal switch smoothly discharges the output through the VOS pin if the Enable Output Discharge bit is set to 1.

In shutdown mode (EN = Low), the I^2C interface is disabled to reduce the current consumption of the module. Thus no registers can be accessed.

The typical enable threshold value of the EN pin is 0.66V for rising input signals and the typical shutdown threshold is 0.52V for falling input signals. Do not leave the EN pin floating.

The device can also be enabled or disabled by setting the Software Enable Device bit in the CONTROL register while EN = High. After being disabled or enabled by this bit, the device stops switching and initiates a new start-up ramp. There is no additional T_{Delay} time and the registers are not reset.

7.4.2 Output Discharge

The purpose of the output discharge function is to make sure of a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0V. The output discharge is active when the Enable Output Discharge bit is set to 1 and the EN pin is pulled low, when the Input voltage is below the UVLO threshold or during thermal shutdown. The discharge is active down to an input voltage of 1.6V (typical). The Enable Output Discharge bit is reset on the rising edge of the EN pin.

7.4.3 Start-Up Output Voltage and I^2C Target Address Selection (VSET)

During the enable delay (t_{Delay}), the start-up output voltage and device I^2C target address are set by an external resistor connected to the VSET/VID pin through an internal R2D (resistor to digital) converter. The device V_{OUT} Register 1 is also set according to the start-up voltage. Table 7-1 shows the allowed resistor values. The allowed resistor tolerance is shown in Section 6.3.

Table 7-1. Start-up Output Voltage and I^2C Target Address Options

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/VID	TPSM8286xCA2 START-UP OUTPUT VOLTAGE	TPSM8286xCA3 START-UP OUTPUT VOLTAGE	I^2C TARGET ADDRESS
249kΩ	1.15V	2.30V	1000 110 (0x46)
205kΩ	1.10V	2.20V	1000 101 (0x45)
162kΩ	1.05V	2.10V	1000 100 (0x44)
133kΩ	1.00V	2.00V	1000 011 (0x43)
105kΩ	0.95V	1.90V	1000 010 (0x42)
86.6kΩ	0.90V	1.80V	1000 001 (0x41)
68.1kΩ	0.85V	1.70V	1001 000 (0x48)
56.2kΩ	0.80V	1.60V	1001 001 (0x49)
44.2kΩ	0.75V	1.50V	1001 010 (0x4A)
36.5kΩ	0.70V	1.40V	1001 011 (0x4B)
28.7kΩ	0.65V	1.30V	1001 100 (0x4C)
23.7kΩ	0.60V	1.20V	1001 101 (0x4D)
18.7kΩ	0.55V	1.10V	1001 110 (0x4E)
15.4kΩ	0.50V	1.00V	1001 111 (0x4F)
12.1kΩ	0.45V	0.90V	1000 000 (0x40)
10kΩ or lower	0.40V	0.80V	1000 111 (0x47)

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The R2D converter has an internal current source, which applies current through the external resistor, and an internal ADC, which reads back the resulting voltage level. Depending on the level, the correct start-up output voltage and I^2C target address are set. After this R2D conversion is finished, the current source is turned off to avoid current flowing through the external resistor. Make sure that there is no additional current path or capacitance greater than 30pF from this pin to GND during R2D conversion. Otherwise, a false value is set.

During the ramp-up period (t_{Ramp}), the output voltage ramps to the target value set by VSET first, then ramps up or down to the new value when the value of the output register is changed by I^2C interface commands.

7.4.4 Select Output Voltage Registers (VID)

After the start-up period ($t_{Startup}$), the output voltage can be selected between two output voltage registers by the VID pin. When VID is pulled low, the output voltage is set by Table 8-2. When VID is pulled high, the output voltage is set by Table 8-3. This is also called dynamic voltage scaling (DVS). If the VID function is not used, the VSET resistor keeps the VSET/VID pin low and the V_{OUT} Register 1 sets the Output voltage.

During an output voltage change through I^2C or the VSET/VID pin, the device can be configured to operate in FPWM by setting the Enable FPWM Mode during Output Voltage Change bit in CONTROL register to 1. In FPWM Mode, the ramp-up and ramp-down speeds are controlled by the device. In PSM Mode the ramp-up speed is controlled by the device, but the ramp-down speed is determined by the load current and the output capacitance. The output voltage change speed is set by the Voltage Ramp Speed bit.

7.5 Programming

7.5.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both the SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through open-drain I/O pins, SDA and SCL. A *controller* device, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A *target* device receives or transmits data on the bus under control of the controller device, or both.

The TPSM8286xx module works as a *target* and supports the following data transfer *modes*, as defined in the I^2C-Bus Specification: standard mode (100kbps) and fast mode (400kbps), fast mode plus (1Mbps) and high-speed mode (3.4Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.8V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, standard and fast modes are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and is referred to as HS mode.

TI recommends that the I^2C controller initiates a STOP condition on the I^2C bus after the initial power up of the SDA and SCL pullup voltages to make sure of a reset of the I^2C engine.

7.5.2 Standard-Mode, Fast-Mode, and Fast-Mode Plus Protocol

The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 7-3. All I^2C-compatible devices recognize a start condition.

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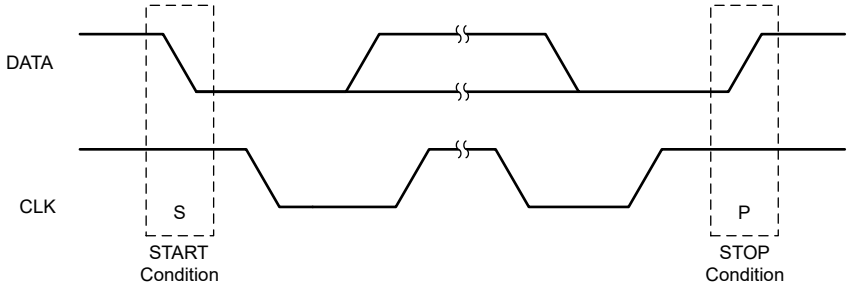

Figure 7-3. START and STOP Conditions

The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/$\overline{W}$ on the SDA line. During all transmissions, the controller makes sure that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 7-4). All devices recognize the address sent by the controller and compare the address to the internal fixed addresses. Only the target device with a matching address generates an acknowledge (see Figure 7-5) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that a communication link with the target has been established.

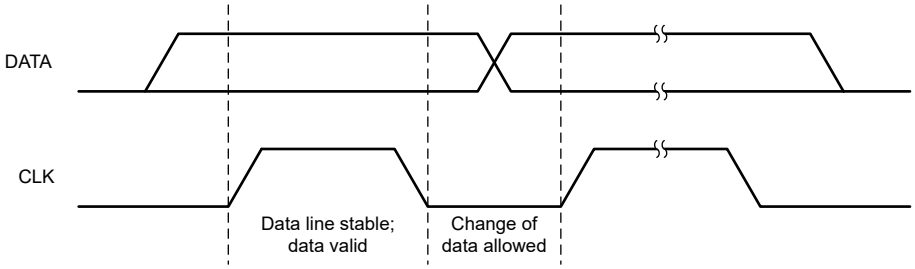

Figure 7-4. Bit Transfer on the Serial Interface

The controller generates further SCL cycles to either transmit data to the target (R/$\overline{W}$ bit 0) or receive data from the target (R/$\overline{W}$ bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 7-3). This action releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and the devices wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 0x00 being read out.

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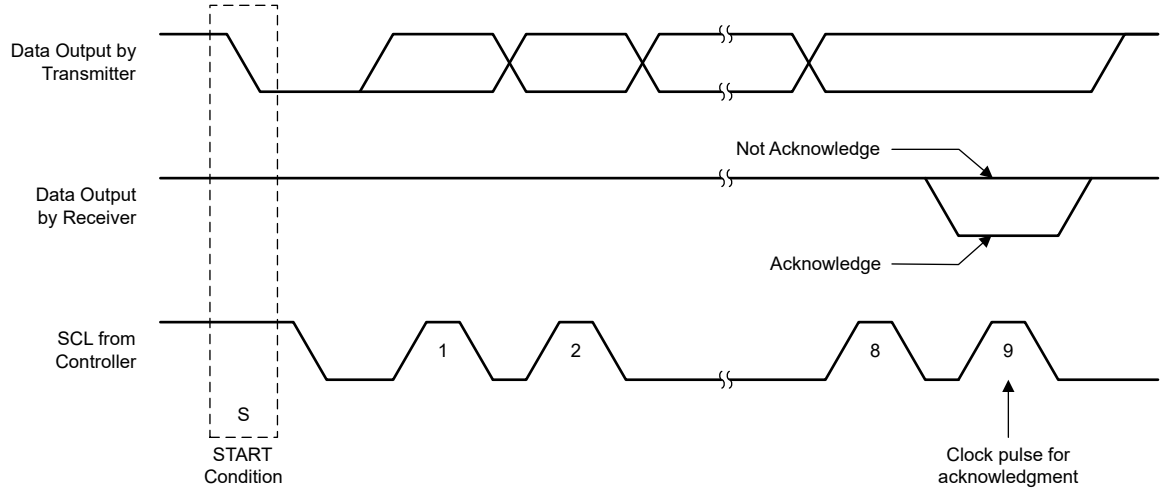

Figure 7-5. Acknowledge on the I²C Bus

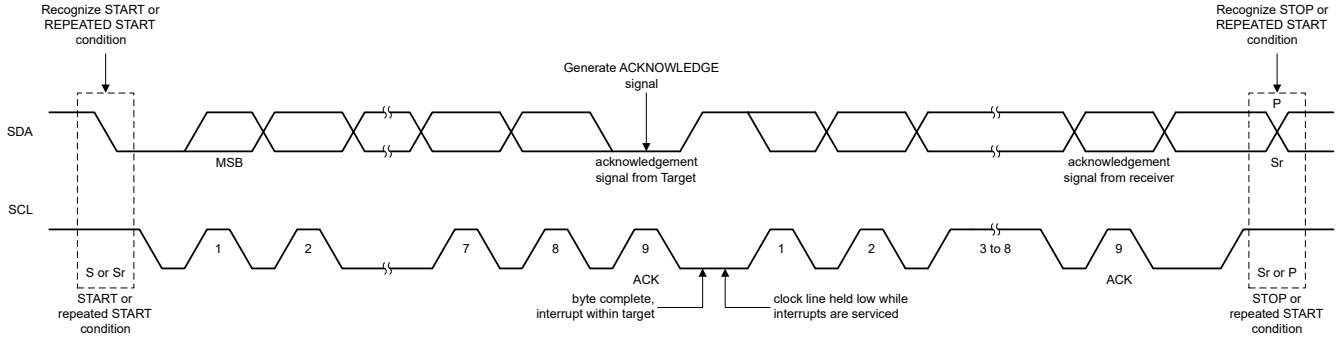

Figure 7-6. Bus Protocol

7.5.3 HS-Mode Protocol

The controller generates a start condition followed by a valid serial byte containing HS controller code 00001XXX. This transmission is made in F/S-mode at no more than 400kbps. No device is allowed to acknowledge the HS controller code, but all devices must recognize the HS controller code and switch the internal setting to support 3.4Mbps operation.

The controller then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the target devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in 0x00 being read out.

7.5.4 I²C Update Sequence

The sequence requires a start condition, a valid I²C target address, a register address byte, and a data byte for a single update. After the receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the device. The device performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

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Figure 7-7. *Write* Data Transfer Format in Standard Modes, Fast Modes, and Fast-Plus Modes

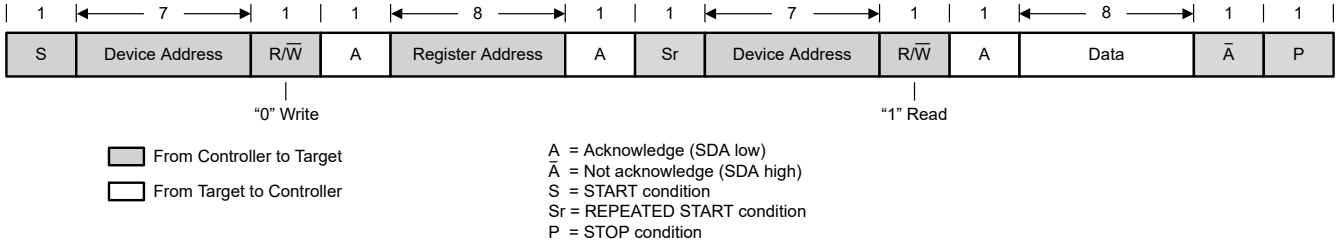

Figure 7-8. *Read* Data Transfer Format in Standard Modes, Fast Modes, and Fast-Plus Modes

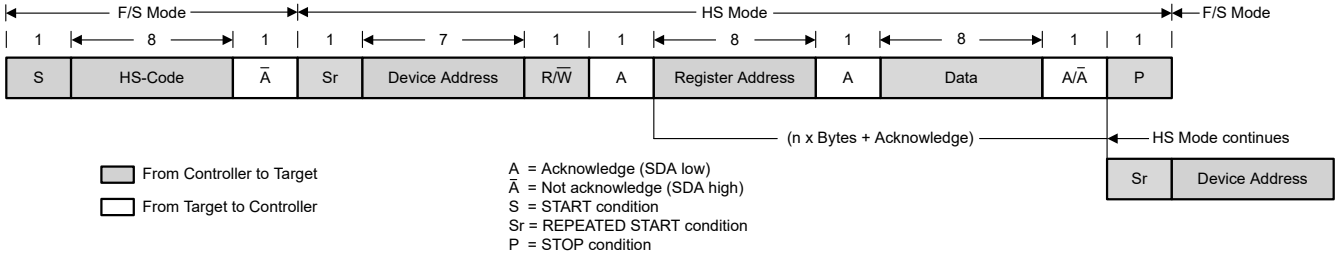

Figure 7-9. Data Transfer Format in HS Mode

7.5.5 I²C Register Reset

The I²C registers can be reset by:

- Pulling the input voltage below 1.8V (typical)
- A high-to-low transition on EN
- Setting the Reset bit in the CONTROL register. When Reset is set to 1, all registers are reset to the default values and a new start-up is begun immediately. After t_{Delay}, the I²C registers can be programmed again.

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8 Register Map

Table 8-1. Register Map

REGISTER ADDRESS (HEX)	REGISTER NAME	FACTORY DEFAULT (HEX)	DESCRIPTION
0x01	V_{OUT} Register 1	Set through VSET/VID pin	Sets the target output voltage when VSET/VID is low
0x02	V_{OUT} Register 2	0x64	Sets the target output voltage when VSET/VID is high
0x03	CONTROL Register	0x6F	Sets miscellaneous configuration bits
0x05	STATUS Register	0x00	Returns status flags

8.1 Target Address Byte

7	6	5	4	3	2	1	0
1	x	x	x	x	x	x	R/$\overline{W}$

The target address byte is the first byte received following the START condition from the controller device. The target I^2C address is assigned by the VSET/VID resistor; see Table 7-1.

8.2 Register Address Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	D2	D1	D0

Following the successful acknowledgment of the target address, the bus controller sends a byte to the device, which contains the address of the register to be accessed.

8.3 V_{OUT} Register 1

Table 8-2. V_{OUT} Register 1 Description

REGISTER ADDRESS 0X01 READ/WRITE				
BIT	FIELD	VALUE(1) (HEX)	TPSM8286xCA2 OUTPUT VOLTAGE (TYPICAL)	TPSM8286xCA3 OUTPUT VOLTAGE (TYPICAL)
7:0	VO1_SET	0x00	400mV	800mV
		0x01	405mV	810mV
		...		
		0x64	900mV	1800mV
		...		
		0xFE	1670mV	3340mV
		0xFF	1675mV	3350mV

(1) The start-up value is assigned by the VSET/VID resistor; see Table 7-1.

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8.4 V_{OUT} Register 2

Table 8-3. V_{OUT} Register 2 Description

REGISTER ADDRESS 0X02 READ/WRITE				
BIT	FIELD	VALUE (HEX)	TPSM8286xCA2 OUTPUT VOLTAGE (TYPICAL)	TPSM8286xCA3 OUTPUT VOLTAGE (TYPICAL)
7:0	VO2_SET	0x00	400mV	800mV
		0x01	405mV	810mV
		...		
		0x64	900mV (default value)	1800mV (default value)
		...		
		0xFE	1670mV	3340mV
		0xFF	1675mV	3350mV

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8.5 CONTROL Register

Table 8-4. CONTROL Register Description

REGISTER ADDRESS 0X03 READ/WRITE				
BIT	**FIELD**	**TYPE**	**DEFAULT**	**DESCRIPTION**
7	Reset	R/W	0	1 - Reset all registers to default.
6	Enable FPWM Mode during Output Voltage Change	R/W	1	0 - Keep the current mode status during output voltage change 1 - Force the device in FPWM during output voltage change.
5	Software Enable Device	R/W	1	0 - Disable the device. All registers values are still kept. 1 - Re-enable the device with a new start-up without the t_{Delay} period.
4	Enable FPWM Mode	R/W	0	0 - Set the device in power save mode at light loads. 1 - Set the device in forced PWM mode at light loads.
3	Enable Output Discharge	R/W	1	0 - Disable output discharge 1 - Enable output discharge
2	Enable HICCUP	R/W	1	0 - Disable HICCUP. Enable latching protection. 1 - Enable HICCUP. Disable latching protection.
0:1	Voltage Ramp Speed	R/W	11	00 - 20mV/µs (0.25µs/step) 01 - 10mV/µs (0.5µs/step) 10 - 5mV/µs (1µs/step) 11 - 1mV/µs (5µs/step)

8.6 STATUS Register

Table 8-5. STATUS Register Description

REGISTER ADDRESS 0X05 READ ONLY(1)				
BIT	**FIELD**	**TYPE**	**DEFAULT**	**DESCRIPTION**
7:5	Reserved			
4	Thermal Warning	R	0	1: Junction temperature is higher than 130°C.
3	HICCUP	R	0	1: Device has HICCUP status once.
2	Reserved			
1	Reserved			
0	UVLO	R	0	1: The input voltage is less than UVLO threshold (falling edge).

(1) All bit values are latched until the device is reset, or the STATUS register is read. Then, the STATUS register is reset to the default values.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSM8286xx is a synchronous, step-down converter, power module family. The following section discusses the selection of the external components to complete the power supply design. The required power inductor is integrated inside the TPSM8286xx. The integrated shielded inductor has a value of 0.20µH with a ±20% tolerance. The TPSM82864x and TPSM82866x are pin-to-pin and BOM-to-BOM compatible. The 4A and 6A version give the same efficiency and performance and are different only in the rated output current.

9.2 Typical Application

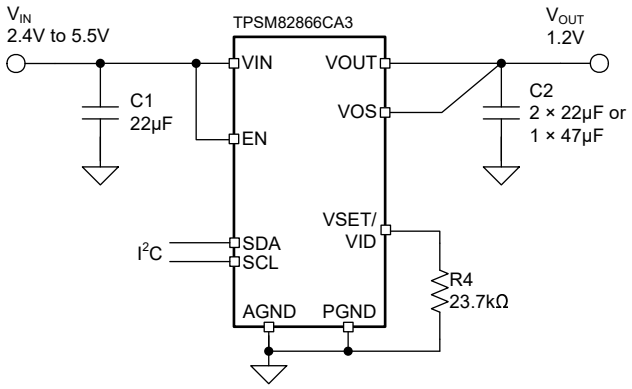

Figure 9-1. Typical Application

9.2.1 Design Requirements

For this design example, use Table 9-1 as the input parameters.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4V to 5.5V
Output voltage	1.2V
Maximum output current	6A

Table 9-2 lists the components used for the example.

Table 9-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	22µF, ceramic capacitor, 6.3V, X7R, size 0805, GRM21BZ70J226ME44	Murata
C2	47µF, ceramic capacitor, 6.3V, X6S, size 0805, GRM21BC80J476ME01L	Murata
R4(2)	Depending on the output voltage, Chip resistor, 1/16W, 1%	Std

(1) See the *Third-Party Products disclaimer*.
(2) See Table 7-1 for the VSET/VID resistor values.

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9.2.2 Detailed Design Procedure

9.2.2.1 Input and Output Capacitor Selection

For the best output and input voltage filtering, low-ESR ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. The input capacitor must be placed between VIN and PGND as close as possible to those pins. For most applications, 22µF is sufficient, though a larger value reduces input current ripple. The input capacitor plays an important role in the EMI performance of the system as explained in the *Simplify Low EMI Design With Power Modules white paper*.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. The capacitor value can range from 2 × 22µF up to 150µF. The recommended typical output capacitors are 2 × 22µF or 1 × 47µF with an X5R or better dielectric. Values over 150µF can degrade the loop stability of the converter.

Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering ith package size and voltage rating. Make sure that the effective input capacitance is at least 10µF and the effective output capacitance is at least 22µF.

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9.2.3 Application Curves

V_{IN} = 5.0V, V_{OUT} = 1.2V, T_A = 25°C, BOM = Table 9-2, unless otherwise noted. Solid lines show the FPWM mode and dashed lines show PSM.

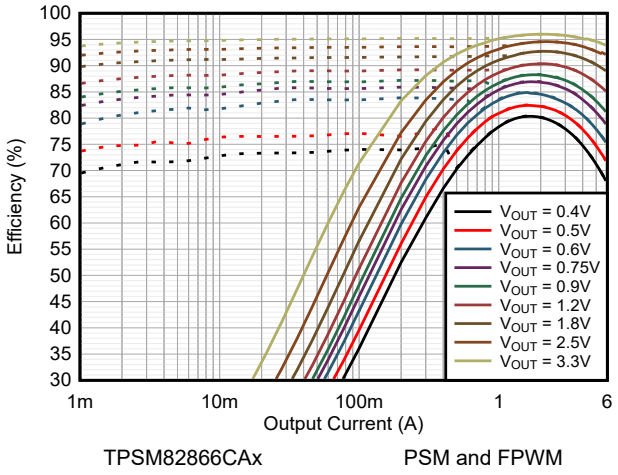


Figure 9-2. Efficiency V_{IN} = 5.0V and T_A = 25°C

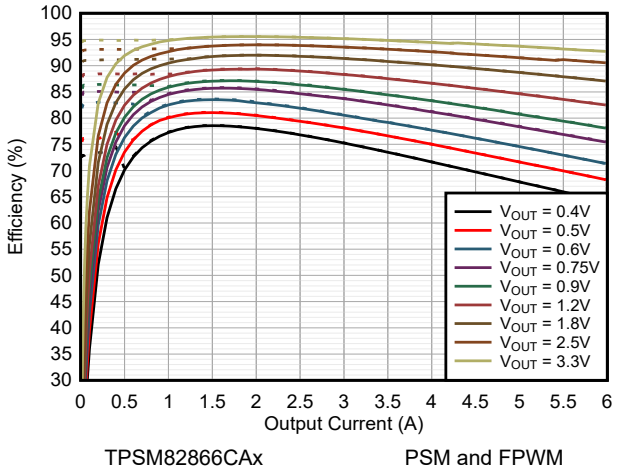


Figure 9-3. Efficiency V_{IN} = 5.0V and T_A = 85°C

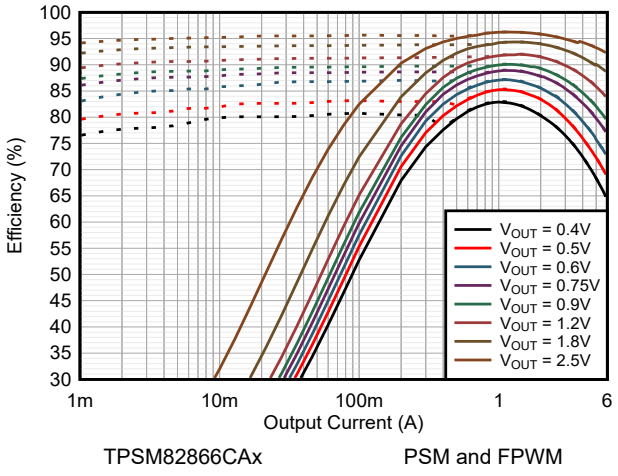


Figure 9-4. Efficiency V_{IN} = 3.3V and T_A = 25°C

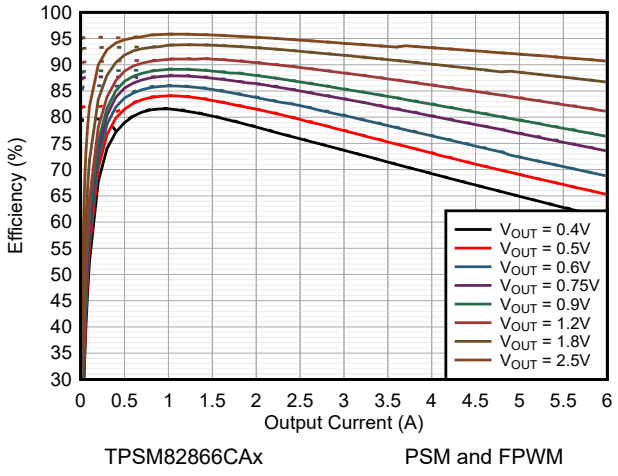


Figure 9-5. Efficiency V_{IN} = 3.3V and T_A = 85°C

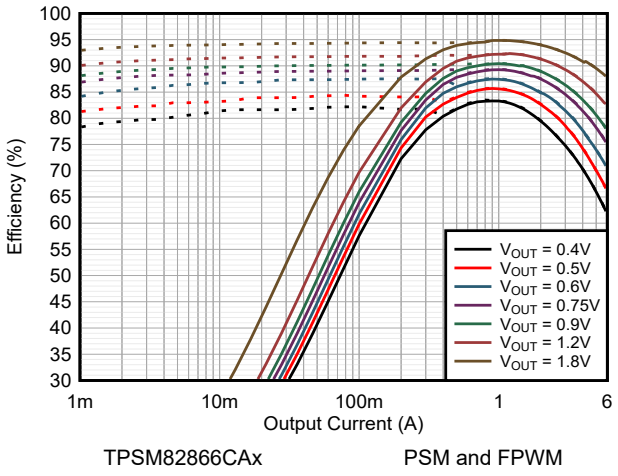


Figure 9-6. Efficiency V_{IN} = 2.8V and T_A = 25°C

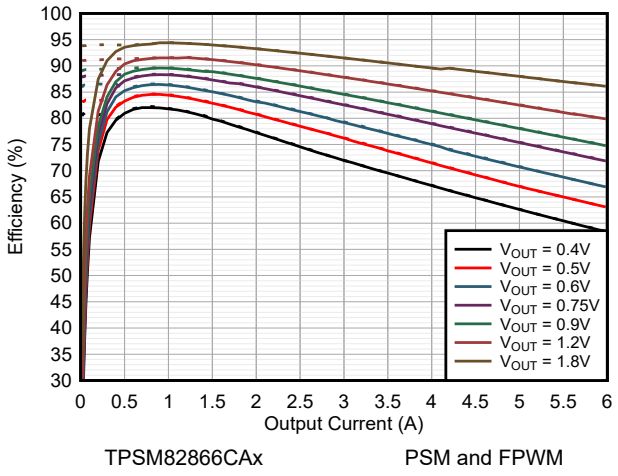


Figure 9-7. Efficiency V_{IN} = 2.8V and T_A = 85°C

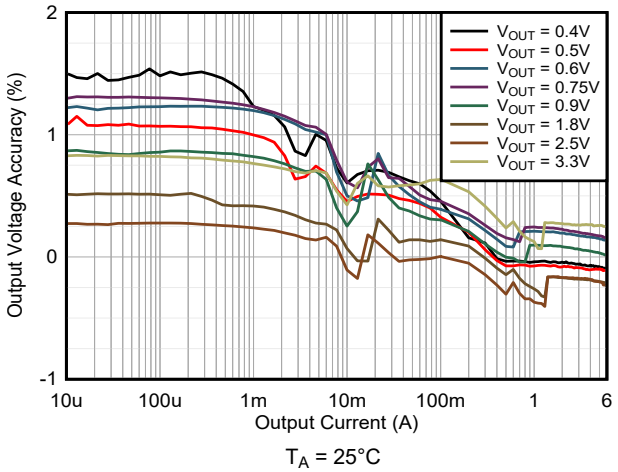


Figure 9-8. Load Regulation V_{IN} = 5.0V and PSM

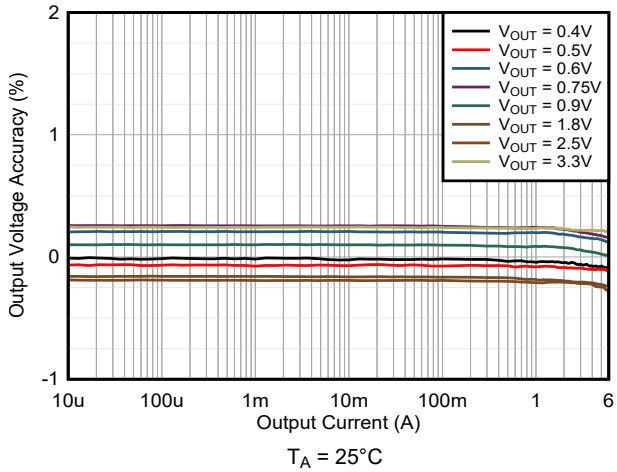


Figure 9-9. Load Regulation V_{IN} = 5.0V and FPWM

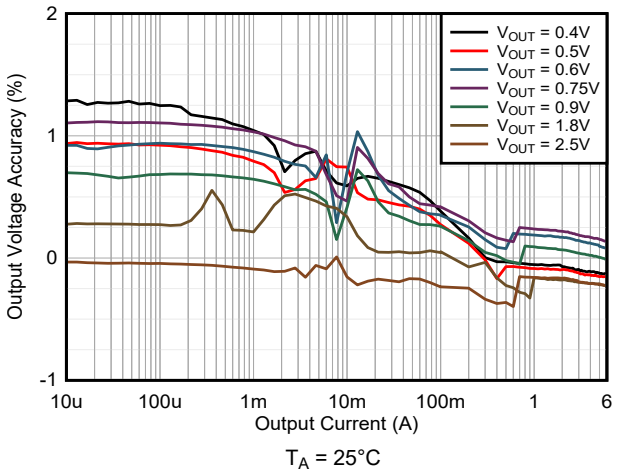


Figure 9-10. Load Regulation V_{IN} = 3.3V and PSM

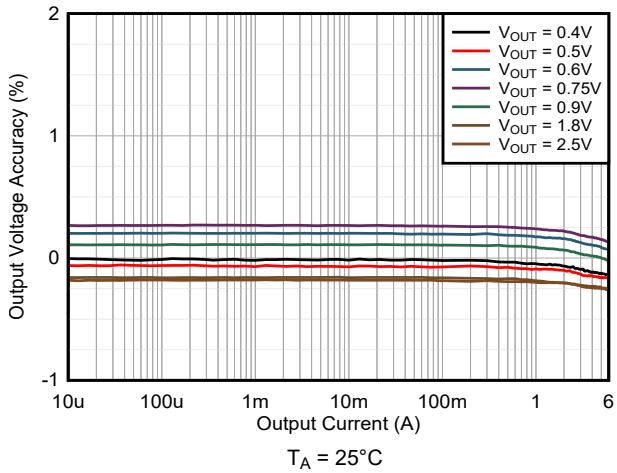


Figure 9-11. Load Regulation V_{IN} = 3.3V and FPWM

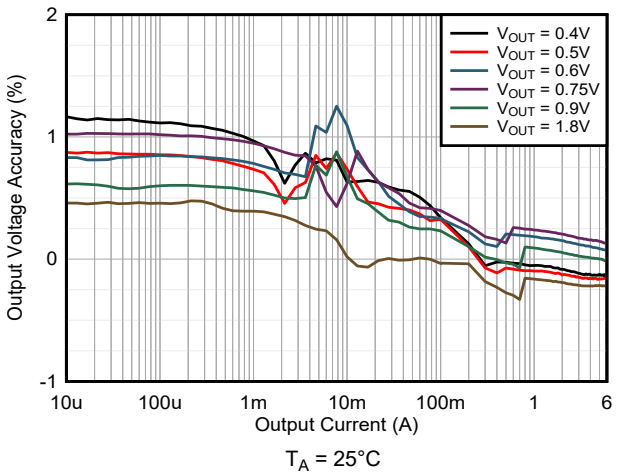


Figure 9-12. Load Regulation V_{IN} = 2.8V and PSM

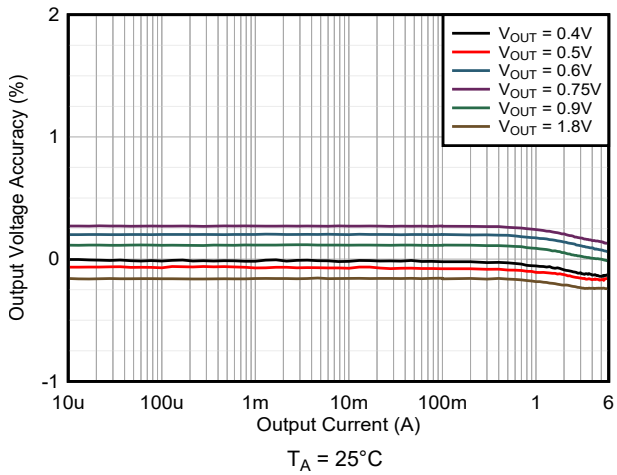
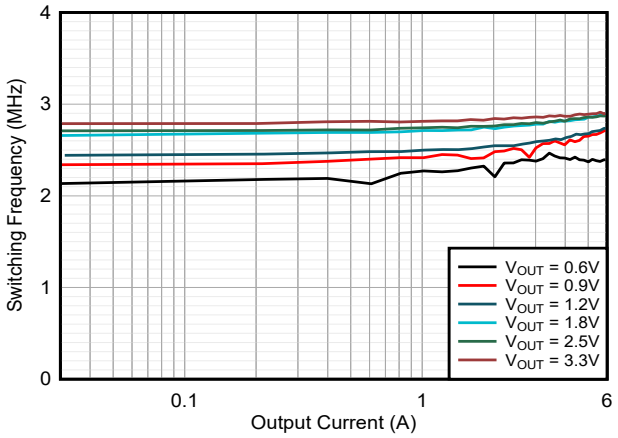


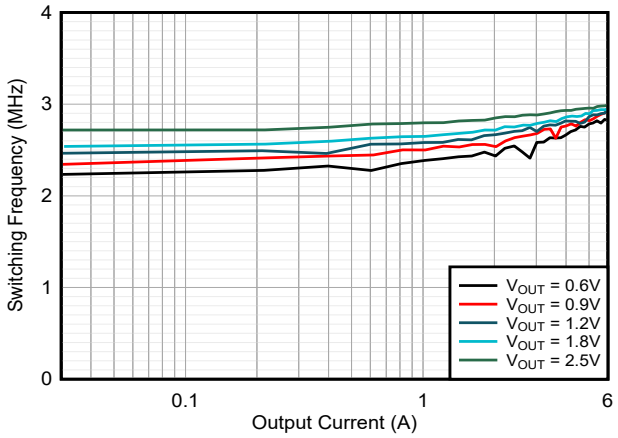
Figure 9-13. Load Regulation V_{IN} = 2.8V and FPWM

ADVANCE INFORMATION



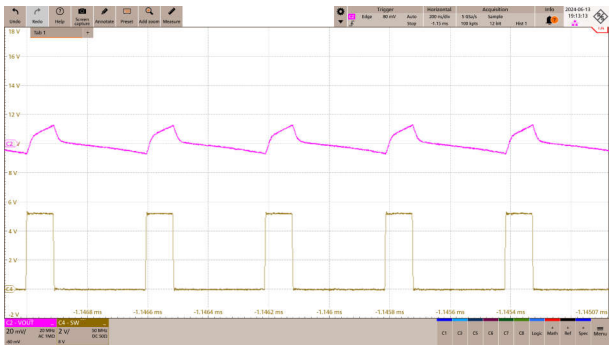
FPWM T_A = 25°C

Figure 9-14. Switching Frequency V_{IN} = 5.0V



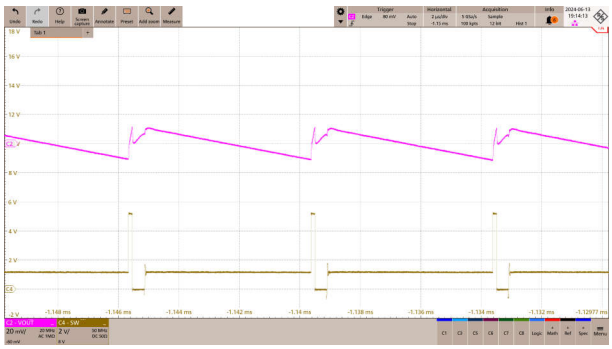
FPWM T_A = 25°C

Figure 9-15. Switching Frequency V_{IN} = 3.3V



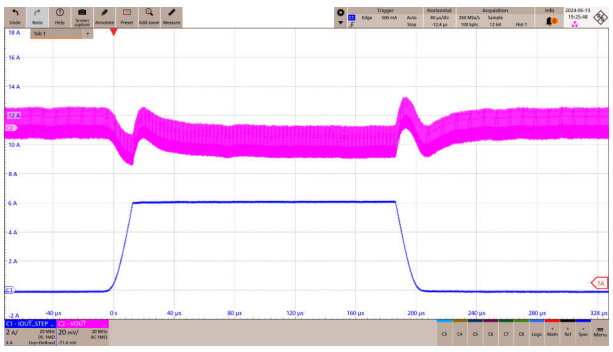
V_{IN} = 5.0V V_{OUT} = 1.2V T_A = 25°C

Figure 9-16. FPWM Operation I_{OUT} = 6A



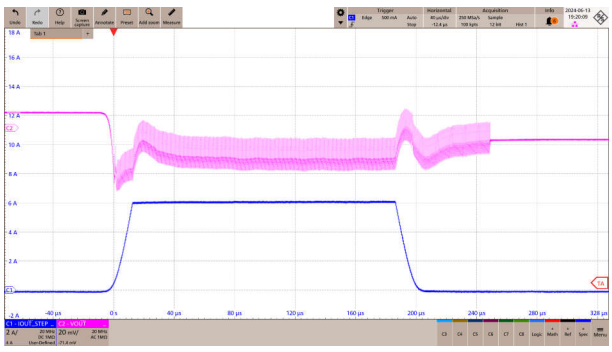
V_{IN} = 5.0V V_{OUT} = 1.2V T_A = 25°C

Figure 9-17. PSM Operation I_{OUT} = 0.1A



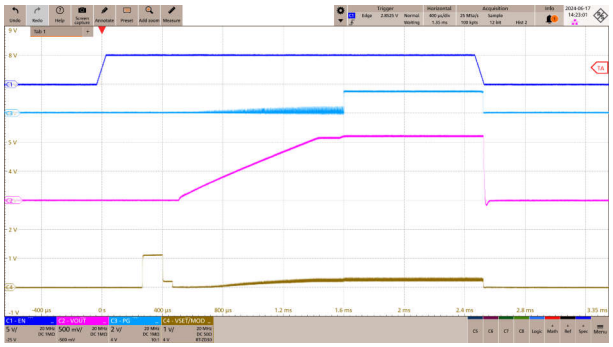
V_{IN} = 5.0V V_{OUT} = 1.2V T_A = 25°C

Figure 9-18. Load Transient FPWM I_{OUT} = 0A → 6A



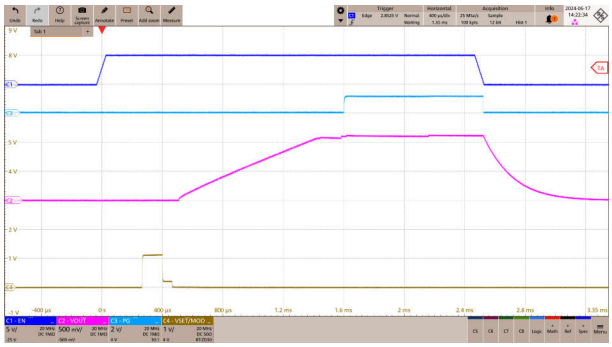
V_{IN} = 5.0V V_{OUT} = 1.2V T_A = 25°C

Figure 9-19. Load Transient PSM I_{OUT} = 0A → 6A



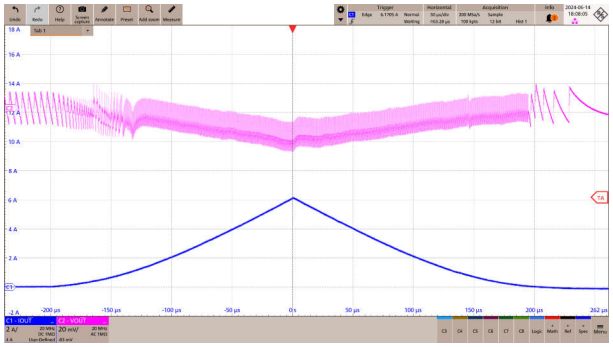
R_{VSET} = 56.2kΩ I_{OUT} = 6.0A

Figure 9-20. Start-Up into Full Load



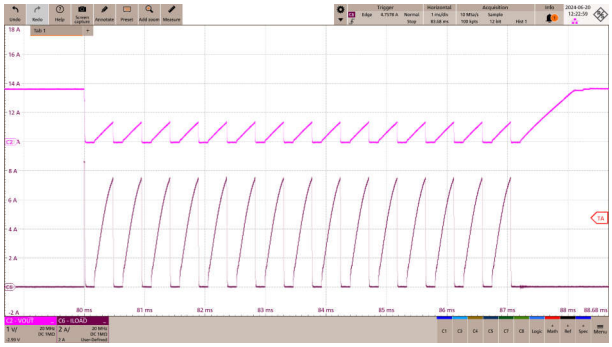
R_{VSET} = 56.2kΩ I_{OUT} = 0A

Figure 9-21. Start-Up With No Load



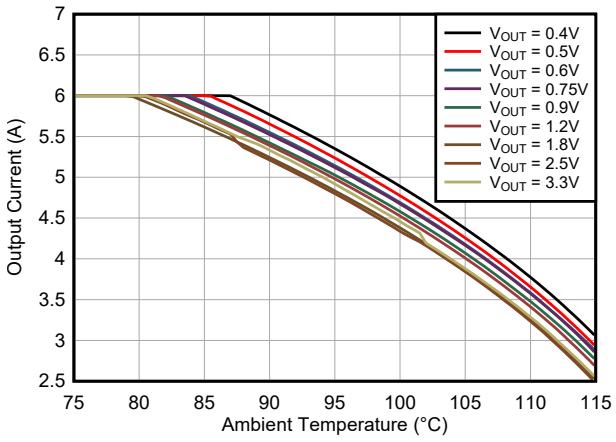
V_{IN} = 5.0V V_{OUT} = 1.2V T_A = 25°C

Figure 9-22. Load Sweep I_{OUT} = 20mA → 6A



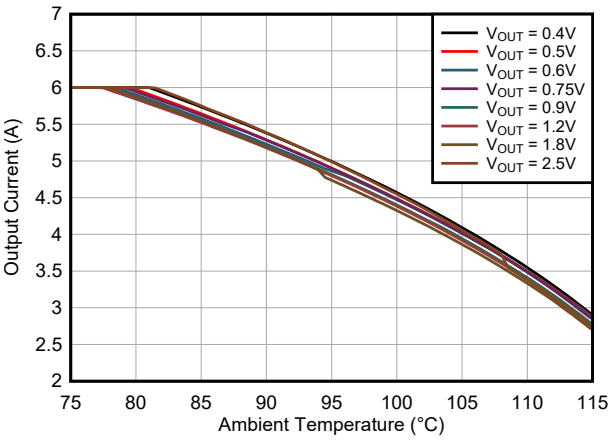
R_{LOAD} = 100mΩ (during overload)

Figure 9-23. HICCUP Short-Circuit Protection



$R_{\theta JA}$ = 29.7°C/W T_{Jmax} = 125°C

Figure 9-24. Safe Operating Area V_{IN} = 5.0V TPSM82866CAx



$R_{\theta JA}$ = 29.7°C/W T_{Jmax} = 125°C

Figure 9-25. Safe Operating Area V_{IN} = 3.3V TPSM82866CAx

ADVANCE INFORMATION

9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4V to 5.5V. The average input current of the TPSM8286xx is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (5)$$

Make sure that the input power supply has a sufficient current rating for the application. The power supply must avoid a fast ramp down. The falling ramp speed must be slower than 10mV/µs if the input voltage drops below V_{UVLO}.

9.4 Layout

9.4.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM8286xx demands careful attention to make sure of best performance. A poor layout can lead to issues like the following:

- Bad line and load regulation
- Instability
- Increased EMI radiation
- Noise sensitivity

Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal* for a detailed discussion of general best practices. The following are specific recommendations for the TPSM8286xx:

- Place the input capacitor as close as possible to the VIN and PGND pins of the device. This placement is the most critical component placement. Route the input capacitor directly to the VIN and PGND pins avoiding vias.
- Place the output capacitor close to the VOUT and PGND pins and route directly avoiding vias.
- Place R4 close to the VSET/VID pin to minimize noise pickup.
- Take special care to avoid noise being induced. Keep the trace away from SW. The sense traces connected to the VOS pin is a signal trace.
- Directly connect the AGND and PGND pins together on the top PCB layer.
- Refer to Figure 9-26 for an example of component placement, routing, and thermal design.
- See the recommended land pattern for the TPSM8286xx shown at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD) when some pins (such as VIN, VOUT, and PGND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

9.4.2 Layout Example

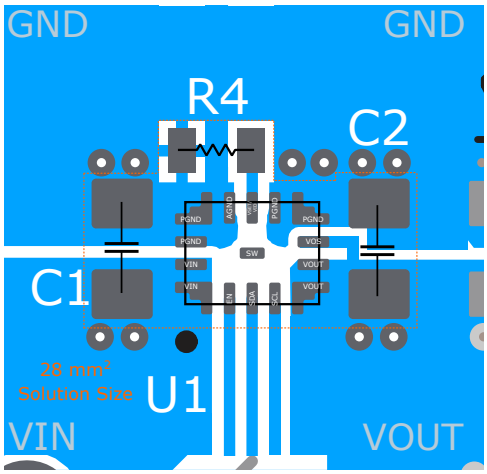


Figure 9-26. Layout Example

9.4.2.1 Thermal Considerations

The TPSM8286xx power module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM8286xx, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the thermal resistance. Using this method to compute the maximum device temperature, the Safe Operating Area (SOA) graphs demonstrate the required derating in maximum output current at high ambient temperatures. For more details on how to use the thermal parameters in real applications, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application report* and *Semiconductor and IC Package Thermal Metrics application note*.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics application note*
- Texas Instruments, *Benefits of a Resistor-to-Digital Converter in Ultra-Low Power Supplies white paper*
- Texas Instruments, *Simplify Low EMI Design With Power Modules white paper*
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2024	*	Initial Release

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

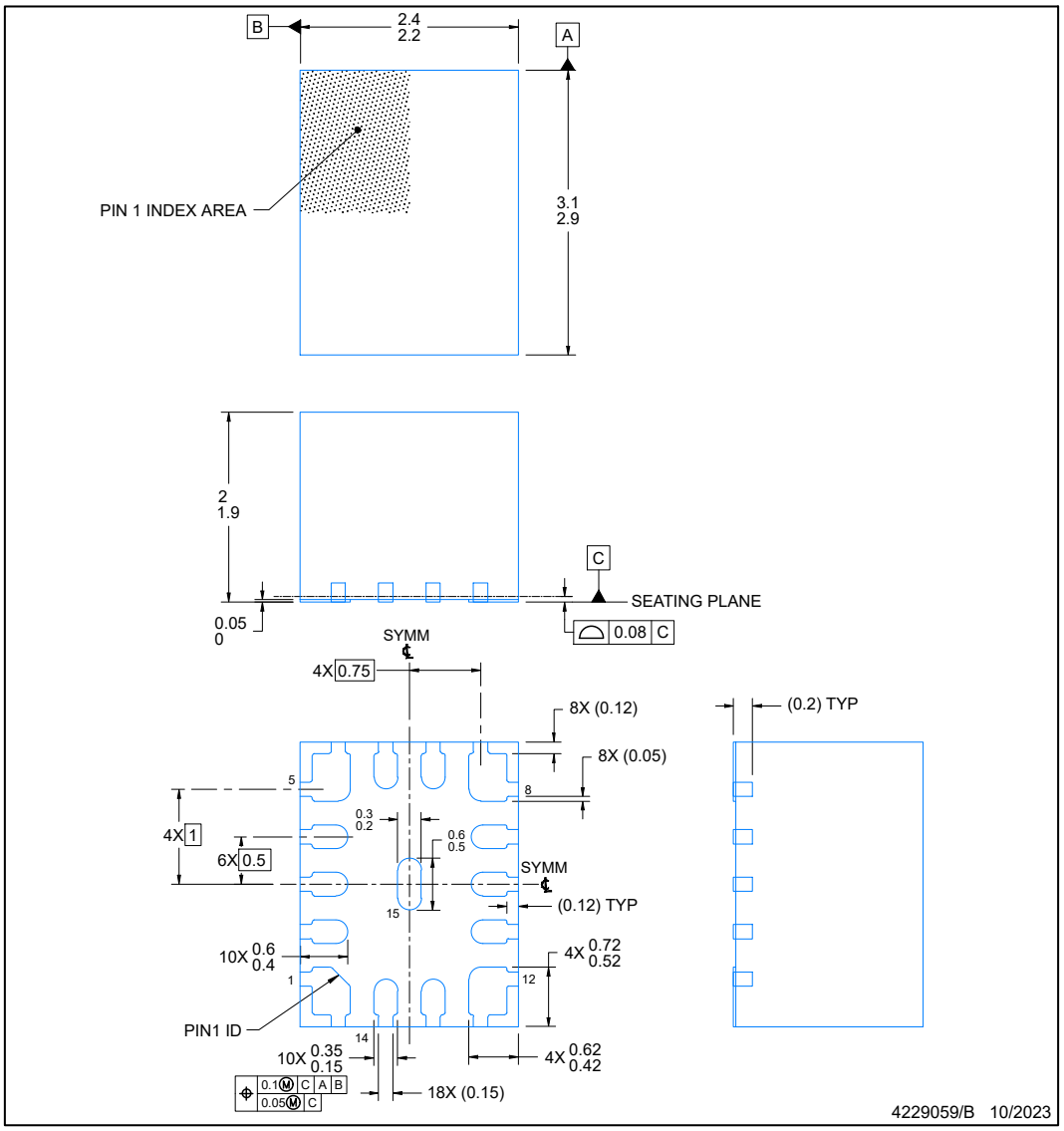
ADVANCE INFORMATION

PACKAGE OUTLINE

RCF0015A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



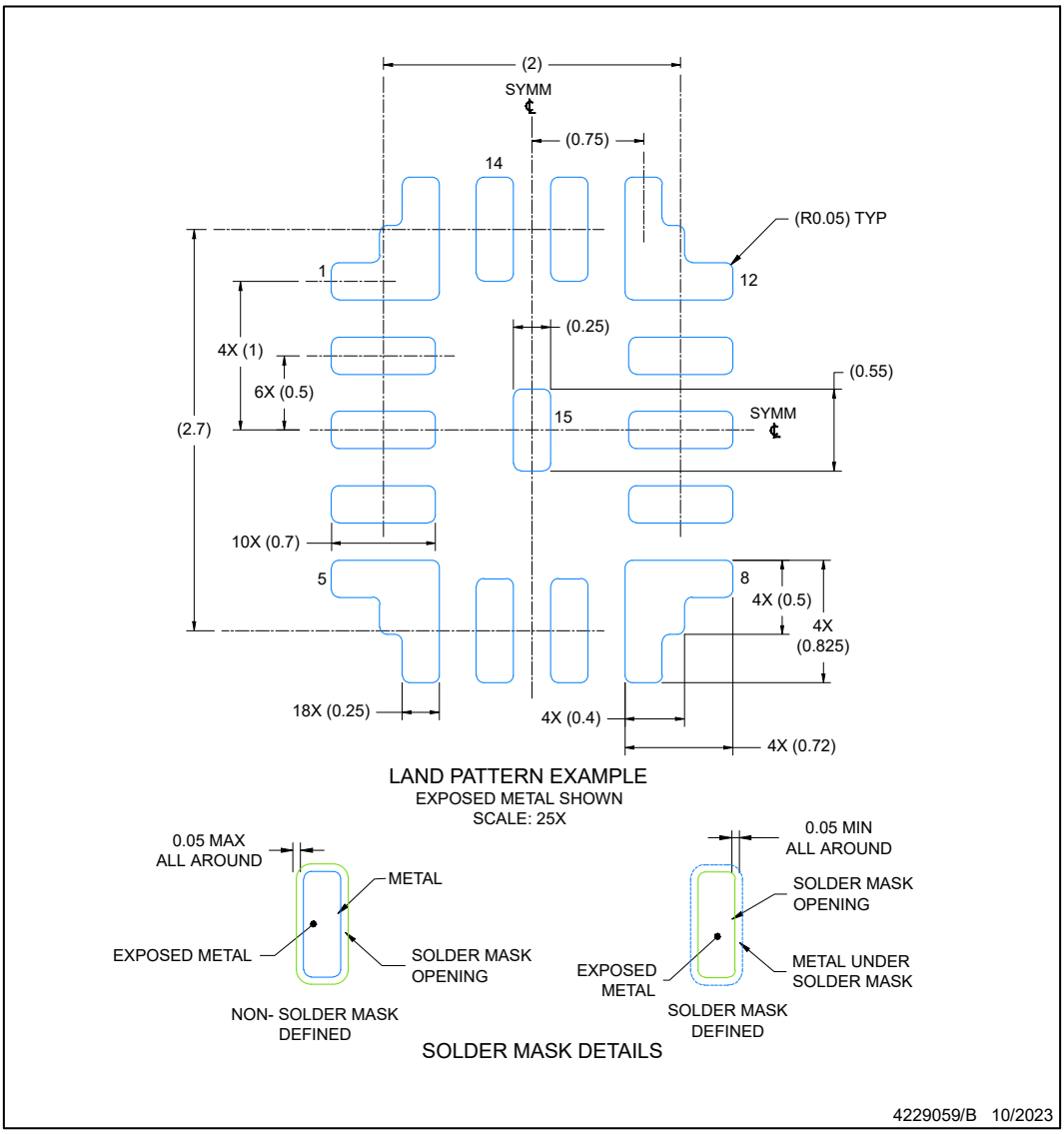
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RCF0015A — **QFN-FCMOD - 2 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

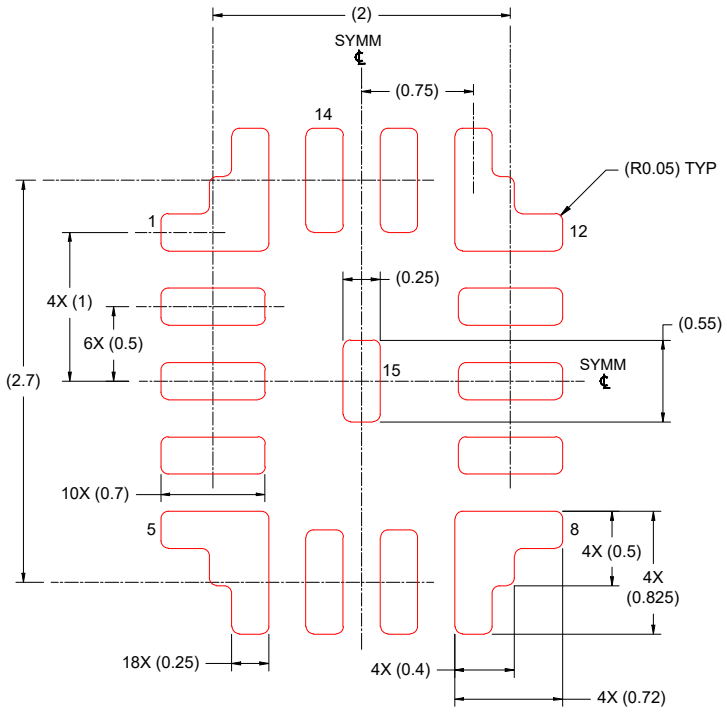
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RCF0015A — **QFN-FCMOD - 2 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

4229059/B 10/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XPSM82866CA3PRCFR	ACTIVE	QFN-FCMOD	RCF	15	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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