FEATURES

- **Offers Bandwidth Allocation of PCI Express™ Signal Using Two-Lane 1:2 Multiplexer/Demultiplexer**
- **Vcc Operating Range From 1.7 V to 1.9 V**
- **Supports Data Rates of 2.5 Gbps**
- **Port-Port Crosstalk (–39 dB at 1.25 GHz)**
- **OFF Port Isolation (–38 dB at 1.25 GHz)**
- **Low ON-State Resistance (10 Ω Typ)**
- **Low Input/Output Capacitance (3.5 pF Typ)**

- **Excellent Differential Skew (5 ps Max)**
- **Minimal Propagation Delay**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
 - **1000-V Charged-Device Model (C101)**

DESCRIPTION/ORDERING INFORMATION

The TS2PCIE2212 can be used to muxltiplex/demultiplex two PCI Express™ lanes, each representing differential pairs of receive (RX) and transmit (TX) signals. The switch operates at the PCI Express bandwidth standard of 2.5-Gbps signal-processing speed. The device is composed of two banks, with each bank accommodating two sources (source A and source B) and two destinations (destination A and destination B).

When a logic-level low is applied to the control (CTRL) pin, source A is connected to destination A and source B is connected to destination B. When a logic-level high is applied to CTRL, source A is connected to destination B, while source B and destination A are open.

ORDERING INFORMATION

T$_A$	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 85°C	BGA – ZAH	Tape and reel	TS2PCIE2212ZAHR	

ZAH PACKAGE
(BOTTOM VIEW)
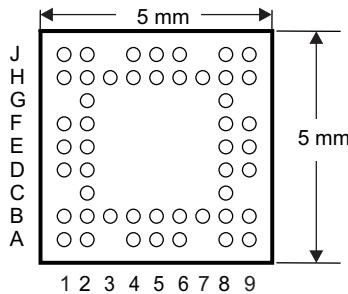
TERMINAL ASSIGNMENTS

|	1	2	3	4	5	6	7	8	9
A	CTRL0	TxSB:0P		TxSA:0P	GND	TxDA:0P		TxDB:0P	NC
B	RxSA:0P	GND	TxSB:0N	TxSA:0N	VDD	TxDA:0N	TxDB:0N	GND	RxDA:0P
C		RxSA:0N						RxDA:0N	
D	RxSB:0P	RxSB:0N						RxDB:0N	RxDB:0P
E	GND	VDD						VDD	GND
F	TxSA:1P	TxSA:1N						TxDA:1N	TxDA:1P
G		TxSB:1N						TxDB:1N	
H	TxSB:1P	GND	RxSA:1N	RxSB:1N	VDD	RxDB:1N	RxDA:1N	GND	TxDB:1P
J	NC	RxSA:1P		RXSB:1P	GND	RXDB:1P		RxDA:1P	CTRL1

![Warning icon] Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PCI Express is a trademark of PCI-SIG.

PIN DESCRIPTION

NAME	FUNCTION
TxSA:nP, TxSA:nN	Source A transmit pair
RxSA:nP, RxSA:nN	Source A receive pair
TxSB:nP, TxSB:nN	Source B transmit pair
RxSB:nP, RxSB:nN	Source B receive pair
TxDA:nP, TxDA:nN	Destination A transmit pair
RxDA:nP, RxDA:nN	Destination A receive pair
TxDB:nP, TxDB:nN	Destination B transmit pair
RxDB:nP, RxDB:nN	Destination B receive pair
CTRL0	Control signal for bank 0
CTRL1	Control signal for bank 1
V_{DD}	Positive supply voltage
GND	Ground (0 V)
NC	No internal connection

LOGIC DIAGRAM
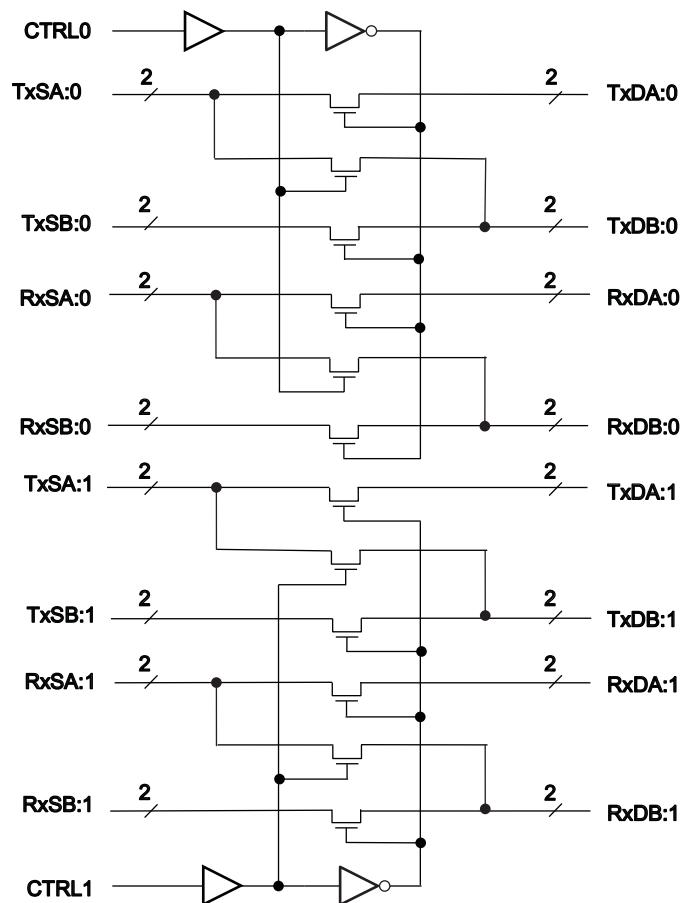
FUNCTION TABLE

CTRLn	FUNCTION
L	SA:n = DA:n, SB:n = DB:n
H	SA:n = DB:n, DA:n = open, SBin = open

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		−0.5	2.5	V
V_{IN}	Control input voltage range[2][3]		−0.5	2.5	V
$V_{I/O}$	Switch I/O voltage range[2][3][4]		−0.5	2.5	V
I_{IK}	Control input clamp current	$V_{IN} < 0$ and $V_{I/O} < 0$		50	mA
$I_{I/OK}$	I/O port clamp current	$V_{IN} < 0$ and $V_{I/O} < 0$		50	mA
$I_{I/O}$	ON-state switch current[5]			±100	mA
	Continuous current through V_{DD} or GND			±100	mA
θ_{JA}	Package thermal impedance[6]			TBD	°C/W
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		1.7	1.8	1.9	V
V_{IH}	High-level control input voltage	CTRL	0.65 V_{DD}			V
V_{IL}	Low-level control input voltage	CTRL			0.35 V_{DD}	V
V_{IO}	Data input/output voltage		0		V_{DD}	V
T_A	Operating free-air temperature		0		85	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			$T_A = 0°C$ to $85°C$			UNIT
					MIN	TYP	MAX	
V_{IK}	Control inputs	$V_{DD} = 1.7$ V,	$I_{IN} = -18$ mA				−1.8	V
I_{IN}	Control inputs	$V_{DD} = 1.9$ V,	$V_{IN} = V_{DD}$ or GND				±1	µA
I_{OZ}		$V_{DD} = 1.9$ V,	$V_O = 0$ to 1.9 V, $V_I = 0$,	Switch OFF			±5	µA
I_{CC}		$V_{DD} = 1.9$ V, $V_{IN} = V_{DD}$ or GND,	$I_{I/O} = 0$,	Switch ON or OFF		160	300	µA
C_{in}	Control inputs	$V_{DD} = 1.9$ V,	$V_{IN} = V_{DD}$ or GND			0.5	1.0	pF
$C_{IO(OFF)}$	SB or DA port	$V_{I/O} = 0$ V,	Switch OFF			1.4	1.5	pF
$C_{IO(ON)}$		$V_{I/O} = 0$ V,	Switch ON			3.5	4	pF
r_{on}		$V_{DD} = 1.7$ V,	$V_I = 0$ V,	$I_O = 10$ mA		10	14	Ω
		$V_{DD} = 1.7$ V,	$V_I = 1.5$ V,	$I_O = -10$ mA		12	17	
$\Delta r_{on(flat)}$		$V_{DD} = 1.7$ V,	$I_O = 10$ mA,	$V_I = 1.5$ V ± 0.4 V		2.5	5	Ω

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	$T_A = 0°C$ to $85°C$			UNIT
			MIN	TYP	MAX	
DR	Data rate per TX or RX pair			2.5		Gbps
t_{pd}	Propagation delay, Sx to Dx	See Figure 7		250		ps
t_{sk}	Intra-pair skew	f =1.25 GHz, See Figure 7			5	ps
t_{en} (t_{PZL}, t_{PZH})	Switch turn-on delay, CTRL to DA	See Figure 6			5	ns
t_{dis} (t_{PLZ}, t_{PHZ})	Switch turn-off delay, CTRL to DA	See Figure 6			2.5	ns
I_{LOSS}	Differential insertion loss	f =1.25 GHz, $R_{LOAD} = 50$ Ω, See Figure 1		−2.5	−3.2	dB
R_{LOSS}	Differential return loss	f =1.25 GHz, $R_{LOAD} = 50$ Ω, See Figure 2	−7.2	−9.5		dB
$I_{LOSS(CM)}$	Common-mode insertion loss	f =1.25 GHz, $R_{LOAD} = 50$ Ω, See Figure 3		−2		dB
O_{IFF}	Differential OFF isolation	f =1.25 GHz, $R_{LOAD} = 50$ Ω, See Figure 4	−33	−38		dB
X_{TALK}	Differential crosstalk	f =1.25 GHz, $R_{LOAD} = 50$ Ω, See Figure 5	−33	−39		dB

## OPERATING CHARACTERISTICS
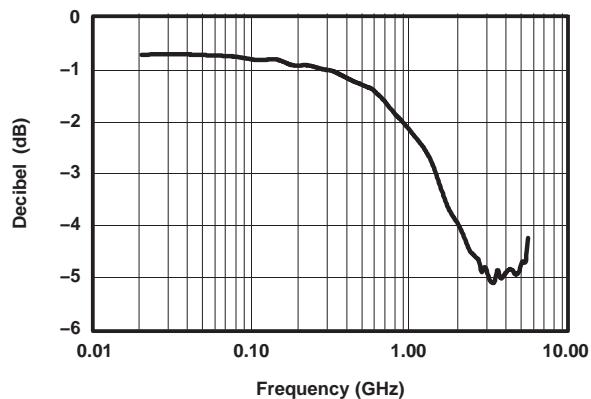
Figure 1. Differential Insertion Loss vs Frequency
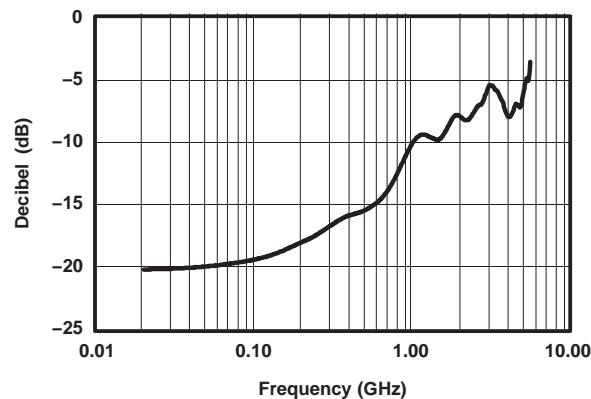

Figure 2. Differential Return Loss vs Frequency
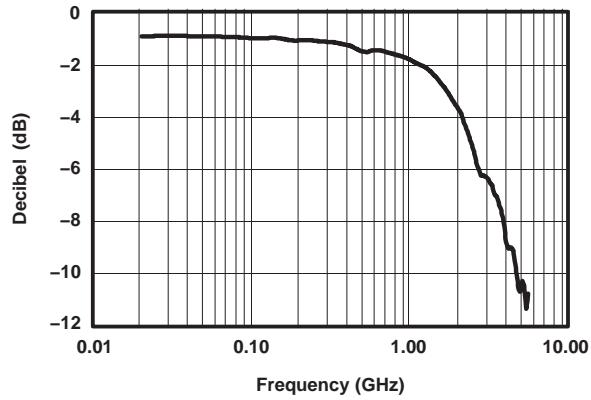

Figure 3. Common-Mode Insertion Loss vs Frequency
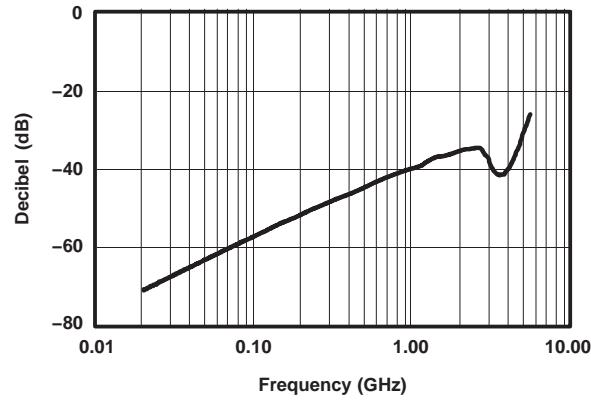


Figure 4. Differential OFF Isolation vs Frequency
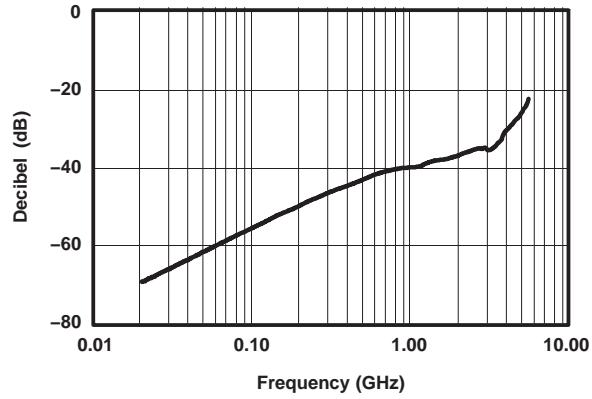
Figure 5. Differential Crosstalk vs Frequency

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)
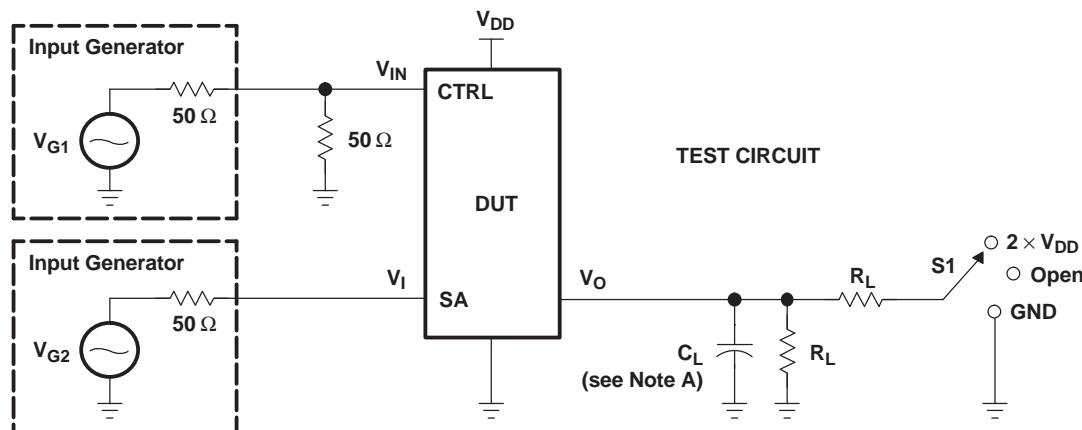
TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	1.8 V $\pm$ 0.1 V	$2 \times V_{DD}$	100 Ω	GND	No Load	0.3 V
t_{PHZ}/t_{PZH}	1.8 V $\pm$ 0.1 V	GND	100 Ω	V_{DD}	No Load	0.3 V
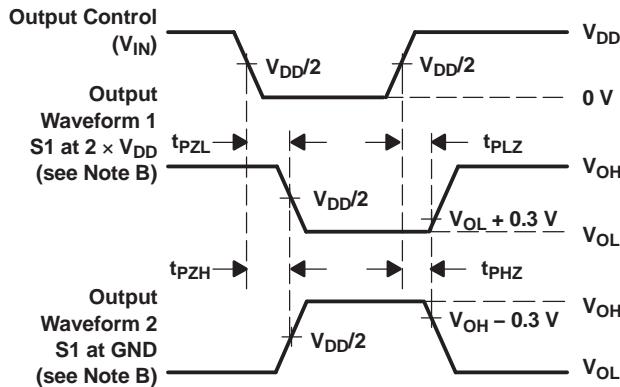
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
      D. The outputs are measured one at a time, with one transition per measurement.
      E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
      F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

| TEST PATH		T1[1]
SA:n = DA:n,	SB:n = DB:n	GND
SA:n = DB:n,	DA:n = open	V_{DD}

(1) T1 is an external terminal.

$V_{COM} = 1.5$ V

V_{CRS} is the cross point of the differential signal.

$t_{sk} = |t_{PLHn} - t_{PHLn}|$
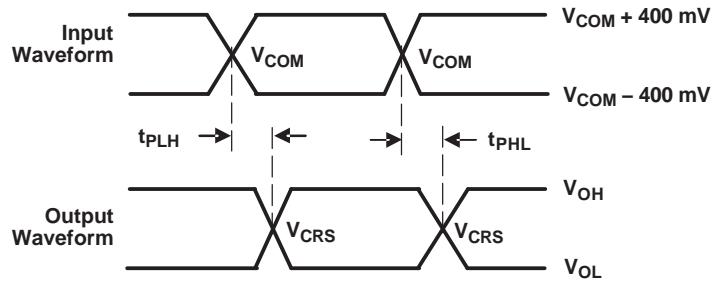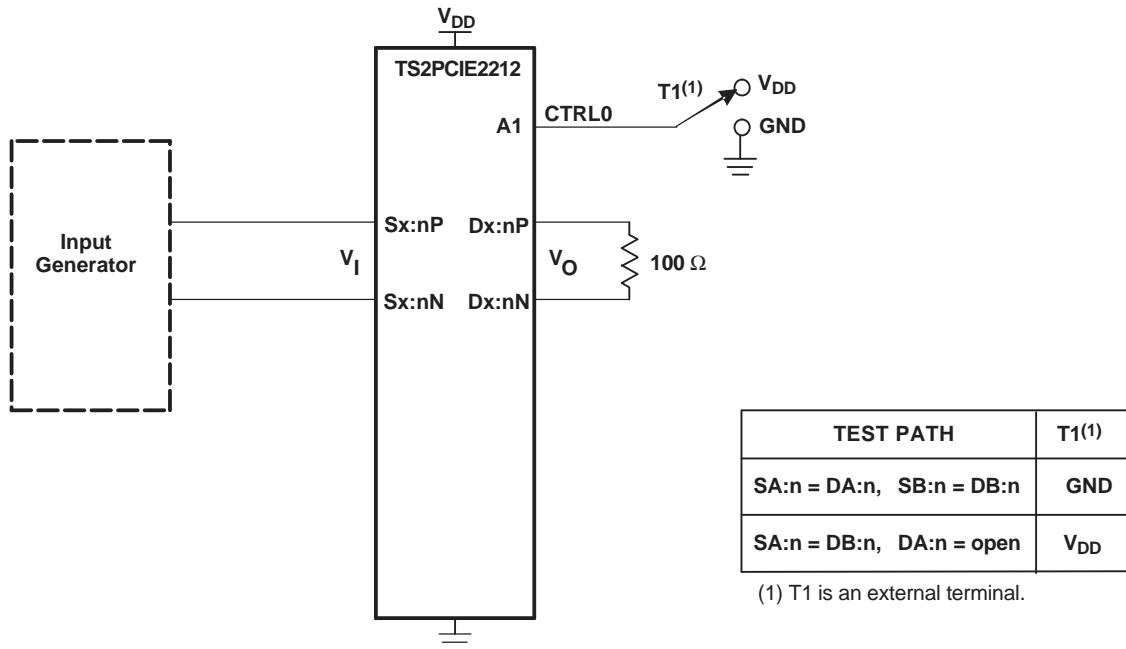
**Figure 7. Test Circuit for Propagation Delay and Intra-Pair Skew**

PARAMETER MEASUREMENT INFORMATION (continued)
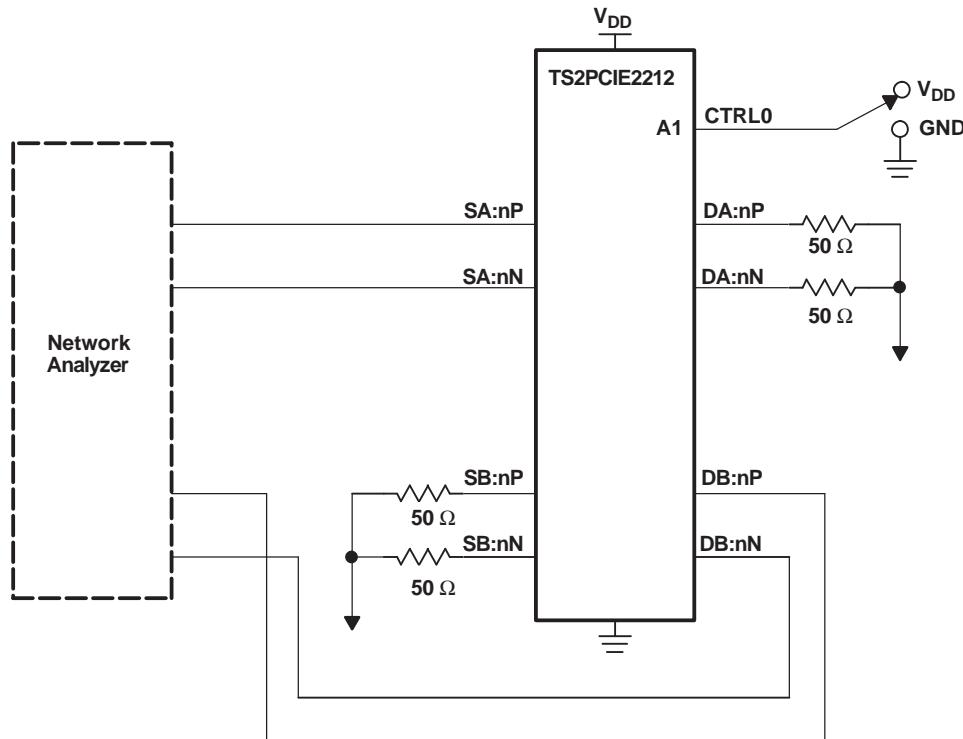
TEST	VNA MEASUREMENT
Differential insertion loss	S_{21}
Differential return loss	S_{11}
Common-mode insertion loss	S_{21}

**Figure 8. Differential Insertion Loss, Differential Return Loss,
and Common-Mode Insertion Loss Test Circuit**

PARAMETER MEASUREMENT INFORMATION (continued)
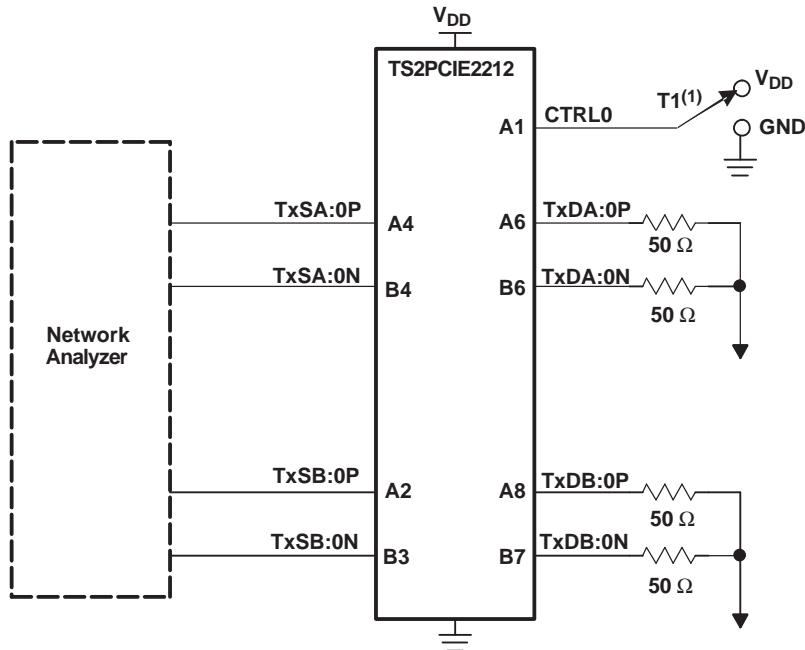
TEST	T1[1]
Differential crosstalk	GND
Differential OFF isolation	V_{DD}

(1) T1 is an external terminal.

Figure 9. Differential Crosstalk and OFF Isolation Test Circuit

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS2PCIE2212ZAHR	Last Time Buy	Production	NFBGA (ZAH) | 48	3000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	SE212
TS2PCIE2212ZAHR.A	Last Time Buy	Production	NFBGA (ZAH) | 48	3000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	SE212
TS2PCIE2212ZAHRG1	Last Time Buy	Production	NFBGA (ZAH) | 48	3000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-	SE212
TS2PCIE2212ZAHRG1.A	Last Time Buy	Production	NFBGA (ZAH) | 48	3000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	SE212

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)
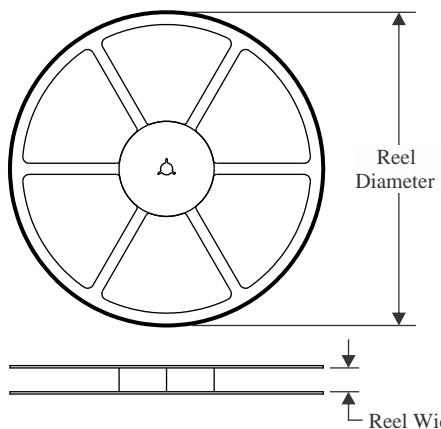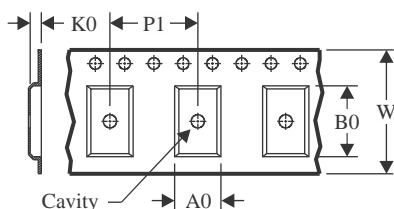
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

| Q1 | Q2 |
| Q3 | Q4 |

Sprocket Holes

User Direction of Feed

Pocket Quadrants
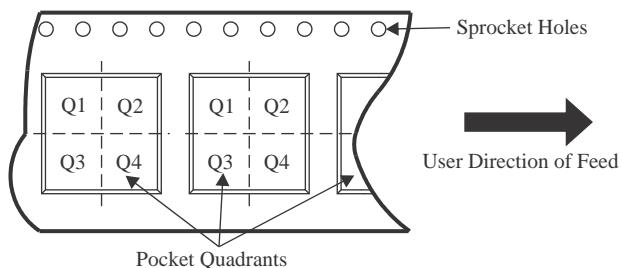
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS2PCIE2212ZAHRG1	NFBGA	ZAH	48	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS
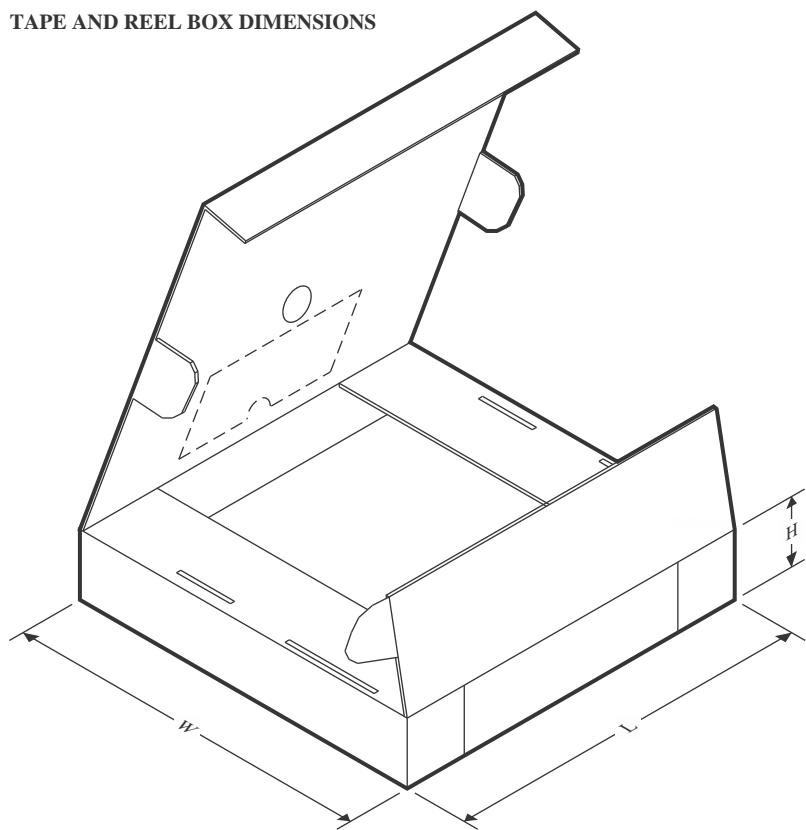
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS2PCIE2212ZAHRG1	NFBGA	ZAH	48	3000	336.6	336.6	31.8

ZAH0048A

A | 5.1 / 4.9 | B

BALL A1 CORNER INDEX AREA

5.1 / 4.9

(0.89)

1.2 MAX

C

SEATING PLANE

0.25 / 0.15 TYP

BALL TYP

◯ 0.08 C

4 TYP

SYMM ℄

(0.5) TYP

J H G F E D C B A

1 2 3 4 5 6 7 8 9

4 TYP

(0.5) TYP

SYMM ℄

48X ∅ 0.35 / 0.25

⊕ | ∅ 0.15 Ⓜ | C | A Ⓢ | B Ⓢ
∅ 0.05 Ⓜ | C

0.5 TYP

0.5 TYP
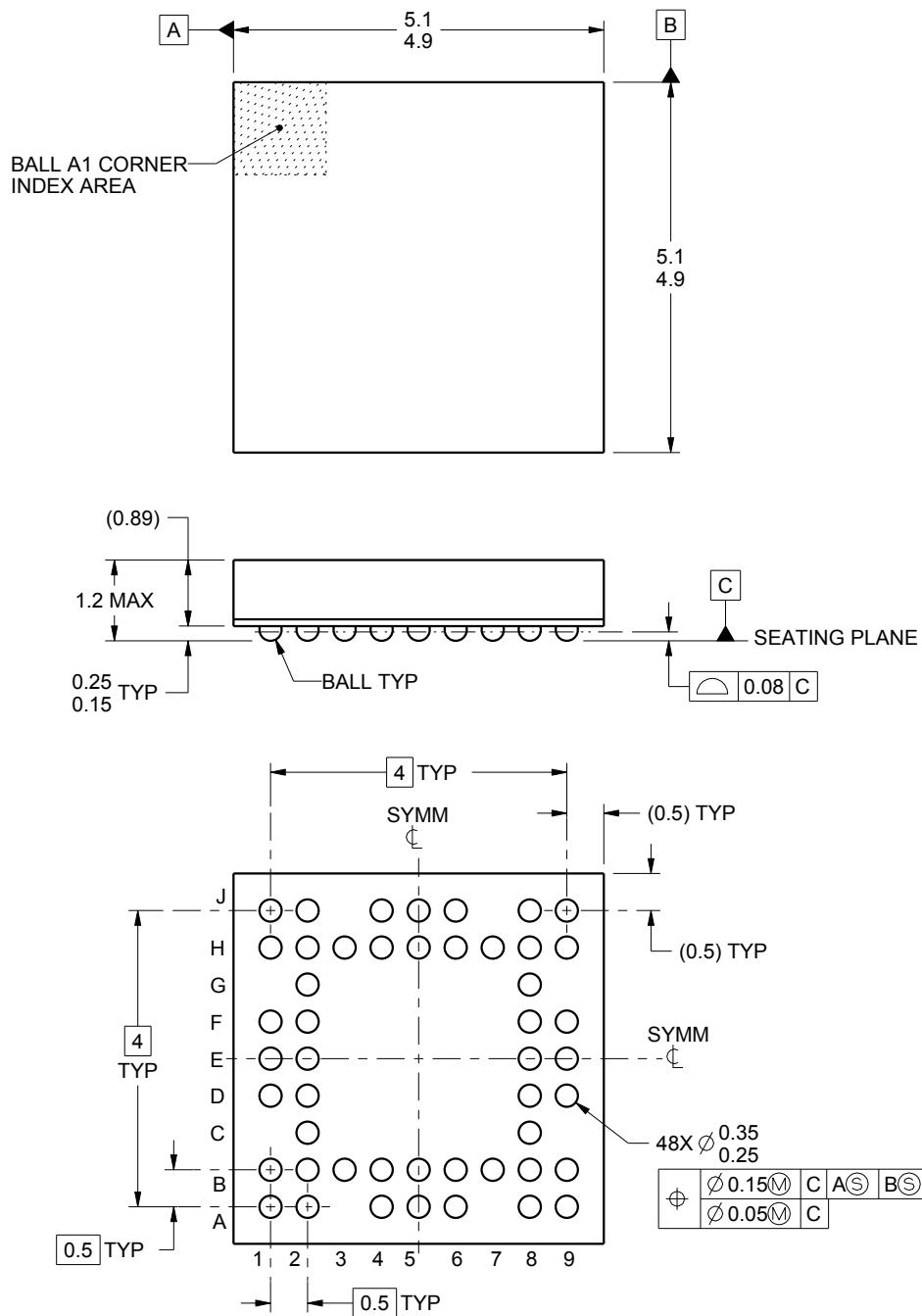
4221741/A   10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

48X (⌀ 0.25)

(0.5) TYP

(0.5) TYP

SYMM ₵

SYMM ₵
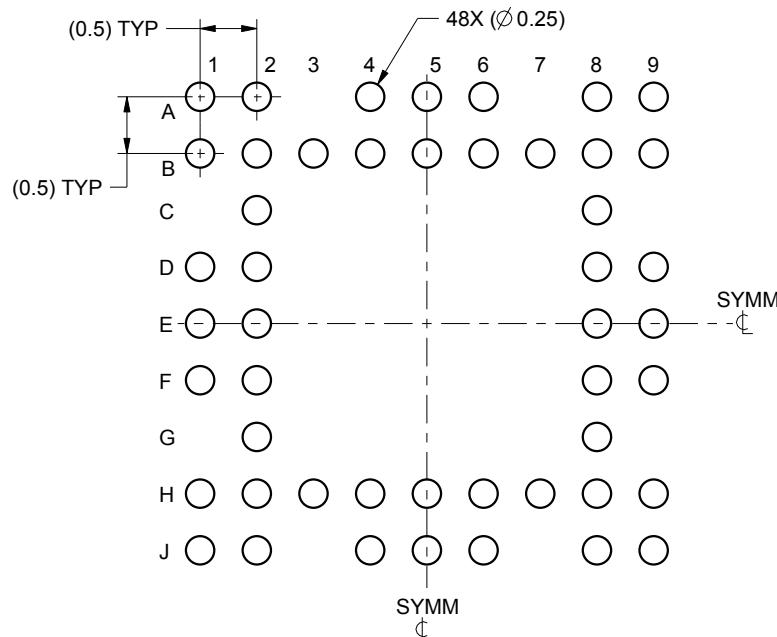
LAND PATTERN EXAMPLE
SCALE:15X

0.05 MAX

(⌀ 0.25)
METAL

SOLDER MASK
OPENING

**NON-SOLDER MASK
DEFINED
(PREFERRED)**

0.05 MIN

METAL UNDER
SOLDER MASK

(⌀ 0.25)
SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**
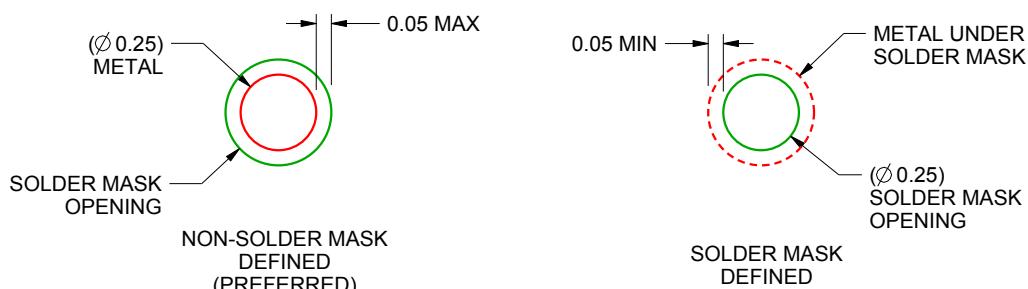
SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SSYZ015 (www.ti.com/lit/ssyz015).

ZAH0048A

PLASTIC BALL GRID ARRAY

48X (□ 0.25)

(0.5) TYP

(R0.05) TYP

(0.5) TYP

METAL
TYP

SYMM
℄

SYMM
℄
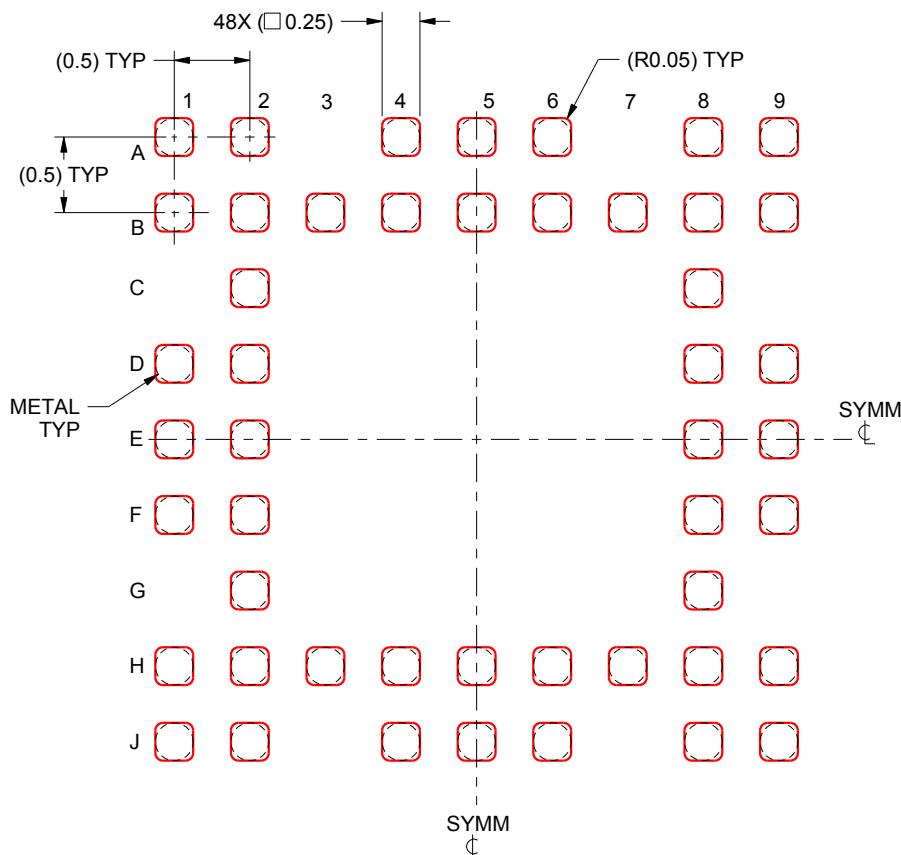
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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