

2 X 2 Crosspoint Switch for Audio Applications

Check for Samples: [TS3A26746E](#)

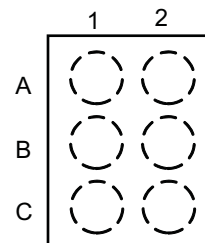
FEATURES

- Ultra Low R_{ON} for GND Switch (80-m Ω typical)
- R_{ON} for MIC Switch <10- Ω
- 3.0V to 3.6V V+ Operation
- Control Input is 1.8-V Logic Compatible
- 6-bump, 0.5mm pitch CSP Package (1.45mm x 0.95mm x 0.5mm)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 500-V Charged-Device Model (C101)
- ESD Performance (SLEEVE, RING2)
 - \pm 8-kV Contact Discharge (IEC 61000-4-2)

APPLICATIONS

- Cellular phones
- PDAs
- Portable Instrumentation
- Digital Still Cameras
- Portable Navigation Devices

PINOUT



DESCRIPTION

The TS3A26746E is a 2 x 2 cross-point switch that is used to interchange the Ground and MIC connections on a headphone connector. The Ground switch has an ultra low R_{ON} of <0.1 Ω to minimize voltage drop across it, preventing undesired increases in headphone ground reference voltage. The switch state is controlled via the SEL input. When SEL=High, GND is connected to RING2 and MIC is connected to SLEEVE. When SEL=Low, GND is connected to SLEEVE and MIC is connected to RING2. An internal 100k pull-up resistor on the SEL input sets the default state of the switch.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION BLOCK DIAGRAM

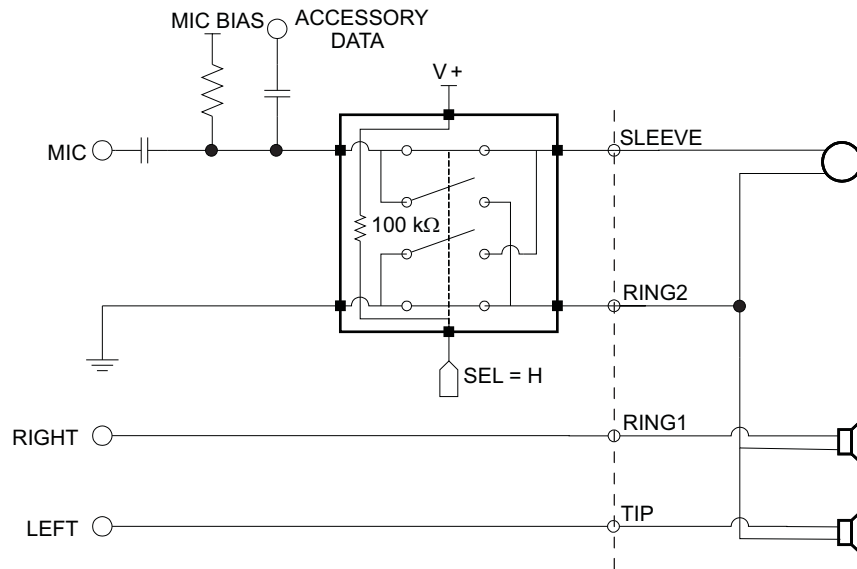


Figure 1. Standard Headphone Configuration (SEL=H)

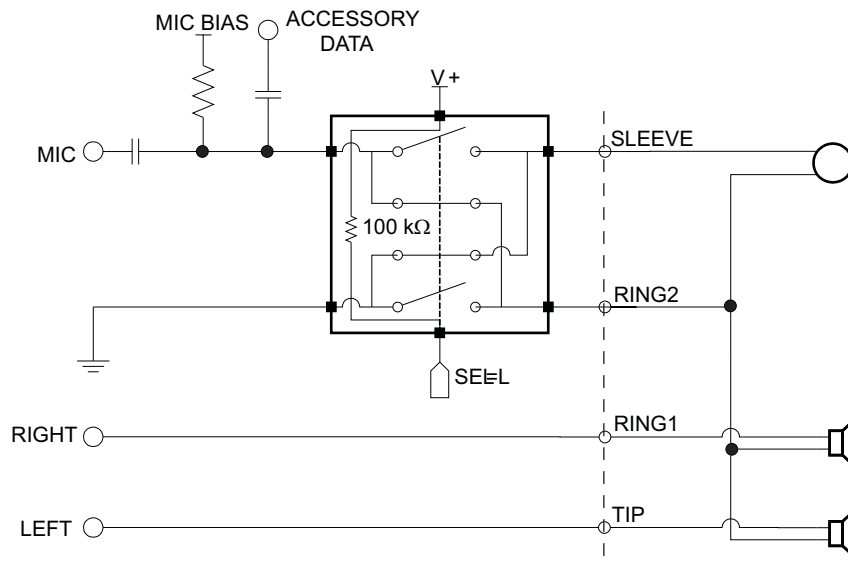
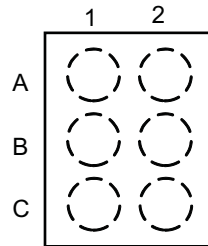


Figure 2. Alternate Headphone Configuration (SEL=L)

PINOUT



TERMINAL ASSIGNMENTS

	1	2
A	SEL	V+
B	MIC	SLEEVE
C	GND	RING2

PIN FUNCTIONS

BALL #	PIN		DESCRIPTION
	NAME	TYPE	
A1	SEL	Input	Control Input
A2	V+	Power	Supply Voltage
B1	MIC	I/O	MIC
B2	SLEEVE	I/O	Sleeve Connection on Headphone Jack
C1	GND	Ground	Ground
C2	RING2	I/O	2 nd Ring Connection on Headphone Jack

Table 1. FUNCTION TABLE

SEL	MIC to SLEEVE, GND to RING2	MIC to RING2, GND to SLEEVE
L	OFF	ON
H	ON	OFF

TS3A26746E

SCDS313C – FEBRUARY 2011 – REVISED MAY 2013

www.ti.com
ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V ₊	Supply voltage range ⁽³⁾		-0.3	4.0	V
V _{MIC} V _{SLEEVE} V _{RING2}	Analog voltage range ⁽³⁾		-0.3	4.0	V
I _K	Analog port diode current	V _{MIC} , V _{SLEEVE} , V _{RING2} < 0 V	-50		mA
V _I	Digital input voltage range		-0.3	4.0	V
I _{IK}	Digital input clamp current ⁽³⁾	V _I < 0 V	-50		mA
I ₊	Continuous current through V ₊			100	mA
I _{GND}	Continuous current through GND		-100		mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	YZP package		102	°C/W
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY⁽¹⁾

 V₊ = 3 V to 3.6 V, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A	V ₊	MIN	TYP	MAX	UNIT
MIC SWITCH							
V _{MIC} , V _{SLEEVE} , V _{RING2}	Analog signal range			0		V+	V
r _{on}	ON-state resistance	0 ≤ V _{SLEEVE} or V _{RING2} ≤ V ₊ , I _{MIC} = -32 mA	Switch ON	25°C	3 V	5 8	Ω
				Full		10	
r _{on(flat)}	ON-state resistance flatness	0 ≤ V _{SLEEVE} or V _{RING2} ≤ V ₊ , I _{MIC} = -32 mA	Switch ON	25°C	3 V	1 2.3	Ω
				Full		2.5	
I _{SLEEVE(OFF)} , I _{RING2(OFF)}	SLEEVE, RING2 OFF leakage current	V _{SLEEVE} or V _{RING2} = 1 V, V _{MIC} = 3 V, or V _{SLEEVE} or V _{RING2} = 3 V, V _{MIC} = 1 V	Switch OFF	25°C	3.6 V	-0.5 0.05 0.5	μA
				Full		-2	
I _{MIC(OFF)}	MIC OFF leakage current	V _{SLEEVE} or V _{RING2} = 3 V, V _{MIC} = 1 V, or V _{SLEEVE} or V _{RING2} = 1 V, V _{MIC} = 3 V	Switch OFF	25°C	3.6 V	-1 0.1 1	μA
				Full		-2	
I _{SLEEVE(ON)} , I _{RING2(ON)}	SLEEVE, RING2 ON leakage current	V _{SLEEVE} or V _{RING2} = 1 V, V _{MIC} = Open, or V _{SLEEVE} or V _{RING2} = 3 V, V _{MIC} = Open	Switch ON	25°C	3.6 V	-2 0.5 2	μA
				Full		-2	
I _{MIC(ON)}	MIC ON leakage current	V _{SLEEVE} or V _{RING2} = Open V, V _{MIC} = 1 V, or V _{SLEEVE} or V _{RING2} = Open, V _{MIC} = 3 V	Switch ON	25°C	3.6 V	-2 0.5 2	μA
				Full		-2	
GND SWITCH							
r _{on}	ON-state resistance	I _{SLEEVE} or I _{RING2} = +32 mA, V _{GND} = 0 V, I _{GND} = -32 mA	Switch ON	25°C	3 V	0.08 0.09	Ω
				Full			
I _{SLEEVE(OFF)} , I _{RING2(OFF)}	SLEEVE, RING2 OFF leakage current	V _{SLEEVE} or V _{RING2} = 3V and V _{GND} = 0 V	Switch OFF	25°C	3.6 V	-0.5 0.05 0.5	μA
						Full	
I _{SLEEVE(PWROFF)} , I _{RING2(PWROFF)}	SLEEVE, RING2 OFF leakage current	V _{SLEEVE} or V _{RING2} = 0 to 3.6 V and V _{GND} = 0 V	Switch OFF	25°C	0 V	-1 0.5 1	μA
						Full	

- (1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY⁽¹⁾ (continued)
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
DIGITAL CONTROL INPUTS (SEL)								
V_{IH}	Input logic high		Full	3.6 V	1.2		3.6	V
V_{IL}	Input logic low		Full	3.6 V	0		0.4	V
I_{IH}	Input logic high leakage current	$V_I = V_+$	25°C	3.6 V	-1	0.05	1	μA
			Full		-2		2	
I_{IL}	Input logic low leakage current	$V_I = 0\text{ V}$	25°C	3.6 V	-38	-36	-34	μA
			Full		-45		-30	
DYNAMIC								
t_{ON}	Turn-on time	$V_{MIC} = V_+$, $R_L = 50\ \Omega$	$C_L = 35\ \text{pF}$	25°C	3.3 V		150 200	ns
				Full	3 V to 3.6 V			
t_{OFF}	Turn-off time	$V_{MIC} = V_+$, $R_L = 50\ \Omega$	$C_L = 35\ \text{pF}$	25°C	3.3 V		5 10	ns
				Full	3 V to 3.6 V			
t_{BBM}	Break-before-make time	$V_{MIC} = V_+$	25°C	3.3 V		70	330	ns
			Full	3 V to 3.6 V			330	
C_{MIC}	MIC capacitance	SEL=High	25°C	3.3 V		100	140	pF
		SEL=Low	25°C	3.3 V		100	140	
C_{SLEEVE}	SLEEVE / RING2 capacitance	SEL=High	25°C	3.3 V		100	140	pF
		SEL=Low	25°C	3.3 V		100	140	
C_I	Digital input capacitance	$V_I = V_+$ or 0 V	25°C	3.3 V		4.0		pF
THD	Total harmonic distortion	$R_L = 1\text{ k}\ \Omega$, $V = 30\text{ mVPP}$	f = 20 Hz to 20 kHz 25°C	3.3 V		0.01%		
SUPPLY								
V_+	Power Supply Voltage				3.0	3.3	3.6	V
I_+	Positive supply current	$V_I = V_+$	25°C	3.6 V		0.01	1	μA
			Full				5	
		$V_I = 0\text{ V}$	25°C			40	41	μA
			Full				50	

OPERATIONAL CHARACTERISTICS

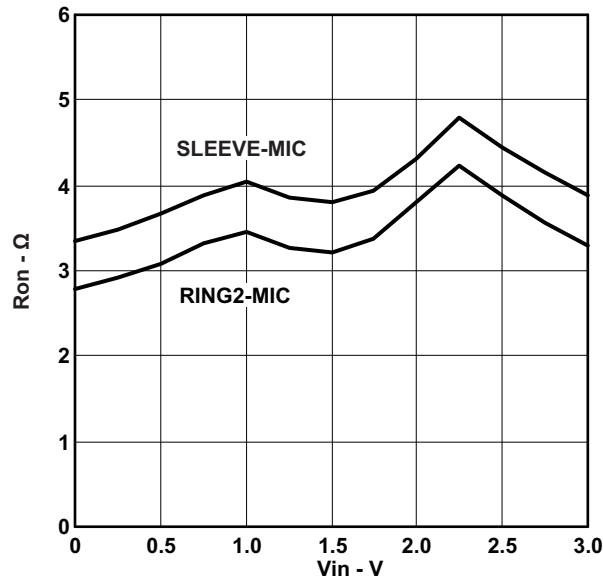
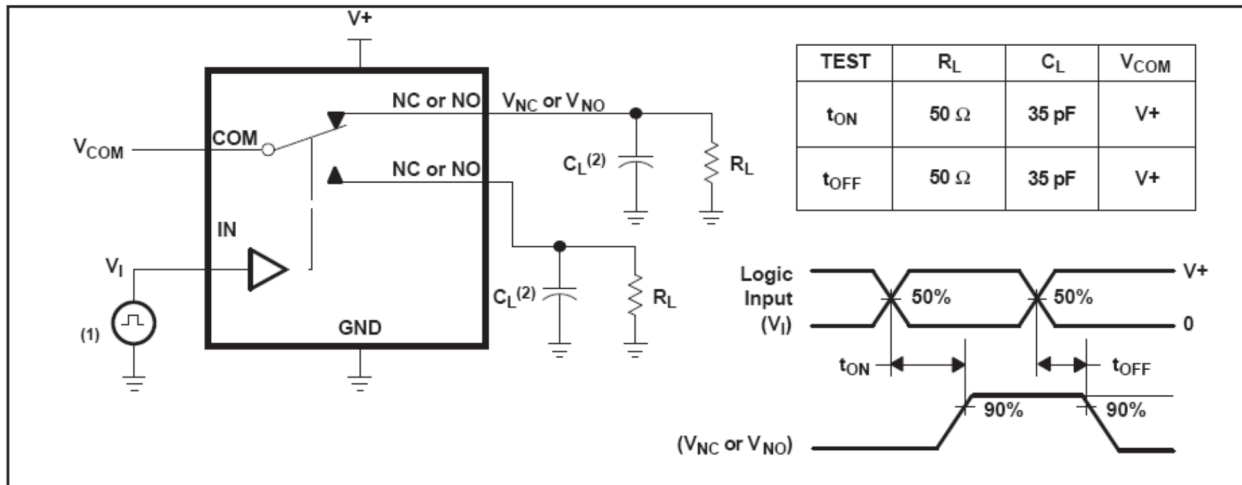


Figure 3. R_{ON} vs V_{IN} (MIC Switch)

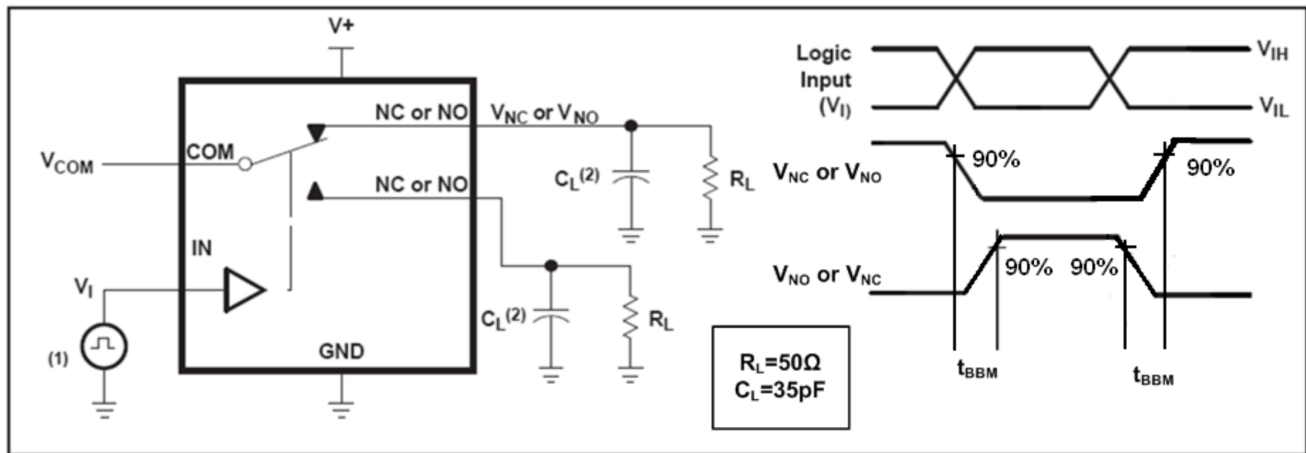
PARAMETER MEASUREMENT INFORMATION



- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- B. C_L includes probe and jig capacitance.

Figure 4. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

Figure 5. Break-Before-Make Time (t_{BBM})

REVISION HISTORY

Changes from Revision B (November 2011) to Revision C	Page
• Replaced 1 page preview with full document.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A26746EYZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A26746EYZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A26746EYZPR	DSBGA	YZP	6	3000	182.0	182.0	20.0

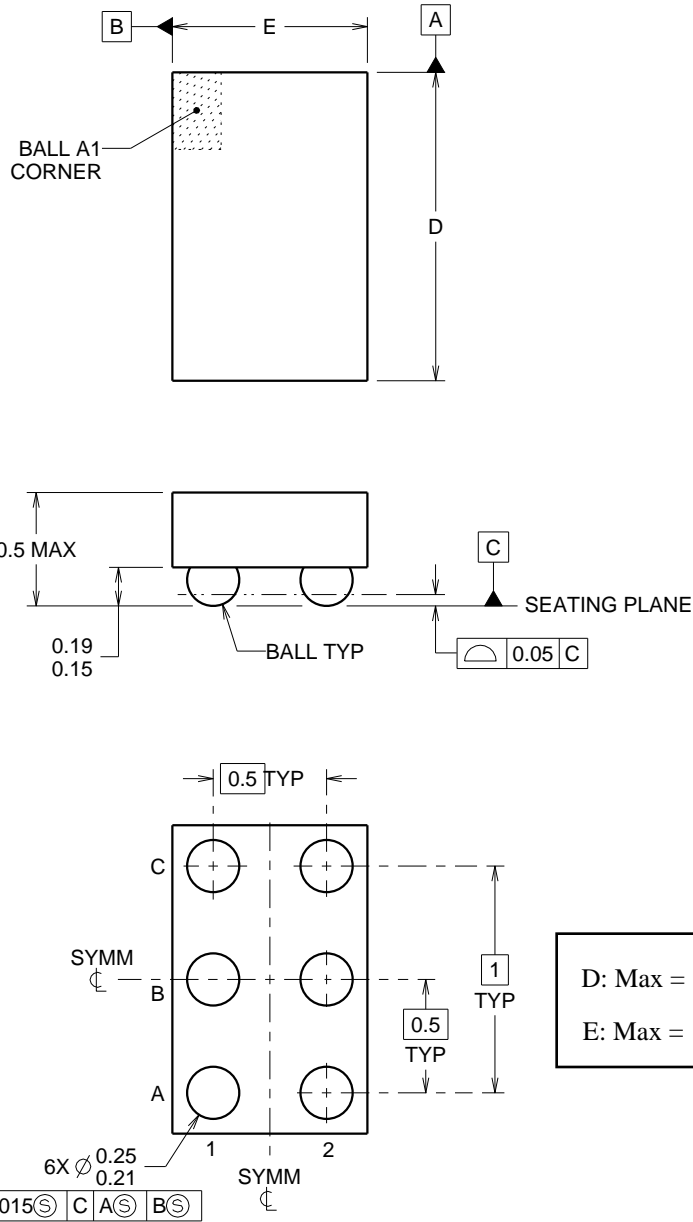
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm
E: Max = 0.917 mm, Min = 0.857 mm

4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

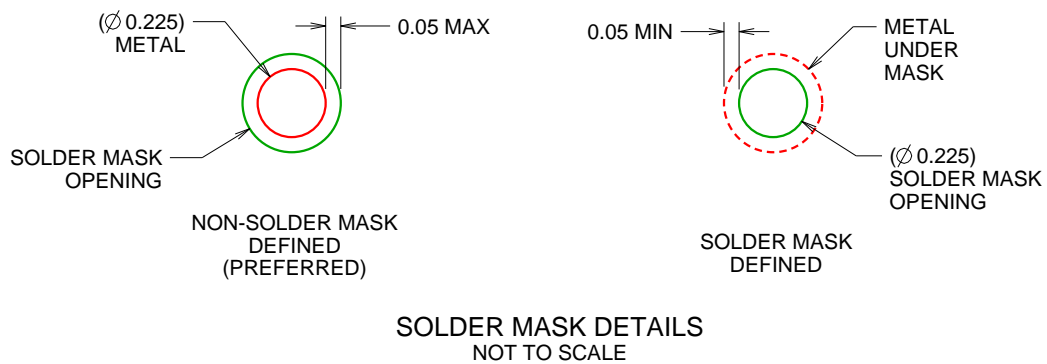
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

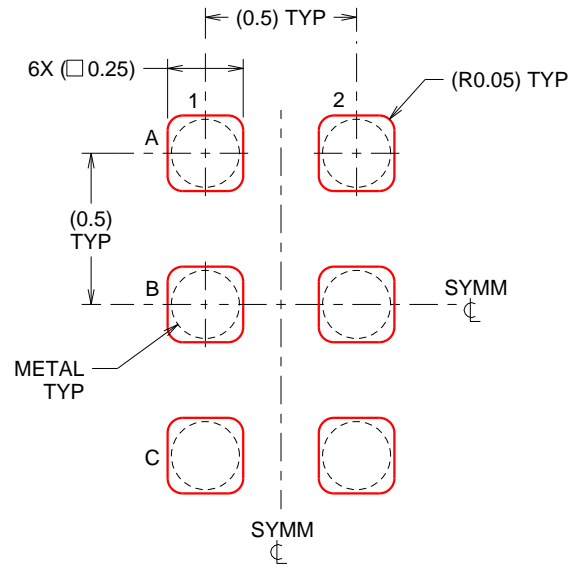
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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