TUSB2E22 eUSB2-USB 2.0 Dual Repeater

1 Features

- Compliance to USB 2.0 and eUSB2 (rev 1.1)
- Support for low-speed (LS), full-speed (FS), high-speed (HS)
- Dual repeater with 2:2 crossbar mux
- Host and device mode (DRD) support
- Four eUSB2 compensation settings to meet different system requirements
- eUSB2 LS/FS signaling meets 1.2V option of the eUSB2 interface

2 Applications

- Communications equipment
- Enterprise systems
- Notebooks and desktops
- Industrial
- Tablets
- Portable electronics

3 Description

TUSB2E22 enables implementation of USB 2.0 compliance port on newer processors using lower voltage processes.

TUSB2E22 is a USB-compliant eUSB2-USB 2.0 repeater supporting both device and host modes.

TUSB2E22 supports USB low-speed (LS) and full-speed (FS) signals and high-speed (HS) signals.

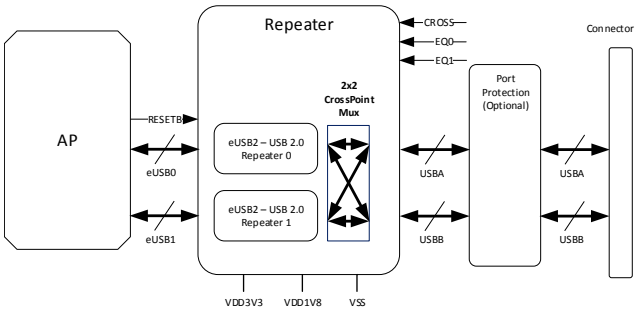
TUSB2E22 is designed to interface with eUSB2 eDSPr or eUSPr operating at 1.2V single-ended signaling.

TUSB2E22 has four levels of compensation settings through the EQ0 and EQ1 pins. These settings can be used to optimize compensation for different eUSB2 channel loss profiles.

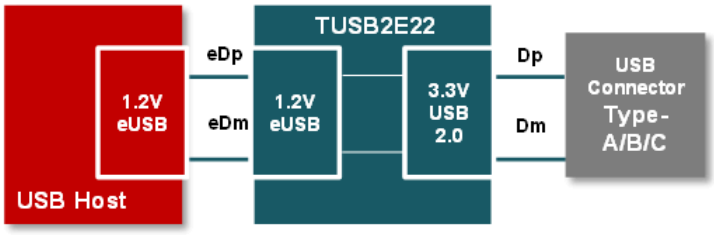
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TUSB2E22	YCG (DSBGA, 25)	2mm × 2mm
	RZA (VQFN, 20)	3.5mm × 3.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



TUSB2E22

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4 Pin Configuration and Functions

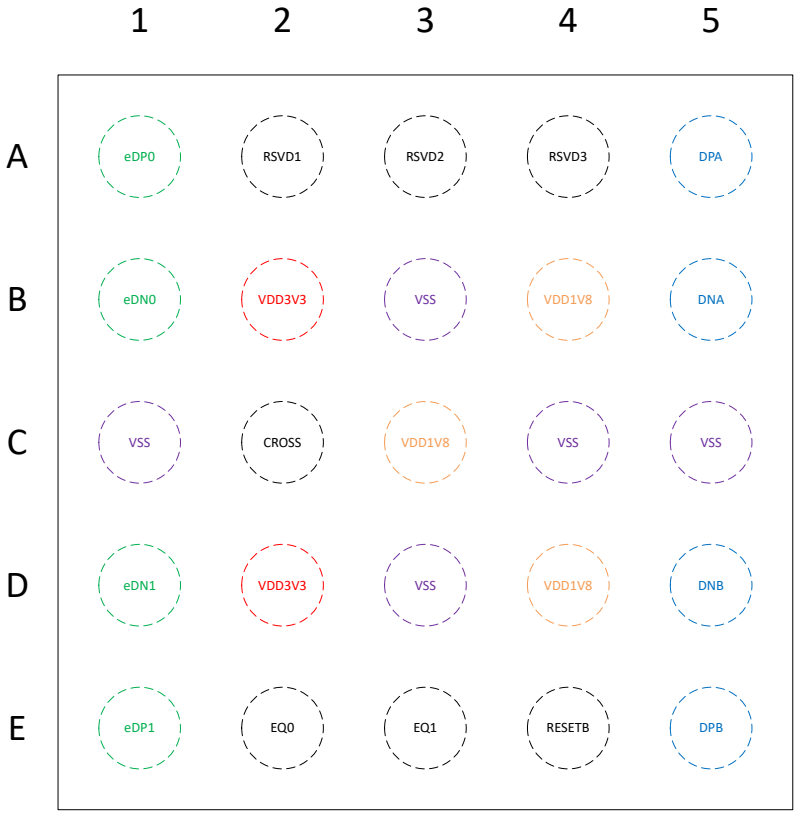


Figure 4-1. YCG Package, 25-Pin DSBGA (Top View)

Legend		
3.3 V Rails	1.8 V Rails	eUSB2 Data Signals
USB2 Data Signals	GPIO Digital Input or Output	

Table 4-1. Pin Functions

PIN		TYPE	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NO.	NAME				
B2, D2	VDD3V3	PWR	N/A	N/A	3.3 V Supply Voltage
C3, B4, D4	VDD1V8	PWR	N/A	N/A	1.8 V Analog Supply Voltage
C1, C4, B3, D3, C5	VSS	GND	N/A	N/A	GND
E4	RESETB	Digital Input	N/A	VDD1V8	Active Low Reset. Upon deassertion of RESETB both repeaters will be enabled and be in eUSB2 default mode awaiting configuration from eDSPr or eUSPr.
C2	CROSS	Digital Input	N/A	VDD3V3	Indicates mux orientation. Used to specify orientation of internal Crossbar switch CROSS = Low: eUSB0 «–» USBA and eUSB1 «–» USBB CROSS = High: eUSB0 «–» USBB and eUSB1«–» USBA Sampled at deassertion of RESETB
A2	RSVD1	Digital I/O	Hi-Z	VDD3V3	Reserved pins connect 1 kΩ pull up to 1.8 V
A3	RSVD2	Digital I/O	Hi-Z	VDD3V3	Reserved pins connect 1 kΩ pull up to 1.8 V
A4	RSVD3	Digital Output	Hi-Z	VDD3V3	Reserved pin leave it unconnected
E2	EQ0	Digital I/O	Hi-Z (input)	VDD3V3	Compensation Level 0: EQ1=low EQ0= low Compensation Level 1: EQ1=low EQ0=high Compensation Level 2: EQ1=high EQ0=low Compensation Level 3: EQ1=high EQ0=high Pins are sampled at RESETB deassertion
E3	EQ1	Digital I/O	Hi-Z (input)	VDD3V3	

Table 4-1. Pin Functions (continued)

PIN		TYPE	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NO.	NAME				
A1	eDP0	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D+ pin
B1	eDN0	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D- pin
D1	eDN1	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D- pin
E1	eDP1	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D+ pin
A5	DPA	Analog I/O	Hi-Z	VDD3V3	USB port A D+ pin
B5	DNA	Analog I/O	Hi-Z	VDD3V3	USB port A D- pin
D5	DNB	Analog I/O	Hi-Z	VDD3V3	USB port B D- pin
E5	DPB	Analog I/O	Hi-Z	VDD3V3	USB port B D+ pin

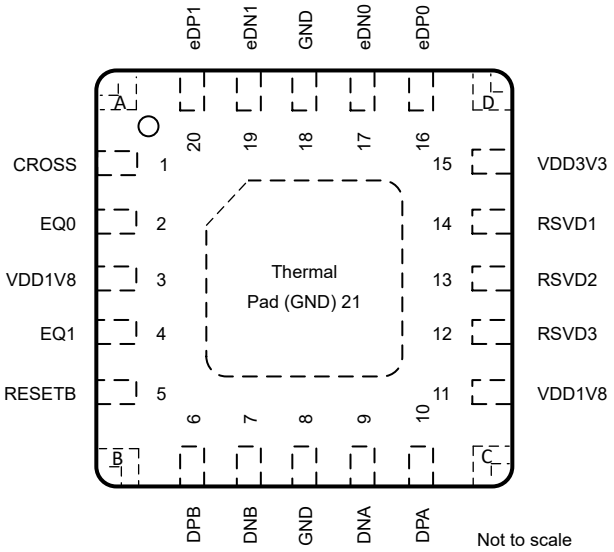


Figure 4-2. 0.5-mm Pitch RZA Package, 20-Pin VQFN (Top View)

Table 4-2. Pin Functions

PIN		TYPE[1]	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NAME	NO.				
VDD3V3	15	PWR	N/A	N/A	3.3 V supply voltage
VDD1V8	3, 11	PWR	N/A	N/A	1.8 V analog supply voltage
GND	8, 18, Thermal Pad (21), Corner Anchors (A, B, C, D)	GND	N/A	N/A	GND
RESETB	5	Digital Input	N/A	VDD1V8	Active Low Reset. Upon deassertion of RESETB both repeaters will be enabled and be in eUSB2 default mode awaiting configuration from eDSPr or eUSPr.
CROSS	1	Digital Input	N/A	VDD3V3	Indicates mux orientation. Used to specify orientation of internal Crossbar switch CROSS = Low: eUSB0 «–» USBA and eUSB1 «–» USBB CROSS = High: eUSB0 «–» USBB and eUSB1«–» USBA Sampled at deassertion of RESETB
RSVD1	14	Digital I/O	Hi-Z	VDD3V3	Reserved pins connect 1 kΩ pull up to 1.8 V
RSVD2	13	Digital I/O	Hi-Z	VDD3V3	Reserved pins connect 1 kΩ pull up to 1.8 V
RSVD3	12	Digital Output	Hi-Z	VDD3V3	Reserved pin leave it unconnected
EQ0	2	Digital I/O	Hi-Z (input)	VDD3V3	Compensation Level 0: EQ1=low EQ0= low Compensation Level 1: EQ1=low EQ0=high Compensation Level 2: EQ1=high EQ0=low Compensation Level 3: EQ1=high EQ0=high Pins are sampled at RESETB deassertion
EQ1	4	Digital I/O	Hi-Z (input)	VDD3V3	
eDP0	16	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D+ pin

Table 4-2. Pin Functions (continued)

PIN		TYPE(1)	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NAME	NO.				
eDN0	17	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D- pin
eDN1	19	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D- pin
eDP1	20	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D+ pin
DPA	10	Analog I/O	Hi-Z	VDD3V3	USB port A D+ pin
DNA	9	Analog I/O	Hi-Z	VDD3V3	USB port A D- pin
DNB	7	Analog I/O	Hi-Z	VDD3V3	USB port B D- pin
DPB	6	Analog I/O	Hi-Z	VDD3V3	USB port B D+ pin

(1) PWR = power, GND = ground, I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	V_{DD3V3}	–0.3	4.32	V
Analog Supply voltage range	V_{DD1V8}	–0.3	2.1	V
Voltage range	DPA, DNA, DPB, DNB , 1000 total number of short events and cumulative duration of 1000 hrs.	–0.3	6	V
Voltage range	eDP0, eDN0, eDP1, eDN1	–0.3	1.6	V
Voltage range	CROSS, RESETB, RSVD1, RSVD2, RSVD3, EQ1, EQ0	–0.3	2.1	V
Junction temperature	$T_{J(max)}$		125	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD3V3}	Supply voltage (VDD3V3)	3.0	3.3	3.6	V
V_{DD1V8}	Analog Supply voltage (VDD1V8)	1.62	1.8	1.98	V
T_A	Operating free-air temperature	-20		85	°C
T_J	Junction temperature	-20		105	°C
T_{CASE}	Case temperature	-20		105	°C
T_{PCB}	PCB temperature (1mm away from the device)	-20		92	°C

5.4 Thermal Information

THERMAL METRIC[1]		TUSB2E22 YCG (DSBGA) 25 PINS	TUSB2E22 RZA (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.5	46.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	39.0	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	—	13.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.9	21.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.9	21.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
V_{IH}	High level input voltage	CROSS, EQ1, EQ0	1.053			V
V_{IL}	Low-level input voltage	CROSS, EQ1, EQ0			0.693	V
V_{IL}	Low-level input voltage	RESETB			0.35	V
V_{IH}	High level input voltage	RESETB	0.75			V
I_{IH}	High level input current	V_{IH} = 1.98 V, VDD3V3=3.0 V or 0 V, VDD1V8=1.62V or 0 V CROSS, RESETB, EQ1, EQ0			2	µA
I_{IL}	Low level input current	V_{IL} = 0 V, VDD3V3=3.0 V or 0 V, VDD1V8=1.62V or 0 V CROSS, RESETB, EQ1, EQ0			2	µA
USBA (DPA, DNA), USBB (DPB, DNB)						
Z_{inp_Dx}	Impedance to GND, no pull up/down	Vin=3.6 V, V_{DD3V3}=3.0 V USB 2.0 Specification Section 7.1.6	390			kΩ
R_{PUI}	Bus Pull-up Resistor on Upstream Facing Port (idle)	USB 2.0 Specification Section 7.1.5	0.92	1.1	1.475	kΩ
R_{PUR}	Bus Pull-up Resistor on Upstream Facing Port (receiving)	USB 2.0 Specification Section 7.1.5	1.525	2.2	2.99	kΩ
R_{PD}	Bus Pull-down Resistor on Downstream Facing Port	USB 2.0 Specification Section 7.1.5	14.35	19	24.6	kΩ
V_{HSTERM}	Termination voltage in highspeed	USB 2.0 Specification Section 7.1.6.2, The output voltage in the high-speed idle state	–10		10	mV
USB TERMINATION						
Z_{HSTERM}	Driver Output Resistance (which also serves as high speed termination)	(VOH= 0 to 600 mV) USB 2.0 Specification Section 7.1.1.1,	40.5	45	49.5	Ω
USBA, USBB INPUT LEVELS LS/FS						
V_{IH}	High (driven)	USB 2.0 Specification Section 7.1.4 (measured at connector)	2			V
V_{IHZ}	High (floating)	USB 2.0 Specification Section 7.1.4 (HOST downstream port pull down resistor enabled and external device pull up 1.5K +/-5% to 3.0-3.6 V).	2.7		3.6	V
V_{IL}	Low	USB 2.0 Specification Section 7.1.4			0.8	V
USBA, USBB OUTPUT LEVELS LS/FS						

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low	USB 2.0 Specification Section 7.1.1, (measured at connector with RL of 1.425 kΩ to 3.6 V.)	0		0.3	V
V_{OH}	High (Driven)	USB 2.0 Specification Section 7.1.1 (measured at connector with RL of 14.25 kΩ to GND.)	2.8		3.6	V
Z_{FSTERM}	Driver Series Output Resistance	USB 2.0 Specification Section 7.1.1, Measured it during VOL or VOH	28		44	Ω
V_{CRS}	Output Signal Crossover Voltage	Measured as in USB 2.0 Specification Section 7.1.1 Figure 7-8; Excluding the first transition from the Idle state	1.3		2	V
USBA, USBB OUTPUT LEVELS HS						
V_{HSOH}	High-speed data signaling high	USB 2.0 Specification Section 7.1.7.2, measured single ended peak voltage per USB 2.0 test measurement spec, Test load is an ideal 45 Ω to GND on DP and DN	360		440	mV
V_{HSOL}	High-speed data signaling low, driver is off termination is on (measured single ended)	USB 2.0 Specification Section 7.1.7.2, Test load is an ideal 45 Ω to GND on DP and DN.	–10		10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	USB 2.0 Specification Section 7.1.7.2 , Test load is an ideal 45 Ω to GND on DP and DN.	700	900	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	USB 2.0 Specification Section 7.1.7.2 , Test load is an ideal 45 Ω to GND on DP and DN.	-900	-700	-500	mV
$U2\_TX_{CM}$	High-speed TX DC Common Mode		-50	200	500	mV
eUSB2 TERMINATION						
R_{SRC_HS}	High speed transmit source termination impedance	eUSB2 Specification Section 7.1.1	33	40	47	Ω
ΔR_{SRC_HS}	High speed source impedance mismatch	eUSB2 Specification Section 7.1.1			4	Ω
R_{RCV_DIF}	High speed differential receiver termination (repeater)	eUSB2 Specification Section 7.1.2	74	80	86	Ω
R_{PD}	Pull-down resistors on eDP/eDN	eUSB2 Specification Section 7.3, active during LS, FS and HS	6	8	10	kΩ
R_{SRC_LSFS}	Transmit output impedance	eUSB2 Specification Section 7.2.1, Table 7-13 TX output impedance to match spec version 1.10	28	44	59	Ω
eUSB0, eUSB1 FS/LS INPUT LEVELS						
V_{IL}	Single-ended input low	eUSB2 Specification Section 7.2.1, Table 7-13	–0.1		0.399	V
V_{IH}	Single-ended input high	eUSB2 Specification Section 7.2.1, Table 7-13	0.819		1.386	V
V_{HYS}	Receive single-ended hysteresis voltage	eUSB2 Specification Section 7.2.1, Table 7-13	43.2			mV
eUSB0, eUSB1 FS/LS OUTPUT LEVELS						
V_{OL}	Single-ended output low	eUSB2 Specification Section 7.2.1, Table 7-13			0.198	V
V_{OH}	Single-ended output high	eUSB2 Specification Section 7.2.1, Table 7-13	0.918		1.32	V
eUSB0, eUSB1 HS INPUT LEVELS						

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RX_CM}	Receive DC common mode range (low)	eUSB2 Specification Section 7.1.2 (normative), low DC common mode RX must tolerate			120	mV
V_{RX_CM}	Receive DC common mode range (high)	eUSB2 Specification Section 7.1.2 (normative), high DC common mode RX must tolerate	280			mV
$V_{CM\_RX\_AC}$	Receiver AC common mode (50MHz-480MHz)	eUSB2 Specification Section 7.1.2 (informative), across the DC common mode range of 120 mV to 280 mV. (RX capability tested with intentional TX Rise/Fall Time mismatch and prop delay mismatch)	–60		60	mV
C_{RX_CM}	Receive center-tapped capacitance	eUSB2 Specification Section 7.1.2 (informative)	15		50	pF
$V_{RX\_DIF\_SENS}$	Receive differential sensitivity, RX should be able to receive less than this value.	eUSB2 Specification Section 7.1.2, V_{CM} = 120 mV to 450 mV			120	mVp-p
eUSB0, eUSB1 HS OUTPUT LEVELS						
$V_{ETX\_CM\_AC}$	Transmit CM AC (50MHz-480MHz)	eUSB2 Specification Section 7.1.1, An ideal 80 Ω Rx differential termination and center tap cap of 15pF, with maximum DC common mode range	–30		30	mV
V_{EHSOD}	Transmit differential (terminated)	Measured p2p, R_L = 80 Ω, ideal 80 Ω Rx differential termination load		400		mV
$V_{E\_TX\_CM}$	Transmit DC common mode	eUSB2 Specification Section 7.1.1	170		230	mV

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DPA, DNA, DPB, DNB, FS Driver Switching Characteristics						
T_{FR}	Rise Time (10% - 90%)	USB 2.0 Specification Figure 7-8; Figure 7-9	4		20	ns
T_{FF}	Fall Time (10% - 90%)	USB 2.0 Specification Figure 7-8; Figure 7-9	4		20	ns
T_{FRFM}	(T_{FR}/T_{FM})	USB 2.0 Specification 7.1.2, Excluding the first transition from the Idle state	90		111.1	%
DPA, DNA, DPB , DNB, LS Driver Switching Characteristics						
T_{LR}	Rise Time (10% - 90%)	USB 2.0 Specification Figure 7-8	75		300	ns
T_{LF}	Fall Time (10% - 90%)	USB 2.0 Specification Figure 7-8	75		300	ns
eDP0, eDN0, eDP1, eDN1, HS Driver Switching Characteristics						
T_{EHSRF_MM}	Transmit rise/fall mismatch	eUSB2 Specification Section 7.2.1, Rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).			25	%
eDP0, eDN0, eDP1, eDN1, LS/FS Driver Switching Characteristics						
T_{ERF}	Rise/Fall Time (10% - 90%)	eUSB2 Specification Section 7.2.1	2		6	ns
T_{ERF_MM}	Transmit rise/fall mismatch	eUSB2 Specification Section 7.2.1			25	%

5.7 Timing Requirements

		MIN	NOM	MAX	UNIT
RESET TIMING					
$t_{\_VDD1V8\_RAMP}$	Ramp time for VDD1V8 to reach minimum 1.62 V			2	ms
$t_{\_VDD3V3\_RAMP}$	Ramp time for VDD3V3 to reach minimum 3.0 V			2	ms
$t_{\_su\_CROSS}$	Setup time for CROSS sampled at the deassertion of RESETB	0			ms
$t_{\_hd\_CROSS}$	Hold time for CROSS sampled at the deassertion of RESETB	3			ms
$t_{\_aRESETB}$	duration for RESETB to be asserted low to complete reset while powered	10			us
$t_{\_RH\_READY}$	Time for eUSB2 interface to be ready after RESETB is deasserted or (VDD1V8 and VDD3V3) reach minimum recommended voltages, whichever is later			3	ms

6 Parametric Measurement Information

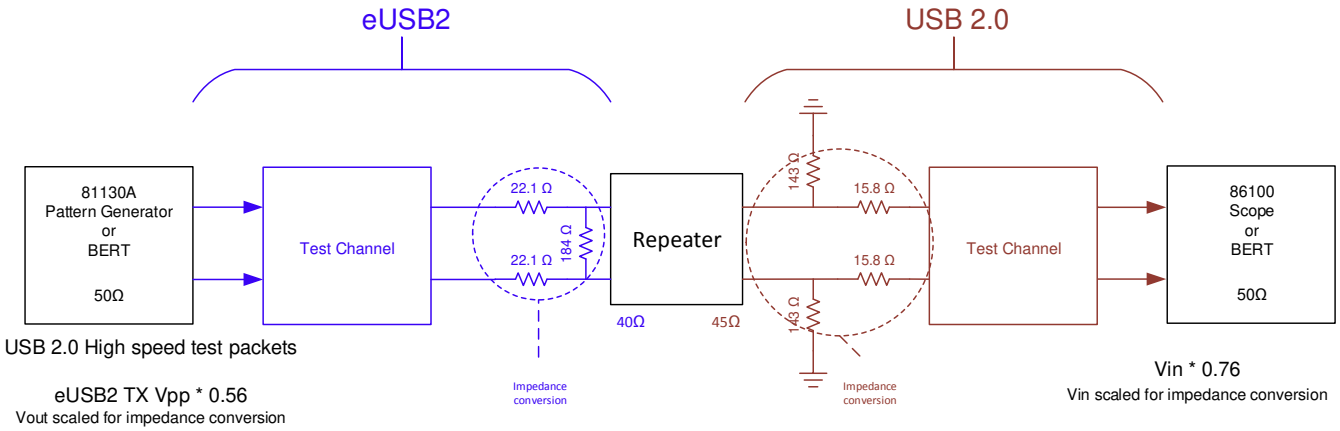


Figure 6-1. USB 2.0 TX Output (Egress) Jitter, Eye Mask Test Setup

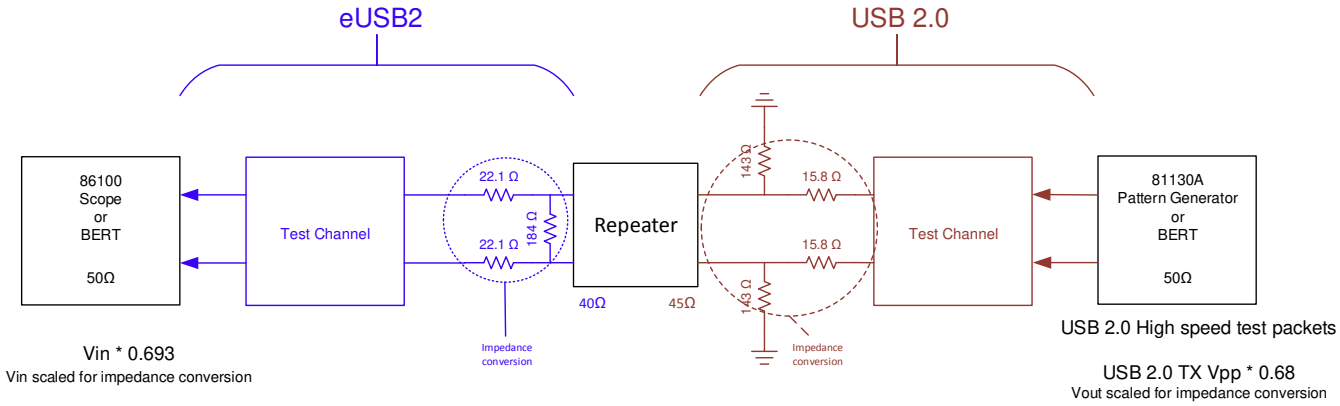


Figure 6-2. eUSB2 TX Output (Ingress) Jitter, Eye Mask Test Setup

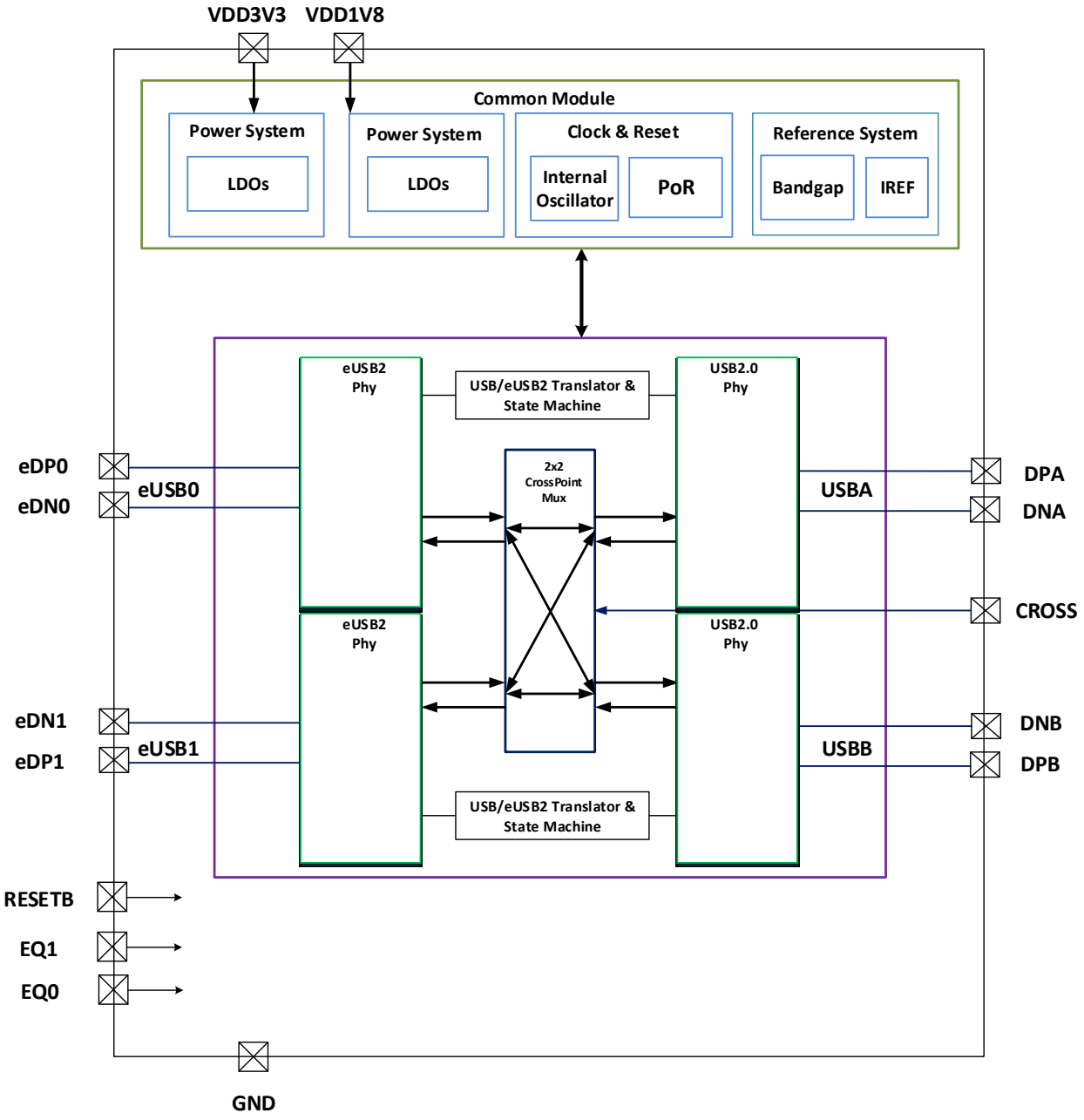
7 Detailed Description

7.1 Overview

The TUSB2E22 is a dual eUSB2 to USB 2.0 repeater that resides between SoC with one or two eUSB2 port and an external connector that supports USB 2.0. Each repeater is independently configurable as either a host or device repeater (DRD repeater).

The USB 2.0 ports A and B can be swapped by an internal crossbar switch by configuring CROSS pin at reset. CROSS pin is ignored after power up reset.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 USB 2.0

TUSB2E22 supports two USB 2.0 ports. Each port supports Low Speed, Full Speed and High Speed operations.

7.3.2 eUSB2

TUSB2E22 supports two eUSB2 ports with 1.2V single ended signaling. Each port support Low Speed, Full Speed and High Speed operations.

7.3.3 Cross MUX

TUSB2E22 supports a cross mux functionality that can map either of the two eUSB2 ports to the two USB 2.0 ports providing design flexibility.

7.4 Device Functional Modes

7.4.1 Repeater Mode

Upon deassertion of RESETB and after t_{RH_READY} , TUSB2E22 will enable and enter default state and be ready to accept eUSB2 packets.

Table 7-1. Number of Hubs Supported with Host and/or Peripheral Repeater

Number of eUSB2 Repeaters	Number of Hubs Operating at HS	Number of Hubs Operating at FS	
1	4	2	Number of hubs operating at FS is reduced due to $T_{e\_to\_U\_DJ1}$ and T_{RJR1}. Number of hubs operating at HS is reduced due to SOP truncation and EOP dribble
2	3	1	
0	5	5	non-eUSB2 system for reference

7.4.2 Power Down Mode

RESETB could be used as a power down pin when asserted low. Power down mode will put TUSB2E22 in lowest power mode.

7.4.3 CROSS

CROSS pin will control the orientation of the integrated cross bar mux.

Upon deassertion of RESETB followed by internally generated reset signal and 1ms delay, CROSS pin is sampled and latched.

The system needs to make sure that CROSS meets t_{su_CROSS} and t_{hd_CROSS} with respect to power supply ramp and RESETB deassertion per Section 8.3 .

Changes to the state of the CROSS input while RESETB is high will be ignored.

Table 7-2. eUSB2 to USB Mapping

	CROSS = 0	CROSS = 1
eUSB0 (eDP0, eDN0)	USBA (DPA, DNA)	USBB (DPB, DNB)
eUSB1 (eDP1, eDN1)	USBB (DPB, DNB)	USBA (DPA, DNA)

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

TUSB2E22 can be used in either HOST or Peripheral implementation. The mode is configured by the eUSB2 SoC.

8.2 Typical Dual Port System Implementation

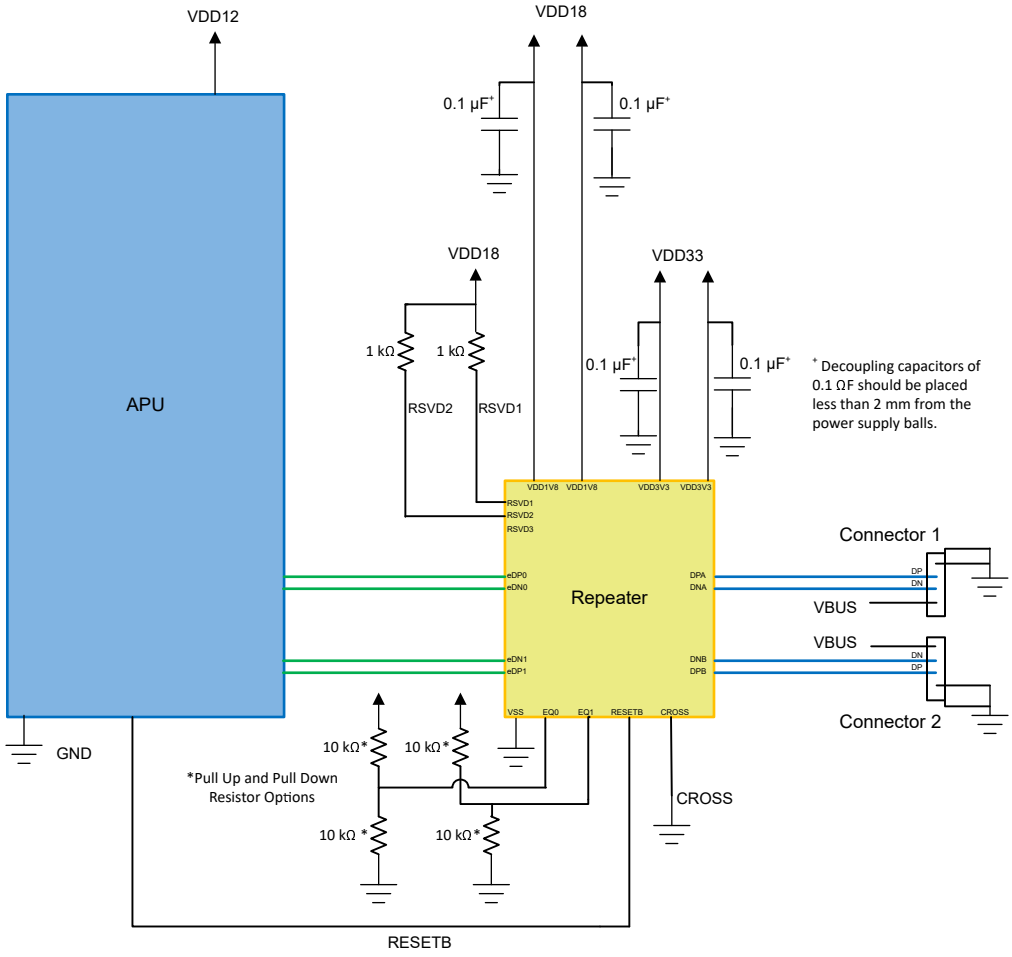


Figure 8-1. Typical Dual Port System Implementation

8.2.1 Design Requirements

TUSB2E22 supports the 1.2 V option of the eUSB2 specification. eUSB2 SoC must be compliant to the 1.2 V option of the eUSB2 specification.

8.2.2 Detailed Design Procedure

TUSB2E22 has four loss compensation settings for high speed operation and proper setting should be selected to match the system loss profile to optimize jitter performance. USB 2.0 high speed eye diagram measurements could be used as a guide to confirm the loss compensation is optimum for a given system.

8.2.3 Application Curve

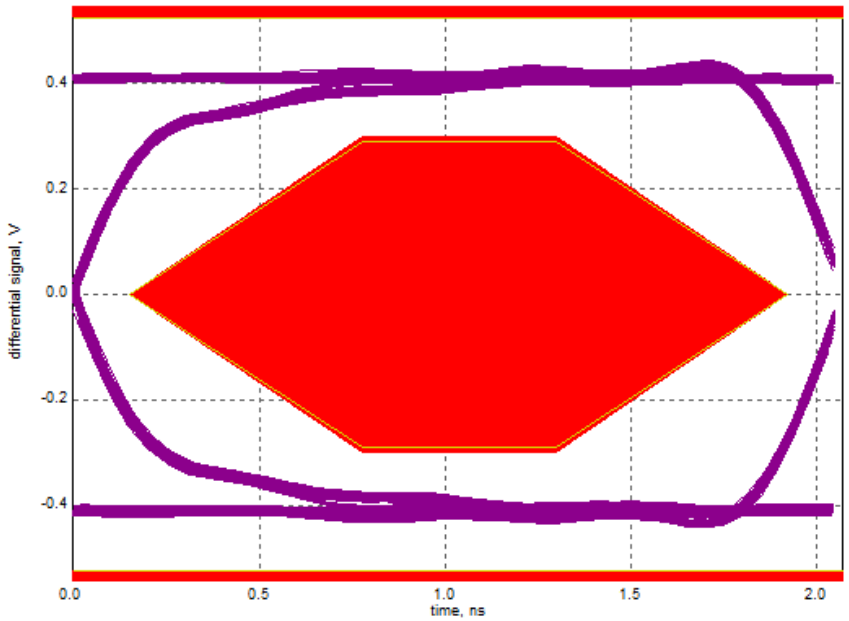


Figure 8-2. Typical USB 2.0 High Speed Eye Diagram

8.3 Power Supply Recommendations

8.3.1 Power Up Reset

RESETB pin is active low reset pin and can also be used as a power down pin.

TUSB2E22 does not have power supply sequence requirements between VDD3V3 and VDD1V8.

Maximum VDD3V3 and VDD1V8 ramp time to reach minimum supply voltages should be 2 ms.

Internal power on reset circuit along with the external RESETB input pin allows for proper initialization when RESETB is deasserted high prior to the power rails being valid. If RESETB deassert high before the power supplies are stable, internal power on reset circuit will hold off internal reset until the supplies are stable.

Upon deassertion of RESETB followed by internally generated reset signal and 1ms delay, CROSS pin is sampled and latched.

Upon deassertion of RESETB and after t_{RH_READY}, TUSB2E22 will enable and enter default state and be ready to accept eUSB2 packets. Each repeater will either be in host repeater mode or device repeater mode depending on the receipt of either host mode enable or peripheral mode enable.

8.4 Layout

8.4.1 Layout Guidelines

1. Place supply bypass capacitors as close to VDD1V8 and VDD3V3 pins as possible and avoid placing the bypass caps near the eDP/eDN and DP/DN traces.
2. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
3. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals due to signal reflections. If a stub is unavoidable, then the stub must be less than 200 mil.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
7. Avoid crossing over anti-etch, commonly found with plane splits.
8. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 8-3.

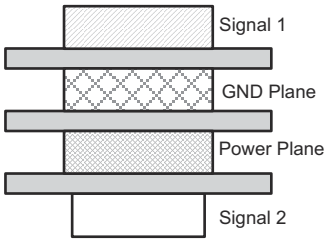


Figure 8-3. Four-Layer Board Stack-Up

8.4.2 Example YCG Layout For Application With No Cross MUX Function.

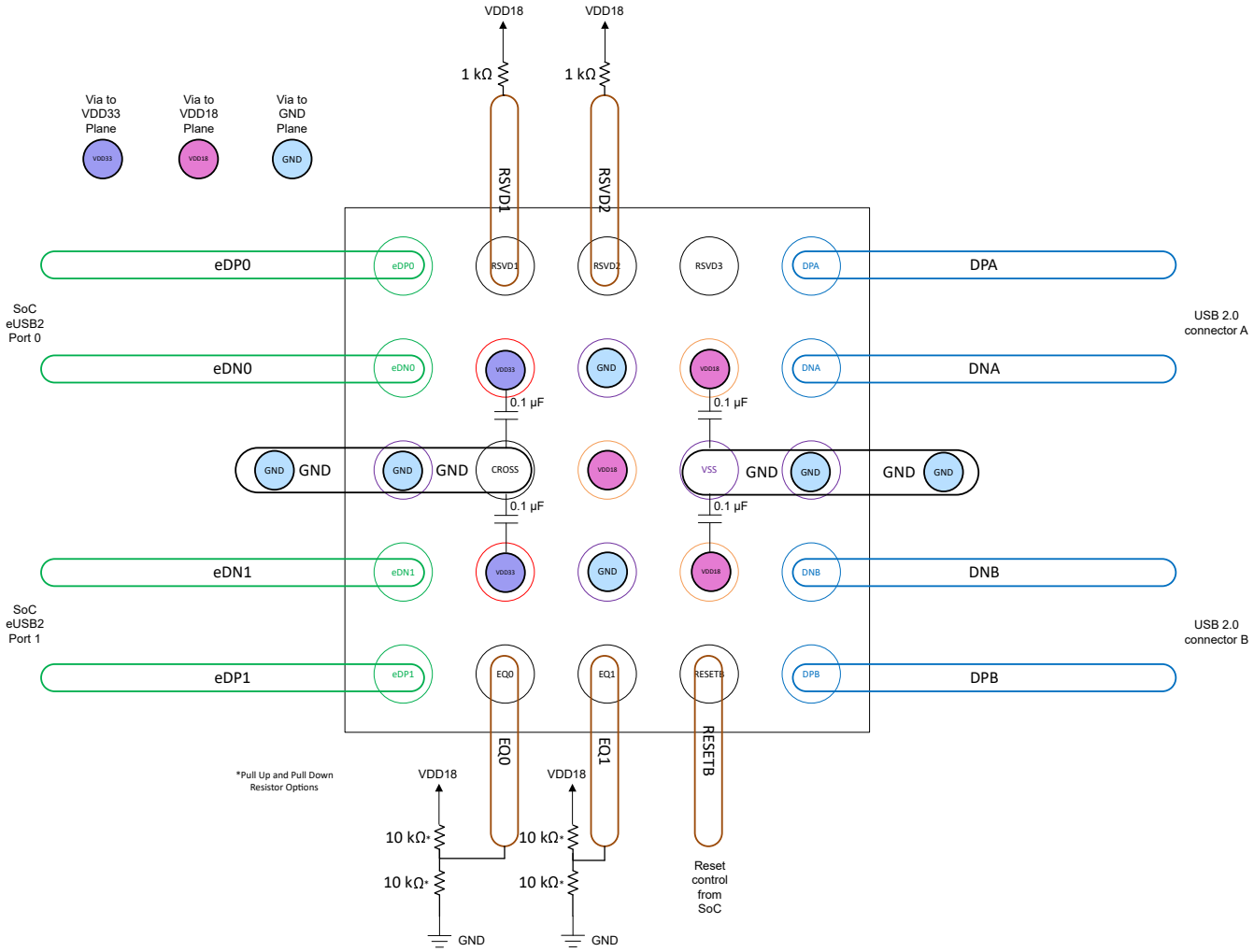


Figure 8-4. Example Layout of Application With No Cross MUX Function

8.4.3 Example RZA Layout For Application With No Cross MUX Function

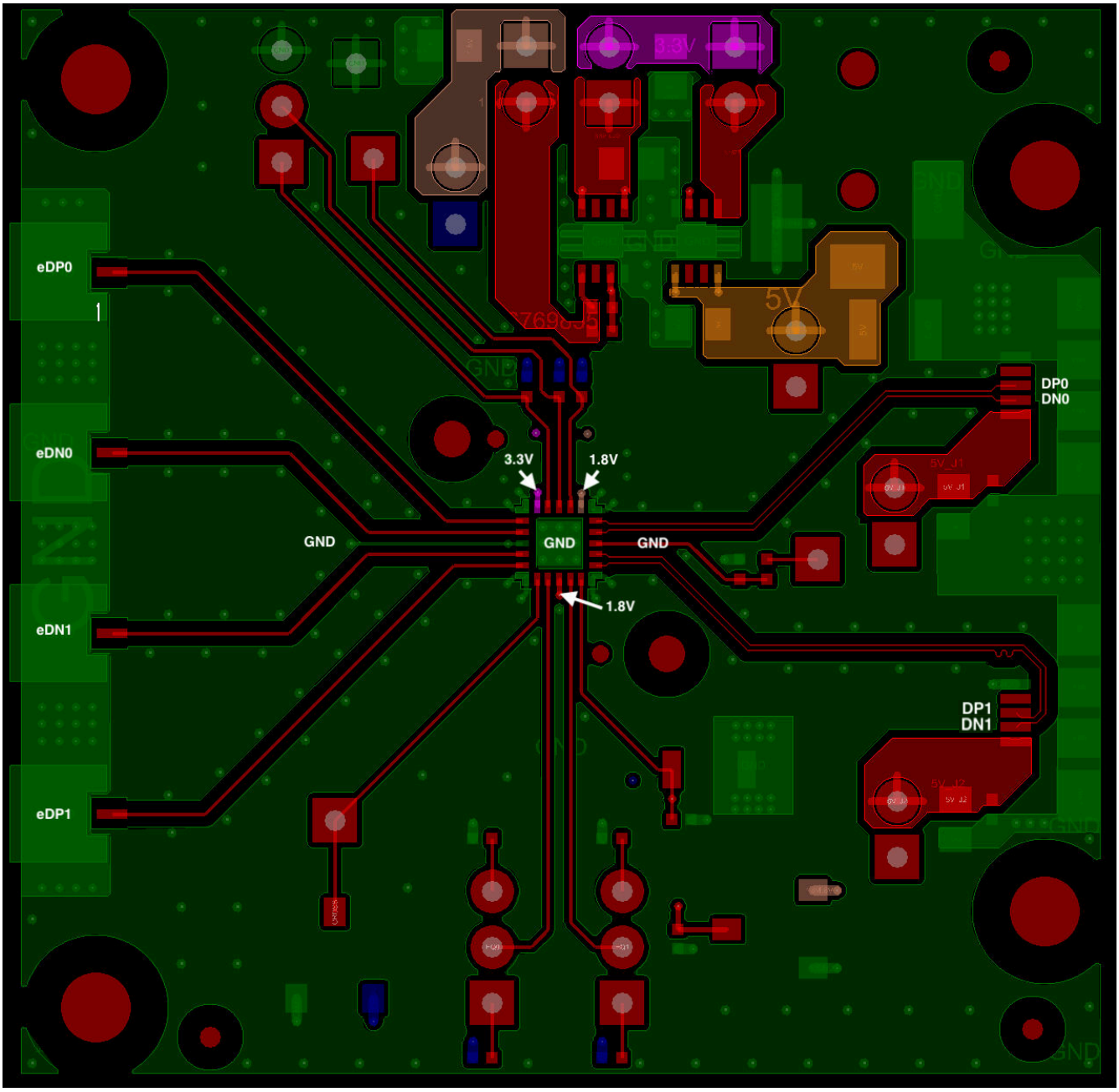


Figure 8-5. VQFN Example Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *USB 2.0 Board Design and Layout Guidelines*
- Texas Instruments, *High-Speed Layout Guidelines Application Report*
- Texas Instruments, *High-Speed Interface Layout Guidelines*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2023) to Revision C (August 2024)	Page
• Changed YCG (DSBGA, 25) package size from: 1.75mm × 1.75mm to: 2mm × 2mm	1

Changes from Revision A (December 2019) to Revision B (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Package Information* table to include package lead size	1
• Added the RZA VQFN package option	3
• Added example layout for VQFN with no cross MUX control	18

Changes from Revision * (February 2019) to Revision A (December 2019)	Page
• First public release of the data sheet	1

11 Mechanical, Packaging, and Orderable Information

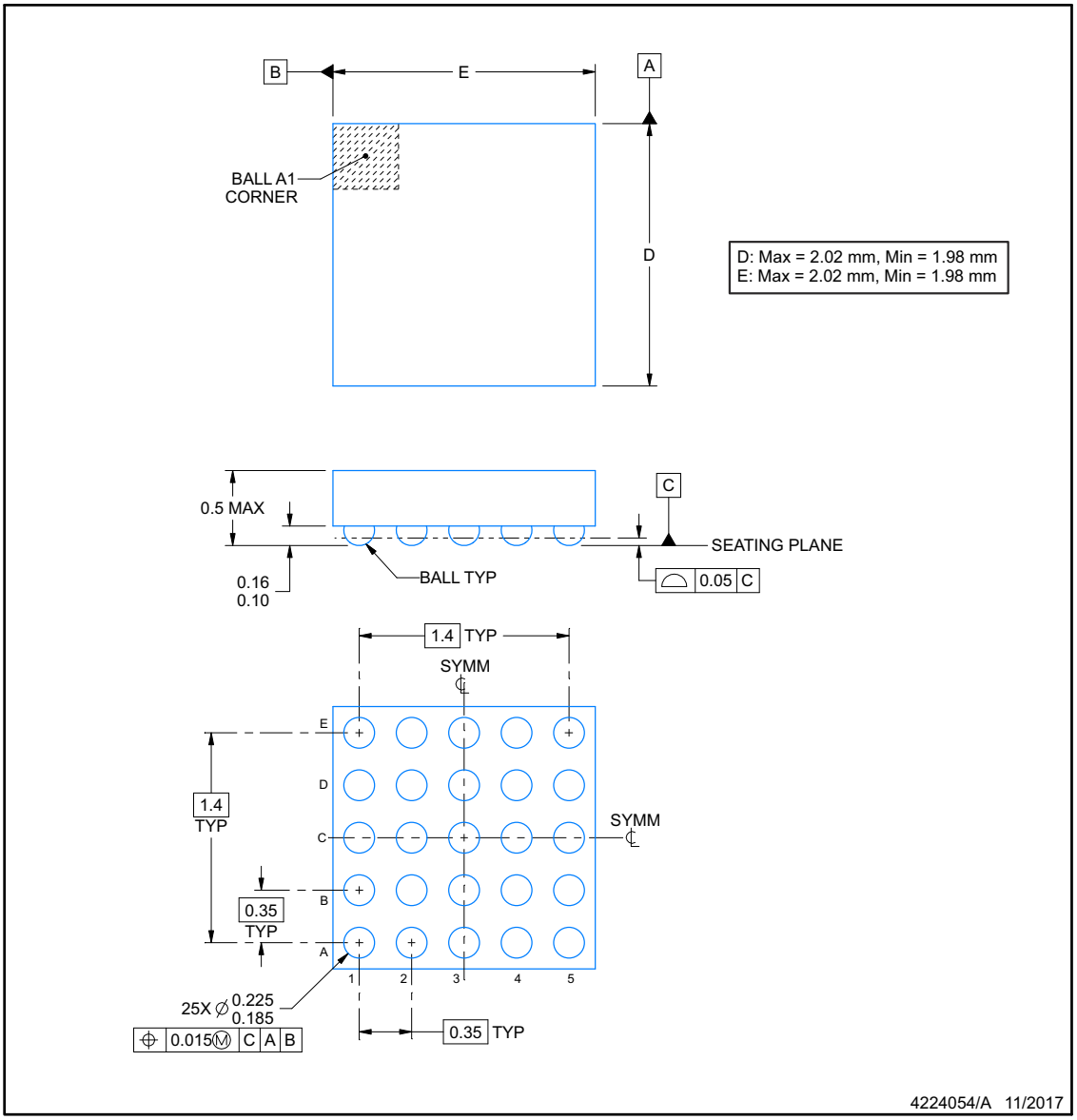
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

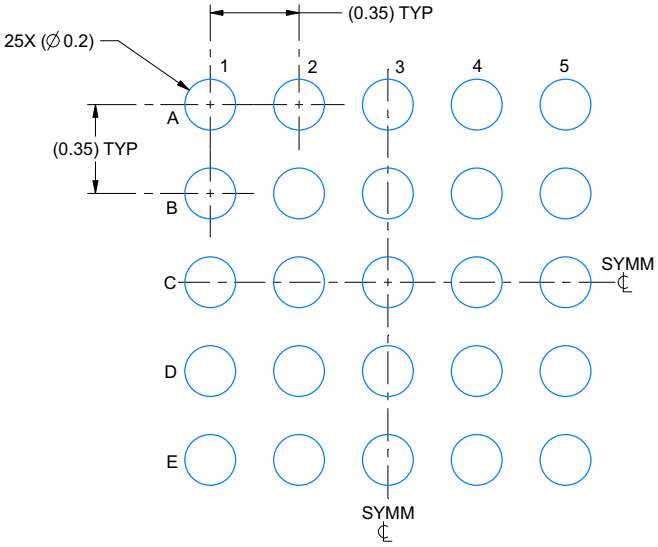
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

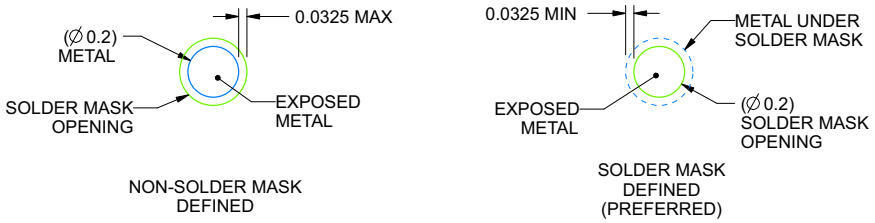
YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224054/A 11/2017

NOTES: (continued)

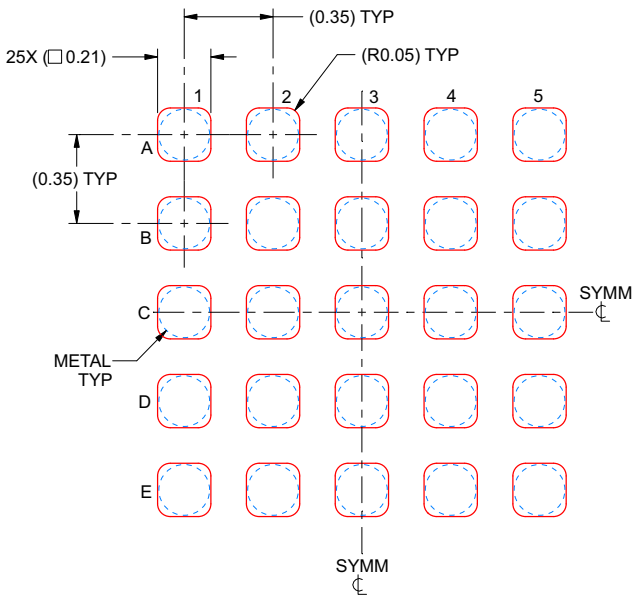
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4224054/A 11/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB2E22RZAR	ACTIVE	VQFN-FCRLF	RZA	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	2E22	Samples
TUSB2E22RZAT	ACTIVE	VQFN-FCRLF	RZA	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	2E22	Samples
TUSB2E22YCGR	ACTIVE	DSBGA	YCG	25	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E2	Samples
TUSB2E22YCGT	ACTIVE	DSBGA	YCG	25	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

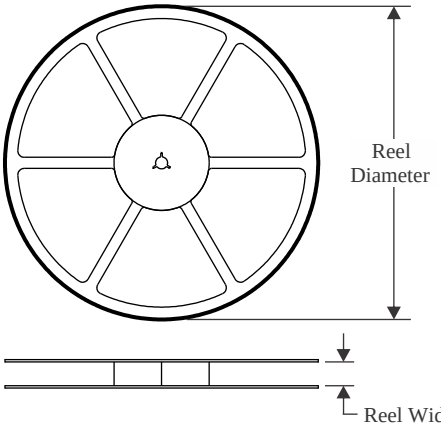
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

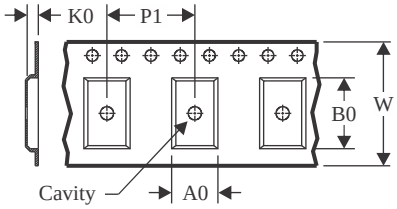
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

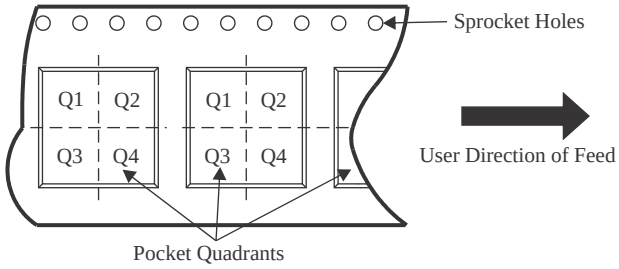


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

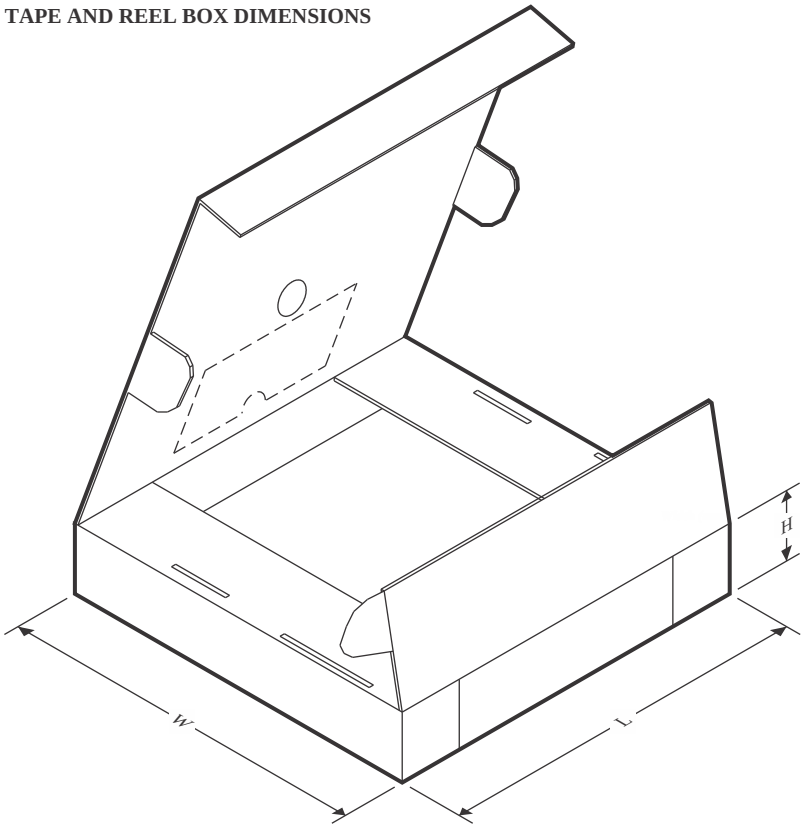
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB2E22RZAR	VQFN-FCRLF	RZA	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TUSB2E22RZAT	VQFN-FCRLF	RZA	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TUSB2E22YCGR	DSBGA	YCG	25	3000	180.0	8.4	2.14	2.14	0.7	4.0	8.0	Q1
TUSB2E22YCGT	DSBGA	YCG	25	250	180.0	8.4	2.14	2.14	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

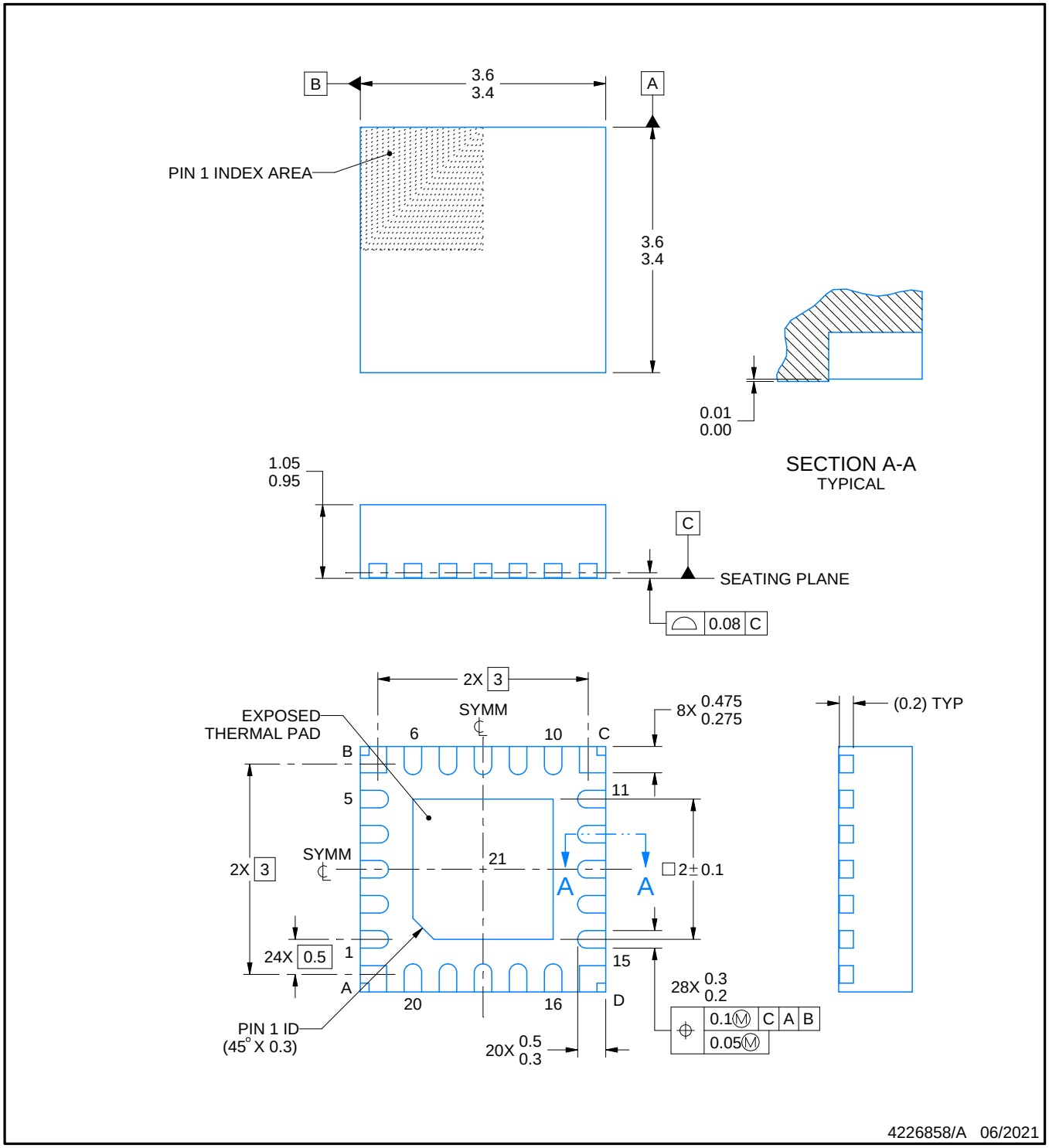
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB2E22RZAR	VQFN-FCRLF	RZA	20	3000	367.0	367.0	35.0
TUSB2E22RZAT	VQFN-FCRLF	RZA	20	250	210.0	185.0	35.0
TUSB2E22YCGR	DSBGA	YCG	25	3000	182.0	182.0	20.0
TUSB2E22YCGT	DSBGA	YCG	25	250	182.0	182.0	20.0

PACKAGE OUTLINE

RZA0020A

VQFN - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

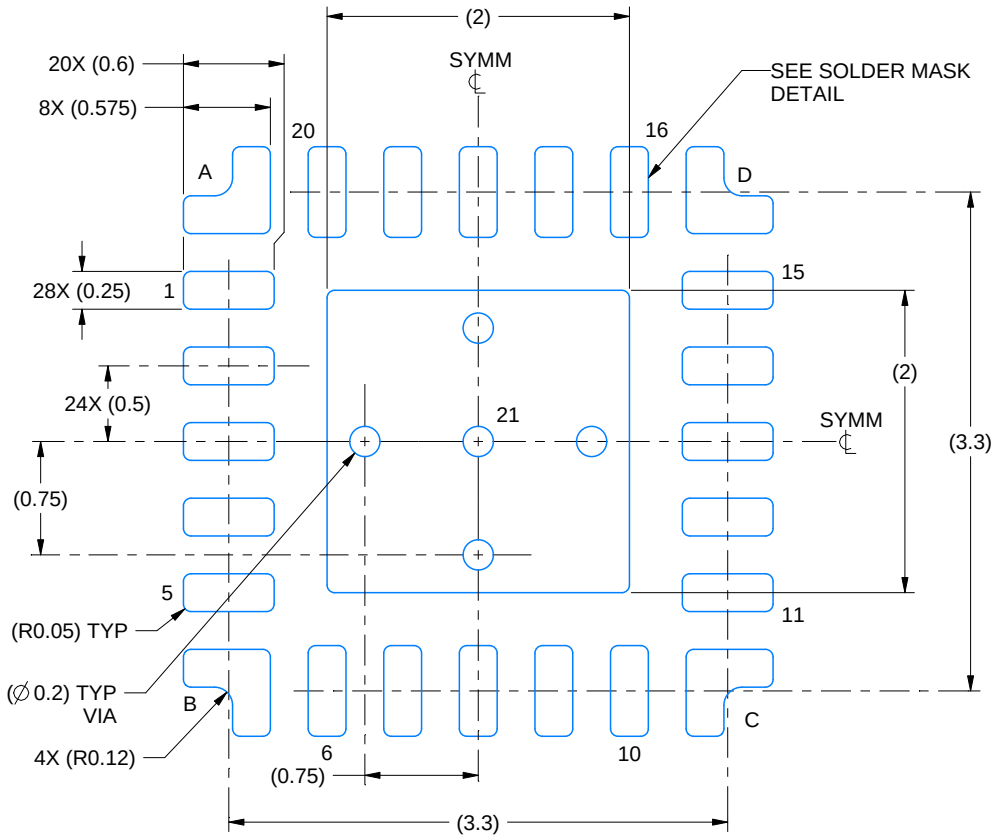
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

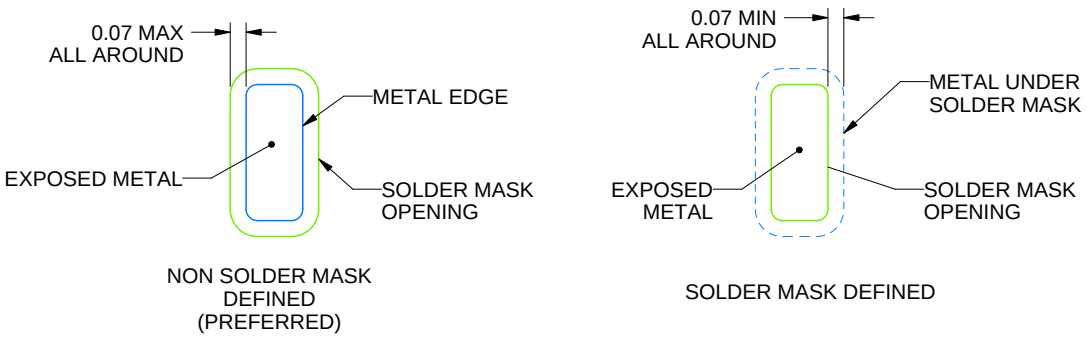
RZA0020A

VQFN - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

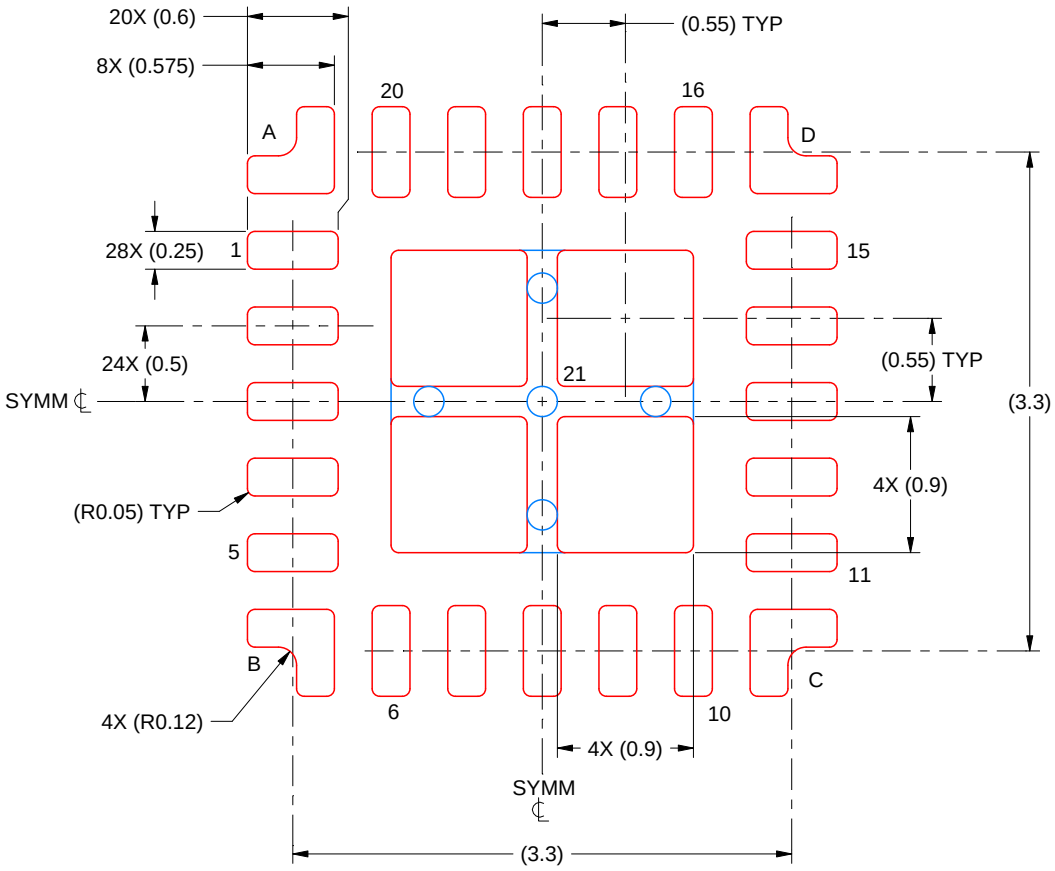


SOLDER MASK DETAILS

4226858/A 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4226858/A 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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